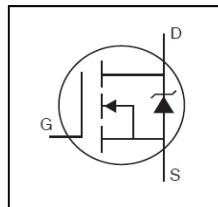


Features

- Advanced Planar Technology
- Low On-Resistance
- Dynamic dV/dT and dI/dT capability
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

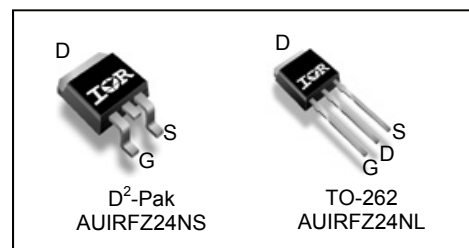


HEXFET® Power MOSFET

V_{DSS}	55V
R_{DS(on)} max.	0.07Ω
I_D	17A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFZ24NL	TO-262	Tube	50	AUIRFZ24NL
AUIRFZ24NS	D²-Pak	Tube	50	AUIRFZ24NS
		Tape and Reel Left	800	AUIRFZ24NSTRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	17	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	12	
I _{DM}	Pulsed Drain Current ①	68	
P _D @ T _A = 25°C	Maximum Power Dissipation	3.8	W
P _D @ T _C = 25°C	Maximum Power Dissipation	45	
	Linear Derating Factor	0.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	71	mJ
I _{AR}	Avalanche Current ①	10	A
E _{AR}	Repetitive Avalanche Energy ①	4.5	mJ
dv/dt	Peak Diode Recovery ③	6.8	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	3.3	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount), D² Pak⑤	—	40	

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

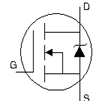
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.07	Ω	$V_{GS} = 10V, I_D = 10A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Trans conductance	4.5	—	—	S	$V_{DS} = 25V, I_D = 10A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

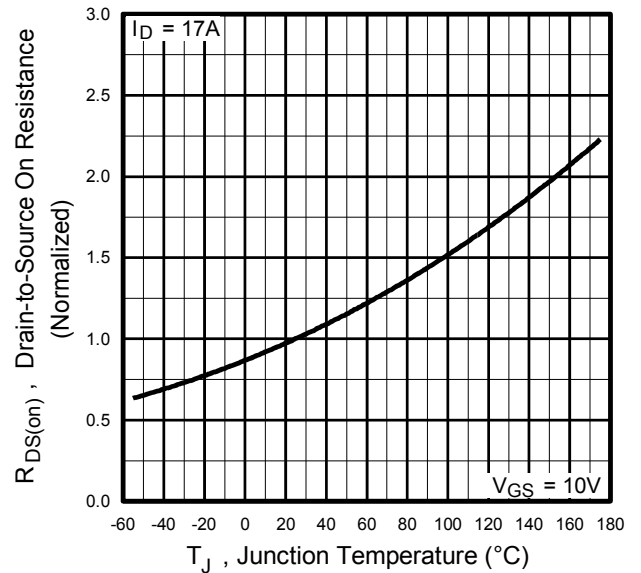
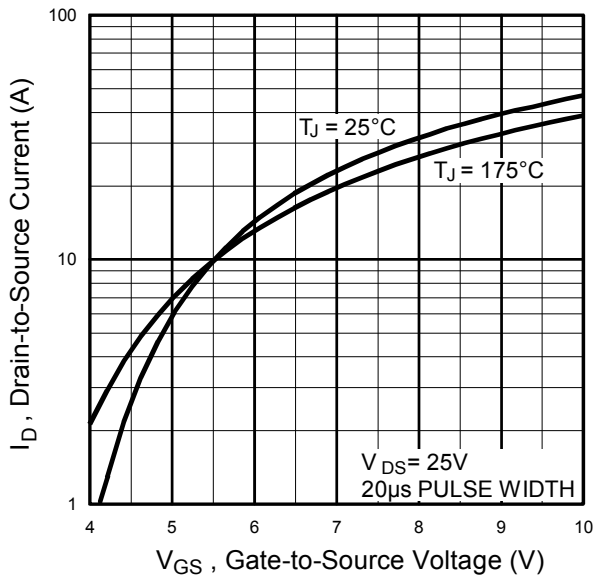
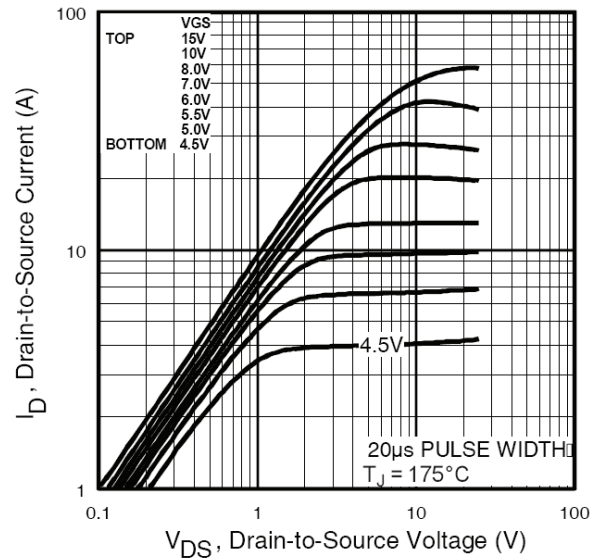
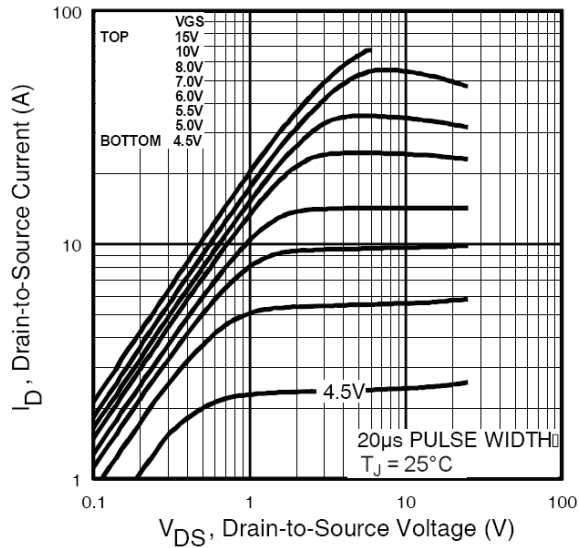
Q_g	Total Gate Charge	—	—	20	nC	$I_D = 10A$
Q_{gs}	Gate-to-Source Charge	—	—	5.3		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain Charge	—	—	7.6		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	4.9	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	34	—		$I_D = 10A$
$t_{d(off)}$	Turn-Off Delay Time	—	19	—		$R_G = 24\Omega$
t_f	Fall Time	—	27	—		$R_D = 2.6\Omega$, See Fig. 10 ④
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	370	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	140	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	65	—		$f = 1.0MHz$, See Fig. 5

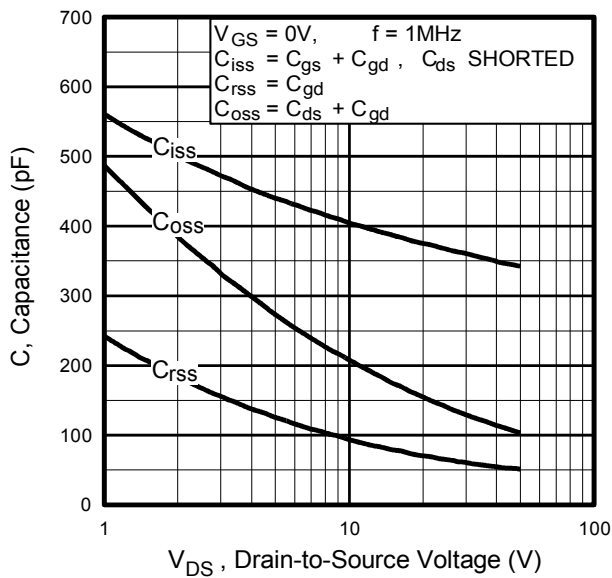
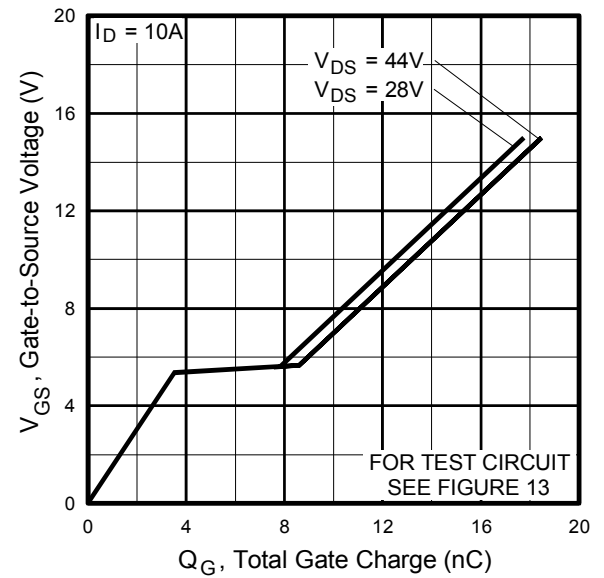
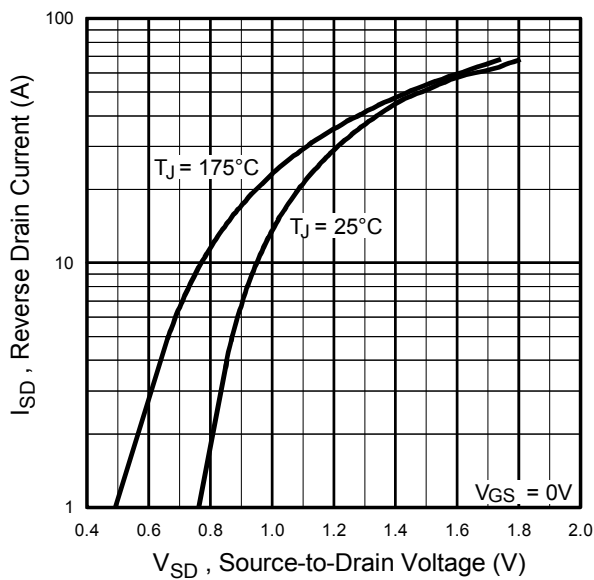
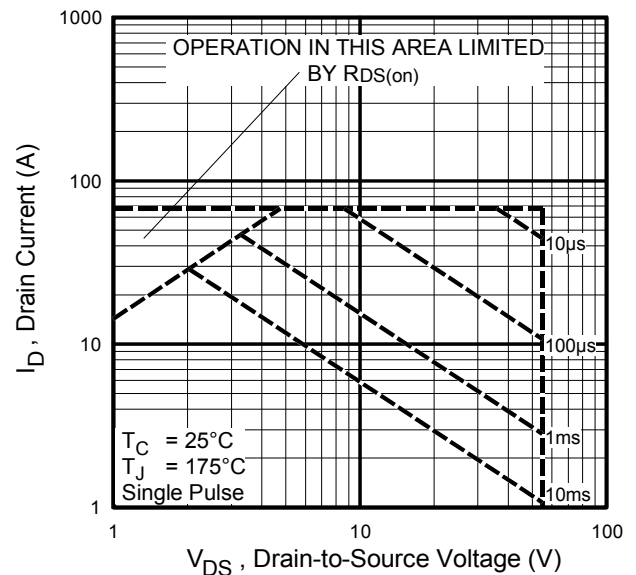
Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	68		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 10A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	56	83	ns	$T_J = 25^\circ\text{C}, I_F = 10A$
Q_{rr}	Reverse Recovery Charge	—	120	180	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1.0mH$, $R_G = 25\Omega$, $I_{AS} = 10A$, $V_{GS} = 10V$. (See fig.12)
- ③ $I_{SD} \leq 10A$, $di/dt \leq 280A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994




Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

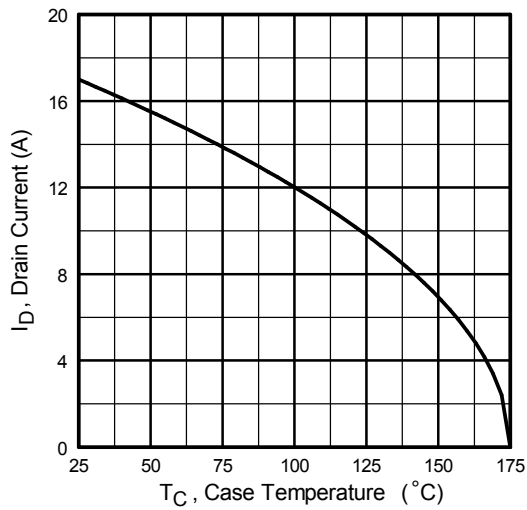


Fig 9. Maximum Drain Current vs. Case Temperature

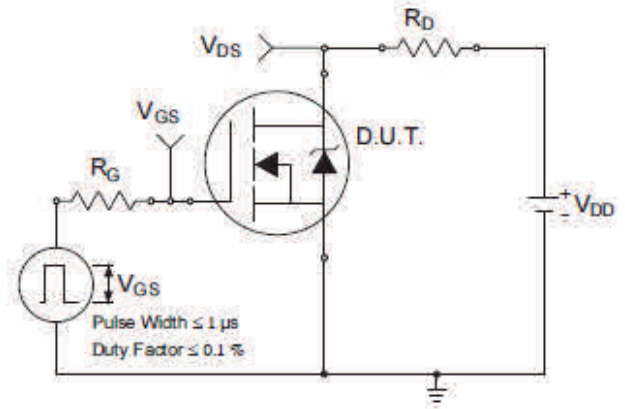


Fig 10a. Switching Time Test Circuit

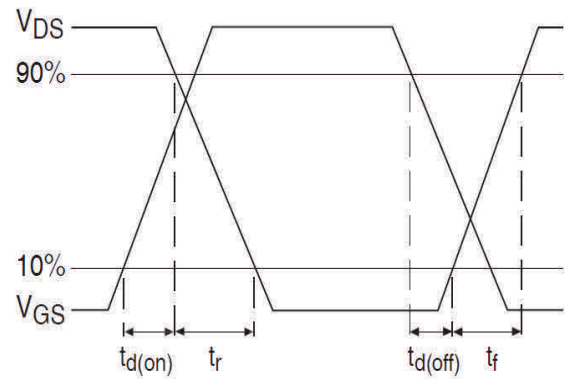


Fig 10b. Switching Time Waveforms

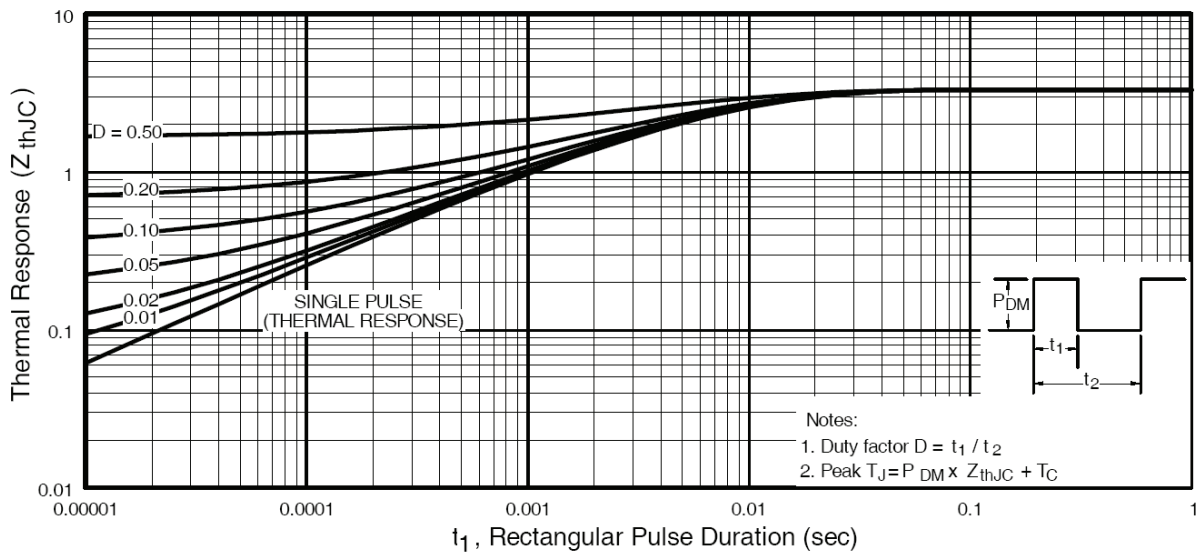
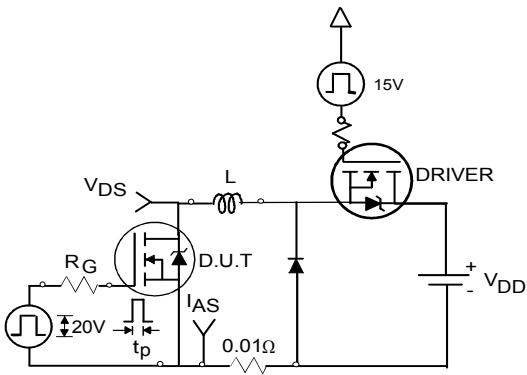
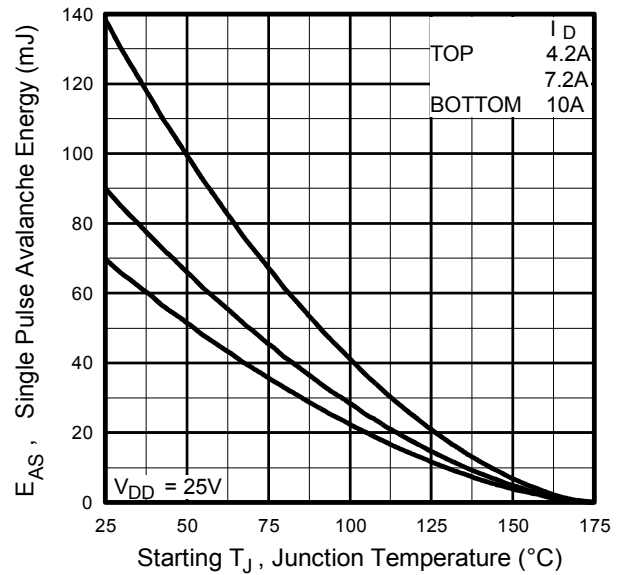
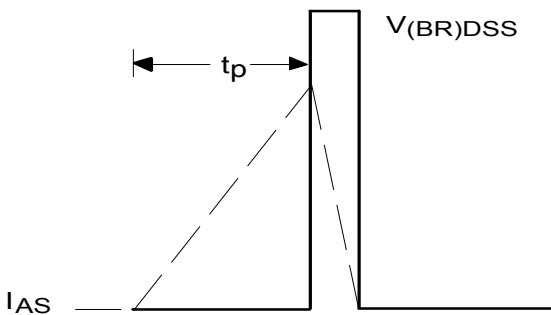
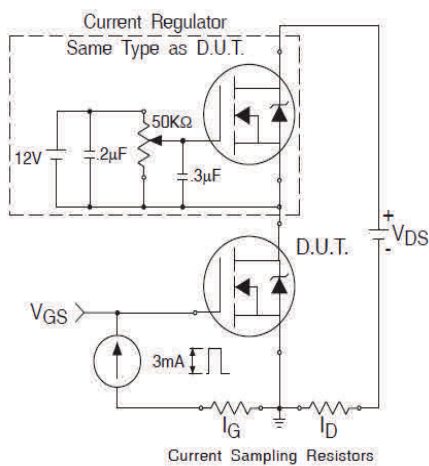
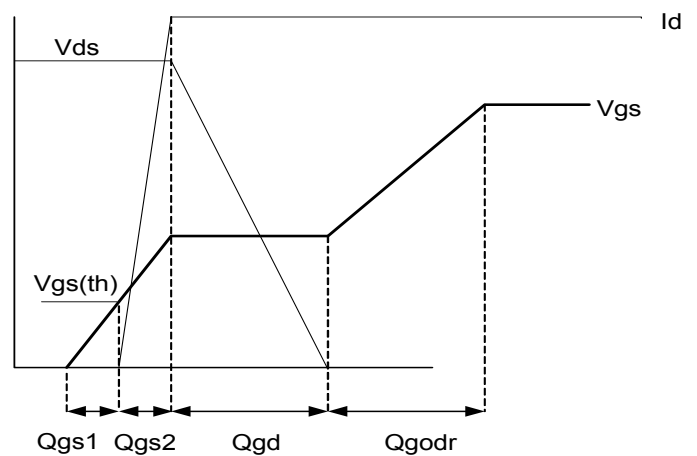


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Test Circuit

Fig 13b. Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit

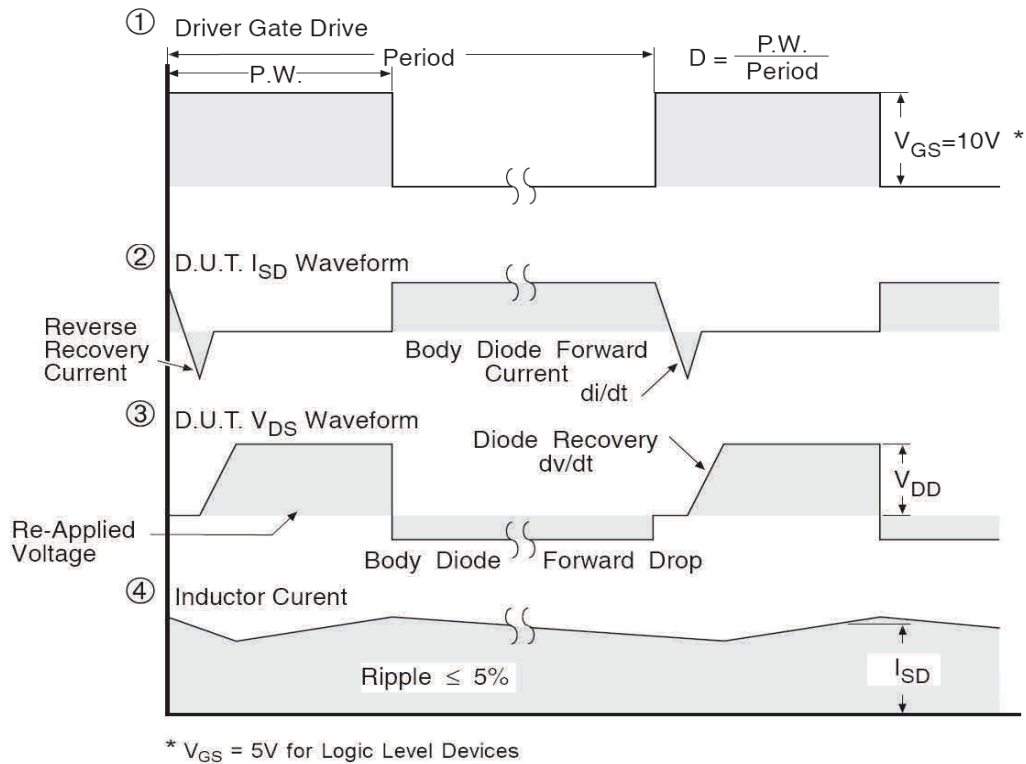
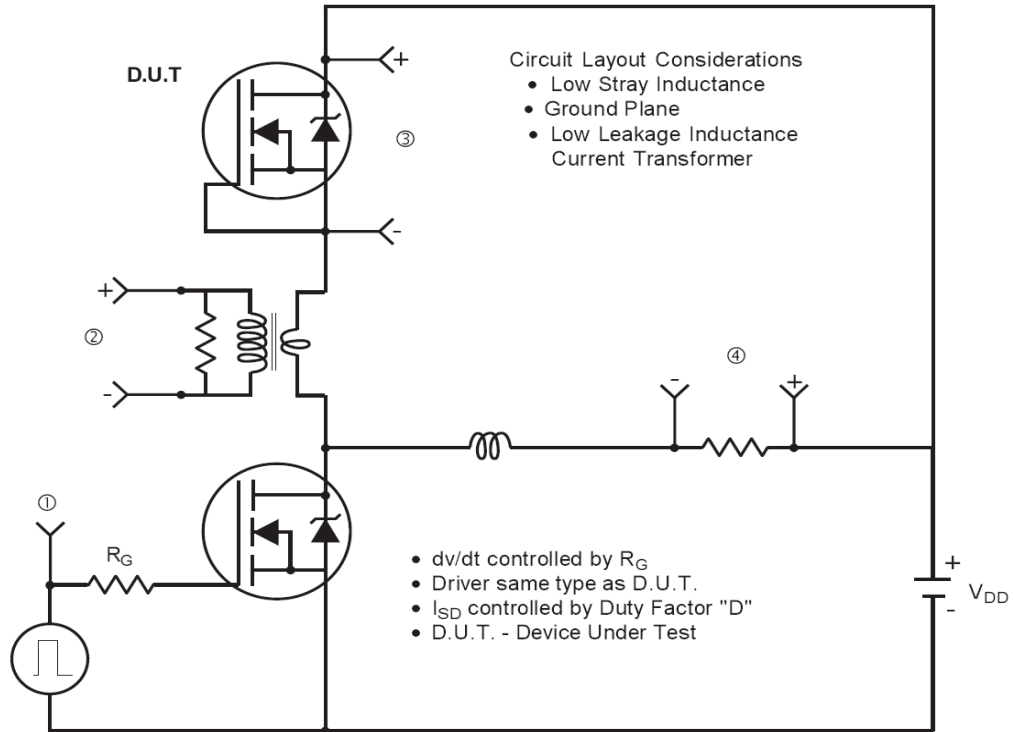
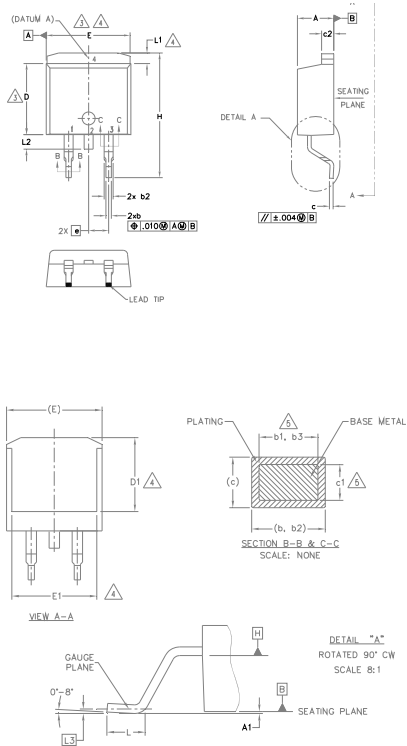


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D²- Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

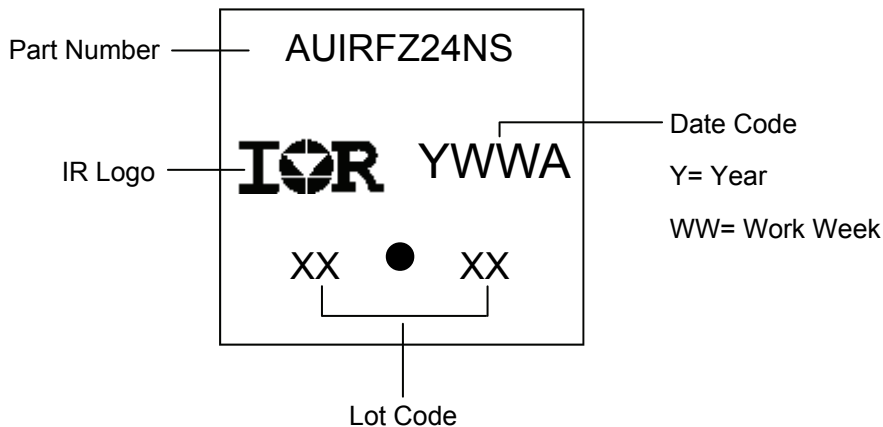
HEXFET

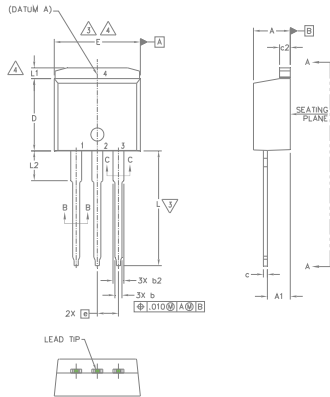
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

D²- Pak (TO-263AB) Part Marking Information



TO-262 Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS
IGBTs, CoPACK

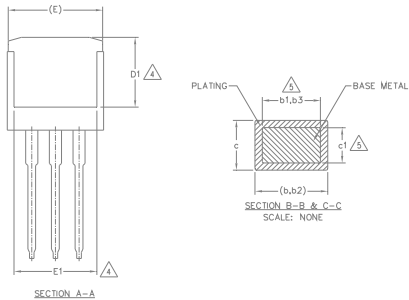
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

HEXFET

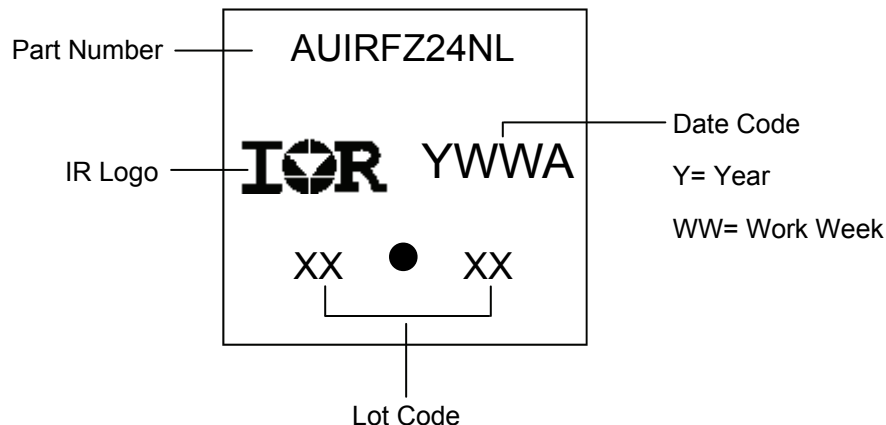
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	4
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	

TO-262 Part Marking Information


Technical drawing of a 2x2 array of microstrip patch antennas. The drawing includes top and side views of the antenna array, a detailed view of the patch antenna, and a detailed view of the feed structure. Dimensions are given in inches and millimeters. The feed direction is indicated by arrows.

Top View Dimensions:

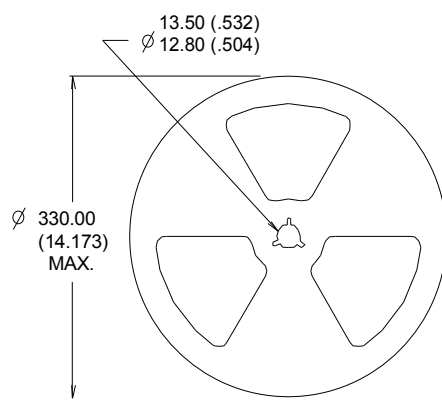
- Overall width: 16.10 (.634)
- Overall height: 11.60 (.457)
- Distance between patch centers (horizontal): 10.90 (.429)
- Distance between patch centers (vertical): 11.40 (.449)
- Distance from left edge to first patch center: 4.10 (.161)
- Distance from right edge to last patch center: 1.60 (.063)
- Distance from top edge to first patch center: 1.85 (.073)
- Distance from bottom edge to last patch center: 1.50 (.059)
- Distance from left edge to first patch center: 3.90 (.153)
- Distance from right edge to last patch center: 1.50 (.059)
- Distance from top edge to first patch center: 1.60 (.063)
- Distance from bottom edge to last patch center: 1.50 (.059)

Side View Dimensions:

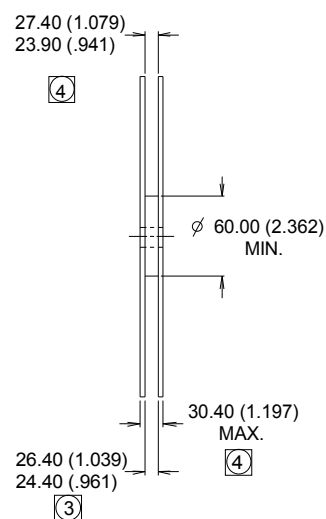
- Overall height: 24.30 (.957)
- Distance from top edge to patch center: 15.42 (.609)
- Distance from bottom edge to patch center: 15.22 (.601)
- Distance from top edge to patch center: 23.90 (.941)
- Distance from bottom edge to patch center: 4.72 (.136)
- Distance from top edge to patch center: 4.52 (.178)

Feed Structure Dimensions:

- Distance from top edge to feed center: 0.368 (.0145)
- Distance from bottom edge to feed center: 0.342 (.0135)



- NOTES :
1. COMFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D ² -Pak	MSL1
		TO-262	
ESD	Machine Model	Class M2 (+/- 150V) [†] AEC-Q101-002	
	Human Body Model	Class H1A (+/- 500V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
10/27/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1.
10/13/2017	<ul style="list-style-type: none"> Corrected typo error on part marking on page 8,9.

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