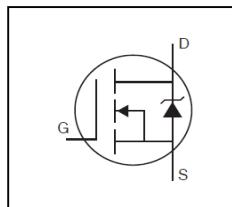


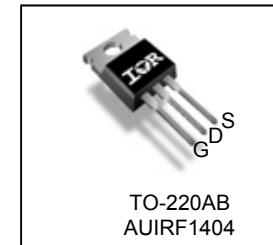
**Features**

- Advanced Planar Technology
- Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



HEXFET® Power MOSFET

$V_{DSS}$	40V
$R_{DS(on)}$ typ.	3.5mΩ
	4.0mΩ
$I_D$ (Silicon Limited)	202A⑥
$I_D$ (Package Limited)	160A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF1404	TO-220	Tube	50	AUIRF1404

**Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	202A⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	143	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	160	
$I_{DM}$	Pulsed Drain Current ①	808	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	333	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	620	mJ
$I_{AR}$	Avalanche Current ①	See Fig.15,16, 12a, 12b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	1.5	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1N·m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

HEXFET® is a registered trademark of Infineon.

 \*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.039	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	3.5	4.0	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 121\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Trans conductance	76	—	—	S	$V_{DS} = 25\text{V}, I_D = 121\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	100	$\text{nA}$	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

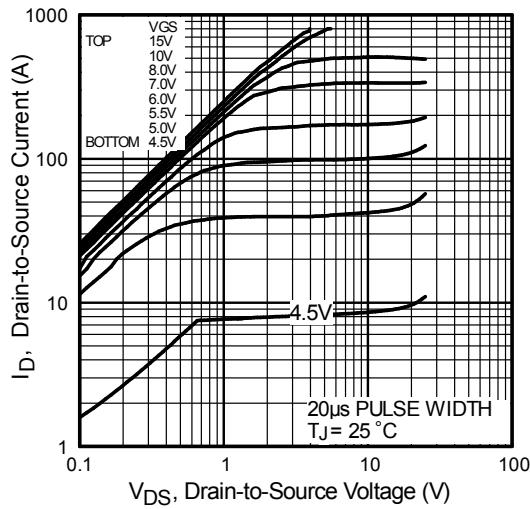
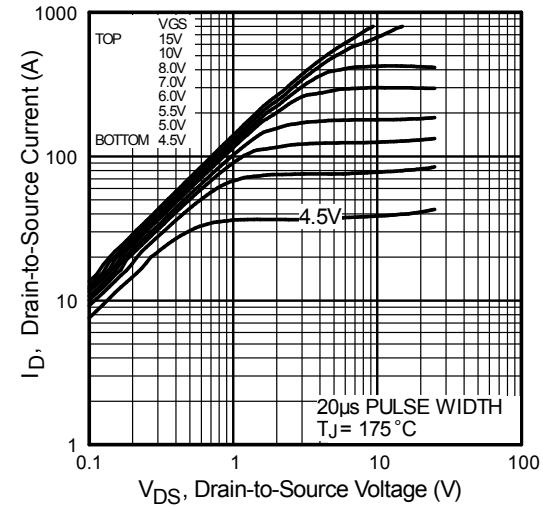
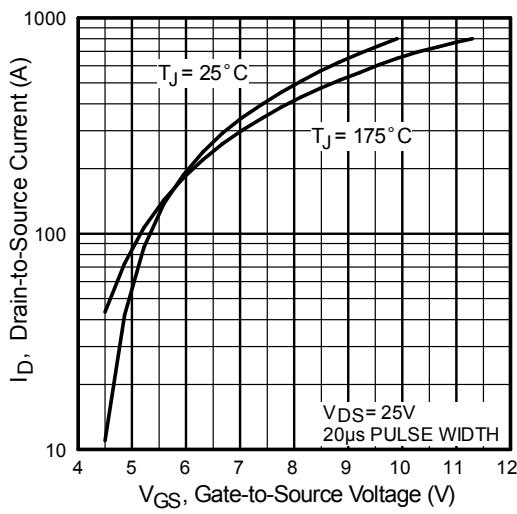
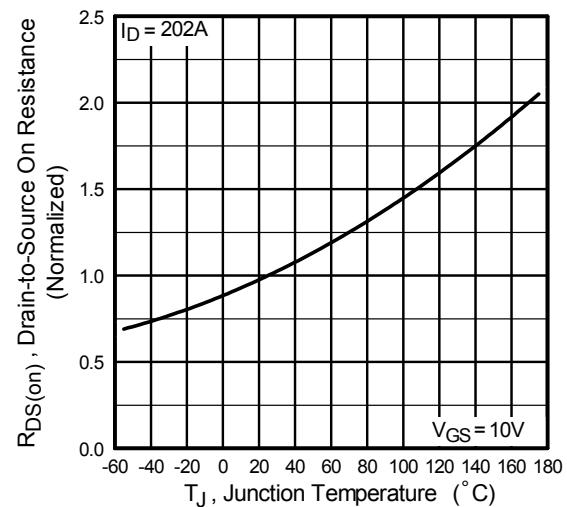
$Q_g$	Total Gate Charge	—	131	196	nC	$I_D = 121\text{A}$ $V_{DS} = 32\text{V}$ $V_{GS} = 10\text{V}$ ④
$Q_{gs}$	Gate-to-Source Charge	—	36	—		
$Q_{gd}$	Gate-to-Drain Charge	—	37	56		
$t_{d(\text{on})}$	Turn-On Delay Time	—	17	—		$V_{DD} = 20\text{V}$
$t_r$	Rise Time	—	190	—		$I_D = 121\text{A}$
$t_{d(\text{off})}$	Turn-Off Delay Time	—	46	—	ns	$R_G = 2.5\Omega$
$t_f$	Fall Time	—	33	—		$R_D = 0.2\Omega$
$L_D$	Internal Drain Inductance	—	4.5	—		Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—	nH	
$C_{iss}$	Input Capacitance	—	5669	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	1659	—		$V_{DS} = 25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	223	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	6205	—		$V_{GS} = 0\text{V}, V_{DS} = 1.0\text{V}$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1467	—		$V_{GS} = 0\text{V}, V_{DS} = 32\text{V}$ $f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	2249	—		$V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$

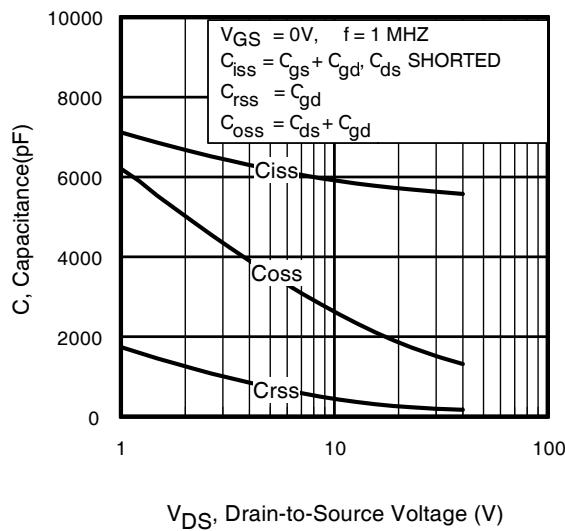
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	202⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{sM}$	Pulsed Source Current (Body Diode) ①	—	—	808		
$V_{SD}$	Diode Forward Voltage	—	—	1.5		$T_J = 25^\circ\text{C}, I_s = 121\text{A}, V_{GS} = 0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	78	117		$T_J = 25^\circ\text{C}, I_F = 121\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	163	245		$di/dt = 100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

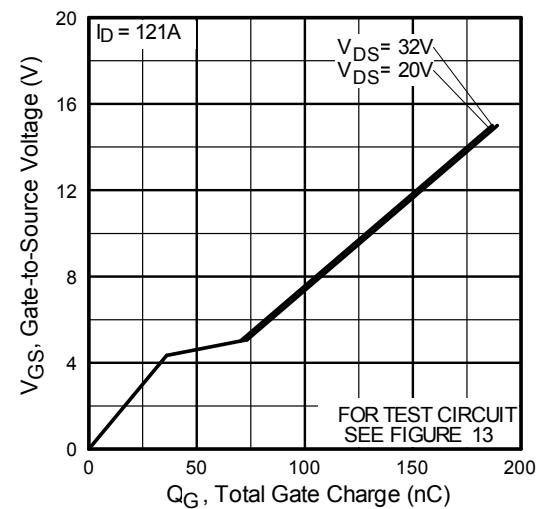
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② starting  $T_J = 25^\circ\text{C}$ ,  $L = 85\mu\text{H}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 121\text{A}$ ,  $V_{GS} = 10\text{V}$ . (See fig. 12)
- ③  $I_{SD} \leq 121\text{A}$ ,  $di/dt \leq 130\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 160A.
- ⑦  $R_g$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

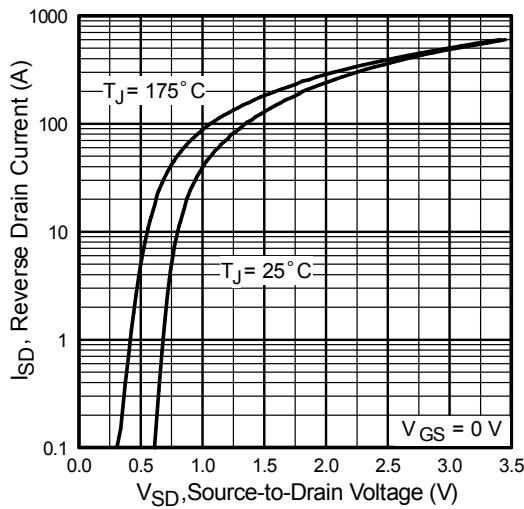
**Fig. 1** Typical Output Characteristics**Fig. 2** Typical Output Characteristics**Fig. 3** Typical Transfer Characteristics**Fig. 4** Normalized On-Resistance vs. Temperature



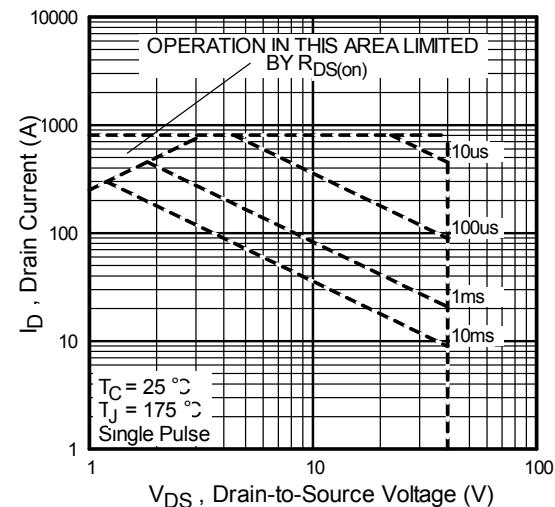
**Fig 5.** Typical Capacitance vs.  
Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs.  
Gate-to-Source Voltage



**Fig. 7** Typical Source-to-Drain Diode  
Forward Voltage



**Fig 8.** Maximum Safe Operating Area

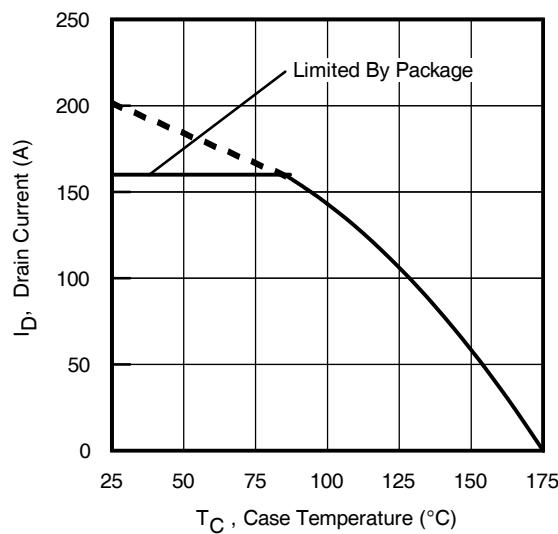


Fig 9. Maximum Drain Current vs. Case Temperature

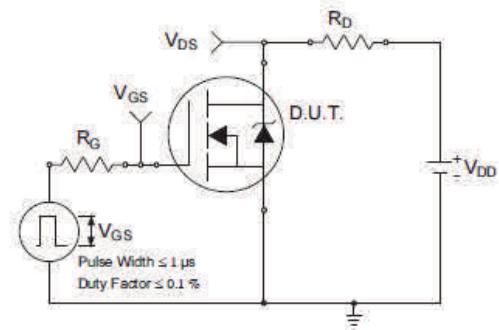


Fig 10a. Switching Time Test Circuit

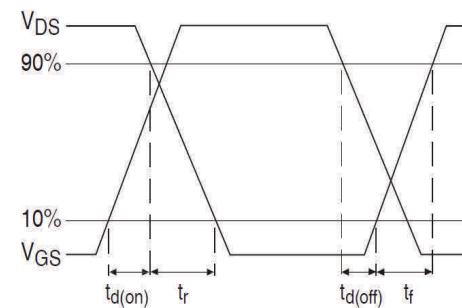


Fig 10b. Switching Time Waveforms

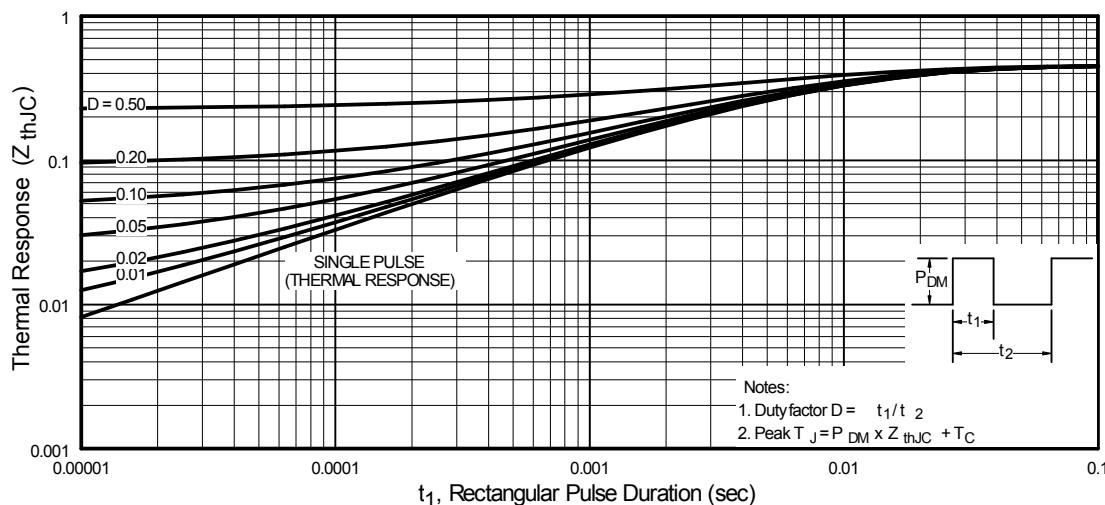


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

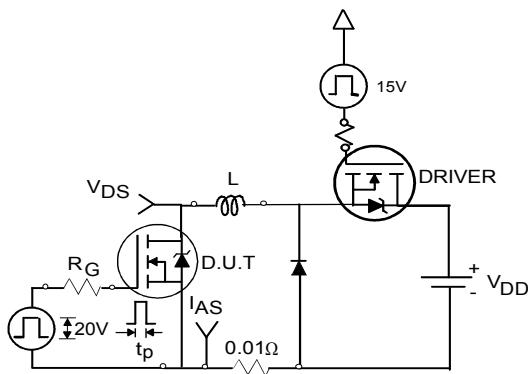


Fig 12a. Unclamped Inductive Test Circuit

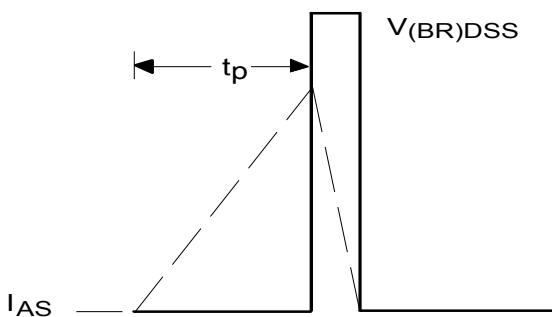


Fig 12b. Unclamped Inductive Waveforms

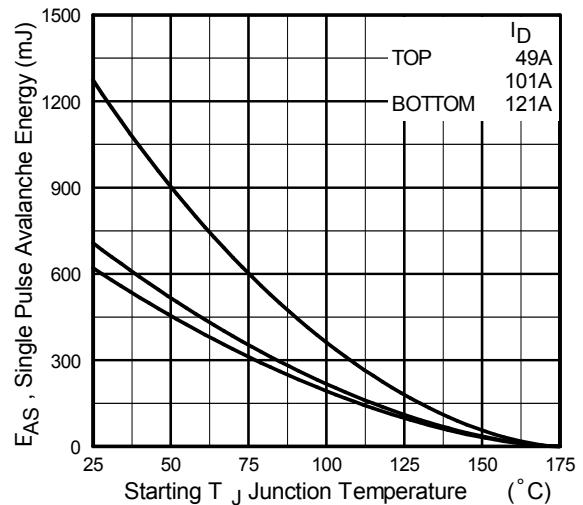


Fig 12c. Maximum Avalanche Energy vs. Drain Current

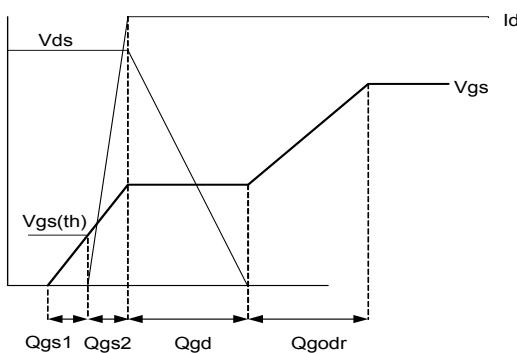


Fig 13a. Gate Charge Waveform

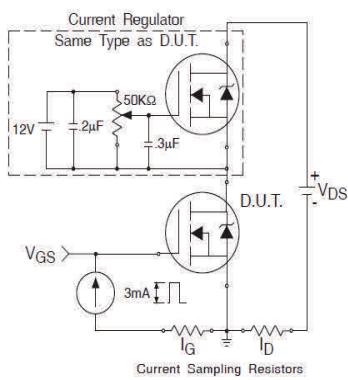


Fig 13b. Gate Charge Test Circuit

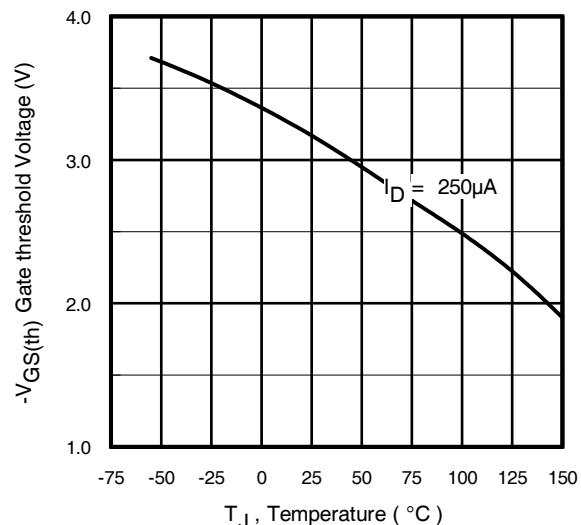
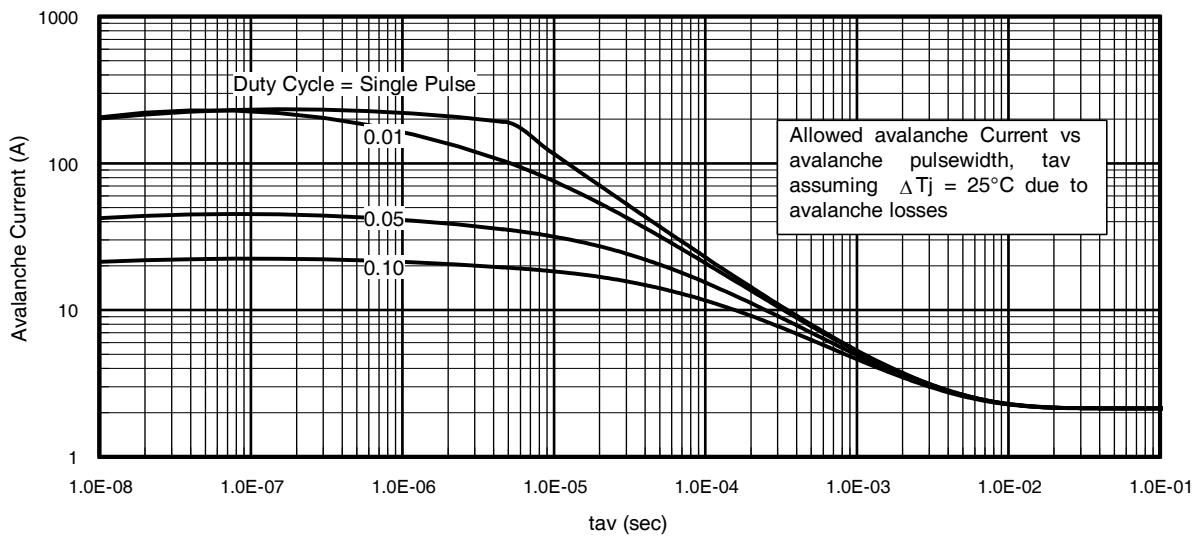
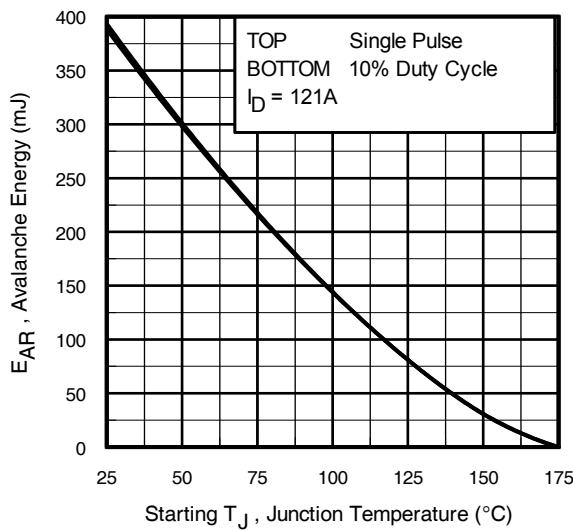


Fig 14. Threshold Voltage vs. Temperature



**Fig 15.** Typical Avalanche Current vs. Pulse width



**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).

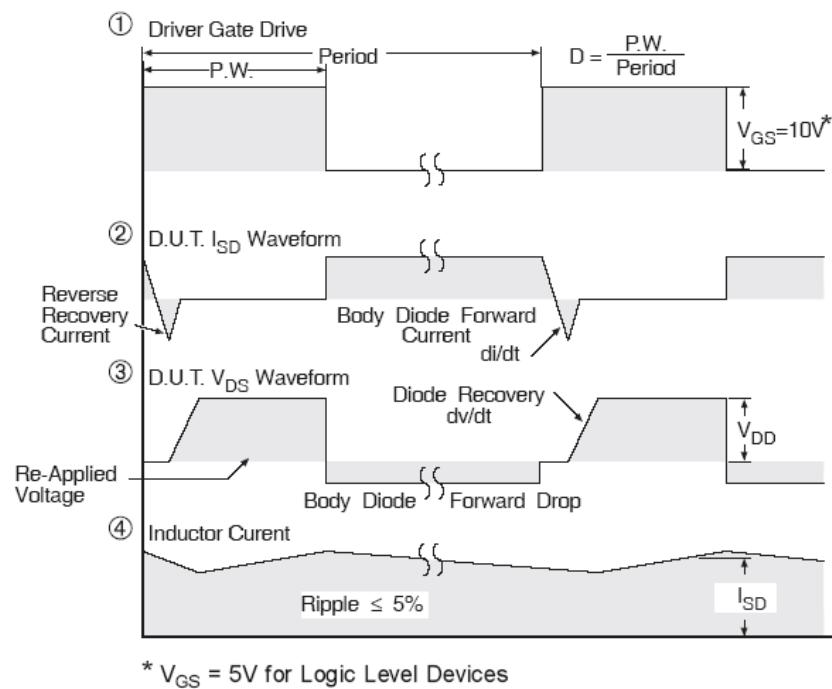
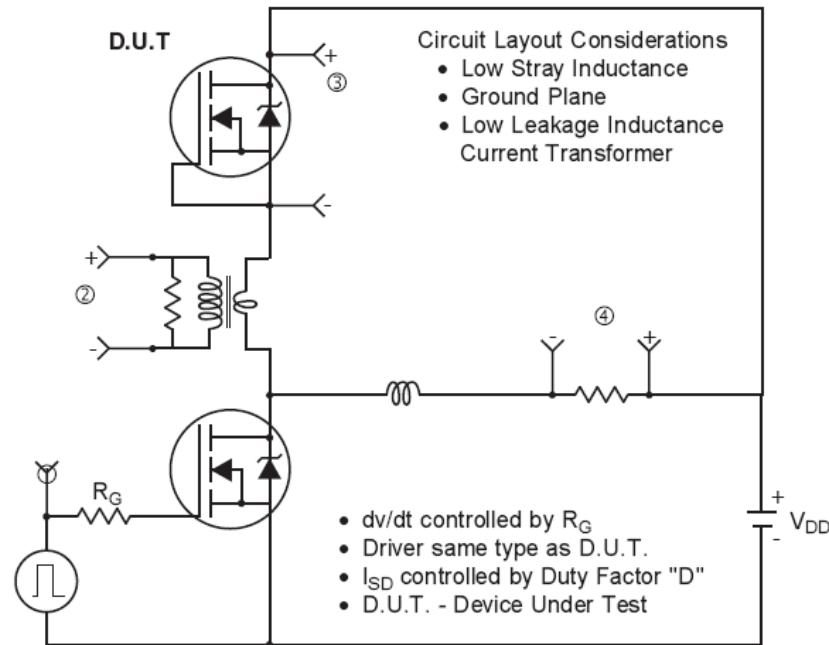
tav = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, tav)$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

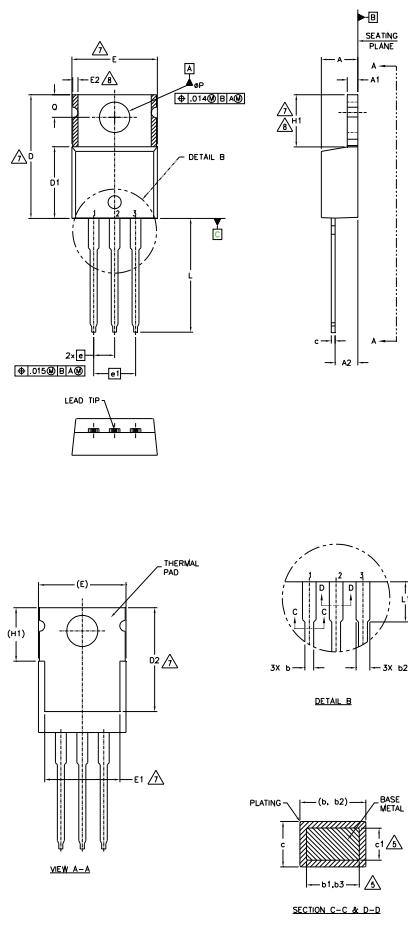
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

## Peak Diode Recovery dv/dt Test Circuit



**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

## TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



## NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E1, H1, D2 & E2
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.83	.140	.190		
A1	1.14	1.40	.045	.055		
A2	2.03	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.97	.015	.038	5	
b2	1.14	1.78	.045	.070	5	
b3	1.14	1.73	.045	.068	5	
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650	4	
D1	8.38	9.02	.330	.355		
D2	11.68	12.88	.460	.507	7	
E	9.65	10.67	.380	.420	4,7	
E1	6.86	8.89	.270	.350	7	
E2	—	0.76	—	.030	8	
e	2.54 BSC		.100 BSC			
e1	5.08 BSC		.200 BSC			
H1	5.84	6.86	.230	.270	7,8	
L	12.70	14.73	.500	.580		
L1	3.56	4.06	.140	.160	3	
OP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		

## LEAD ASSIGNMENTS

## HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

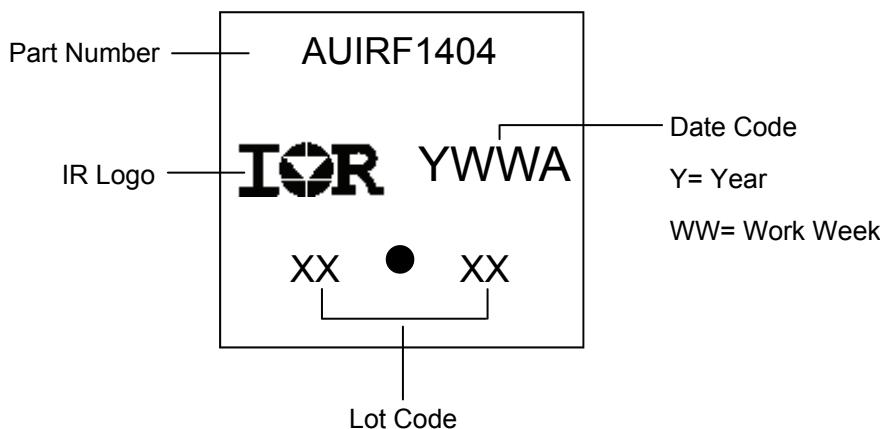
## IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter

## DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

## TO-220AB Part Marking Information



TO-220AB package is not recommended for Surface Mount Application.

## Qualification Information

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		TO-220AB	N/A
<b>ESD</b>	Machine Model	Class M4 (+/- 425V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

<sup>†</sup> Highest passing voltage.

## Revision History

Date	Comments
9/30/2015	<ul style="list-style-type: none"> <li>• Updated datasheet with corporate template.</li> <li>• Corrected typo on IDSS test condition on page 2.</li> <li>• Updated Package outline on page 9.</li> </ul>
9/18/2017	<ul style="list-style-type: none"> <li>• Corrected typo error on part marking on page 9.</li> </ul>

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