

# **CIPOS™ Maxi IPM**

## IM12B10CC1, 1200 V 10 A

### **Description**

The CIPOS™ Maxi IM12B10CC1 product offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs. It is designed to control three phase AC motors and permanent magnet motors in variable speed drives applications such as low power motor drives (GPI, Servo drives), pumps, fan drives and active filter for HVAC (Heating, Ventilation, and Air Conditioning). The product concept is specially adapted to power applications, which need good thermal performance and electrical isolation as well as EMI save control and overload protection. Three phase inverter with 1200 V TRENCHSTOP™ IGBTs and Emitter Controlled diodes are combined with an optimized 6-channel SOI gate driver for excellent electrical performance.

### **Features**

#### Package

- Fully isolated Dual In-Line molded module
- Very low thermal resistance due to DCB substrate
- · Lead-free terminal plating; RoHS compliant

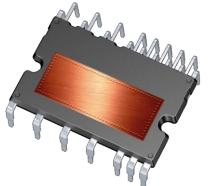
#### Inverter

- 1200 V TRENCHSTOP<sup>™</sup> IGBT7 S7
- Rugged 1200 V SOI gate driver technology with stability against transient and negative voltage
- Allowable negative V<sub>S</sub> potential up to -11 V for signal transmission at V<sub>BS</sub> = 15 V
- Integrated bootstrap functionality
- Overcurrent shutdown
- Built-in NTC thermistor for temperature monitoring
- Undervoltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection
- · Programable fault clear timing and enable input

## **Potential applications**

Fan drives and pumps Active filter for HVAC Low power motor drives (GPI, Servo drives)





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## **Product validation**

## **Product validation**

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

### **Table 1** Product information

Base part number	Dackage type	Stand	Domark	
	Package type	Form	моQ	Remark
IM12B10CC1	DIP 36x23D	14 pcs / Tube	280 pcs	



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**Internal electrical schematic** 



## 1 Internal electrical schematic

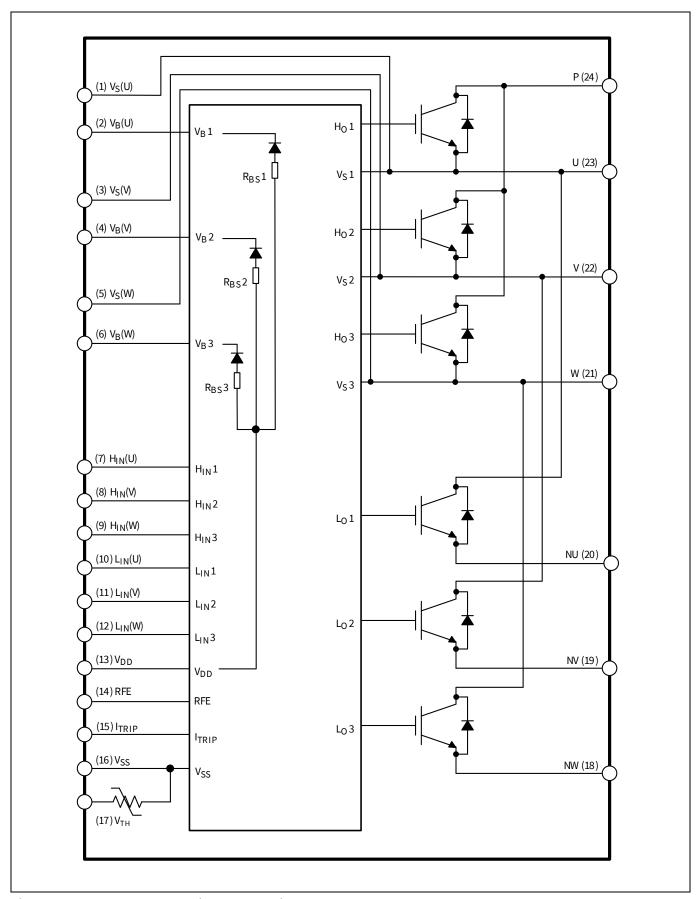


Figure 1 Internal electrical schematic

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### Pin description

# 2 Pin description

## 2.1 Pin assignment

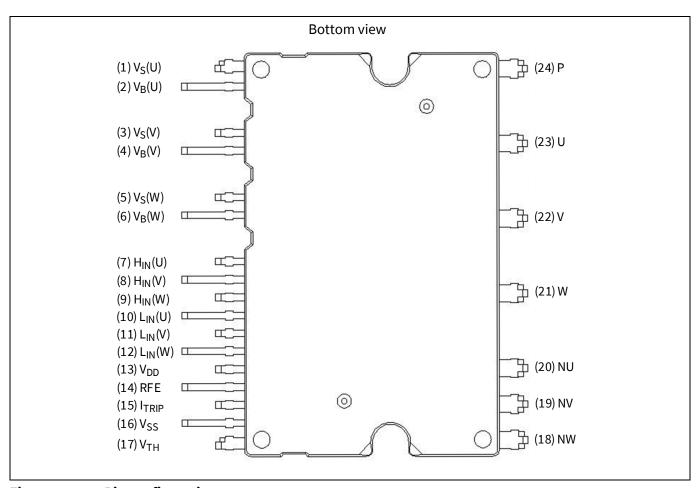


Figure 2 Pin configuration

Table 2 Pin assignment

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Pin number	Pin name	Pin description
1	V <sub>S</sub> (U)	U-phase high-side floating IC supply offset voltage
2	V <sub>B</sub> (U)	U-phase high-side floating IC supply voltage
3	V <sub>S</sub> (V)	V-phase high-side floating IC supply offset voltage
4	V <sub>B</sub> (V)	V-phase high-side floating IC supply voltage
5	V <sub>S</sub> (W)	W-phase high-side floating IC supply offset voltage
6	V <sub>B</sub> (W)	W-phase high-side floating IC supply voltage
7	H <sub>IN</sub> (U)	U-phase high-side gate driver input
8	H <sub>IN</sub> (V)	V-phase high-side gate driver input
9	H <sub>IN</sub> (W)	W-phase high-side gate driver input
10	L <sub>IN</sub> (U)	U-phase low-side gate driver input
11	L <sub>IN</sub> (V)	V-phase low-side gate driver input
12	L <sub>IN</sub> (W)	W-phase low-side gate driver input
13	V <sub>DD</sub>	Low-side control supply



### Pin description

Pin number	Pin name	Pin description
14	RFE	Programmable fault clear time, fault output, enable input
15	I <sub>TRIP</sub>	Overcurrent shutdown input
16	V <sub>SS</sub>	Low-side control negative supply
17	V <sub>TH</sub>	Temperature output
18	NW	W-phase low-side emitter
19	NV	V-phase low-side emitter
20	NU	U-phase low-side emitter
21	W	Motor W-phase output
22	V	Motor V-phase output
23	U	Motor U-phase output
24	Р	Positive bus input voltage

## 2.2 Pin description

# $H_{IN}$ (U, V, W) and $L_{IN}$ (U, V, W) (High-side pins, Pin 7 – 9 and Low-side pins, Pin 10 - 12)

These pins are positive logic, and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 5 k $\Omega$  is internally provided to pre-bias inputs during supply start-up. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time  $t_{\text{FIL}, IN}$  The filter acts according to Figure 4. It is not recommended for proper work to provide input pulse-width lower than 1  $\mu$ s.

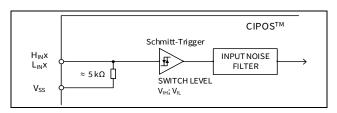


Figure 3 Input pin structure

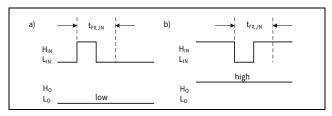


Figure 4 Input filter timing diagram

The integrated gate driver provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e.,  $H_01$  and  $L_01$ ,  $H_02$  and  $L_02$ ,  $H_03$  and  $L_03$ ). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 360 ns is also provided by driver IC, in order to reduce crossconduction of the external power switches.

#### RFE (Fault / Fault-clear time / Enable, Pin 14)

The RFE pin combines three functions in one pin: programmable fault clear time by RC network, fault out and enable input.

The programmable fault-clear time can be adjusted by RC network, which is external pull-up resistor and capacitor. For example, typical value is about 1 ms at 1 M $\Omega$  and 2 nF. The fault-out indicates a module failure in case of undervoltage at pin V<sub>DD</sub> or in case of triggered overcurrent detection at I<sub>TRIP</sub>. The microcontroller can pull this pin low to disable the IPM functionality. This is enabling function.

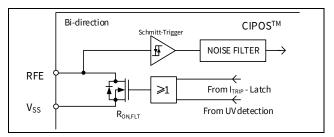


Figure 5 Internal circuit at pin RFE

# CIPOS™ Maxi IPM

### IM12B10CC1, 1200 V 10 A

#### Pin description



The  $V_{TH}$  pin provides direct access to the NTC thermistor, which is referenced to  $V_{SS}$ . An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

#### I<sub>TRIP</sub> (Over-current detection function, Pin 15)

The IM12B10CC1 product provides an overcurrent detection function by connecting the  $I_{TRIP}$  input with the IGBT current feedback. The  $I_{TRIP}$  comparator threshold (typical 0.5 V) is referenced to  $V_{SS}$  ground. An input noise filter ( $I_{ITRIP}$  = typ. 500 ns) prevents the driver to detect false overcurrent events.

Overcurrent detection generates a shutdown of outputs of the gate driver. After the shutdown propagation delay of typically 1  $\mu$ s.

The fault-clear time is set to typical 1.1 ms at  $R_{RCIN} = 1 \text{ M}\Omega$  and  $C_{RCIN} = 2 \text{ nF}$ .

# V<sub>DD</sub>, V<sub>SS</sub> (Control supply and reference, Pin 13 and reference, Pin 16)

 $V_{\text{DD}}$  is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to  $V_{\text{SS}}$  ground.

The undervoltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of  $V_{DDUV+} = 12.2 \text{ V}$  is present.

The IC shuts down all the gate drivers power outputs, when the  $V_{DD}$  supply voltage is below  $V_{DDUV} = 11.2 \text{ V}$ . This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.



# $V_B(U, V, W)$ and $V_S(U, V, W)$ (High-side supplies, Pin 1 - 6)

 $V_B$  to  $V_S$  is the high-side supply voltage. The high-side circuit can float with respect to  $V_{SS}$  following the external high-side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typical  $V_{BSUV+} = 11.2 \text{ V}$  and a falling threshold of  $V_{BSUV-} = 10.2 \text{ V}$ .

 $V_{s}$  (U, V, W) provide a high robustness against negative voltage in respect of  $V_{ss}$  of -50 V transiently. This ensures very stable designs even under rough conditions.

### NW, NV, NU (Low-side emitter, Pin 18 - 20)

The low-side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin  $V_{SS}$  as short as possible in order to avoid unnecessary inductive voltage drops.

# W, V, U (High-side emitter and low-side collector, Pin 21 - 23)

These pins are connected to motor U, V, W input pins.

### P (Positive bus input voltage, Pin 24)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 900 V.

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### **Absolute maximum ratings**

# 3 Absolute maximum ratings

 $(V_{DD} = 15 \text{ V and } T_{J} = 25^{\circ}\text{C}$ , if not stated otherwise)

## 3.1 Module section

Description	Symbol	Condition	Value	Unit
Storage temperature range	$T_{STG}$		-40 ~ 125	°C
Operating case temperature	T <sub>c</sub>	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	TJ		-40 ~ 150	°C
Isolation voltage	V <sub>ISO</sub>	1 min, RMS, f = 60 Hz	2500	V

## 3.2 Inverter section

Description	Symbol	Condition	Value	Unit	
Maximum blocking voltage	V <sub>CES</sub> /V <sub>RRM</sub>	Ι <sub>C</sub> = 250 μΑ	1200	V	
DC link supply voltage of P - N	$V_{PN}$	Applied between P - N	900	V	
DC link supply voltage (surge) of P - N	$V_{PN(Surge)}$	Applied between P - N	1000	V	
Callagta a suggesti		$T_{C} = 25^{\circ}C, T_{J} < 150^{\circ}C$	±16	А	
Collector current <sup>1</sup>	I <sub>C</sub>	$T_{C} = 80^{\circ}C, T_{J} < 150^{\circ}C$	±10		
Maximum peak collector current	I <sub>CP</sub>	$T_C = 25$ °C, $T_J < 150$ °C, limited by $T_{Jmax.}$	±20	А	
Power dissipation per IGBT	P <sub>tot</sub>		55	W	
Short circuit withstand time	t <sub>sc</sub>	$V_{DD} = 15 \text{ V}, V_{DC} \le 800 \text{ V}, T_{J} \le 150^{\circ}\text{C}$	5	μs	

## 3.3 Control section

Description	Symbol	Condition	Value	Unit
High-side offset voltage	Vs		1200	V
Repetitive peak reverse voltage of bootstrap diode	$V_{RRM}$		1200	V
Module control supply voltage	$V_{DD}$	Applied between V <sub>DD</sub> - V <sub>SS</sub>	-1 ~ 20	V
High-side floating supply voltage (V <sub>B</sub> reference to V <sub>S</sub> )	$V_{BS}$	Applied between V <sub>B</sub> - V <sub>S</sub>	-1 ~ 20	V
Input voltage (L <sub>IN</sub> , H <sub>IN</sub> , I <sub>TRIP</sub> , RFE)	V <sub>IN</sub>		-1 ~ V <sub>DD</sub> + 0.3	V

## Thermal characteristics

#### **Thermal characteristics** 4

Dogovinskien	Compleal	Condition		11		
Description	Symbol Condition		Min.	Тур.	Max.	Unit
Single IGBT thermal resistance, junction-case	$R_{thJC}$	High-side V-phase	-	-	2.25	K/W
Single diode thermal resistance, junction-case	R <sub>thJC, D</sub>	(See Figure 7 for T <sub>c</sub> measurement point)	-	-	2.80	K/W

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## **Recommended operation conditions**

# 5 Recommended operation conditions

All voltages are absolute voltages referenced to V<sub>SS</sub>-potential unless otherwise specified.

D	Completed		I I mit		
Description	Symbol	Min.	Тур.	Max.	Unit
DC link supply voltage of P - N	$V_{PN}$	350	600	800	V
Low-side supply voltage	$V_{DD}$	13.5	15	18.5	V
High-side floating supply voltage (V <sub>B</sub> vs. V <sub>S</sub> )	$V_{BS}$	12.5	-	18.5	V
Logic input voltages L <sub>IN</sub> , H <sub>IN</sub> , I <sub>TRIP</sub> , RFE	V <sub>IN</sub> V <sub>ITRIP</sub> V <sub>RFE</sub>	0	-	5	V
Inverter PWM carrier frequency	f <sub>PWM</sub>	-	-	20	kHz
External dead time between H <sub>IN</sub> & L <sub>IN</sub>	DT	0.5	-	-	μs
Voltage between V <sub>ss</sub> - N (including surge)	V <sub>COMP</sub>	-5	-	5	V
Minimum input pulse width	PW <sub>IN(ON)</sub> , PW <sub>IN(OFF)</sub>	1	-	-	μs
Control supply variation	$\Delta V_{BS}$ $\Delta V_{DD}$	-1 -1	-	1 1	V/µs

## **Static parameters**



# **6** Static parameters

 $(V_{DD} = 15 \text{ V and } T_{J} = 25^{\circ}\text{C}$ , if not stated otherwise)

## 6.1 Inverter section

Description	Ch al	Candition	Value			11!4
Description	Symbol	Condition	Min.	Тур.	Max.	Unit
Collector-emitter saturation voltage	V <sub>CE(Sat)</sub>	$I_{c} = 10 \text{ A}, T_{J} = 25^{\circ}\text{C}$	-	1.90	2.30	V
		$I_C = 10 \text{ A}, T_J = 150^{\circ}\text{C}$	-	2.30	-	
Collector-emitter leakage current	I <sub>CES</sub>	V <sub>CE</sub> = 1200 V	-	-	1	mA
5	.,	I <sub>F</sub> = 10 A, T <sub>J</sub> = 25°C	-	1.85	2.20	
Diode forward voltage	$V_{F}$	$I_F = 10 \text{ A}, T_J = 150^{\circ}\text{C}$	-	1.80	-	V

## 6.2 Control section

Description	Cumbal	Candition		Value		llm:4
Description	Symbol	Condition	Min.	Тур.	Max.	Unit
Logic "1" input voltage (L <sub>IN</sub> , H <sub>IN</sub> )	V <sub>IH</sub>		-	1.9	2.3	V
Logic "0" input voltage (L <sub>IN</sub> , H <sub>IN</sub> )	V <sub>IL</sub>		0.7	0.9	-	V
I <sub>TRIP</sub> positive going threshold	$V_{IT,TH^+}$		475	500	525	mV
I <sub>TRIP</sub> input hysteresis	$V_{IT,HYS}$		-	55	-	mV
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage	$V_{\text{DDUV+}}$		11.5	12.2	13.0	V
positive going threshold	$V_{BSUV}$		10.5	11.2	12.0	V
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage	$V_{ extsf{DDUV}}$		10.5	11.2	12.0	V
negative going threshold	$V_{BSUV}$		9.5	10.2	11.0	V
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage lockout hysteresis	V <sub>DDUVH</sub> , V <sub>BSUVH</sub>		-	1.0	-	V
Quiescent V <sub>BSx</sub> supply current (V <sub>BSx</sub> only)	I <sub>QBS</sub>	V <sub>HIN</sub> = 0 V	-	175	-	μА
Quiescent V <sub>DD</sub> supply current (V <sub>DD</sub> only)	I <sub>QDD</sub>	$V_{LIN} = 0 V, V_{HINX} = 5 V$	-	1.0	-	mA
Input bias current for L <sub>IN</sub> , H <sub>IN</sub>	I <sub>IN+</sub>	V <sub>IN</sub> = 5 V	-	1.0	-	mA
Input bias current for ITRIP	I <sub>ITRIP+</sub>	$V_{ITRIP} = 5 V$	-	30	100	μΑ
Input bias current for RFE	I <sub>RFE</sub>	$V_{RFE} = 5 \text{ V}, V_{ITRIP} = 0 \text{ V}$	-	-	5	μΑ
RFE output voltage	$V_{RFE}$	$I_{RFE} = 10 \text{ mA}, V_{ITRIP} = 1 \text{ V}$	-	0.4	-	V
V <sub>RFE</sub> positive going threshold	$V_{RFE,TH^+}$		-	1.9	2.3	V
V <sub>RFE</sub> negative going threshold	$V_{RFE,TH ext{-}}$		0.7	0.9	-	V
Bootstrap diode forward voltage	$V_{F,BSD}$	$I_F = 0.3 \text{ mA}$	-	0.9	-	V
Bootstrap diode resistance	R <sub>BSD</sub>	Between $V_F = 4 V$ and $V_F = 5 V$	-	120	-	Ω

## **Dynamic parameters**



# 7 Dynamic parameters

 $(V_{DD} = 15 \text{ V and } T_J = 25^{\circ}\text{C}$ , if not stated otherwise)

## 7.1 Inverter section

B				Value			
Description	Symbol	Condition	Min.	Тур.	Max.	Unit	
Turn-on propagation delay time	t <sub>on</sub>		-	755	-	ns	
Turn-on rise time	t <sub>r</sub>	$V_{\text{LIN, HIN}} = 5 \text{ V},$	-	25	-	ns	
Turn-on switching time	t <sub>c(on)</sub>	$I_{C} = 10 \text{ A},$ $V_{DC} = 600 \text{ V}$	-	155	-	ns	
Reverse recovery time	t <sub>rr</sub>	VDC 300 V	-	190	-	ns	
Turn-off propagation delay time	t <sub>off</sub>	$V_{\text{LIN, HIN}} = 0 \text{ V},$	-	950	-	ns	
Turn-off fall time	t <sub>f</sub>	I <sub>C</sub> = 10 A,	-	135	-	ns	
Turn-off switching time	t <sub>c(off)</sub>	V <sub>DC</sub> = 600 V	-	195	-	ns	
Short circuit propagation delay time	t <sub>SCP</sub>	From V <sub>IT, TH+</sub> to 10% I <sub>SC</sub>	-	1110	-	ns	
IGBT turn-on energy (includes reverse recovery of diode)	E <sub>on</sub>	V <sub>DC</sub> = 600 V, I <sub>C</sub> = 10 A T <sub>J</sub> = 25°C 150°C	-	0.86 1.43	-	mJ	
IGBT turn-off energy	E <sub>off</sub>	V <sub>DC</sub> = 600 V, I <sub>C</sub> = 10 A T <sub>J</sub> = 25°C 150°C	-	0.48 0.81	-	mJ	
Diode recovery energy	E <sub>rec</sub>	$V_{DC} = 600 \text{ V}, I_{C} = 10 \text{ A}$ $T_{J} = 25^{\circ}\text{C}$ $150^{\circ}\text{C}$		0.25 0.57	-	mJ	

## 7.2 Control section

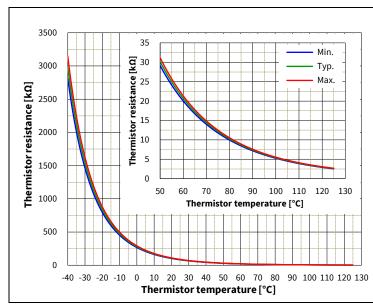
D	Complete al	Canaditi an	Value		11*4	
Description	Symbol	Condition	Min.	Тур.	Max.	Unit
Input filter time I <sub>TRIP</sub>	t <sub>ITRIP</sub>	V <sub>ITRIP</sub> = 1 V	-	500	-	ns
Input filter time at $L_{\text{IN}}$ , $H_{\text{IN}}$ for turn on and off	t <sub>FIL, IN</sub>	$V_{LIN, HIN} = 0 V \text{ or } 5 V$	-	350	-	ns
Fault clear time after I <sub>TRIP</sub> -fault	t <sub>FLT, CLR</sub>	$V_{ITRIP} = 1 V,$ $V_{pull-up} = 5 V$ $(R = 1 M\Omega, C = 2 nF)$	-	1.1	-	ms
I <sub>TRIP</sub> to fault propagation delay	t <sub>FLT</sub>	$V_{LIN, HIN} = 0 \text{ or } 5 \text{ V},$ $V_{ITRIP} = 1 \text{ V}$	-	650	900	ns
Internal deadtime	DT <sub>IC</sub>	$V_{IN} = 0$ or $V_{IN} = 5$ V	300	-	-	ns
Matching propagation delay time (On & Off) all channels	M <sub>T</sub>	External dead time > 500 ns	-	-	130	ns

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### **Thermistor characteristics**

## **8** Thermistor characteristics

Paravirtia:	Complete	Condition	Value			11:4
<b>Description</b>	Symbol	Condition	Min.	Тур.	Max.	Unit
Resistance	R <sub>NTC</sub>	T <sub>NTC</sub> = 25°C	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient) thermistor	B (25/100)		-	4092	-	К



Temp. [°C]	R <sub>Min.</sub> [kΩ]	R <sub>Typ.</sub> [kΩ]	$R_{Max.}[k\Omega]$
50	29.151	30.157	31.178
60	20.018	20.669	21.329
70	13.994	14.424	14.858
80	9.946	10.234	10.523
90	7.177	7.373	7.569
100	5.253	5.388	5.523
110	3.884	3.99	4.096
120	2.908	2.991	3.075
125	2.527	2.601	2.676

Figure 6 Thermistor resistance – temperature curve and table
(For more information, please refer to application note 'AN-2024-05 CIPOS™ Maxi IPM IM12BxxxC1 Series application note'.)

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## **Mechanical characteristics and ratings**

# 9 Mechanical characteristics and ratings

Description	Candition	Value			11:4
	Condition	Min.	Тур.	Max.	N·m
Comparative Tracking Index (CTI)		600	-	-	
Mounting torque	M3 screw and washer	0.49	-	0.78	N⋅m
Backside curvature	Refer to Figure 8	0	-	150	μm
Weight		-	7.1	-	g



## **Qualification information**

#### **Qualification information** 10

UL certification	File number: E314539		
Moisture sensitivity level	-		
RoHS compliant	Yes (Lead-free terminal plating)		
ESD (Electrostatic Discharge)	HBM (Human body model) class	2	
	CDM (Charged device model) class	C3	



**Diagrams and tables** 

## 11 Diagrams and tables

## 11.1 T<sub>c</sub> measurement point

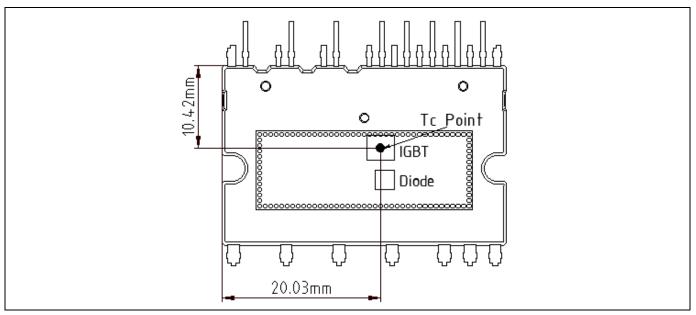


Figure 7 T<sub>c</sub> measurement point<sup>1</sup>

## 11.2 Backside curvature measurement point

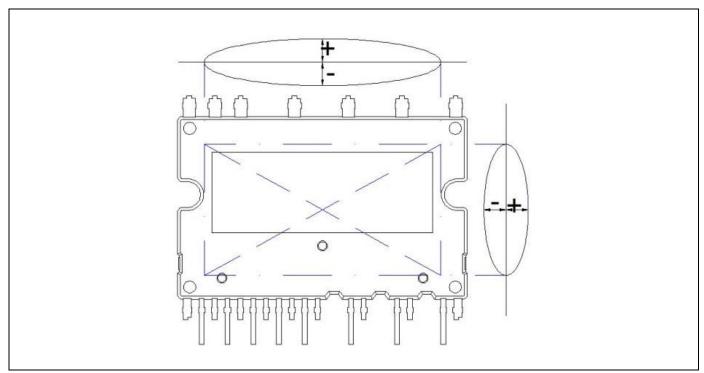


Figure 8 Backside curvature measurement position

V 1.00

<sup>&</sup>lt;sup>1</sup>Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.



## Diagrams and tables

## 11.3 Switching time definition

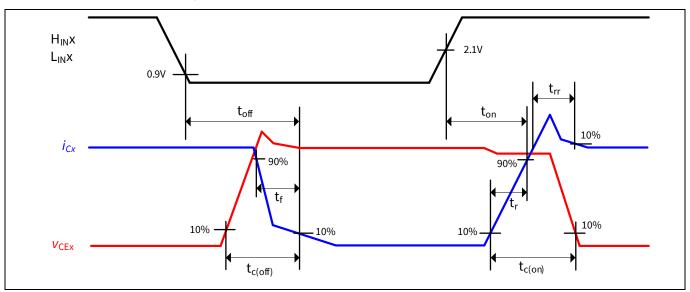


Figure 9 Switching times definition

# 11.4 Sleep function timing diagram

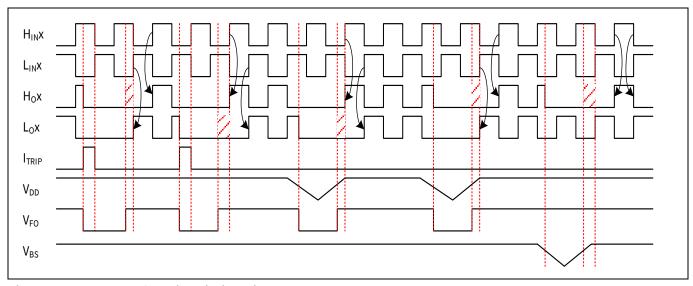


Figure 10 Sleep function timing diagram

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#### **Application guide**

## 12 Application guide

## 12.1 Typical application schematic

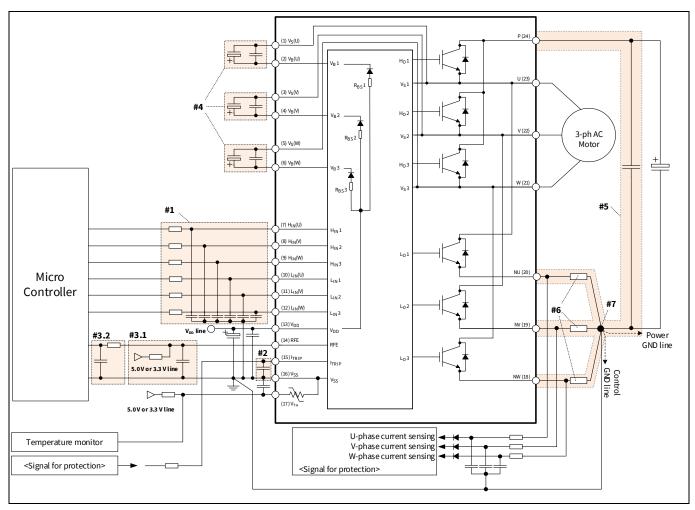


Figure 11 Typical application circuit

#### 1. Input circuit

- To reduce input signal noise by high speed switching, the R<sub>IN</sub> and C<sub>IN</sub> filter circuit should be mounted. (100 Ω, 1 nF)
- C<sub>IN</sub> should be placed as close to V<sub>SS</sub> pin as possible.

### 2. $I_{TRIP}$ circuit

- To prevent protection function errors, C<sub>ITRIP</sub> should be placed as close to I<sub>TRIP</sub> and V<sub>SS</sub> pins as possible.
- To prevent fault operation of the protection function, an RC filter is recommended around 1.5~2.0  $\mu$ s (68  $\Omega$ , 22 nF, "Signal for protection" in the schematic leads the signal into the microcontroller").

### RFE circuit

- 3.1 Pull-up resistor and pull-down capacitor
- RFE output is an open drain output. This signal line should be pulled up to the positive side of the 5.0 V/3.3 V logic power supply with a proper resistor  $R_{PU}$ .
- The fault-clear time is adjusted by RC network of a pull-up resistor, a pull-down capacitor and pull-up voltage.
  - $t_{FLT, CLR} = -R_{pull-up} \cdot C_{pull-down} \cdot ln(1 V_{RFE, TH+} / V_{pull-up}) + internal fault-clear time 160 \mu s$
  - $t_{FLT, CLR} = -1 \text{ M}\Omega \times 2 \text{ nF} \times \ln(1 1.9 / 5 \text{ V}) + 160 \text{ μs} \cong 1.1 \text{ ms at R} = 1 \text{ M}\Omega, C = 2 \text{ nF and V}_{pull-up} = 5 \text{ V}$
  - $\blacksquare$  A pull-up resistor is limited to max. 2 MΩ

#### 3.2 RC filter

- It is recommended that RC filter be placed as close to the controller as possible.



### **Application guide**

- 4. V<sub>B</sub>-V<sub>S</sub> circuit
  - Capacitor for high side floating supply voltage should be placed as close to V<sub>B</sub> and V<sub>S</sub> pins as possible.
- 5. Snubber capacitor
  - The wiring between IPM and snubber capacitor including shunt resistor should be as short as possible.
- 6. Shunt resistor
  - The shunt resistor of SMD type should be used for reducing its stray inductance.
- 7. Ground pattern
  - Ground pattern should be separated at only one point of shunt resistor as short as possible.

### 12.2 Performance chart

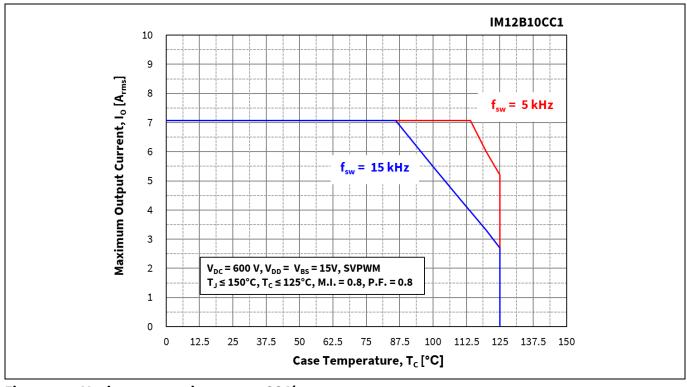


Figure 12 Maximum operating current SOA<sup>1</sup>

2024-05-15

<sup>&</sup>lt;sup>1</sup>This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

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#### **Package outline 13**

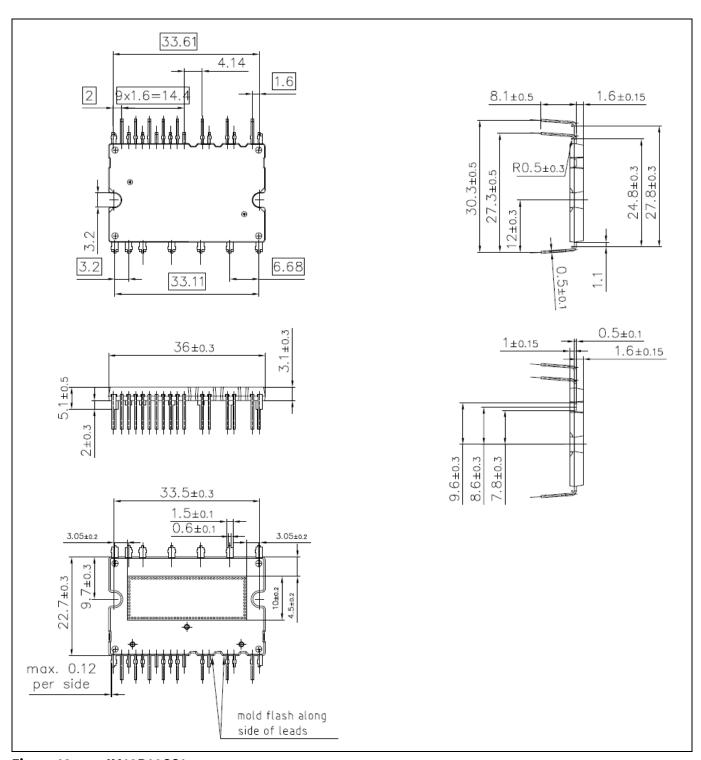


Figure 13 IM12B10CC1



**Revision history** 

# **Revision history**

Document version	Date of release	Description of changes
V 1.00	2024-05-15	Initial release

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