S71KS512SC0
S71KL256SC0
S71KL512SC0

SUPPLEMENT

HyperFlash™ and HyperRAM™ Multi-Chip Package 1.8V/3V

Distinctive Characteristics

- HyperFlash™ and HyperRAM™ in Multi-Chip Package (MCP)
  - 1.8V, 512 Mb HyperFlash and 64 Mbit HyperRAM (S71KS512SC0)
  - 3.0V, 512 Mb HyperFlash and 64 Mbit HyperRAM (S71KL512SC0)
  - 3.0V, 256 Mb HyperFlash and 64 Mbit HyperRAM (S71KL256SC0)
  - FBGA 24-ball, 6 × 8 × 1.0 mm package
- HyperBus Interface
  - 1.8V I/O, 12 bus signals
    - Differential clock (CK/CK#)
  - 3.0V I/O, 11 bus signals
    - Single ended clock (CK)
  - Chip Select (CS#)
  - 8-bit data bus (DQ[7:0])
  - Read-Write Data Strobe (RWDS)
    - Bidirectional Data Strobe/Mask
    - Output at the start of all transactions to indicate refresh latency
    - Output during read transactions as Read Data Strobe
    - Input during write transactions as Write Data Mask (HyperRAM only)
- Optional Signals
  - Reset
  - INT# output to generate external interrupt
    - Busy to Ready Transition
  - RSTO# Output to generate system level Power-On Reset (POR)
    - User configurable RSTO# Low period
- High Performance
  - Double-Data Rate (DDR)
    - Two data transfers per clock
  - Up to 166-MHz clock rate (333 MB/s) at 1.8V V_{CC}
  - Up to 100-MHz clock rate (200 MB/s) at 3.0V V_{CC}

Contents

General Description

This supplementary datasheet provides MCP device related information for a HyperBus MCP family, incorporating both HyperFlash and HyperRAM memories. The document describes how the features, operation, and ordering options of the related memories have been enhanced or changed from the standard memory devices incorporated in the MCP. The information contained in this document modifies any information on the same topics established by the documents listed in Table 1 and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the listed documents. The information is intended for hardware system designers and software developers of applications, operating systems, or tools.

Table 1. Affected Documents/Related Documents

Title	Cypress Publication Number
HyperBus™ Specification Low Signal Count, High Performance DDR Bus	001-99253
S26KL512S / S26KS512S / S26KL256S / S26KS256S / S26KL128S / S26KS128S, 512 MBIT (64 MBYTE), 256 Mbit (32 Mbyte), 128 Mbit (16 Mbyte) 1.8V/3.0V HyperFlash™ Family	001-99198
S27KL0641, S27KS0641, S71KL1281, S71KS1281: HyperRAM™ Self-Refresh DRAM 3.0V/ 1.8V 64/128 Mbit (8/16 Mbyte)	001-97964

HyperBus MCP Family with HyperFlash and HyperRAM

For systems needing both Flash and self-refresh DRAM, the HyperBus products family includes MCP devices that combine HyperFlash and HyperRAM in a single package. A HyperBus MCP reduces board space and Printed Circuit Board (PCB) signal routing congestion while also maintaining or improving signal integrity over separately packaged memory configurations.

The HyperBus MCP family offers 1.8V/3V interface HyperFlash densities of 512 Mb (64 Mbyte) and 256 Mb (32 Mbyte) in combination with HyperRAM 64 Mb (8 Mbyte).

This supplemental datasheet addresses only the MCP related differences from the HyperBus Specification and the individual HyperFlash and HyperRAM datasheets. For all other information related to the individual memories in the MCP, refer to the HyperBus, HyperFlash, and HyperRAM datasheets.

HyperBus MCP 3 V Signal Descriptions

Figure 1. HyperBus MCP Signal Diagram

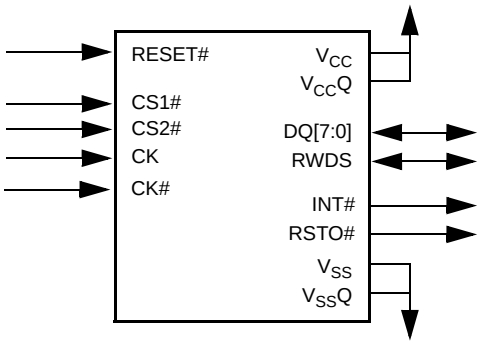
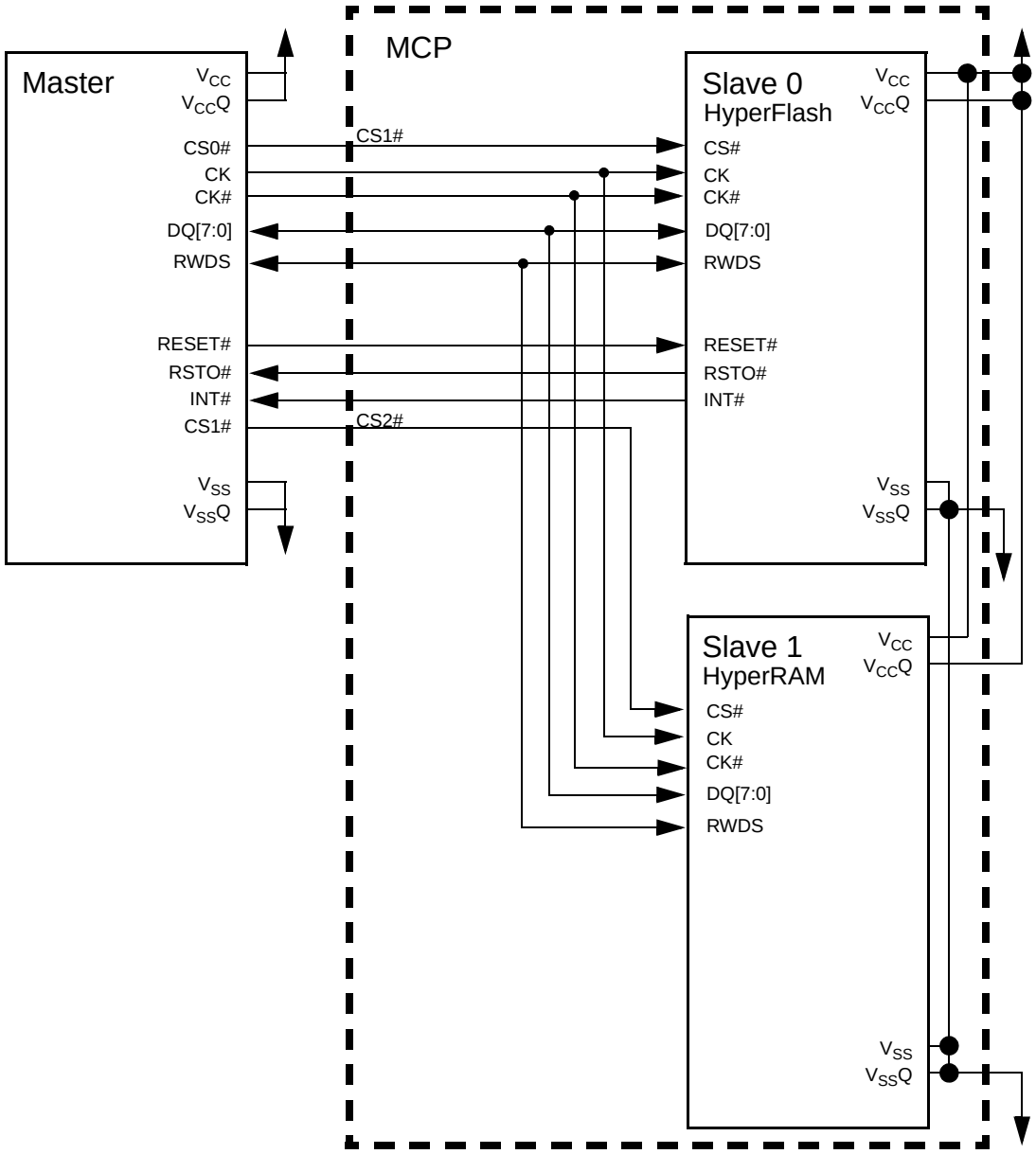


Table 2. Signal Descriptions

Symbol	Type	Description
CS1#	Input	Chip Select 1: Chip Select for the HyperFlash memory. HyperBus transactions are initiated with a High to Low transition. HyperBus transactions are terminated with a Low to High transition.
CS2#	Input	Chip Select 2: Chip Select for the HyperRAM memory. HyperBus transactions are initiated with a High to Low transition. HyperBus transactions are terminated with a Low to High transition.
CK	Input	Single-ended Clock 3.0V: Command-Address/Data information is input or output with respect to the edges of the CK. Note: Single-ended clock is available on 3.0V devices only.
CK/CK#	Input	Differential Clock 1.8V: Command-Address/Data information is input or output with respect to the crossing edges of the CK/CK# pair. Note: Differential clock is available on 1.8V devices only.
RWDS	Output	Read-Write Data Strobe: Output data during read transactions are edge aligned with RWDS. RWDS is an input during write transactions to function as a HyperRAM data mask. At the beginning of all bus transactions RWDS is an output and indicates whether additional initial latency count is required. 1 = Additional latency count 0 = No additional latency count
DQ[7:0]	Input/Output	Data Input/Output: Command-Address/Data information is transferred on these DQs during Read and Write transactions.
INT#	Output (open drain)	INT Output (Optional): When Low, the HyperFlash device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.
RESET#	Input	Hardware RESET (Optional): When Low, the HyperFlash memory will self initialize and return to the idle state. RWDS and DQ[7:0] is placed into the High-Z state when RESET# is Low. RESET# includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the High state. RESET# is not connected to the HyperRAM.
RSTO#	Output (open drain)	RSTO# Output (Optional): RSTO# is an open-drain output used to indicate when a POR is occurring within the HyperFlash memory and can be used as a system level reset signal. Upon completion of the internal POR the RSTO# signal will transition from Low to high impedance after a user defined timeout period has elapsed. Upon transition to the high impedance state the external pull-up resistance will pull RSTO# High and the device immediately is placed into the Idle state.
V_{CC}	Power Supply	Core Power
$V_{CC}Q$	Power Supply	Input/Output Power
V_{SS}	Power Supply	Core Ground
$V_{SS}Q$	Power Supply	Input/Output Ground

HyperBus MCP Block Diagram

Figure 2. HyperBus Connections Including Optional Signals

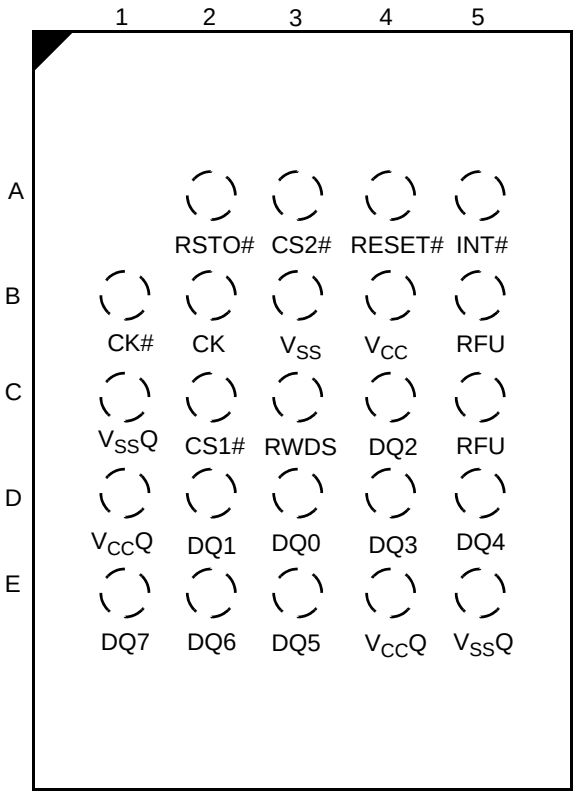


Note
1. CK# is for 1.8V devices only.

Physical Interface

HyperBus MCP — FBGA 24-Ball, 5x5 Array Footprint

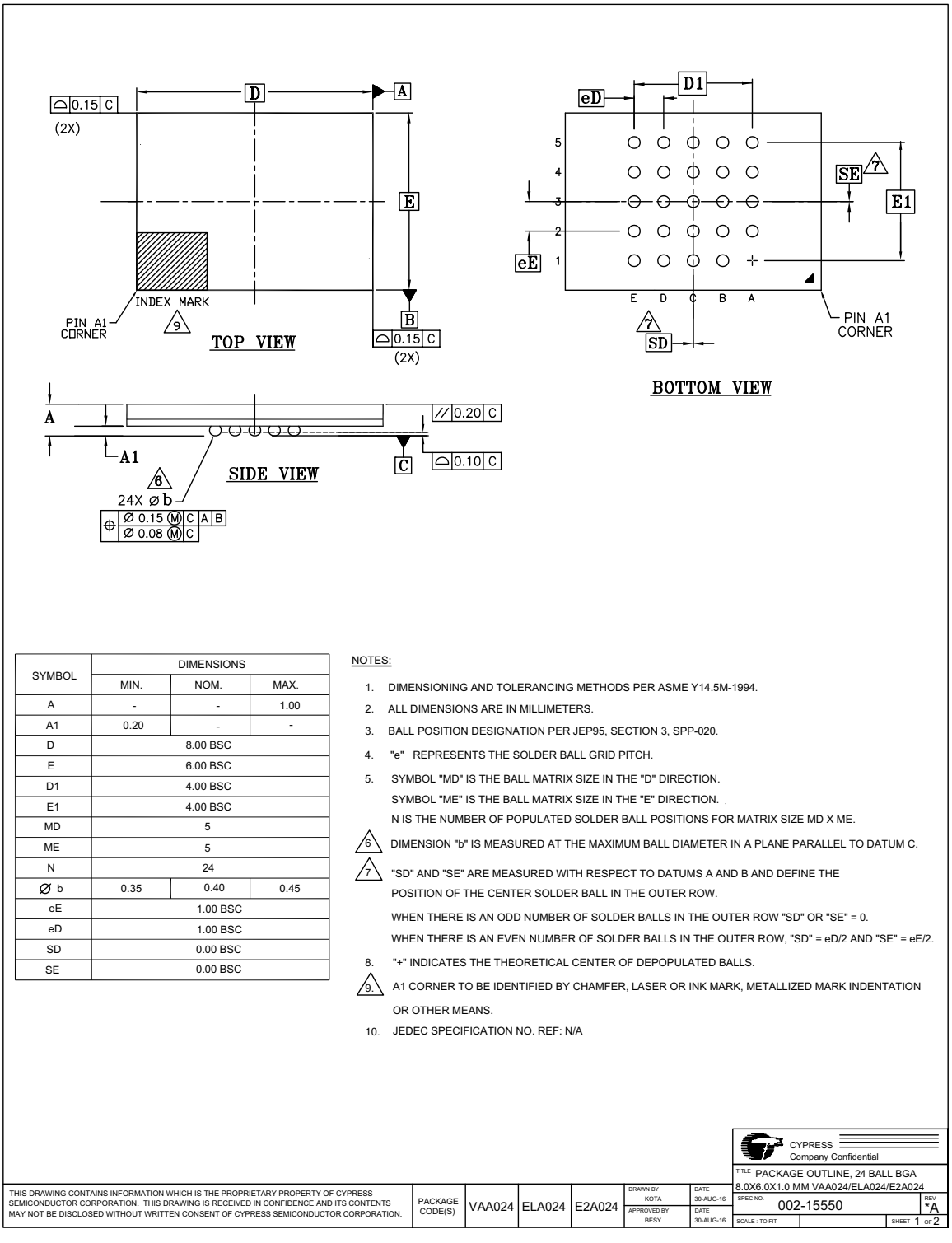
Figure 3. 24-Ball FBGA, 6 x 8 mm, 5 x 5 Ball Footprint (Top View)



Notes
2. C2 and A3 are chip select (CS#) signals 1 and 2 used for HyperFlash and HyperRAM devices respectively.
3. V_{SS} and V_{SSQ} are internally connected.
4. CK# (B1) is RFU in 3.0V devices

Physical Diagram

Figure 4. ELA024 — FBGA 24-Ball 6 x 8 x 1 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
⌀ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

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PACKAGE CODE(S)	VAA024	ELA024	E2A024	DRAWN BY KOTA	DATE 30-AUG-16
				APPROVED BY BESY	DATE 30-AUG-16

TITLE: PACKAGE OUTLINE, 24 BALL BGA 8.0X6.0X1.0 MM VAA024/ELA024/E2A024
SPEC NO. 002-15550 REV *A
SCALE : TO FIT SHEET 1 OF 2

Electrical Specifications

For the general description of the HyperBus interface electrical specifications, refer to the HyperBus Specification. The following section describes HyperFlash device dependent aspects of electrical specifications.

Absolute Maximum Ratings

Ambient Temperature with Power Applied: –65 °C to +105 °C

DC Characteristics

Only one memory may have its chip select active (Low) at any point in time. For each of the conditions below refer to the HyperFlash and HyperRAM datasheets for the most accurate information:

- Active core read or write current will be that of the selected device plus the standby current of the non-selected device. But, the added standby current is generally not significant as it is less than 300 µA.
- Active IO read current will be that of the selected device.
- Active clock stop current will be that of the selected device plus the standby current of the non-selected device. But, the added standby current is generally not significant as it is less than 300 µA.
- Program or erase current will be that of the HyperFlash device. Note however, that program and erase operations are long time frame events that extend beyond the duration of a HyperFlash chip select period. Thus, if the HyperRAM is selected for read or write during an on going HyperFlash program or erase operation, the active current will be the sum of the HyperFlash program or erase operation and the HyperRAM read or write current.
- Standby current, when neither memory is selected and no embedded flash operation is in progress, is the sum of the memory standby currents.
- Deep Power Down (DPD) current, is the sum of the memory DPD currents.
- Power On Reset (POR) current is the sum of the memory standby currents.
- Input leakage current is the sum of the memory input leakage currents.

For reference purpose, Table 3 aids in the estimation of the above operating conditions current consumption. However, refer to the HyperFlash and HyperRAM datasheets for the most accurate information.

Table 3. 3.0V DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions	Min	Typ[6]	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	±4.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	±2.0	µA
I_{CC1HF}	V_{CC} Active Read Current - HyperFlash reading (core current only, IO switching current is not included)	CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	80.2	100.3	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 1.95V	–	130.2	180.3	mA
I_{IO1HF}	V_{CC}Q Active Read Current of IOs - HyperFlash reading	CS# = V_{IL}, @100 MHz, V_{CC}Q = 3.6V, C_{LOAD} = 20 pF	–	80	100	mA
		CS# = V_{IL}, @166 MHz, V_{CC}Q = 1.95V, C_{LOAD} = 20 pF	–	80	100	mA
I_{CC1HR}	V_{CC} Active Read Current - HyperRAM reading	CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	20.1	35.3	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 1.95V	–	20.1	60.3	mA
I_{CC2HR}	V_{CC} Active Write Current - HyperRAM writing	CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	15.1	35.3	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 1.95V	–	15.1	60.3	mA
$I_{CC1HFHR}$	V_{CC} Active Read Current - HyperFlash embedded operation plus HyperRAM reading[6]	CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	80	135	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 1.95V	–	80	160	mA
$I_{CC2HFHR}$	V_{CC} Active Write Current - HyperFlash embedded operation plus HyperRAM writing[6]	CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	75	135	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 1.95V	–	75	160	mA
I_{CC3P}	V_{CC} Active Program Current[5, 6]	$V_{CC} = V_{CC}$ max	–	60	100	mA
I_{CC3E}	V_{CC} Active Erase Current[5, 6]	$V_{CC} = V_{CC}$ max	–	60	100	mA
I_{CC4I}	V_{CC} Standby Current for Industrial Temperature (–40 °C to +85 °C)	CS#, RESET# = V_{CC}, $V_{CC} = V_{CC}$ max	–	160	300	µA
I_{CC4IC}	V_{CC} Standby Current for Industrial Plus Temperature (–40 °C to +105 °C)	CS#, RESET# = V_{CC}, $V_{CC} = V_{CC}$ max	–	160	600	µA
I_{CC5}	V_{CC} Reset Current	CS# = V_{IH}, RESET# = V_{SS}, $V_{CC} = V_{CC}$ max (1.8V/3.0V)	–	10	20	mA
I_{CC6}	Active Clock Stop Mode[7]	$V_{IH} = V_{CC}$, $V_{IL} = V_{SS}$, V_{CC} = 1.95V/3.6V	–	11.3	24	mA
I_{CC7}	V_{CC} Current during Power-Up (POR)	CS# = X, $V_{CC} = V_{CC}$ max (1.95V/3.6V)	–	100	135	mA

Notes
5. I_{CC} active while Embedded Algorithm is in progress.
6. Not 100% tested.
7. Active Clock Stop Mode enables the lower power mode when the CK signals remain stable for t_{ACC} + 30 ns
8. Typical I_{CC} values are measured at t_{AI} = 25 °C and $V_{CC} = V_{CCQ}$ = 1.8V/3.0V (not applicable to I_{DPD} for 85 °C and 105 °C).

Table 3. 3.0V DC Characteristics (CMOS Compatible) (Continued)

Parameter	Description	Test Conditions	Min	Typ[6]	Max	Unit
I_{DPD}	Deep Power-Down Current 512/64 Mb @ 25°C	CS#, RESET#, V_{CC} = V_{CC} max (1.95V/3.6V) HyperFlash in Standby HyperRAM in Deep Power Down	–	34.1	112	µA
	Deep Power-Down Current 512/64 Mb @ 85°C		–	36.6	120	µA
	Deep Power-Down Current 512/64 Mb @ 105°C		–	37.4	340	µA
	Deep Power-Down Current (all other densities) @ 25°C		–	34.1	112	µA
	Deep Power-Down Current (all other densities) @ 85°C		–	37.4	140	µA
	Deep Power-Down Current (all other densities) @ 105°C		–	37.4	340	µA
	Deep Power-Down Current 512/64 Mb @ 25°C	CS#, RESET#, V_{CC} = V_{CC} max (1.95V/3.6V) HyperFlash in Deep Power Down HyperRAM in Standby		143	218	µA
	Deep Power-Down Current 512/64 Mb @ 85°C			165	250	µA
	Deep Power-Down Current 512/64 Mb @ 105°C			230	350	µA
	Deep Power-Down Current (all other densities) @ 25°C			138	206	µA
	Deep Power-Down Current (all other densities) @ 85°C			139	210	µA
	Deep Power-Down Current (all other densities) @ 105°C			140	215	µA

Notes
5. I_{CC} active while Embedded Algorithm is in progress.
6. Not 100% tested.
7. Active Clock Stop Mode enables the lower power mode when the CK signals remain stable for t_{ACC} + 30 ns
8. Typical I_{CC} values are measured at t_{AI} = 25 °C and V_{CC} = V_{CCQ} = 1.8V/3.0V (not applicable to I_{DPD} for 85 °C and 105 °C).

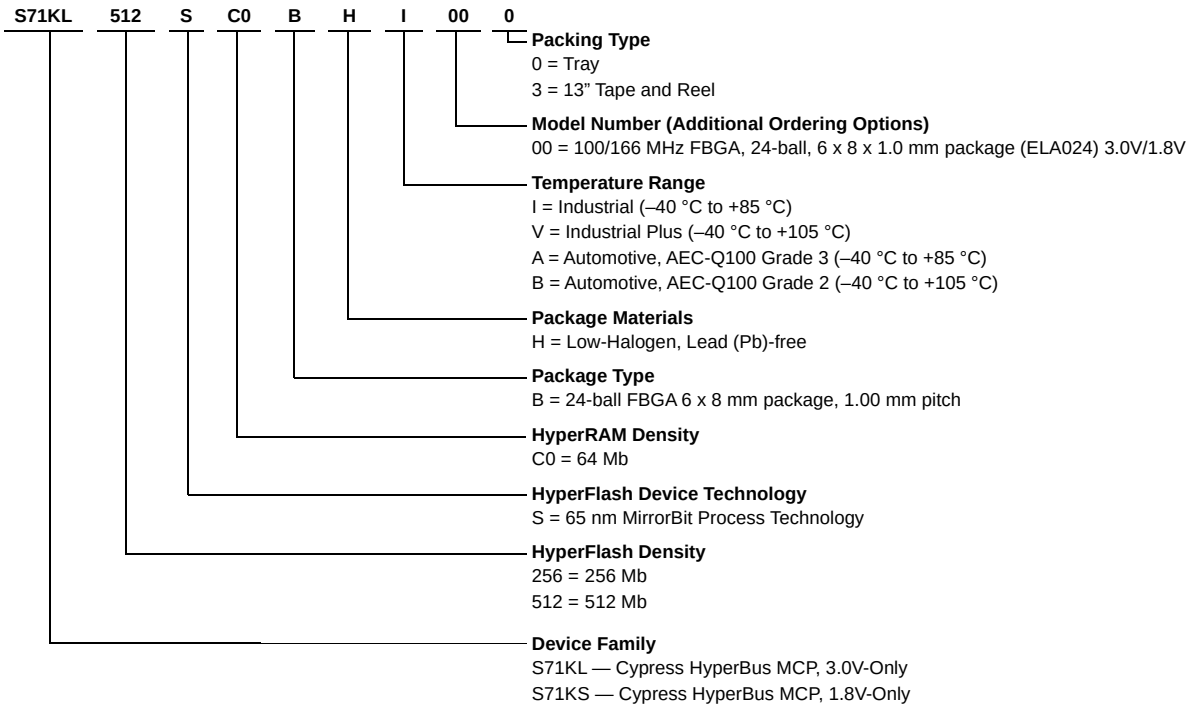
Table 4. 1.8V/3.0V Capacitive Characteristics

Description		Parameter	Min	Max	Unit
Input Capacitance (CK, CK#)[7,8,9]		CI	6.0	10.0	pF
Output Capacitance (RWDS)[7,8,9]	S71KL/S512SC0	CO	8.0	10.0	pF
	S71KL/S256SC0			10.5	
I/O Pin Capacitance (DQx)[7,8,9]	S71KL/S512SC0	CIO	8.0	10.0	pF
	S71KL/S256SC0		8.0	10.5	
I/O Pin Capacitance Delta (DQx)[7,8,9]		CIOD	—	1.0	pF
INT#, RSTO# Pin Capacitance, RST#[7,8,9]		COP	—	8.0	pF

Notes
9. These values are guaranteed by design and are tested on a sample basis only.
10. Pin capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, V_{CC}Q are applied and all other pins (except the pin under test) floating. DQs should be in the High Impedance state.
11. The capacitance values for the CK, CK#, RWDS and DQx pins must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.

Ordering Part Numbers

The ordering part number is formed by a valid combination of the following:



Valid Combinations - Standard

Table 5 lists configurations planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Table 5. Valid Standard Combinations

Device Number	HyperRAM Density	Package and Material	Temperature Range	Model Number	Packing Type	Ordering Part Number (x = Packing Type)	Package Marking
S71KL256S	C0	BH	I, V	00	0, 3	S71KL256SC0BHI00x	1KL256SC0HI00
						S71KL256SC0BHV00x	1KL256SC0HV00
S71KL512S	C0	BH	I, V	00	0, 3	S71KL512SC0BHI00x	1KL512SC0HI00
						S71KL512SC0BHV00x	1K5L12SC0HV00
S71KS512S	C0	BH	I, V	00	0, 3	S71KS512SC0BHI00x	1KS512SC0HI00
						S71KS512SC0BHV00x	1KS512SC0HV00

Note
12. FBGA package marking omits the leading S7, the package type character and packing type character from the ordering part number from the ordering part number.

Valid Combinations — Automotive Grade / AEC-Q100

Table 6 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 6. Valid Combinations — Automotive Grade / AEC-Q100

Device Number	HyperRAM Density	Package and Material	Temperature Range	Model Number	Packing Type	Ordering Part Number (x = Packing Type)	Package Marking
S71KL256S	C0	BH	A, B	00	0, 3	S71KL256SC0BHA00x	1KL256SC0HA00
						S71KL256SC0BHB00x	1KL256SC0HB00
S71KL512S	C0	BH	A, B	00	0, 3	S71KL512SC0BHA00x	1KL512SC0HA00
						S71KL512SC0BHB00x	1KL512SC0HB00
S71KS512S	C0	BH	A, B	00	0, 3	S71KS512SC0BHA00x	1KS512SC0HA00
						S71KS512SC0BHB00x	1KS512SC0HB00

Note
FBGA package marking omits the leading S7, the package type character and packing type character from the ordering part number from the ordering part number.

Document History Page

Document Title: S71KS512SC0, S71KL256SC0, S71KL512SC0, HyperFlash™ and HyperRAM™ Multi-Chip Package 1.8V/3V Document Number: 002-03902				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5023814	MAMC	11/23/2015	Initial release.
*A	5188954	RYSU	07/07/2016	Updated HyperBus MCP 3 V Signal Descriptions: Updated Table 2: Updated details in “Description” column corresponding to RESET# pin. Updated HyperBus MCP Block Diagram. Updated Physical Interface: Updated HyperBus MCP — FBGA 24-Ball, 5x5 Array Footprint: Added Note 2. Updated Physical Diagram: Added Figure 4. Updated Electrical Specifications: Updated DC Characteristics: Updated Table 3: Changed typical value of I_{CC5} parameter from 20 mA to 10 mA. Changed maximum value of I_{CC5} parameter from 40 mA to 20 mA. Updated Table 4: Updated values of all parameters. Updated to new template.
*B	5442136	RYSU	09/27/2016	Updated Document Title to read as “S71KL512SC0, HyperFlash™ and HyperRAM™ Multi-Chip Package 3V”. Removed part number “S71KL256SC0” related information in all instances across the document. Removed 256 Mb density related information in all instances across the document. Updated Ordering Part Numbers: Added Automotive, AEC-Q100 Grade 3 and Automotive, AEC-Q100 Grade 2 Temperature Range details. Removed 128 Mb, 256 Mb details. Updated Valid Combinations - Standard: Removed S71KL256S and its corresponding details. Added Valid Combinations — Automotive Grade / AEC-Q100. Updated to new template.
*C	5560279	RYSU	12/20/2016	Updated Document Title to read as “S71KL256SC0/S71KL512SC0, HyperFlash™ and HyperRAM™ Multi-Chip Package 3 V”. Added part number “S71KL256SC0” related information in all instances across the document. Added 256 Mb density related information in all instances across the document. Updated Electrical Specifications: Updated DC Characteristics: Updated Table 4: Added values corresponding to S71KL256SC0. Updated Ordering Part Numbers: Added 256 Mb details. Updated Valid Combinations - Standard: Added S71KL256S and its corresponding details. Updated Valid Combinations — Automotive Grade / AEC-Q100: Added S71KL256S and its corresponding details.
*D	5635102	SZZX	02/23/2017	Added S71KS512S and its corresponding details. Updated Sales and Copyright information.

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