

## 2ED2778S01G

### 160 V half bridge SOI gate driver with integrated bootstrap diode

#### Features

- Bootstrap voltage (VB node) of +160 V
- Floating channel designed for bootstrap operation
- Integrated low  $R_{ON}$ , ultra-fast bootstrap diodes
- Independent under voltage lockout for both high and low side
- Integrated shoot-through protection with built-in dead time
- Integrated short pulse / noise rejection input filter
- Schmitt trigger inputs with hysteresis
- 3.3 V, 5 V input logic compatible, outputs in phase with inputs
- Available in small footprint VSON-10 lead, 3 x 3 mm package
- 2.5 kV HBM ESD, RoHS compliant

#### Applications

General purpose half bridge gate driver for N-Channel MOSFETs

- Servo Drives in Robotics and Factory Automation
- General Purpose Low Voltage Drives or inverters
- e-Scooters, e-Bikes, and other e-Vehicles that do not require Automotive Qualification (LSEV)
- Battery operated Small Home Appliances (SHA)
- Commercial and Agricultural Drones
- Professional and Consumer Service Robotics
- Logistics Vehicles (eForklifts, Autonomous warehouse robotics)
- Battery operated hand-held power tools
- Gardening or Outdoor Power Equipment (OPE) Tools

#### Product validation

Qualified for industrial applications according to the relevant tests of JEDEC78/20/22

#### Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
2ED2778S01G	3 x 3 mm VSON-10	Tape and Reel	3000	2ED2778S01GXUMA1

#### Product summary

$V_{B\_OFFSET} = 160 \text{ V max}$   
 $I_{O+pk} / I_{O-pk} \text{ (typ)} = + 4 \text{ A} / - 8 \text{ A}$   
 Deadtime (typ) = 30 ns  
 $t_{ON} / t_{OFF} \text{ (typ)} = 65 \text{ ns} / 65 \text{ ns}$   
 Delay matching = 15 ns max

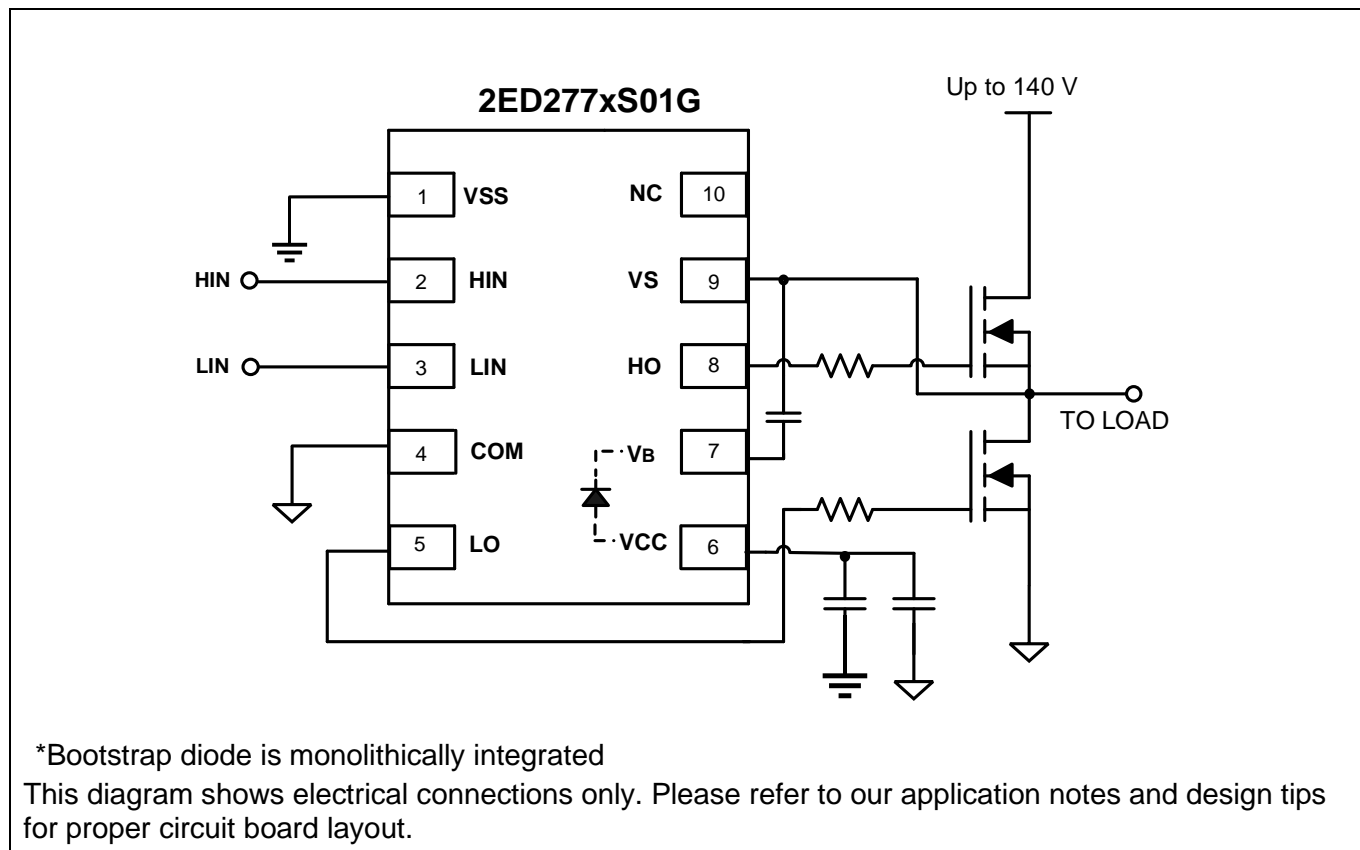
#### Package



VSON-10  
3 x 3 mm

## 1 Description

The 2ED2778S01G is a 160 V SOI based gate driver designed for half bridge BLDC motor drive applications. Integrated bootstrap diodes are used to supply the external high side bootstrap capacitor. Protection features include under voltage lockout on both Vcc and VB pins. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction



**Figure 1** Typical application block diagram

Summary of feature comparison of the 2ED27xxS01G family:

**Table 1**

Part No.	Package	Drive current source / sink	Input logic	Cross conduction prevention logic	Deadtime	Ground pins	t <sub>ON</sub> / t <sub>OFF</sub>
2ED2732S01G	VSON-10 3 x 3 mm	+ 1 A / - 2 A	HIN, LIN	No	None	VSS / COM	50 ns / 50 ns
2ED2734S01G		+ 2 A / - 4 A					65 ns / 65 ns
2ED2738S01G		+ 4 A / - 8 A					65 ns / 65 ns
2ED2742S01G		+ 1 A / - 2 A		Yes	30 ns		50 ns / 50 ns
2ED2772S01G		+ 1 A / - 2 A					50 ns / 50 ns
2ED2744S01G		+ 2 A / - 4 A					65 ns / 65 ns
2ED2778S01G		+ 4 A / - 8 A					65 ns / 65 ns
2ED2778S01G		+ 4 A / - 8 A					65 ns / 65 ns

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### 3 Electrical parameters

#### 3.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**Table 2 Absolute maximum ratings**

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating well supply voltage (Note 1)	-0.3	160	V
$V_S$	High-side floating well supply return voltage	-0.3	140	
$V_{BS}$	High-side floating well supply voltage	-0.3	20	
$V_{HO}$	Floating gate drive output voltage	$V_S - 0.3$	$V_{BS} + 0.3$	
$V_{CC}$	Low side supply voltage	-0.3	20	
$V_{LO}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{LOGIC IN}$	Logic input voltage (HIN, LIN)	$V_{SS} - 0.3$	5	
COM	Low side power ground return	-5.0	+5.0	
$dV_S/dt$	Allowable $V_S$ offset supply transient relative to COM	—	50	V / ns
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$ VSON-10		2	W
$R_{thJA}$	Thermal resistance, junction to ambient VSON-10		57	$^\circ\text{C}/\text{W}$
$T_J$	Junction temperature	—	150	$^\circ\text{C}$
$T_S$	Storage temperature	- 50	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	260	

Note 1: In case  $V_{CC} > V_B$  there is an additional power dissipation in the internal bootstrap diode between pins VCC and  $V_B$ .

### 3.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in Table 2. Recommended operating conditions

**Table 3 Recommended operating conditions**

Symbol	Definition	Min	Max	Units
$V_B$	Bootstrap voltage	$V_S + 7$	140	V
$V_{BS}$	High-side floating well supply voltage	7	18	
$V_S$	High-side floating well supply offset voltage	0	122	
$V_{HO}$	Floating gate drive output voltage	$V_S$	$V_B$	
$V_{CC}$	Low-side supply voltage	7	18	
$V_{LO}$	Low-side output voltage	COM	$V_{CC}$	
$V_{LOGIC\ IN}$	Logic input voltage(HIN, LIN)	$V_{SS}$	5	
$T_A$	Ambient temperature	-40	125	°C

Note 2: Logic operational for  $V_S$  of -8V to +120V. Logic state held for  $V_S$  of -8V to  $-V_{BS}$ .

### 3.3 Static electrical characteristics

$(V_{CC} - COM) = (V_B - V_S) = 12\text{ V}$ ,  $V_{SS} = COM$  and  $T_A = 25\text{ °C}$  unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS} / COM$  and are applicable to the respective input leads: HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S / COM$  and are applicable to the respective output leads HO or LO. The  $V_{CCUV}$  parameters are referenced to COM. The  $V_{BSUV}$  parameters are referenced to  $V_S$ .

**Table 4 Static electrical characteristic**

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{CCUVLO+}$	$V_{CC}$ supply undervoltage positive going threshold	7.8	8.2	8.6	V	
$V_{CCUVLO-}$	$V_{CC}$ supply undervoltage negative going threshold	7.3	7.7	8.1		
$V_{CCUVLOHY}$	$V_{CC}$ supply undervoltage hysteresis	0.3	0.5	0.7		
$V_{BSUVLO+}$	$V_{BS}$ supply undervoltage positive going threshold	7.8	8.2	8.6		
$V_{BSUVLO-}$	$V_{BS}$ supply undervoltage negative going threshold	7.3	7.7	8.1		
$V_{BSUVLOHY}$	$V_{BS}$ supply undervoltage hysteresis	0.3	0.5	0.7		
$I_{LK}$	High-side floating well offset supply leakage	—	—	5	uA	$V_B = V_S = 140\text{ V}$
$I_{QCC}$	Quiescent supply current	—	85	150		

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{OH}$	High level output voltage drop,	—	0.42	—	V	$I_O = 300 \text{ mA}$
$V_{OL}$	Low level output voltage drop	—	0.105	—		
$I_{O+}$	Peak output current turn-on <sup>1</sup>	—	4	—	A	$PW \leq 10 \mu\text{s}$
$I_{O-}$	Peak output current turn-off <sup>1</sup>	—	8	—		$PW \leq 10 \mu\text{s}$
$V_{IH}$	Logic “1” input voltage	2.0	—	—	V	
$V_{IL}$	Logic “0” input voltage	—	—	0.8		
$I_{\text{LOGIC IN+}}$	Input bias current (Output = High)	—	25	50	$\mu\text{A}$	$V_{\text{IN}} = 4 \text{ V}$
$I_{\text{LOGIC IN-}}$	Input bias current (Output = Low)	—	—	2		$V_{\text{IN}} = 0 \text{ V}$
$V_{\text{FBSD}}$	Bootstrap diode forward voltage between $V_{\text{CC}}$ and $V_{\text{B}}$	0.6	0.8	1	V	$I_{\text{F}} = 0.3 \text{ mA}$
$I_{\text{FBSD}}$	Bootstrap diode forward current between $V_{\text{CC}}$ and $V_{\text{B}}$	88	111	133	mA	$V_{\text{CC}} - V_{\text{B}} = 4 \text{ V}$
$R_{\text{BSD}}$	Bootstrap diode resistance	15	21	31	$\Omega$	$V_{\text{F1}} = 4 \text{ V}, V_{\text{F2}} = 5 \text{ V}$

<sup>1</sup> Not subjected to production test, verified by characterization.

### 3.4 Dynamic electrical characteristics

$V_{CC} = V_{BS} = 12\text{ V}$ ,  $V_{SS} = \text{COM}$ ,  $T_A = 25\text{ °C}$  and  $C_L = 4.7\text{ nF}$  unless otherwise specified.

**Table 5 Dynamic electrical characteristics**

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{ON}$	Turn-on propagation delay	40	65	90	ns	Clload = 1nF, IN 50% rise to OUT 10% rise
$t_{OFF}$	Turn-off propagation delay	40	65	90		Clload = 1nF, IN 50% fall to OUT 90% fall
$t_R$	Turn-on rise time	—	24	—		Clload = 1nF, OUT 10% to OUT 90%
$t_F$	Turn-off fall time	—	12	—		Clload = 1nF, OUT 90% to OUT 10%
MT	Delay matching time (HS & LS turn-on/off)	—	—	15		Clload = 1nF, OUT 90% to OUT 10%
DT	Deadtime: LO Turn-off to HO Turn-on & HO Turn-off to LO turn-on	20	30	45		

## 4 Block diagram

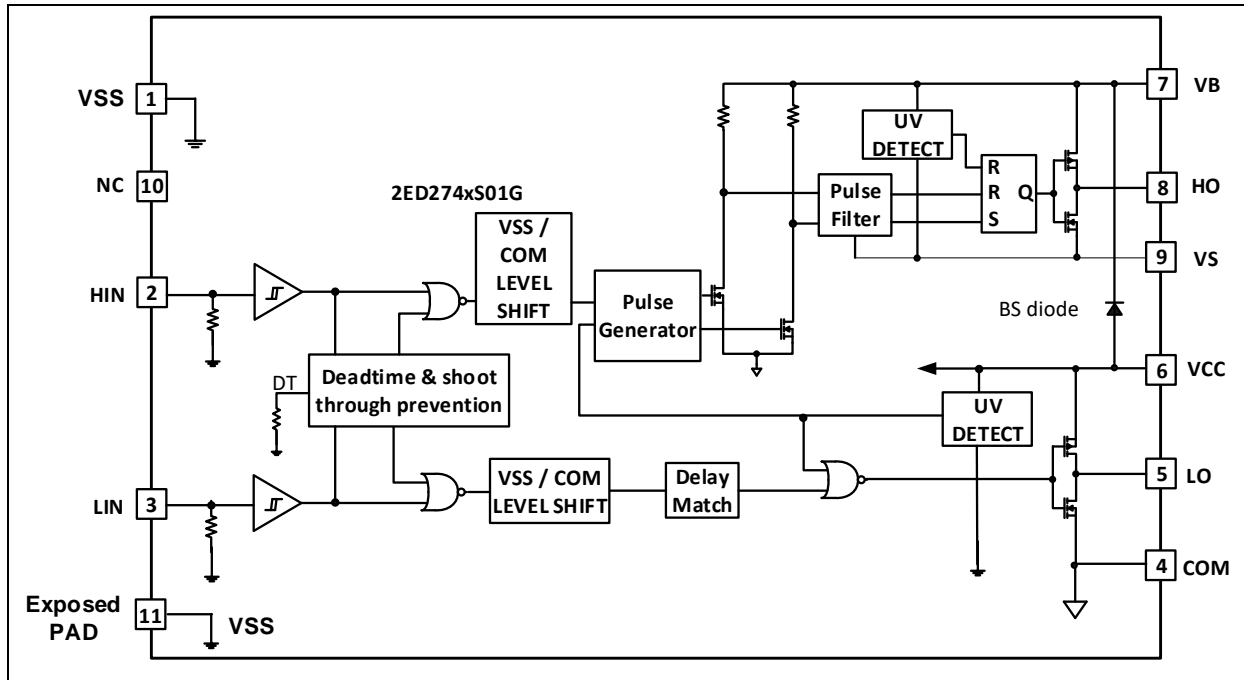


Figure 2 Functional block diagram



## 5 Pin configuration and functionality

### 5.1 Pin configuration

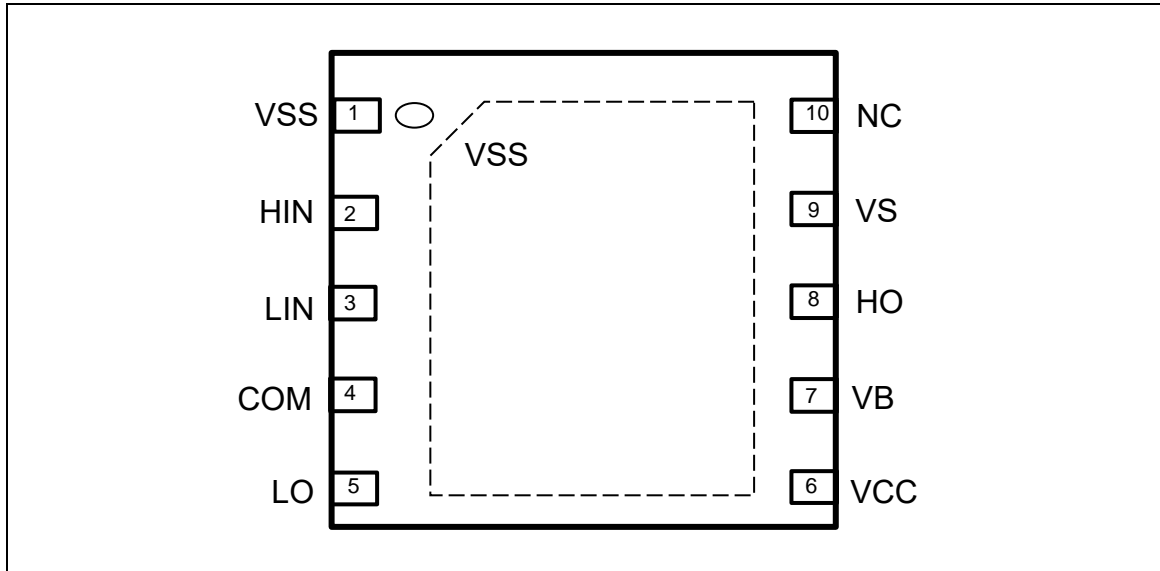


Figure 3 2ED2778S01G pin assignments (top view)

### Pin functionality

Table 6 Pin descriptions

Symbol	Pin No.	Type	Description
VSS	1	Ground	Logic ground
HIN	2	Input	Logic input for high side gate driver output (HO), in phase
LIN	3	Input	Logic input for low side gate driver output (LO), in phase
COM	4	Ground	Low side power ground return
LO	5	Output	Low side gate drive outputs
VCC	6	Input	Low side and logic fixed supply
VB	7	Output	High side floating supplies
HO	8	Output	High side gate drive outputs
VS	9	Input	High side floating supply returns
NC	10	NC	Not Connected
VSS	11	Exposed PAD	Logic ground

## 6 Application information and additional details

### 6.1 MOSFET gate drive

The 2ED2778S01G HVIC is designed to drive MOSFET power devices in battery operated applications. Figures 4 and 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as  $I_O$ . The voltage that drives the gate of the external power switch is defined as  $V_{HO}$  for the high-side power switch and  $V_{LO}$  for the low-side power switch; this parameter is sometimes generically called  $V_{OUT}$  and in this case does not differentiate between the high-side or low-side output voltage.

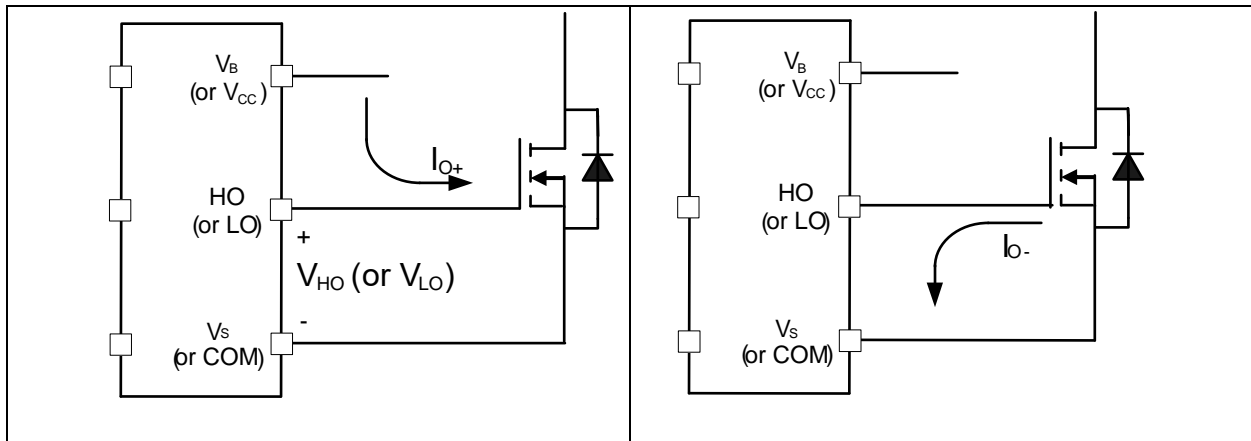


Figure 4 HVIC Sourcing current

Figure 5 HVIC Sinking current

### 6.2 Switching relationships

The relationships between the input and output signals of the 2ED2778S01G are illustrated below in Figure 6. We can see the definitions of several timing parameters (i.e.  $t_{ON}$ ,  $t_{OFF}$ ,  $t_R$ , and  $t_F$ ) associated with this device.

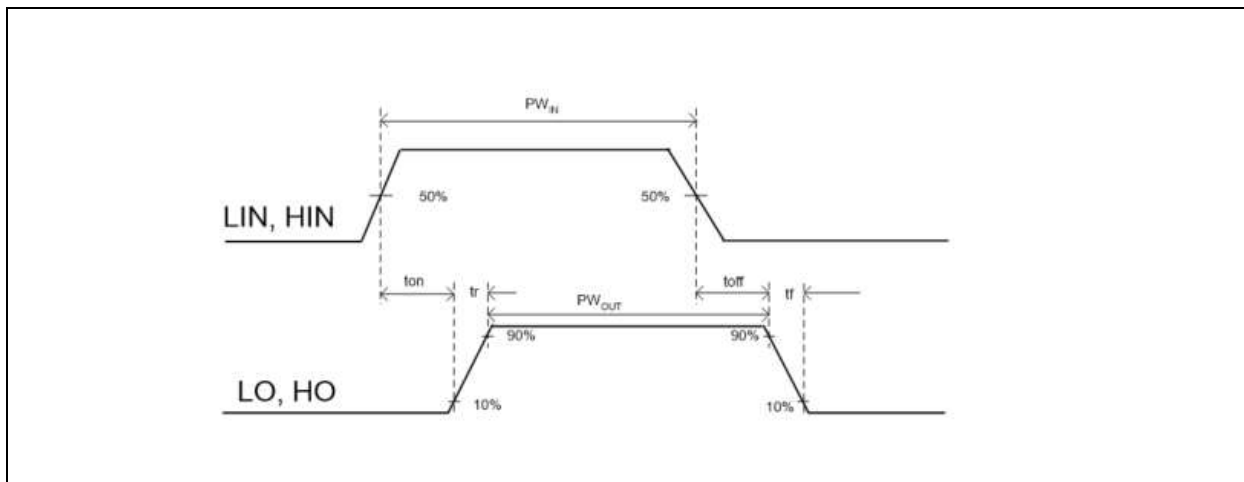
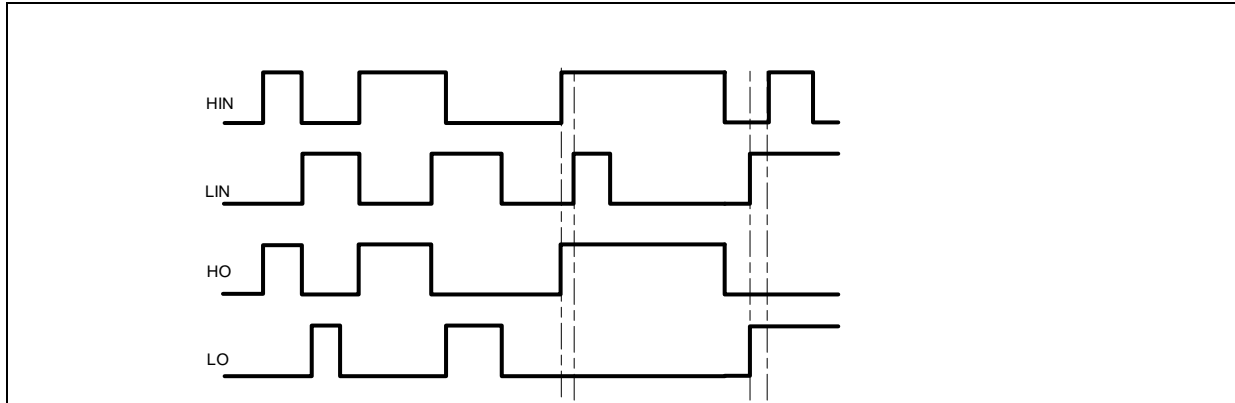


Figure 6 Switching timing diagram

### 6.3 Timing diagrams

The relationships between the input and output signals of the 2ED2778S01G are illustrated below in Figure 7.

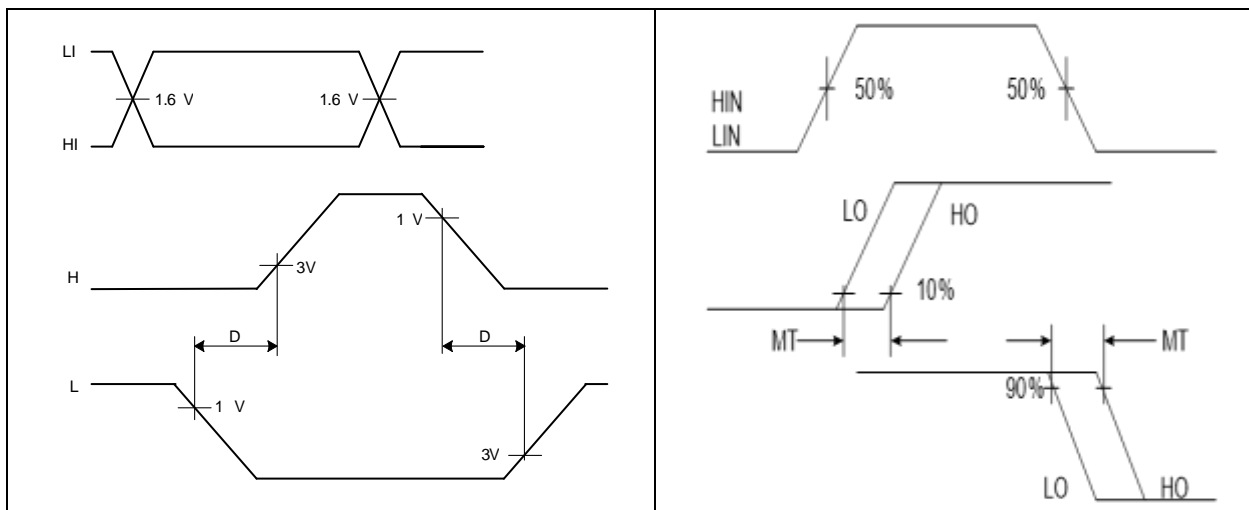


**Figure 7** Ideal Input/output timing diagram

### 6.4 Deadtime and matched propagation delays

This 2ED2778S01G features integrated deadtime protection circuitry. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 8 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of 2ED2778S01G is matched with respect to the high- and low-side outputs. Figure 8 defines the two deadtime parameters (i.e., DTLO-HO and DTHO-LO); the deadtime matching parameter (MDT) associated with the 2ED2778S01G specifies the maximum difference between DTLO-HO and DTHO-LO.



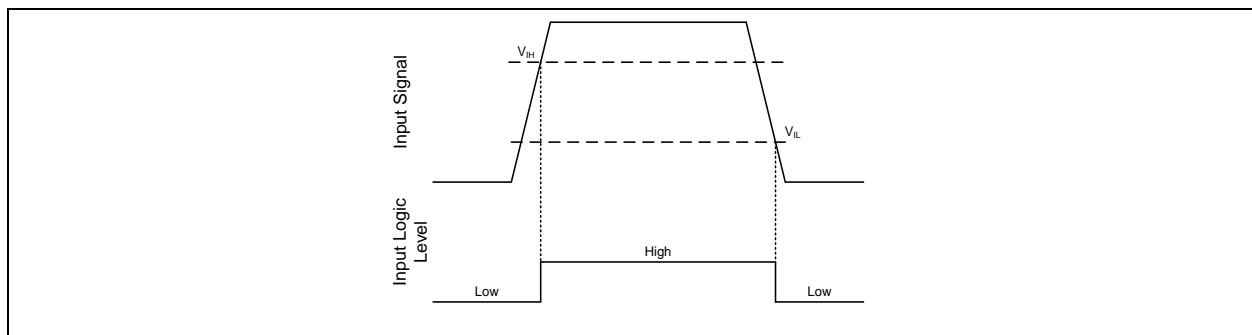
**Figure 8** Dead Time Definitions

**Figure 9** Delay Matching Waveform Definitions

The 2ED2778S01G is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e.,  $t_{ON}$ ,  $t_{OFF}$ ) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay ( $t_{ON}$ ) of the 2ED2778S01G is matched to the propagation turn-on delay ( $t_{OFF}$ ).

## 6.5 Input logic compatibility

The input pins of are based on a TTL and CMOS compatible input-threshold logic that is independent of the  $V_{CC}$  supply voltage. With typical high threshold ( $V_{IH}$ ) of 2.0 V and typical low threshold ( $V_{IL}$ ) of 0.8 V, along with very little temperature variation as summarized in Figure 10, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.8 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 2ED2778S01G also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 2ED2778S01G features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 2ED2778S01G has input pins that are capable of sustaining voltages higher than the bias voltage applied on the  $V_{CC}$  pin of the device.



**Figure 10** HIN & LIN input thresholds

## 6.6 Undervoltage lockout

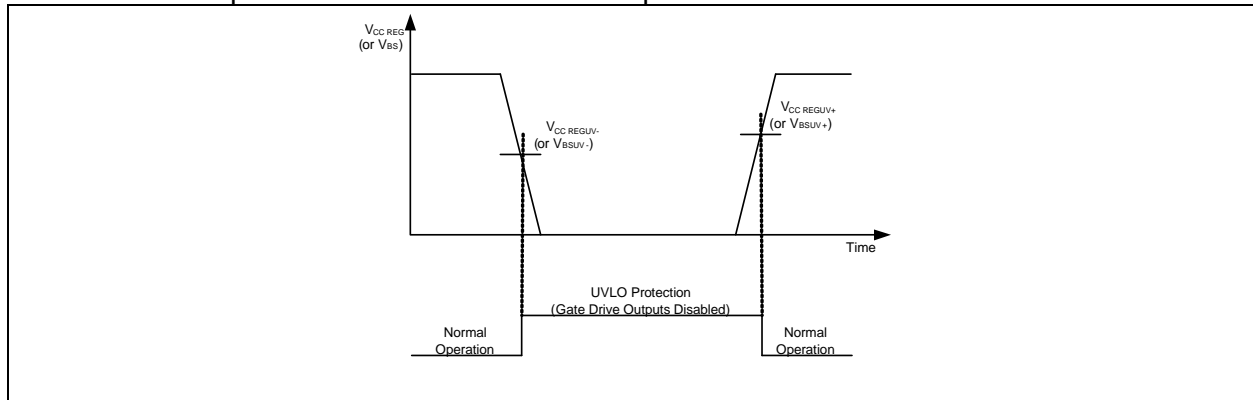
This IC provides undervoltage lockout protection on both the  $V_{CC}$  (logic and low-side circuitry) power supply and the  $V_{BS}$  (high-side circuitry) power supply. Figure 11 is used to illustrate this concept;  $V_{CC}$  (or  $V_{BS}$ ) is plotted over time and as the waveform crosses the UVLO threshold ( $V_{CC_{UVLO+/-}}$  or  $V_{BS_{UVLO+/-}}$ ) the undervoltage protection is enabled or disabled.

Upon power-up, should the  $V_{CC}$  voltage fail to reach the  $V_{CC_{UV+}}$  threshold, the IC won't turn-on. Additionally, if the  $V_{CC}$  voltage decreases below the  $V_{CC_{UV-}}$  threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the  $V_{BS}$  voltage fail to reach the  $V_{BS_{UV+}}$  threshold, the IC won't turn-on. Additionally, if the  $V_{BS}$  voltage decreases below the  $V_{BS_{UVLO-}}$  threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch

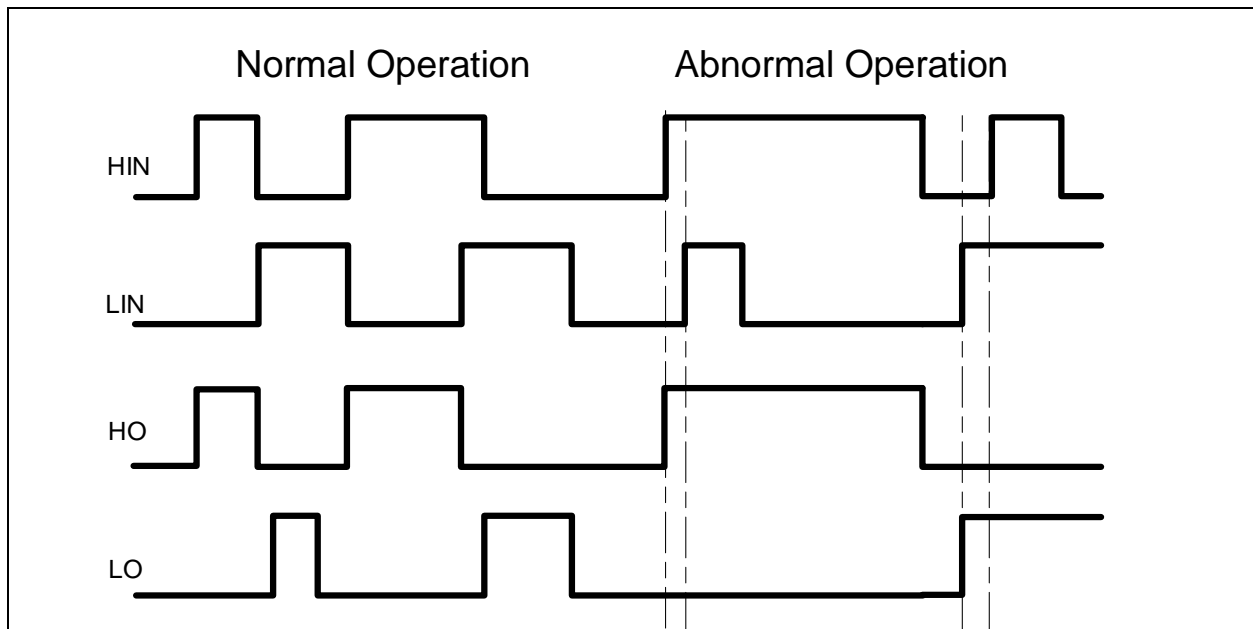
conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.



**Figure 11** UVLO protection

## 6.7 Shoot-through protection

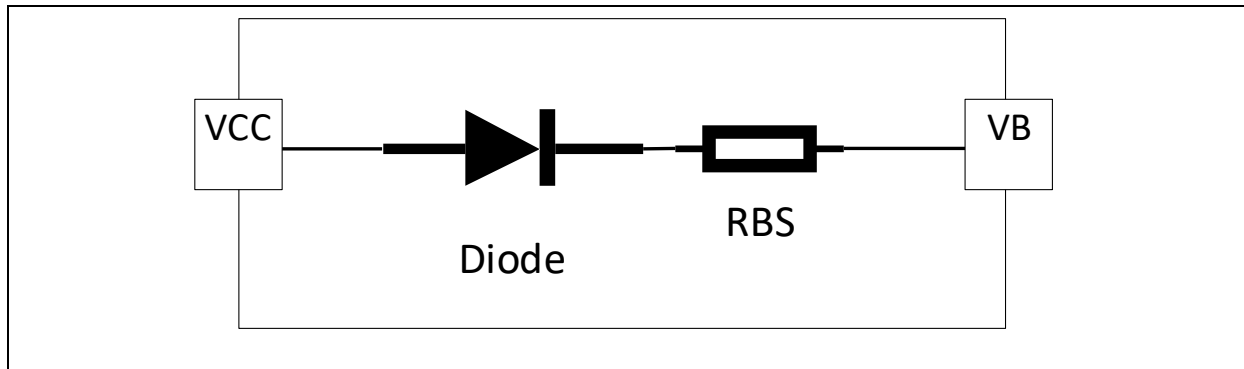
The 2ED2778S01G is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 12 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.



**Figure 12** Illustration of shoot-through protection circuitry

## 6.8 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its low ohmic resistance helps save cost and improve reliability by reducing external components as shown below figure 13.



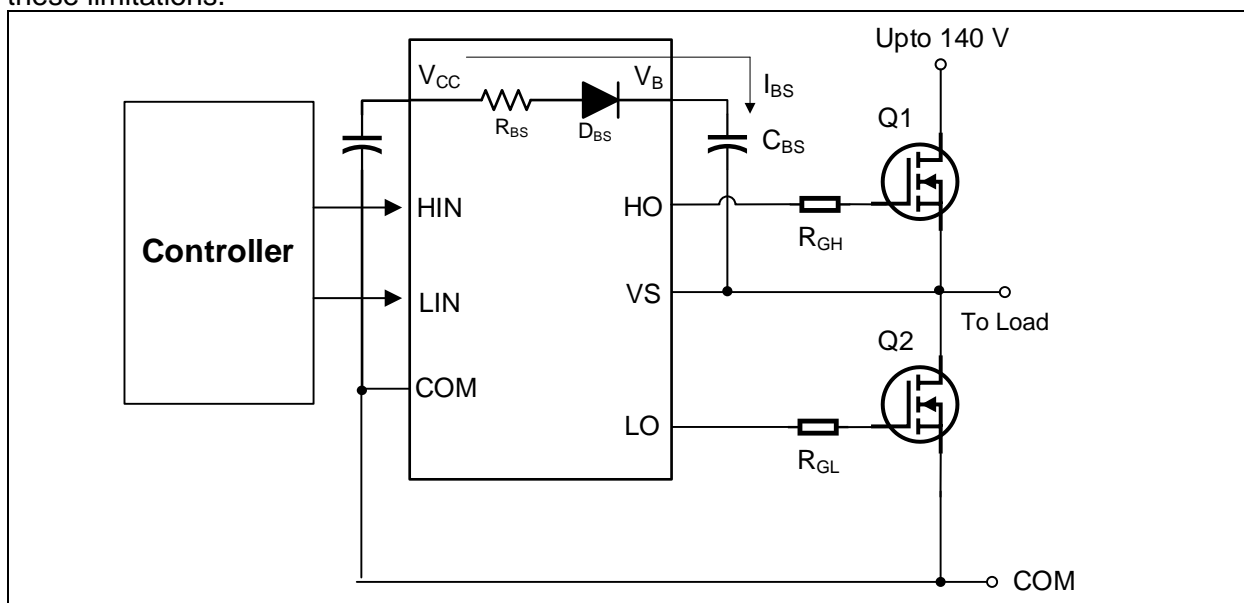
**Figure 13** 2ED2778S01G with integrated components

The low ohmic current limiting resistor (typically 25 Ohms) provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 2ED2778S01G allows faster recharging of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real uni-directional PN-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 2ED2778S01G works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

## 6.9 Calculating the bootstrap capacitance $C_{BS}$

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 14. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.



**Figure 14** Half bridge bootstrap circuit in 2ED2778S01G

When the low side MOSFET turns on, it will force the potential of pin  $V_S$  to GND. The existing difference between the voltage of the bootstrap capacitor  $V_{CBS}$  and  $V_{CC}$  results in a charging current  $I_{BS}$  into the capacitor  $C_{BS}$ . The current  $I_{BS}$  is a pulse current and therefore the ESR of the capacitor  $C_{BS}$  must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode  $D_{BS}$  blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor  $C_{VCC}$ . The bootstrap diode  $D_{BS}$  also takes over the blocking voltage between pin  $V_B$  and  $V_{CC}$ . The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors  $C_{BS}$ , that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 2ED2778S01G, which have the UVLO also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The current limiting resistor  $R_{BS}$  according to Figure 14 reduces the peak of the pulse current during the low side MOSFET turn-on. The pulse current will occur at each turn-on of the low side MOSFET, so that with increasing switching frequency, the capacitor  $C_{BS}$  is charged more frequently. Therefore, a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: the high side quiescent current and gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

$\Delta V_{BS}$  is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (V_{CC} - V_F - V_{GSmin} - V_{DSon})$$

$V_{GSmin} > V_{BSUV-}$ ,  $V_{GSmin}$  is the minimum gate source voltage we want to maintain and  $V_{BSUV-}$  is the high-side supply undervoltage negative threshold.

$V_{CC}$  is the IC voltage supply,  $V_F$  is bootstrap diode forward voltage and  $V_{DSon}$  is drain-source voltage of low side MOSFET.

Please note, that the value  $Q_{GTOT}$  may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing  $V_{BS}$  to decrease are:

- MOSFET turn on required Gate charge ( $Q_G$ )
- MOSFET gate-source leakage current ( $I_{LK\_GS}$ )
- Floating section quiescent current ( $I_{QBS}$ )
- Floating section leakage current ( $I_{LK}$ )
- Bootstrap diode leakage current ( $I_{LK\_DIODE}$ )
- Charge required by the internal level shifters ( $Q_{LS}$ ): typical 1nC
- Bootstrap capacitor leakage current ( $I_{LK\_CAP}$ )
- High side on time ( $T_{HON}$ )

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + (I_{QBS} + I_{LK\_GS} + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP}) * T_{HON}$$

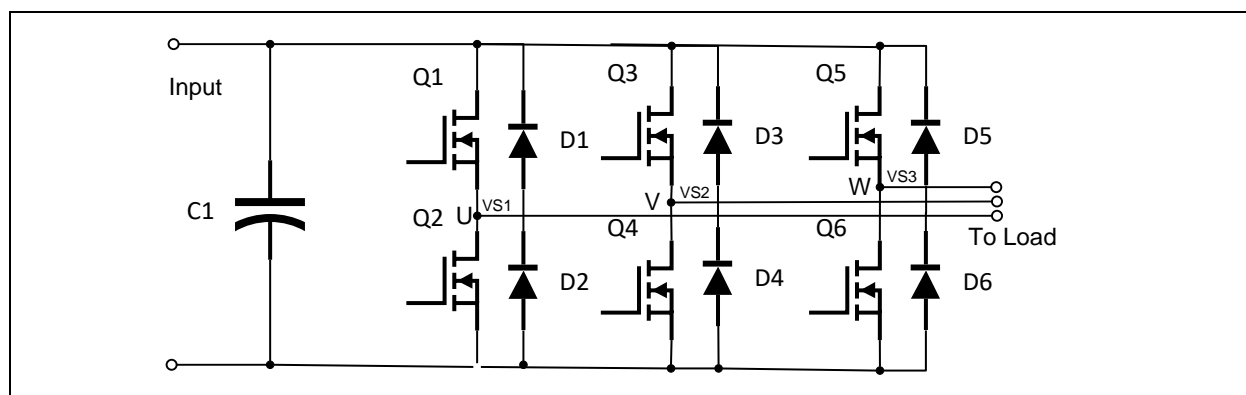
$I_{LK\_CAP}$  is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above  $C_{BS}$  equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7  $\mu F$  for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

## 6.10 Negative voltage transient tolerance of VS pin

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 15, here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the MOSFET Q1 in Figures 16 and 17) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node  $V_{S1}$ , swings from the positive DC bus voltage to the negative DC bus voltage.

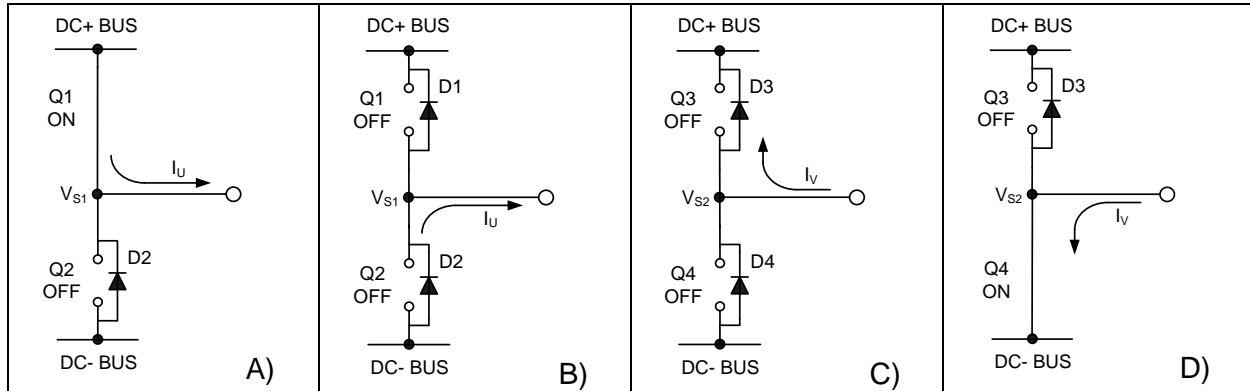


**Figure 15** Half bridge inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figures 16 C) and D)), and Q4 MOSFET switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node,  $V_{S2}$ , swings from the positive DC bus voltage to the negative DC bus voltage.

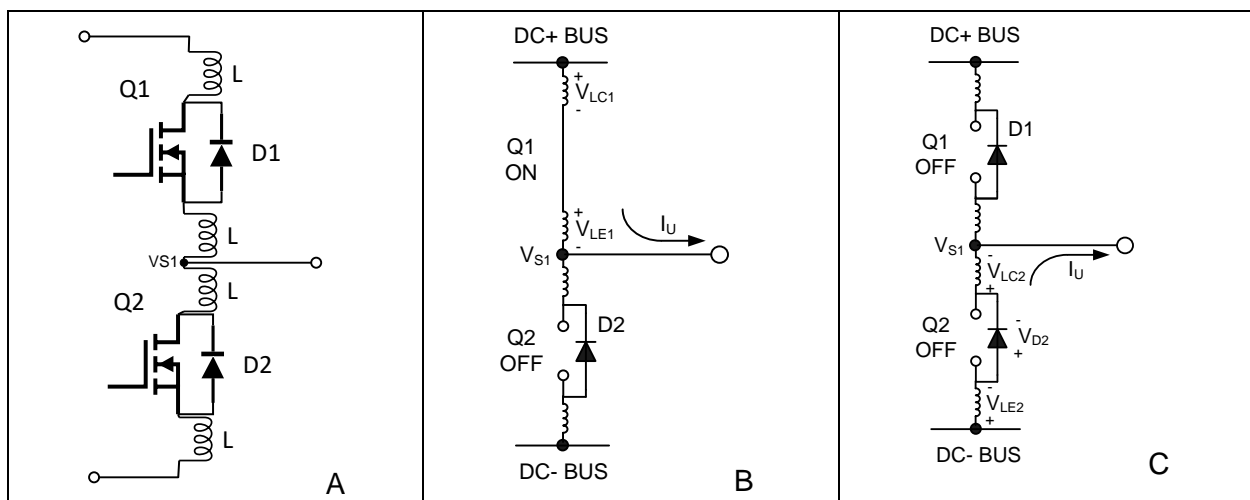
However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus. This undershoot voltage is called "negative  $V_S$  transient"





**Figure 16 A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting**

The circuit shown in Figure 17-A depicts one leg of the half bridge inverter; Figures 17-B and 17-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in  $L_C$  and  $L_E$  for each MOSFET. When the high-side switch is on,  $V_{S1}$  is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to  $V_{S1}$  (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between  $V_{S1}$  and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the  $V_S$  pin).



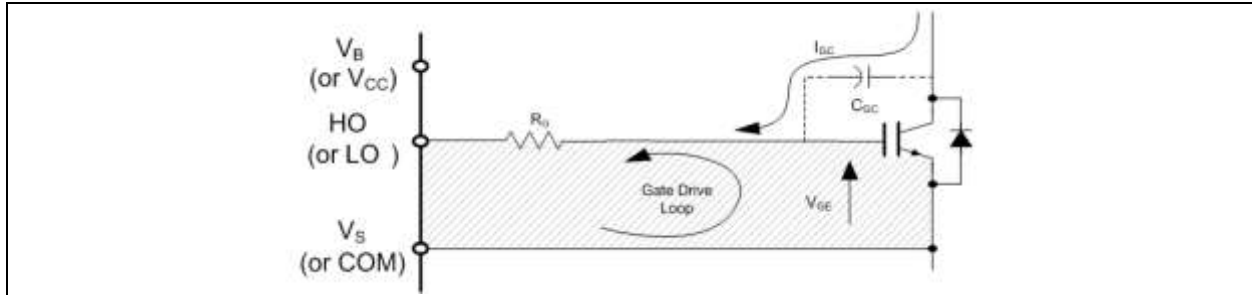
**Figure 17 Figure A shows the Parasitic Elements. Figure B shows the generation of  $V_S$  positive. Figure C shows the generation of  $V_S$  negative**

### 6.11 PCB layout tips

**Distance between high and low voltage components:** It's strongly recommended to place the components tied to the floating voltage pins ( $V_B$  and  $V_S$ ) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

**Ground Plane:** In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

**Gate Drive Loops:** Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 18). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the MOSFET collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

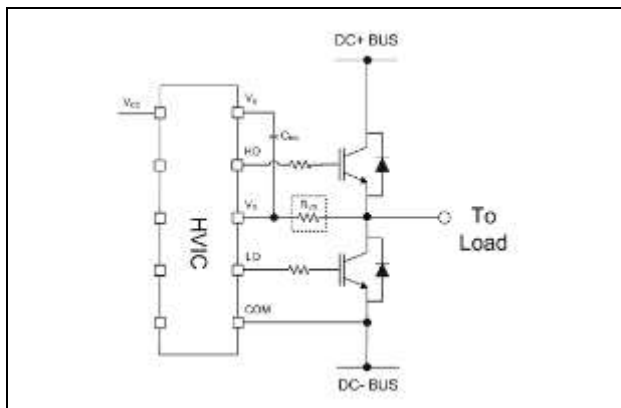


**Figure 18** Avoid antenna loops

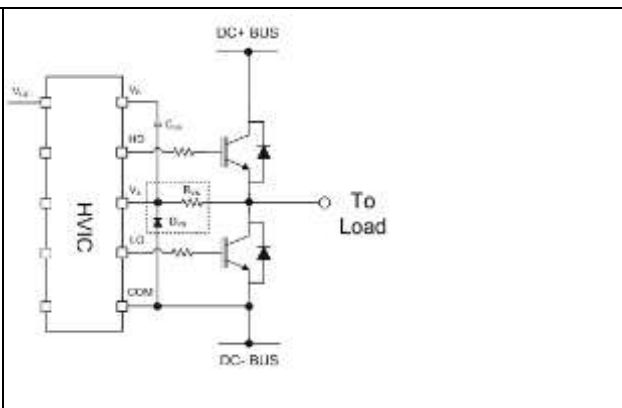
**Supply Capacitor:** It is recommended to place a bypass capacitor ( $C_{IN}$ ) between the VCC and COM pins. A ceramic  $1\mu\text{F}$  ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

**Routing and Placement:** Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative  $V_S$  spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor ( $5\Omega$  or less) between the  $V_S$  pin and the switch node (see Figure 22), and in some cases using a clamping diode between COM and  $V_S$  (see Figure 19).

See DT04-4 at [www.infineon.com](http://www.infineon.com) for more detailed explanations.



**Figure 19** Resistor between the  $V_S$  pin and the switch node



**Figure 20** Clamping diode between COM and  $V_S$

## 7 Qualification information<sup>1</sup>

Table 7 Qualification information

Qualification level		Industrial <sup>2</sup>	
		Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		VSON-10	MSL2, 260 °C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (1.0 kV) (per JEDEC standard JS-002_2018)	
	Human body model	Class 2a (2.5 kV) (per JEDEC standard JS-001_2017)	
IC latch-up test		Class II Level A (per JESD78E)	
RoHS compliant		Yes	

## 8 Related products

Table 8

Product	Description
<b>Gate Driver ICs</b>	
<a href="#">6EDL04N02PR</a>	200 V three-phase gate driver IC with integrated bootstrap diode, over current protection, enable and fault reporting
<a href="#">IRS200x</a>	The IRS2005/7/8 200 V devices are offered in eight-pin DSO-8 or fourteen-pin 4 x 4 mm VQFN14 packages ( <b>IRS2005M</b> ) with various logic input options and standard pin-out configurations for high design flexibility and fast time to market. All devices are MSL2 qualified.
<a href="#">6EDL003L02-F2</a>	EiceDRIVER™ Compact - Full bridge 3 Phase gate driver IC with LS-SOI technology to control power devices like MOS-transistors or 180V IGBTs
<b>Power Switches</b>	
<a href="#">OptiMOS™ 5</a>	The new OptiMOS™ 5 150 V power MOSFETs from Infineon are particularly suitable for low voltage drives such as forklift and e-scooter, as well as telecom and solar applications
<a href="#">OptiMOS™ &amp; StrongIRFET™</a>	OptiMOS™ and StrongIRFET™ low- and medium voltage power MOSFETs enable innovation and performance in applications such as switch mode power supplies (SMPS), battery powered applications, motor control and drives, inverters, and computing
<b>iMOTION™ Controllers</b>	
<a href="#">IRMCK099</a>	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
<a href="#">IMC101T</a>	High performance Motor Control IC for variable speed drives based on field-oriented control (FOC) of permanent magnet synchronous motors (PMSM).

<sup>1</sup> Qualification standards can be found at Infineon's web site [www.infineon.com](http://www.infineon.com)

<sup>2</sup> Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

## 9 Packaging information

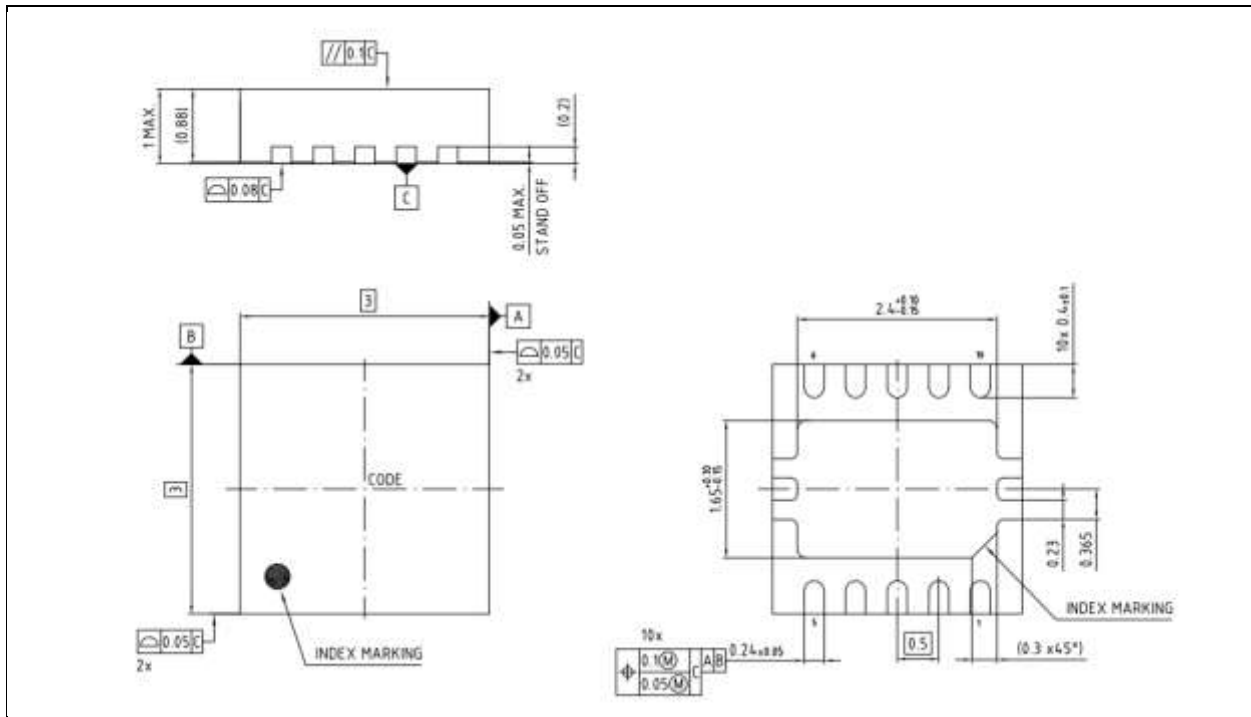


Figure 21 Target Package Dimensions: PG-VSON-10-5 (2ED2778S01G)

## 10 Additional documentation and resources

Several technical documents related to the use of HVICs are available at [www.infineon.com](http://www.infineon.com); use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:

[Understanding HVIC Datasheet Specifications](#)

[HV Floating MOS-Gate Driver ICs](#)

[Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and MOSFETs](#)

[Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality](#)

Design Tips:

[Using Monolithic High Voltage Gate Drivers](#)

[Alleviating High Side Latch on Problem at Power Up](#)

[Keeping the Bootstrap Capacitor Charged in Buck Converters](#)

[Managing Transients in Control IC Driven Power Stages](#)

[Simple High Side Drive Provides Fast Switching and Continuous On-Time](#)

### 10.1 Infineon online forum resources

The Gate Driver Community is live at Infineon Community (<https://community.infineon.com/t5/Gate-Driver-ICs/bd-p/GateDriverICs>). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver community also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at <https://community.infineon.com/> and learn the nuances of efficiently driving a power switch in any given power electronic application.



**11**      **Revision history**

Document version	Date of release	Description of changes
1.0	August 01 2023	Final Datasheet

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