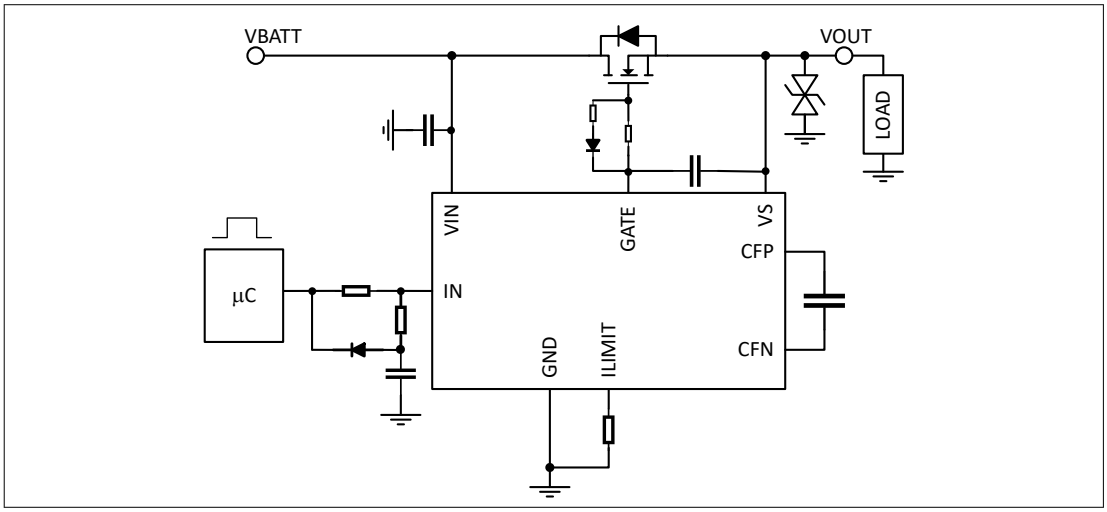
EiceDRIVER™ 125 V High Side Gate Driver

Features

- Wide operating input voltage range of up to 125 V
- Strong gate driver for fast turn-off
- Strong integrated charge pump for fast turn-on
- Internal charge pump for reduced EMI and low voltage operation
- V_{DS} monitoring for overcurrent protection (OCP) and current measurement
- Adjustable current trip threshold with flexible fault time and blanking time

Potential applications

- Power tools
- Gardening tools
- Robotics, e-bikes, vacuum cleaners
- Drones and multicopters



Product validation

Fully qualified according to JEDEC for industrial applications.

Description

The 1EDL8011 gate driver IC provides fast turn-on and turn-off of high side N-channel MOSFETs with its powerful gate current capabilities. It consists of an integrated charge pump with an external capacitor to provide strong start-up. The internal charge pump provides MOSFET gate voltage when the operating input voltage is low. The gate driver IC is used to manage inrush current and protects in case of faults. Undervoltage Lockout (UVLO) protection at input voltage prevents the device from operating under hazardous conditions. The 1EDL8011 is available in DSO-8 package including OCP protection feature, an adjustable current setting threshold, time delay and a safe start-up mechanism with flexible blanking during MOSFET turn-on transitions.

Ordering Information

Product name	Package	Package size	Pin pitch
1EDL8011	PG-DSO-8-92	5.00 mm × 6.00 mm	1.27 mm

Table of contents

1 Pin configuration

Table 1 Pin definitions and functions

Pin number	Name	Description
1	GND	Device ground connection
2	IN	Enable control for the main disconnect switch and power up of the device
3	CFN	Bottom terminal of the flying cap
4	CFP	Top terminal of the flying cap
5	ILIMIT	Set the OCP threshold via pull-down resistor. Short to GND to disable the OCP function
6	GATE	Gate output of the gate driver
7	VS	System output voltage. Connect to source of disconnect switch
8	VIN	Chip supply. Connect to drain of disconnect switch

The top view of pin configuration is shown in Figure 1.

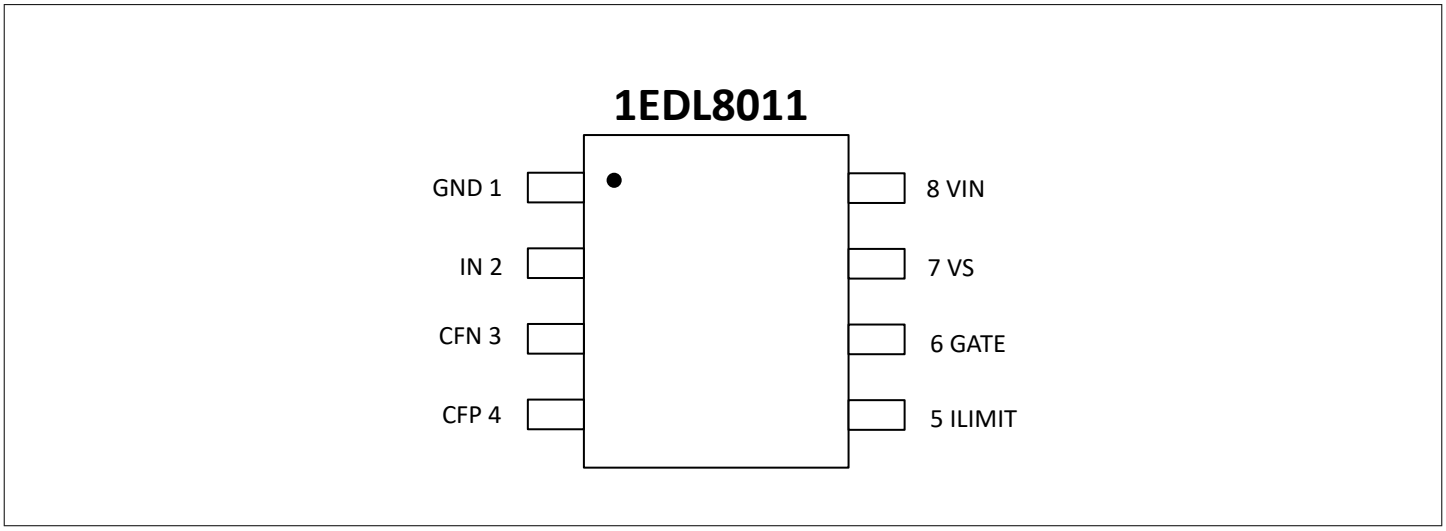


Figure 1 Pin configuration

2 Block diagram

The system block diagram is presented in Figure 2.

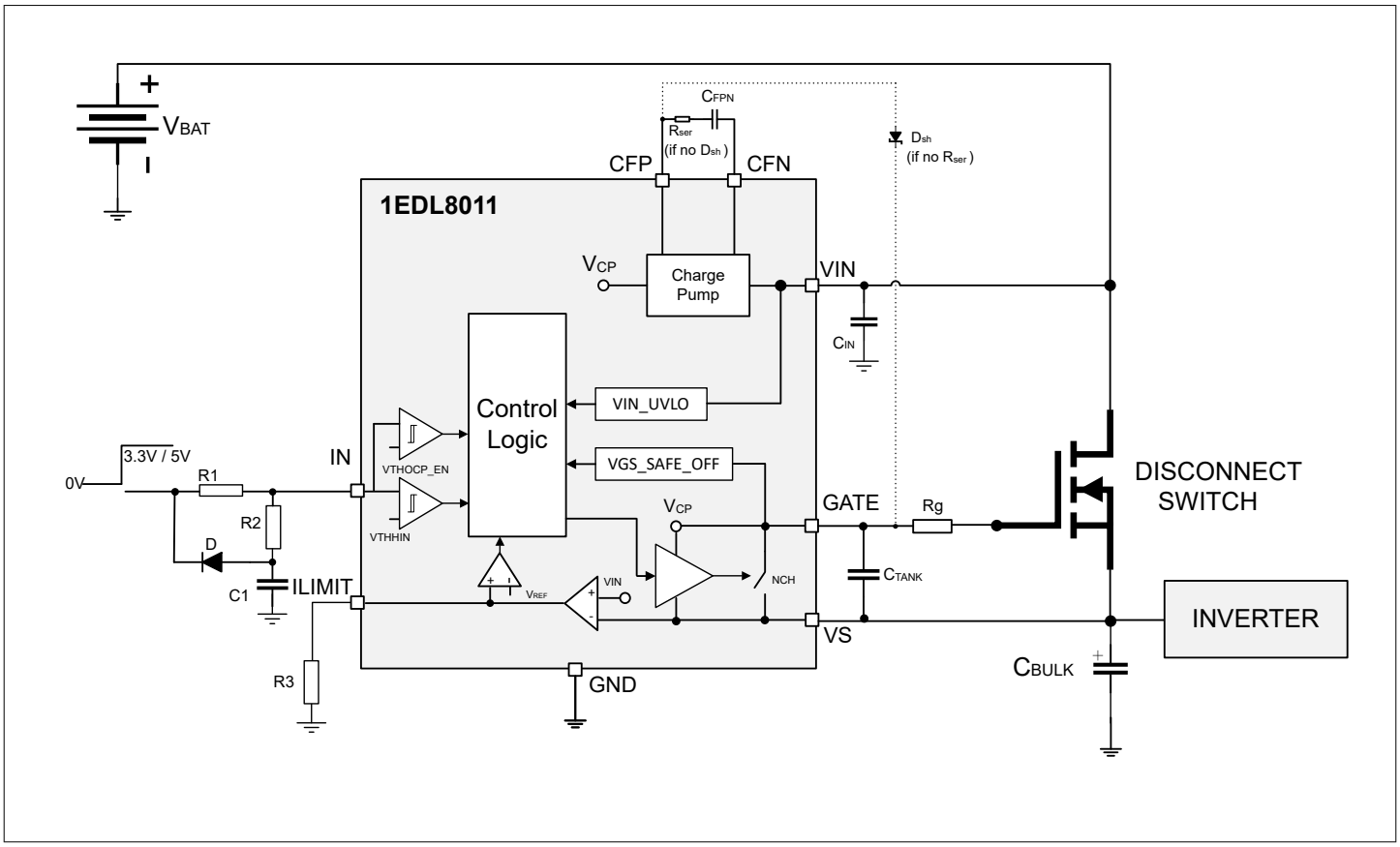


Figure 2 System functional block diagram

3 Introduction

3.1 Product description

In many power applications including motor drives and switched-mode power supplies (SMPS), the supply architecture often requires that a module can be disconnected from the main supply rail when a malfunction occurs in this module. In order to achieve that functionality, it is common to use high side disconnect switches (for example MOSFETs) that isolate the module causing the fault from the main rail. In a battery powered motor drive system, for instance, the battery is typically connected to the main inverter via a disconnect switch. That disconnect switch helps prevent a load short-circuit from affecting the battery, which could lead to a fatal error or even destroy the battery.

Another important aspect of such systems are inrush currents. In a battery powered drive, the inrush current flows when the battery is connected through the disconnect switch to the inverter module and starts charging the bus capacitors for the first time. The current can increase to dangerous levels and even destroy elements in the applications for example, when the SOA (Safe Operating Area) of the disconnect switch is violated. In situations like that, a controlled charge function such as external precharge circuit or high side gate driver with controlled turn-on can help mitigate the effect.

4 General product characteristics

4.1 Absolute maximum ratings

***Note**: Absolute maximum ratings are intended in the temperature range T_J = -40°C to T_J = 150°C, unless otherwise specified.*

***Note**: Absolute maximum ratings are not subject to production test, specified by design.*

***Note**: Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.*

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	VIN	-0.3	–	125	V	–
Source voltage	VS	-10	–	125	V	–
Supply and source voltage slew rate	SR_{VIN}, SR_{VS}	–	–	2	V/µs	$T_{ambient}$ > -10°C
Main switch gate voltage	V_{GATE}	VS-0.3	–	VS+15	V	–
Flying capacitor voltage at the top pin	V_{CFP}	-0.3	–	140	V	–
Flying capacitor negative voltage at the bottom pin	V_{CFN}	-0.3	–	15	V	–
Analog/Digital input pin voltage	V_IN, V_{ILIMIT}	-0.3	–	7	V	–
Maximum current for analog inputs	$I_{AN\_IN\_MAX}$	-1	–	10	mA	–
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_S	-55	–	150	°C	–
Case temperature	T_{CASE}	–	–	145	°C	–

4.2 Recommended operating conditions

Operating at T_A = 25°C. All voltages are referred to ground (GND), positive currents are flowing into the pin (unless otherwise specified).

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	VIN	8	–	125	V	DC plus transients (noise and spikes combined)
Source voltage	VS	-10	–	125	V	DC plus transients (noise and spikes combined) -10 V for 10 µs pulse AC current and -0.3 V for DC constant current. 1)
RRC input slew rate	RRC_{SR}	0.35	–	–	V/µs	This is at the input of the R1-R2-C1 network and applicable only with blanking/OCP delay.
Analog/Digital pins voltage range	V_IN	0	–	5.5	V	–
VDSON comparator input voltage range	VTH_{VDS}	0	–	2	V	1) This is the voltage across the VIN and VS pins.
ILIMIT pin input voltage range	V_{ILIMIT}	0	–	5	V	–
Junction temperature range	T_J	-40	–	125	°C	–

1) Not subject to production test - specified by design

4.3 Electrical characteristics

VIN = 8 to 125 V, T_A = 25°C, unless otherwise specified. All voltages are referred to ground (GND), positive currents are flowing into the pin (unless otherwise specified).

Table 4 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply and UVLO						
VIN quiescent current, active mode	I_{DDQ_ON}	–	2.7	5	mA	Total current consumption on the VIN and VS pins when V_IN > $VTHH_{IN}$
VIN quiescent current, off mode	I_{DDQ_OFF}	–	–	1	µA	T_A = 25 °C, when V_IN < $VTHL_{IN}$
VIN UVLO rising threshold	$V_{VIN\_UVLO\_R}$	9.5	10	10.5	V	–

(table continues...)

Table 4 (continued) Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VIN UVLO falling threshold	$V_{VIN\_UVLO\_F}$	7	7.5	8	V	–
VIN UVLO deglitch filter	T_{VIN_UVLO}	–	750	–	ns	1)
Main Gate Driver						
Gate driver output	V_{GATE} - VS	10	12	15	V	No load on the GATE pin
Gate driver output	V_{GATE} - VS	9	12	15	V	5 mA current load on GATE pin
Gate driver output voltage ripple	V_{GATE_RIPPLE}	–	–	200	mV	No load on GATE. 1)
Peak gate driver sink current	$I_{GD\_SNK\_PEAK}$	–	1	–	A	1)
RDSON of gate pull down	R_{DSON_PD}	–	–	12	Ω	When V_{GATE} - VS = 12 V
Active pull down resistance	R_{PULL}	–	–	1K	Ω	When IN is off and V_{GATE} - VS > 2 V
Start-up time of gate driver	T_{START_UP}	–	96	–	µs	From first rising edge of CFN till gate voltage V_{GATE} - VS = 10 V (C_{FPN} = 2.3 nF, C_{TANK} = 23 nF, MOSFET IRFS7537) 1)
Charge Pump						
Output impedance of charge pump	R_{CP}	–	150	–	Ω	Output impedance directly seen on CFN pin with no external capacitor on CFP, CFN pins. 1)
Charge pump clock frequency	f_{CP_CLK}	280	400	550	kHz	–
VDS Sensor						
VDS sensor input current	I_{VIN_SNS}	–	–	1	mA	Current into VIN pin due to VDS sensor
VDS sensor bandwidth	$V_{DS\_OCP\_BW}$	–	1	–	MHz	Unity gain bandwidth with 5 pF (max. capacitance) that loads the ILIMIT pin. 1)
VDS sensor accuracy	ε_{VDS}	-25	–	25	%	The accuracy is intended to be before calibration. After calibration, the accuracy is based on customer calibration and ensured above 100 mV
VDSON comparator deglitch filter	$t_{OCP\_DEGLITCH}$	500	1000	–	ns	1)
VDS sensor OCP threshold	V_{REF}	1.18	1.23	1.28	V	Internal voltage reference

(table continues...)

Table 4 (continued) Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN Pin						
IN rising threshold	$VTHH_{IN}$	1.15	–	–	V	–
IN falling threshold	$VTHL_{IN}$	0	–	1.0	V	I/O standard specification. Anything below the maximum value results in an Off state.
IN pin initial voltage	$V_{INITIAL}$	1.35	1.4	1.6	V	If connected to an external RC network. 1)
IN pin OCP delay threshold	V_{LOOP}	2.45	2.6	2.75	V	Internal voltage reference
IN pin input current	I_{IN}	–	–	150	µA	V_IN > 2.1 V
IN pin pull down resistance	R_{PD_IN}	0.9	2.5	11	MΩ	V_IN = 5 V
IN pin pull down resistance	R_{PD_IN}	–	11	–	MΩ	1) V_IN = 4 V
IN pin fixed OCP delay threshold	$V_{FIXDELAY}$	2.75	2.9	3.065	V	Internal voltage reference
IN pin OCP fixed delay	$T_{FIXDELAY}$	9	12.5	16.5	µs	–
IN pin, on propagation delay	$T_{ON\_PROP\_DELAY}$	10	–	40	µs	From V_IN = 1.4 V till the first rising edge of CFN.
IN pin, off propagation delay	$T_{OFF\_PROP\_DELAY}$	–	–	10	µs	From V_IN = 1 V till the start of the falling edge of V_{GATE}
Main Gate Comparator						
VGS safe off threshold	$V_{GS\_SAFE\_OFF\_THR}$	–	2	3	V	–

1) Not subject to production test - specified by design

4.4 ESD ratings

Table 5 ESD susceptibility

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Human Body Model (HBM)	V_{ESD_HBM}	-2000	–	2000	V	HBM 1) 2)
Charge Device Model (CDM)	V_{ESD_CDM}	-1000	–	1000	V	CDM 1) 3)

1) Not subject to production test - specified by design
2) ESD robustness, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)
3) ESD robustness, Charge Device Model (CDM) according to ANSI/ESDA/JEDEC JS-002

4.5 Thermal characteristics

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.*

Table 6 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-ambient thermal resistance	$R_{\theta JA}$	–	99.3	–	K/W	1) 2)
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	–	44.87	–	K/W	T_A = 85°C 1)
Junction-to-case (bottom) thermal resistance	$R_{\theta JC(bot)}$	–	33.36	–	K/W	T_A = 85°C 1)

1) Not subject to production test - specified by design
2) The junction-to-ambient thermal resistance is simulated based on standard JESD51-5/7 using a FR4 2s2p board

4.6 Electrical characteristic graphs

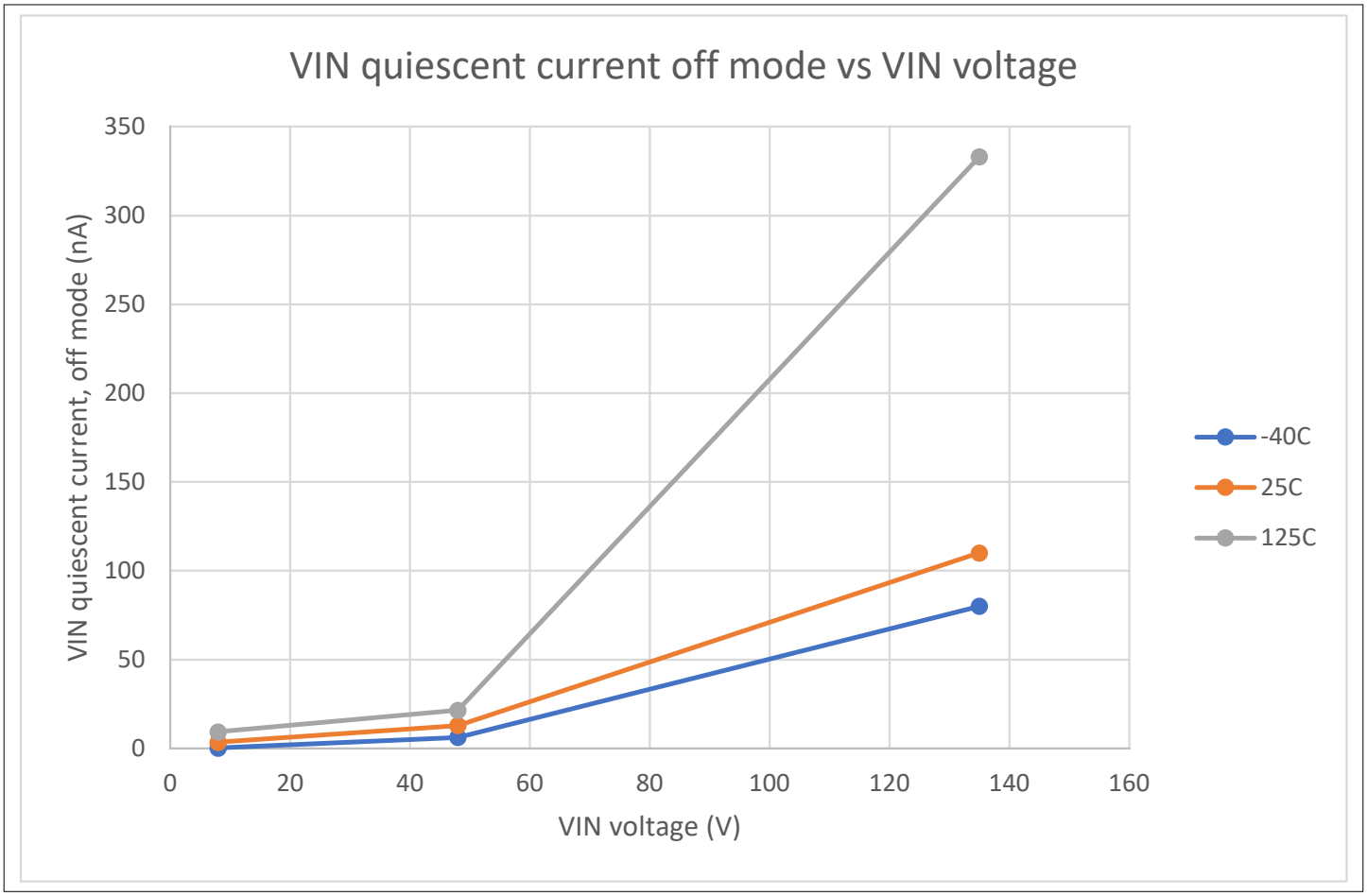


Figure 3 Quiescent current on VIN pin vs VIN voltage in off mode – V_IN < $VTHL_{IN}$

5 Product features

5.1 Feature description

The 1EDL8011 high side gate driver controls high side disconnect switch. The gate driver addresses two main use cases in these systems:

- Inrush current control: Allows controlled turn-on of the disconnect switch by using an external gate resistor (Rg) combined with a safe start-up and blanking mechanism.
- Short circuit protection: Whenever a short occurs on the load side, the load can be disconnected from the source by quickly turning off the disconnect switch. This is achieved by the internal pull-down mechanism of 1EDL8011 which protects the entire system.

The gate driver is supplied via a charge pump which supports fast start-up and ramping up the high side gate driver to 100% operation. The charge pump supports low input voltage operation while maintaining enough voltage at the gate driver output. The charge pump consists of two modules, the primary module uses an external capacitor (supports charging of MOSFET, voltage doubler-charge pump) to bring up the gate voltage V_{GATE}. After the target gate voltage is reached the secondary module becomes active which is an internally implemented charge pump with ultra low power capability allowing to be always connected to the battery rail.

The gate driver offers the following protection features:

- Main supply voltage UVLO
- Overcurrent protection with programmable threshold via resistor or analog signal
- Safe start-up of the disconnect switch with blanking of OCP
- Overcurrent protection latch-off and externally adjustable time delay for more flexibility

5.2 Device enable sequence

5.2.1 IN pin description

The IN pin is the input to the gate driver and controls the turn-on and turn-off of the main disconnect switch.

The IN pin is, however, a multi-function pin that provides the following functions:

1. IN controls the startup of the device:
   - If the IN pin voltage V_IN < $VTHL_{IN}$, the device is in the Off state and no internal circuits are functional. The device has lowest current consumption in Off state.
   - If the IN pin voltage V_IN ≥ $VTHH_{IN}$, first the internal circuits are turned On. Second, the input voltage VIN UVLO is also checked for proper operating voltage.
2. IN is the control signal for the gate driver
3. The IN pin with external RC circuit provides flexible blanking (see section 5.2.2) during start-up to prevent inrush current tripping overcurrent protection (OCP). The resistor circuit provides a programmable time delay (see section 5.5.1) for OCP tripping event.

An overview of the different device statuses is shown below:

Table 7 Device output depending on V_IN voltage

IN	Device status	GATE	VGS
V_IN < $VTHL_{IN}$	Off	Pull down	V_{GATE} - VS < $V_{GS\_SAFE\_OFF\_THR}$
V_IN ≥ $VTHH_{IN}$	On	Pull up	Gate turn-on

5.2.2 Safe start-up description and OCP blanking

A normal start-up sequence must meet various input conditions. Firstly, the supply voltage VIN is above $V_{VIN\_UVLO\_R}$ and secondly IN voltage is above $VTHH_{IN}$. After the device is active, the charge pump voltage rises and provides voltage V_{GATE} above VIN for proper biasing of the high side MOSFET. Then the MOSFETs are turned on and connect the power supply to the load system.

To provide a safe start-up function, user can adjust the OCP blanking time by using an external RC network connected to IN pin. During blanking time, the inrush current does not trigger an OCP event. OCP function and VDS sensing are described in section 5.5. After the blanking time (T_{BLANK}) has passed, the OCP function is activated. An input capacitance (C_{IN}) of atleast 1µF and rated according to supply voltage must be placed at the VIN pin. This capacitance helps in inductance decoupling and should be sized appropriately to prevent transitions on VIN reaching VIN UVLO. The safe start-up condition is shown in Figure 4.

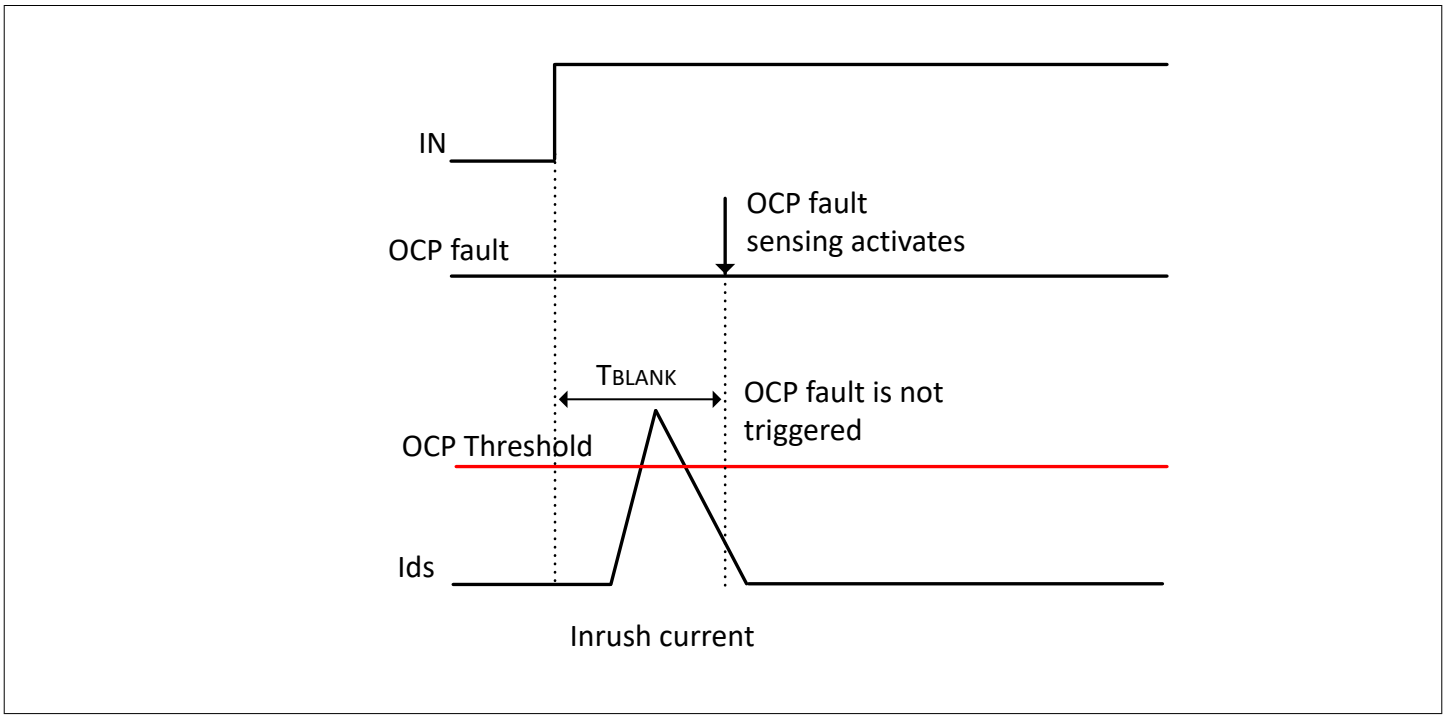


Figure 4 Safe start-up with OCP blanking

The OCP blanking time T_{BLANK} is designed by appropriately choosing the external passive components R1, R2, and C1. When the IN pin voltage V_IN is 5 V then R2 must be equal to R1/2.5 and when IN voltage is 3.3 V then R2 must be equal to R1. The V_IN voltage can be supplied from a microcontroller or other sources like voltage divider network. The RRC input slew rate must be met for proper functioning of OCP blanking and delay time. The RC network on IN pin creates an initial jump of the IN pin voltage to $V_{INITIAL}$ (see Figure 5). This level must be set high and fast enough to cross the $VTHH_{IN}$ threshold and starts the device. The selected RC components define the blanking time from the IN pin voltage $V_{INITIAL}$ to IN pin OCP delay threshold V_{LOOP}. The blanking time can be set as long as needed, however, turning-off should be performed as quickly as possible. A fast recovery Schottky diode D (see Figure 2) is always needed to ensure fast turn-off and prevent re-toggling.

Considering the IN pin propagation delay, the minimum blanking time during turn-on must be at least the maximum value of T_{PROP_DELAY}. Any blanking time calculation using C1 lower than T_{PROP_DELAY} is rounded up to the maximum value of T_{PROP_DELAY} because blanking time includes the IN pin propagation delay time. The approximate blanking time T_{BLANK} is calculated in the equation as the time parameter t:

$$V_{LOOP} = V_{INITIAL} + \left(V\_IN - V_{INITIAL}\right) * \left(1 - e^{-t/\tau}\right) \quad (1)$$

The assumption for calculating the blanking time is that, after the V_{LOOP} threshold is reached, the OCP delay feature immediately takes over to define the OCP event. This is true if the entire regulation current (I) at the IN flows into the internal timer capacitor C_{INT}. However there is still some current flowing to the blanking capacitor C1 which means

blanking period has not passed even though V_{LOOP} threshold is reached. To simplify the blanking time accurately, T_{BLANK} can be separated into two phases:

$$T_{BLANK} = T_{BLANK1} + T_{BLANK2} \quad (2)$$

T_{BLANK1} :

T_{BLANK1} is the approximate time it takes to reach V_{LOOP} when a voltage step is applied to RC network at the IN pin. Using Laplace equations and solving for a step function at V_IN, T_{BLANK1} can be calculated as below:

$$T_{BLANK1} = -\tau\left(1+\frac{a*b}{a+b}\right)*\ln\left[\left(1-\frac{V_{LOOP}}{V\_IN}*\left(1+\frac{a}{b}\right)\right)*\left(1+\frac{1}{a}+\frac{1}{b}\right)\right] \quad (3)$$

where, R = R2, a = R1/R2, b = R_{PD_IN}/R2, τ = R*C1

T_{BLANK2} :

T_{BLANK2} is active when Ids current is more than OCP threshold and stays higher over the entire start-up blanking period. The timer regulation loop starts to regulate the voltage to V_{LOOP} at IN pin. The resulting current is sourced on the internal capacitor C_{INT} to charge the voltage up the internal reference voltage V_{REF} of a fault comparator. With OCP fault observed, T_{BLANK} = T_{BLANK1} + T_{BLANK2}

$$T_{BLANK2} = \frac{V_{REF}}{V_{LOOP}-V_{CBLANK1}}*R*\sqrt{2*C1*Cint*k} \quad (4)$$

Where, C_{int} = 1 nF

The correction factor k is calculated as:

$$k = 1.1+\frac{1\ nF}{1.4*C1} \quad (5)$$

$$V_{CBLANK1} = V\_IN*\frac{b}{a+b}*\left(1-e^{-\frac{T_{BLANK1}}{\tau*\left(1+\frac{ab}{a+b}\right)}}\right) \quad (6)$$

If no OCP fault is detected then T_{BLANK} = T_{BLANK1}

The diagram of the turn-on and OCP blanking time periods is shown in Figure 5

T_{BLANK} calculations

Example 1: When V_IN = 5 V and R1=400 kΩ, R2=R1/2.5=160 kΩ and C1 = 10 nF

Using the equations above T_{BLANK1} = 2.33 ms and T_{BLANK2} = 0.88 ms,

the total blanking time is

$$T_{BLANK} = T_{BLANK1} + T_{BLANK2} = 3.21 \ ms \quad (7)$$

Example 2: When V_IN = 3.3 V and R1=5 kΩ and R2=R1=5 kΩ and C1 = 150 nF
Using the equations above T_{BLANK1} = 1.29 ms and T_{BLANK2} = 0.12 ms

$$T_{BLANK} = T_{BLANK1} + T_{BLANK2} = 1.41 \ ms \quad (8)$$

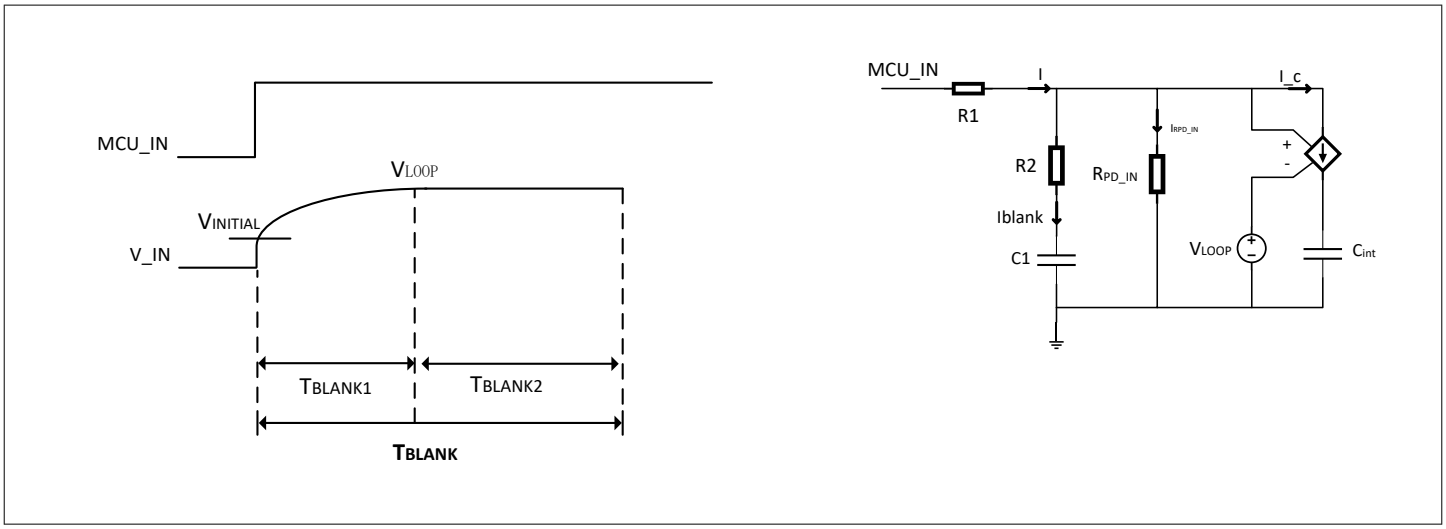


Figure 5 OCP blanking time periods set up and internal mechanism

5.3 Gate driver

5.3.1 Gate driver description

The gate driver controls the gate of the disconnect switch.

- Turn-on: The source current is provided directly by the charge pump.
- Turn-off: The GATE pin is shorted to VS through an internal pull-down mechanism.

Users can optimize the turn-on and turn-off switching behaviors by adding external components like gate resistors and antiparallel diodes.

5.3.2 Unpowered gate clamp

During Off state, the device has an active clamp mechanism to prevent the GATE pin from entering an undefined state. The active clamp circuit (refer to R_{PULL} in Table 4) ensures a proper clamping of the device output when no supply voltage is applied to the device and will deactivate as soon as the pull-up gate driver is turned on.

5.4 Charge pump

Supply for the gate driver is provided by a charge pump with an external flying capacitor C_{FPN} connected at pins CFP and CFN. The output of the charge pump is available at the GATE pin to provide a direct sourcing current. An external capacitor C_{TANK} can be placed between the GATE and VS pins along with an external gate resistor R_G (if needed) as shown in see Figure 2.

The C_{TANK} capacitor must be properly chosen to provide low voltage ripple and the desired turn-on of the disconnect switch. It is recommended to select C_{TANK} = 10×C_{FPN}, where C_{FPN} is the flying capacitor. The recommended value of C_{FPN} is between 100 pF and 10 nF as it reduces stress on internal devices and prevents potential damage to the charge pump by the inrush current. A resistance R_{ser} must be added in series to C_{FPN} based on the value of C_{FPN} as shown in the table below, or a Schottky diode D_{sh} (20 V, 1 A) must be connected between C_{FPN} and GATE pin (if C_{FPN} > 1nF).

C_{FPN} (nF)	R_{ser} (Ω)
≤ 1	Not needed
2.2	25
4.7	50
10	100

The charge pump is enabled when V_IN > $VTHH_{IN}$ and the IN propagation delay has passed. The main reason for having an external flying capacitor is the possibility to achieve a fast startup by properly sizing the flying capacitor with regard to the C_{TANK} capacitor. This also helps in maintaining a low voltage ripple at V_{GATE} during turn-on as the charge pump experiences high load during the turn-on of the disconnect switch. After the switch has turned on, the gate voltage is supplied from the auxiliary charge pump. The start-up time of gate driver is related to the internal impedance of the charge pump, the flying capacitor C_{FPN}, R_{SER}, tank capacitor C_{TANK}, external gate resistor R_G and MOSFET input capacitance.

5.5 VDS sensing

5.5.1 VDS sensor features and activation

The 1EDL8011 integrates a VDS sense feature that allows the device to react safely to OCP events with a certain time delay and provide amplified V_{DS} voltage over the ILIMIT pin. It includes a V_{DS} fault comparator that is used to trigger OCP shutdown by monitoring the voltage difference between VIN and VS pins. The signal on the ILIMIT pin can be measured by a microcontroller for different purposes like current monitoring.

Note: To disable VDS sensing, connect the ILIMIT pin to GND.

Features of the VDS sensor

VDS sensing module offers the following features:

- Amplification stage with possible analog reading through the ILIMIT pin
- External gain setting using the R3 resistor with flexible OCP values
- Configurable OCP filter delay via R1 and R2 to filter out possible system noise
- Fixed minimum OCP time delay provided with no RC network on the IN pin

Activating the VDS Sensor (OCP and current monitoring)

The device monitors the voltage difference between VIN and VS pins which is the same as the voltage across R_{DSON} minus the threshold voltage set by external resistor R3 on the ILIMIT pin. Once the device is active and the IN pin voltage is greater than V_{THOCP_EN} (V_{THOCP_EN} < V_{LOOP}), the OCP function is enabled. The voltage on the ILIMIT pin (V_{ILIMIT}) is then internally compared to a fixed reference V_{REF}. If V_{ILIMIT} > V_{REF}, then the comparator starts the charge of an internal capacitor C_{INT}. The current rate at which this capacitor is charged depends on the selection of T_{DELAY} value, configured via external resistor R1 connected to IN pin. This means user can configure how fast the C_{INT} capacitor is charged with those resistors. Once the voltage on C_{INT} crosses V_{REF}, the OCP_DELAY comparator is activated switching off the disconnect MOSFET. In this way, user can define with R1, how much deglitch filter is applied after VDS sensor detects an OCP condition and before the MOSFET is turned off. The analog signal monitoring on ILIMIT PIN is active since the start-up of the device.

OCP function is only activated after the blanking time, T_{BLANK}, has passed. If no RC network is connected, there is no blanking time.

Pins required for VDS sensing and OCP delay are:

- VIN: MOSFET drain pin. Connected on the PCB to VIN as close as possible to the drain of the disconnect switch
- VS: MOSFET source pin. Connected on the PCB as close as possible to the source of the disconnect switch.
- ILIMIT: R3 resistor on the pin defines the amplifier gain. This pin also holds the analog signal proportional to the V_{DS} voltage. If an application does not need OCP feature, the ILIMIT pin must be pulled down to GND and the VDS sensor is deactivated.
- IN: IN pin not only provides a chip enable function but also OCP time delay value through external resistor R1and R2 on IN pin. Users can decide how long the OCP event will be present in the system before it is acknowledged as a fault. If users do not want to use passive external components on the IN pin then a fixed delay time, $T_{FIXDELAY}$, will be implemented by default.

The block diagram of the internal OCP function blocks and the configurable time delay is shown Figure 6

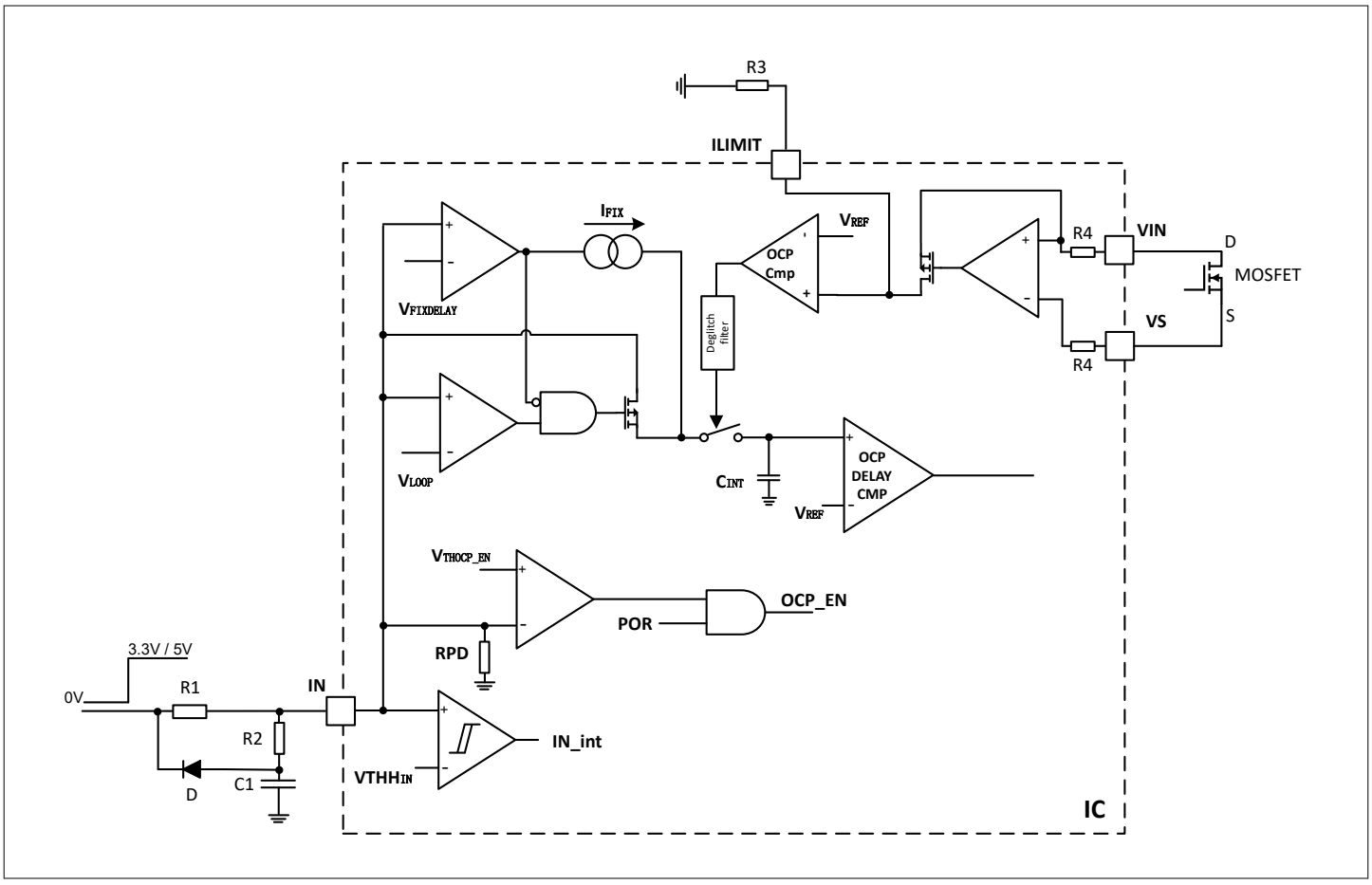


Figure 6 Functional diagram of the flexible OCP time delay and OCP blanking

5.5.2 VDS sensor OCP delay parameters set up

OCP Threshold Setting

The V_{DS} voltage will be transformed into a current flowing through R3 on ILIMIT pin. OCP threshold V_{ILIMIT} is internally compared to V_{REF} voltage. The gain levels can be changed and set by resistor R3 and used for sensing the current through the MOSFET (I_{DS}).

The V_{ILIMIT} can be calculated using the equation below:

$$V_{ILIMIT} = \left[\frac{I_{DS} * \left((R_{DSON} * k1) / N \right)}{R_4} \right] * R_3 \quad (9)$$

Where,

R4 is the internal resistor
R_{DSON} of the MOSFET
N is the number of MOSFETs in parallel
k1 is the temperature coefficient

Sample Overcurrent Threshold (I_{DS}) calculation

In order to calculate overcurrent threshold we use $V_{ILIMIT} = V_{REF} = 1.2$ V because OCP is triggered when $V_{ILIMIT} > V_{REF}$. Using equation 9 for overcurrent I_{DS} calculation when R_{DSON} =3.3 mΩ, R3 = 50 kΩ , N = 1, k1 = 1

$$I_{DS} = \frac{1.2\ V\ *\ 10\ k\Omega}{3.3\ m\Omega\ *\ 50\ k\Omega} \tag{10}$$

Hence, I_{DS} is 72 A

OCP Delay Setting T_{DELAY}

OCP delay time can be set using external resistor R1 to obtain a T_{DELAY} ranging from 10 µs to 200 µs. It is recommended to use a resistor R1 with a value of less than 400 kΩ. OCP delay time T_{DELAY} is defined from the moment $V_{ILIMIT} > V_{REF}$ to the falling edge of gate voltage. MOSFET turn-off time depends on external gate resistor, MOSFET input capacitance and tank capacitor. Therefore, total turn-off time during OCP events is the sum of OCP delay time and MOSFET turn-off time. The equation for calculating T_{DELAY} is

$$T_{DELAY} = \frac{C_{INT} * V_{REF}}{I} \tag{11}$$

$$I = \frac{V\_IN - V_{LOOP}}{R1} \tag{12}$$

Where C_{INT} = 1 nF, V_{REF} is typically 1.2 V, V_{LOOP} is typically 2.6 V (see Table 4), V_IN is typically 5 V or 3.3 V.

T_{DELAY} calculation

Example 1: When V_IN = 5V and R1 = 20 kΩ

$$T_{DELAY} = \frac{1\ nF * 1.2\ V}{(5\ V - 2.6\ V)/(20\ k\Omega)} = 10\ \mu s \tag{13}$$

Example 2: When V_IN = 3.3 V and R1 = 6 kΩ

$$T_{DELAY} = \frac{1\ nF * 1.2\ V}{(3.3\ V - 2.6\ V)/(6\ k\Omega)} = 10\ \mu s \tag{14}$$

The OCP T_{DELAY} and device turn-on diagram is shown in Figure 7

OCP fault reset

The OCP fault is a latched fault and can be reset by cycling the IN pin.

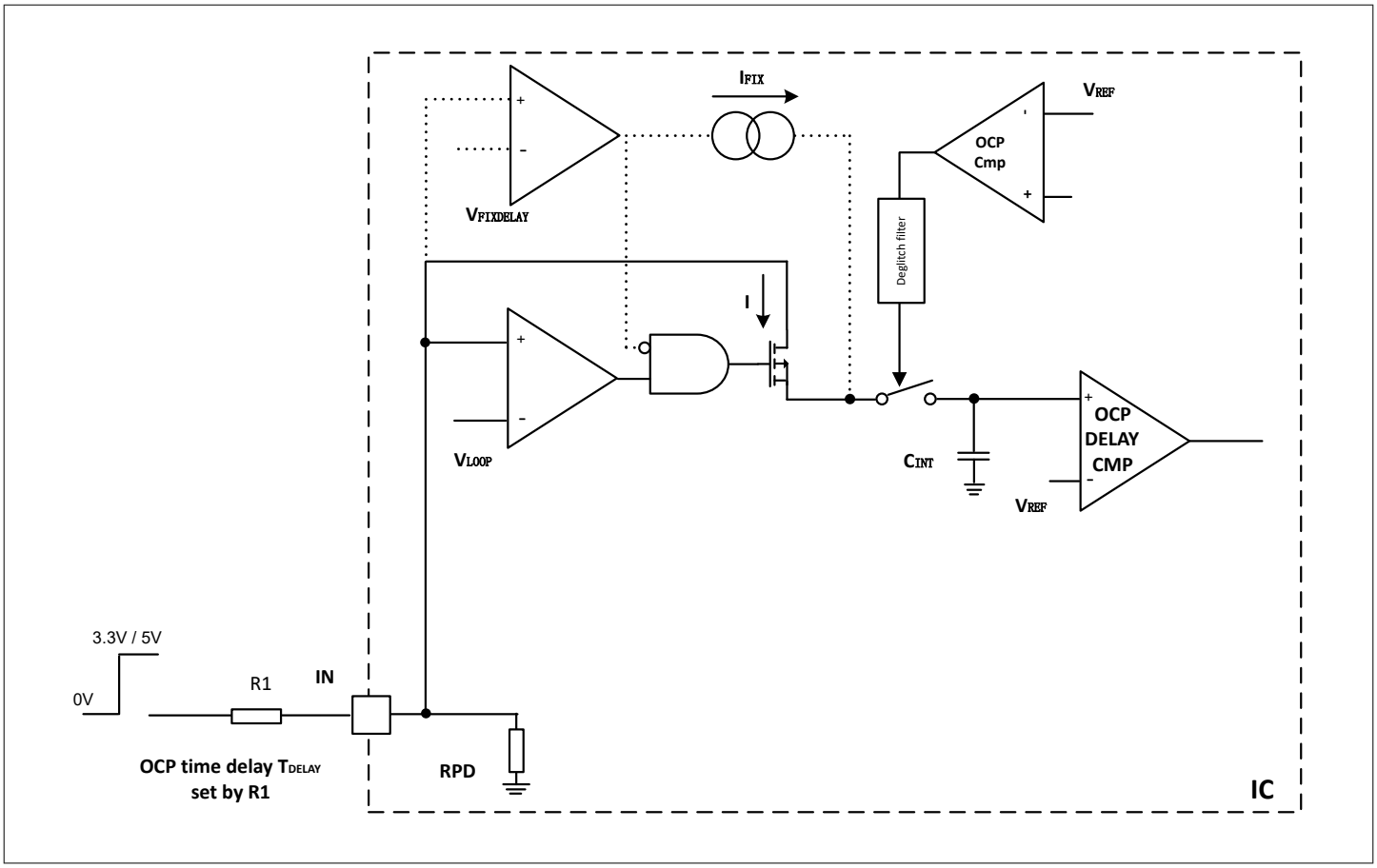


Figure 7 OCP delay time set up diagram

5.5.3 VDS sensor, start-up blanking and OCP delay application use cases

Below are some possible use cases for VDS sensor :

OCP event with fixed delay $T_{FIXDELAY}$

This is an example in which no RC components are used and the blanking time is not configured. The OCP threshold is set by R3 resistor on the ILIMIT pin. In this case, user has to ensure inrush current I_{DS} through the MOSFET does not exceed the OCP threshold. Once IN pin is set high, the OCP circuitry dictated by $V_{FIXDELAY}$ is activated (shown by dotted lines in Figure 7). In the normal On condition of MOSFET, if I_{DS} rises above OCP threshold for a time duration T2 longer than $T_{FIXDELAY}$ (as shown in Figure 8) then OCP fault is triggered. After the fault is triggered the MOSFET is turned off and the device is latched until the IN pin is cycled.

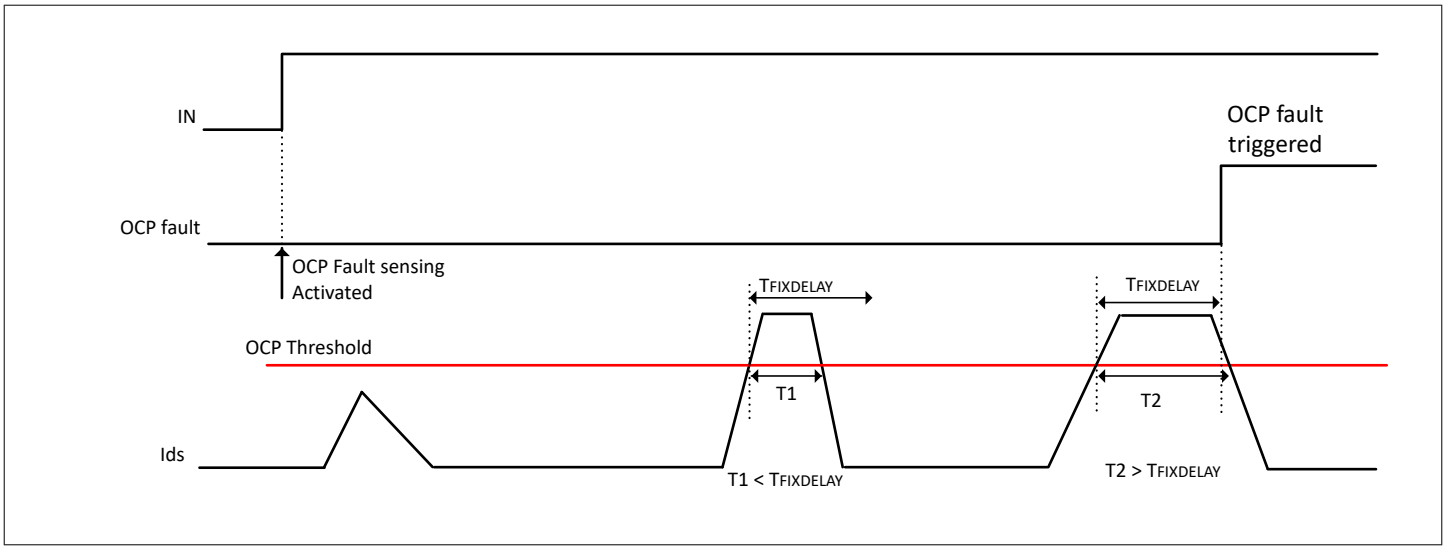


Figure 8 OCP event with fixed delay time

OCP event with flexible time delay and adjustable blanking time, case 1

This is an example for designing flexible delay time T_{DELAY} and a short blanking time. A short blanking time can be configured by appropriately choosing the external RC components (R1, R2 and C1) on the IN pin (see Equation 2) and T_{DELAY} can be configured by choosing R1 (see Equation 11). Three possible scenarios are depicted in Figure 9 depending on I_{DS} current level and duration. A short blanking time can be useful in systems where an external precharge path exists that takes over the inrush current of the load. With an external precharge circuit, if the inrush current through the MOSFET is less than the OCP threshold value, the OCP fault is not triggered. OCP feature is active after the blanking time has passed. During normal operation of MOSFET, if the I_{DS} current exceeds OCP threshold value and stays high for time duration T2 longer than T_{DELAY} then OCP fault is triggered. After the OCP fault is triggered, the MOSFET is turned off and the device is latched until the IN pin is cycled. The external diode (see D in Figure 2) allows the system to ensure that the turn-off is fast enough.

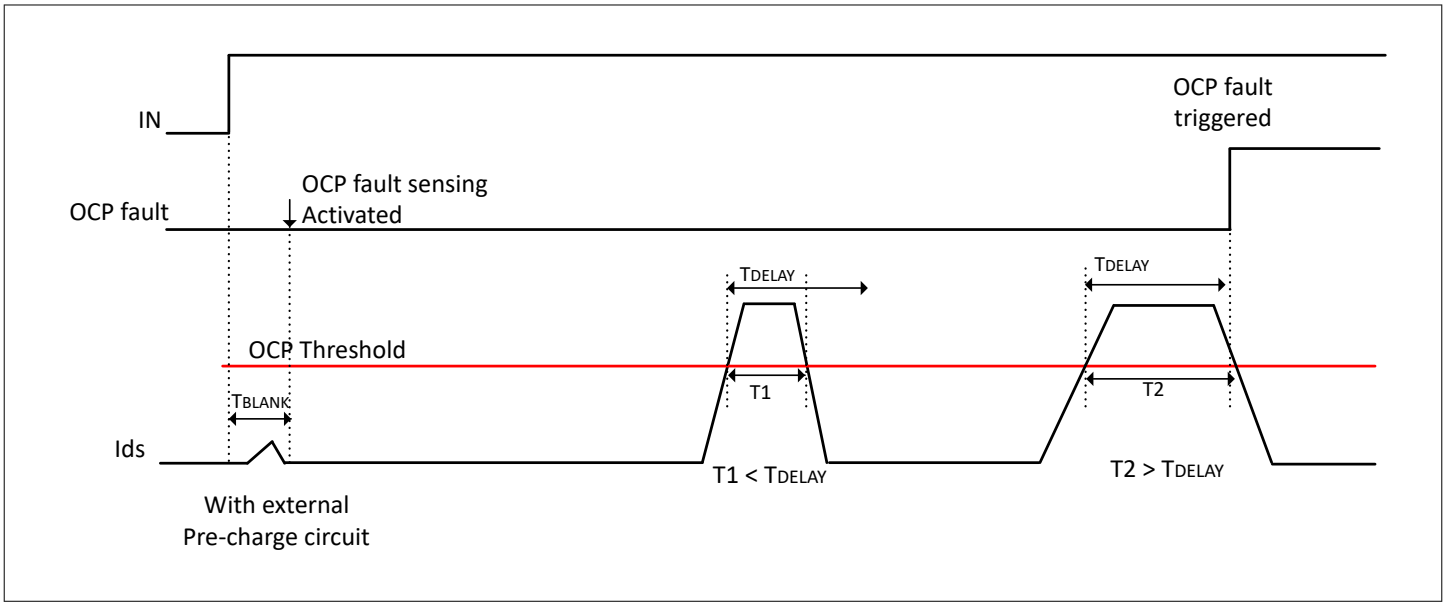


Figure 9 OCP event with short blanking time and flexible time delay, case 1

OCP event with flexible time delay and adjustable blanking time, case 2

This is an example for designing flexible delay time T_{DELAY} and longer blanking time. Three possible scenarios are depicted in Figure 10 similar to case 1. If a system has no external precharge circuit then inrush current through the

MOSFET might exceed OCP threshold. If this current persists for a time duration T1 shorter than T_{BLANK} then OCP fault is not triggered. This configuration is particularly useful if the inrush current is expected for a calculated amount of time. A long blanking time can be configured by setting the external RC components on the IN pin and T_{DELAY} can be configured by setting R1.

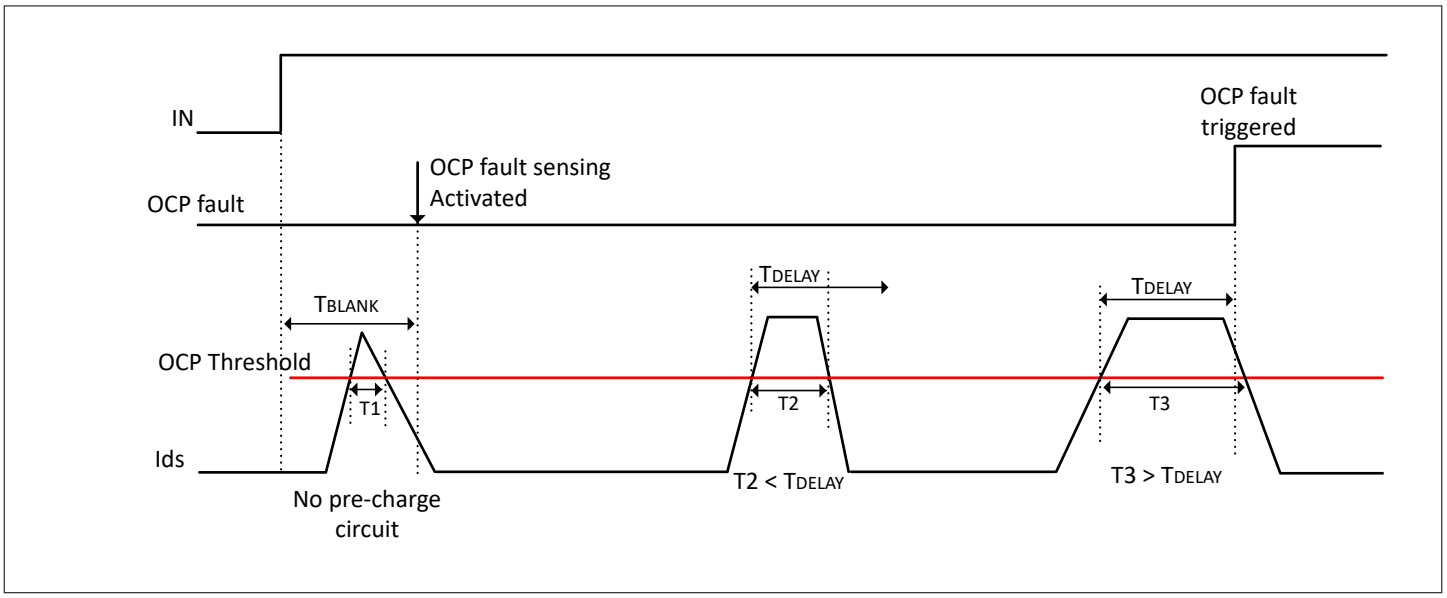


Figure 10 OCP event with long blanking time and flexible time delay, case 2

OCP deactivation

To disable OCP blanking and T_{DELAY} function, ILIMIT pin must be shorted to GND. The device detects this condition and turns off the VDS sensing and OCP circuitry.

5.6 Safe switch off

In order to ensure proper turn-off of the MOSFET (when IN pin is pulled down), it is essential to keep the power supply of the device active to enable all circuits to safely pull down. To ensure this, the gate driver contains a mechanism for switching off safely.

This mechanism works as follows:

- When IN pin is pulled down, GATE pin starts discharging the MOSFET. This causes the V_{GS} voltage to drop.
- Once the V_{GS} voltage reaches the VGS safe off threshold ($V_{GS\_SAFE\_OFF\_THR}$), the device is powered down. During the Off state, R_{PULL} is present between terminals GATE and VS to prevent spurious turn-on.
- To initiate a new power-up sequence, the IN pin must be switched On again.

5.7 Undervoltage lockout protection (UVLO)

5.7.1 VIN UVLO

The device contains a UVLO circuit to monitor the supply voltage VIN, referred to as VIN UVLO. The VIN UVLO works in the following way:

- If the VIN voltage rises above the UVLO rising threshold ($V_{VIN\_UVLO\_R}$) and the IN pin is turned on then the device is enabled.
- When device is On and VIN voltage drops below the UVLO falling threshold ($V_{VIN\_UVLO\_F}$), the VIN UVLO is asserted and the fault is latched. This switches off the disconnect MOSFET and the gate driver is disabled. To restart the operation, the device needs to cycle the IN pin when the VIN voltage is above the UVLO rising threshold.

The UVLO circuitry incorporates a hysteresis ($V_{VIN\_UVLO\_R}$ - $V_{VIN\_UVLO\_F}$) to prevent malfunctions (see Table 4).

5.8 Fault table

Table 8 lists possible fault conditions.

Table 8 Protection features

Name	Description	Filter	Latched	Action
VIN UVLO	Input voltage UVLO	Yes	Yes	• MOSFET turns Off • Gate driver disabled • IN pin must be cycled for reactivation
OCP	Overcurrent protection threshold for VDS sensing	Flexible delay time set using external resistors R1 and R2 on the IN pin	Yes	• MOSFET turns Off • Gate driver is disabled • Cycle VIN and IN pin to continue operation.
Safe switch off	Gate monitoring fault	None	N/A	• MOSFET turns Off • Gate driver is disabled • Cycle VIN and IN pin to continue operation.

6 Application information

6.1 Battery power application system

Note: *The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

Figure 11 shows a possible usage of the high side gate driver in a battery-powered motor drive application.

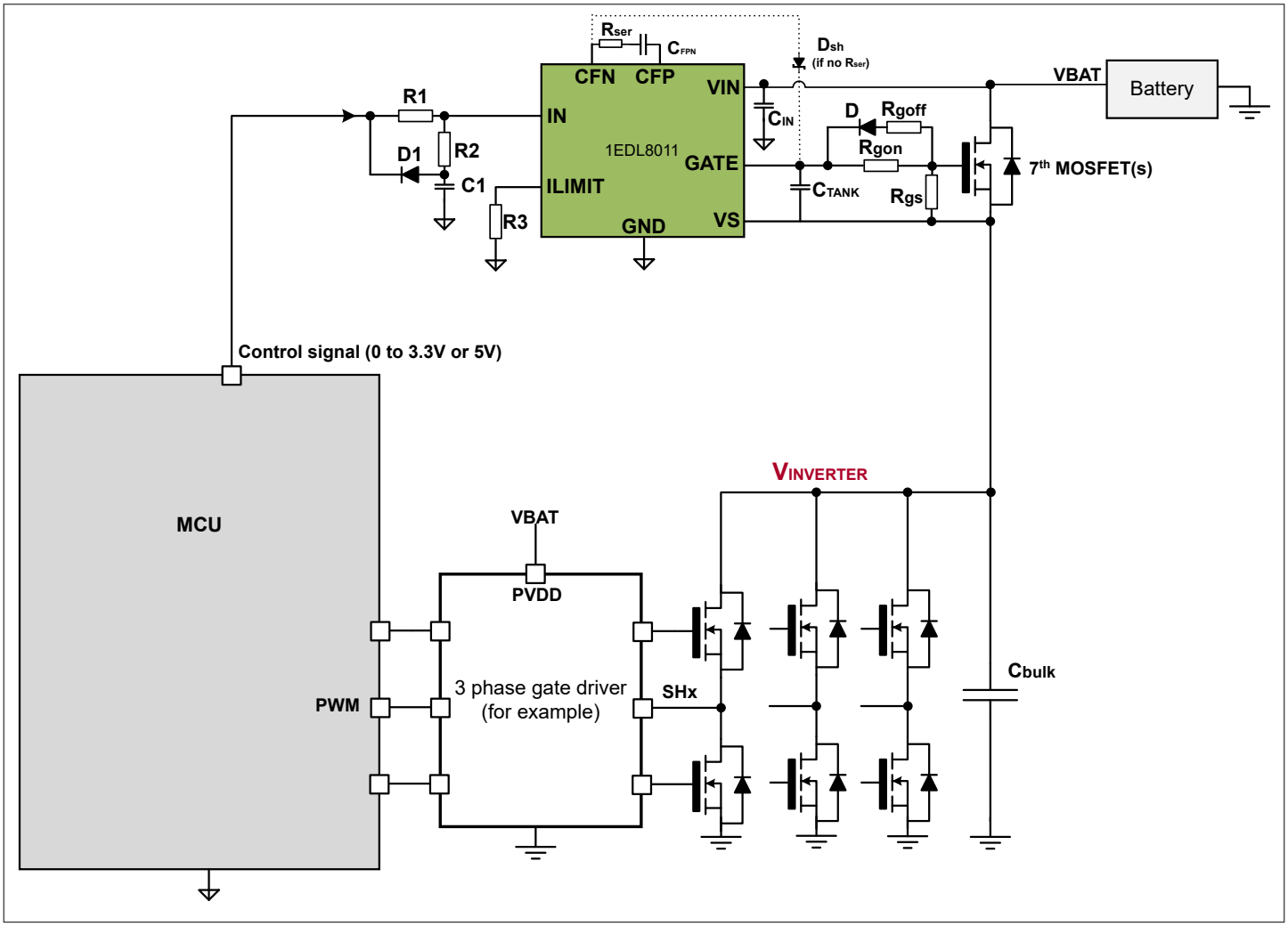


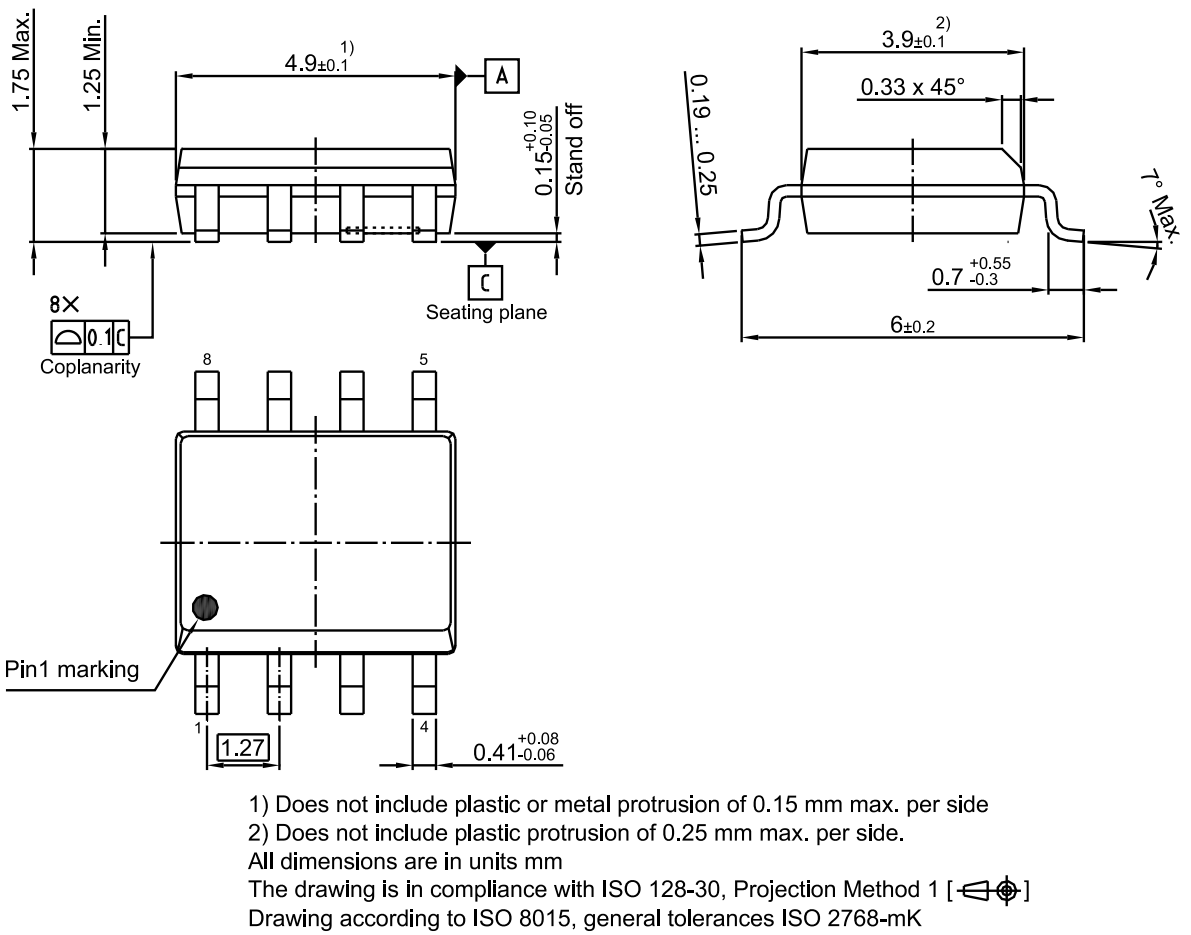
Figure 11 Battery power application system block diagram

7 Package

The high side gate driver is provided in 8 pin package:

Product name	Package	Package size	Lead pitch
1EDL8011	PG-DSO-8-92	5.0 mm × 6.0 mm	1.27 mm

PG-DSO-8-92 package outline and footprint are shown in Figure 12 and Figure 13



1) Does not include plastic or metal protrusion of 0.15 mm max. per side
2) Does not include plastic protrusion of 0.25 mm max. per side.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 12 PG-DSO-8-92 package outline

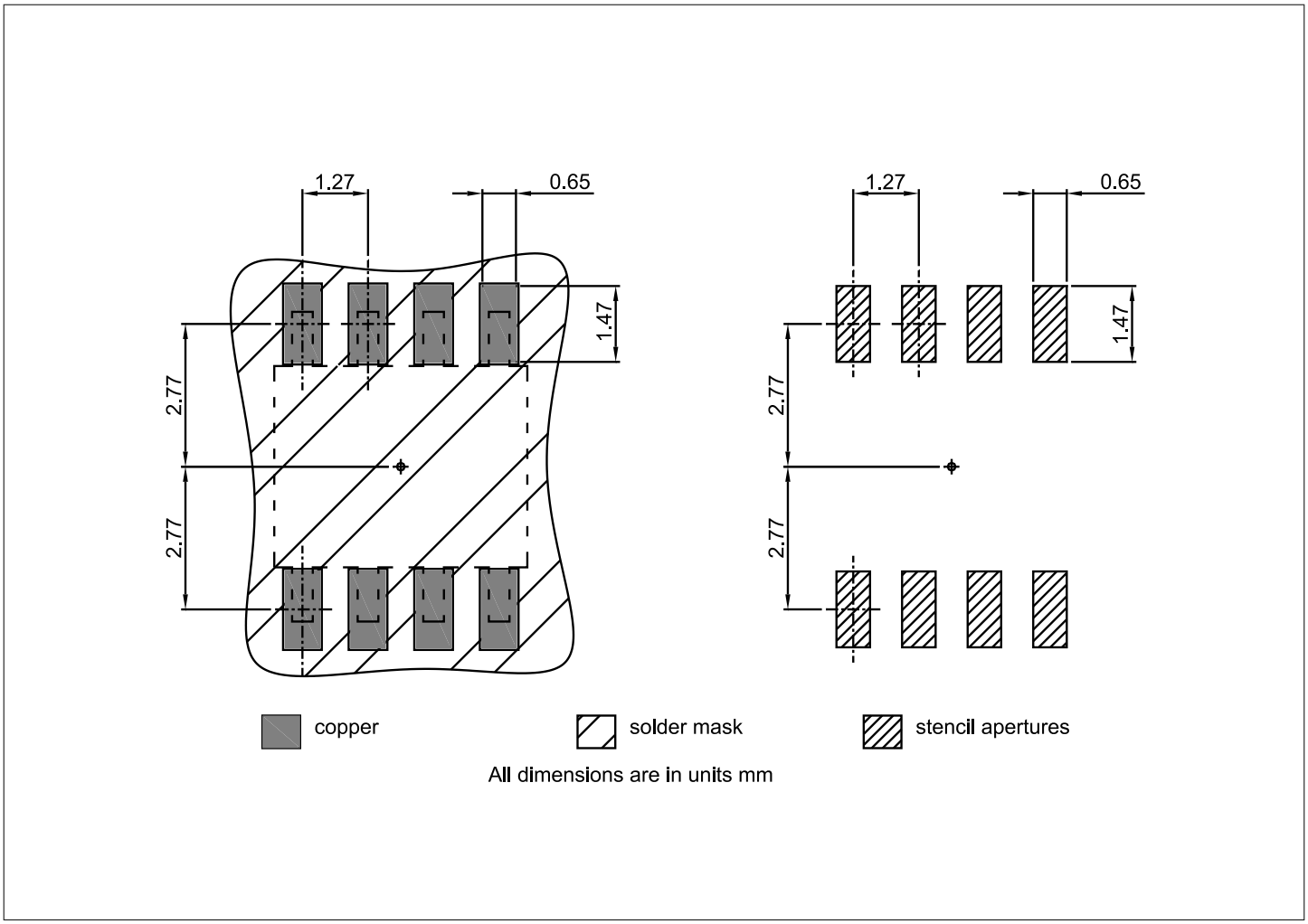


Figure 13 PG-DSO-8-92 package footprint

Green product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

8 Revision history

Revison	Date	Description of changes
Rev. 1.0	2024-06-21	Initial release

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