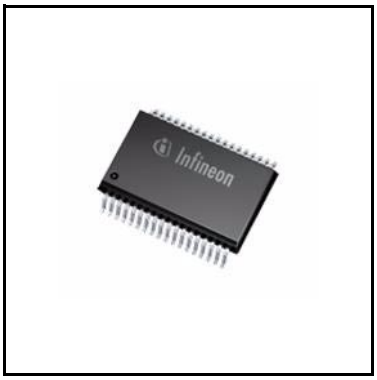
EiceDRIVER™ SENSE

1EDI2010AS

High voltage IGBT driver for automotive applications
Single channel isolated driver
Hardware description
A12 Step

AEC Qualified RoHS



Features

- Single-channel IGBT-driver
- On-chip galvanic insulation
- Support of existing IGBT technologies up to 1200 V
- Low propagation delay and minimal PWM distortion
- Support of 5-V logic levels (primary side)
- Supports both negative and zero-volt V_{EE2} supply voltage
- 16-bit standard SPI interface (up to 2 MBaud) with daisy chain support (primary side)
- Enable input pin (primary side)
- Pseudo-differential inputs for critical signals (primary side)
- Power-on reset pin (primary side)
- Debug mode
- Internal pulse suppressor
- Fully programmable active clamping inhibit signal (secondary side)
- Fully programmable two-level turn-on (TTON)
- Fully programmable two-level turn-off (TTOFF)
- 8-bit ADC with programmable offset and gain, and a flexible trigger mechanism
- Emulated digital channel
- Programmable desaturation monitoring
- Overcurrent protection with programmable threshold
- Automatic emergency turn-off in failure case
- Undervoltage supervision of 5 V and 15 V supplies
- Programmable UVLO2 and DESAT thresholds for MOSFET usage
- Safe internal state machine
- Internal lifesign watchdog
- Weak turn-on
- NFLTA and NFLTB notification pins for fast system response time (primary side)
- Individual error and status flags readable via SPI

- Compatible to EiceBoost family
- 36-pin PG-DSO-36 green package
- Green Product (RoHS compliant)

Potential applications

- Inverters for automotive hybrid electric vehicles (HEV) and electric vehicles (EV)
- High-voltage DC/DC converter
- Industrial drive

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The 1EDI2010AS is a high-voltage IGBT gate driver designed for motor drives above 5 kW. The 1EDI2010AS is based on Infineon's Coreless Transformer (CLT) technology, providing galvanic insulation between low-voltage and high-voltage domains. The device has been designed to support IGBT technologies up to 1200 V.

The 1EDI2010AS can be connected on the low-voltage side ("primary" side) to 5-V logic. A standard SPI interface allows the logic to configure and control the advanced functions implemented in the driver.

On the high-voltage side ("secondary" side), the 1EDI2010AS is dimensioned to drive an external booster stage. Short propagation delays and controlled internal tolerances lead to minimal distortion of the PWM signal.

The 1EDI2010AS supports advanced functions (such as two-level turn-on, two-level turn-off, etc.), that can be controlled and configured via a standard SPI interface.

The internal 8-bit ADC (SAR) with programmable gain and offset enables the sensing of the DC link voltage, the phase voltage, or of the temperature sensor located on the power module (such as NTC, temperature diode, etc.). The digitalized value can be read via the SPI interface on the primary side. The ADC thus enables significant cost savings at the system level, since it removes the need for discrete isolation ICs.

The 1EDI2010AS can be used optimally with Infineon's 1EBN100XAE EiceDRIVER™ Boost booster stage family.

Type	Package	Ordering code
1EDI2010AS	PG-DSO-36	SP001299836

Table of Contents

1 Functional description

1.1 Introduction

The 1EDI2010AS is an advanced single-channel IGBT driver that can also be used for driving power MOS devices. The device has been developed in order to optimize the design of high performance automotive inverters.

The device is based on Infineon's coreless transformer technology and consists of two chips separated by galvanic isolation. The low-voltage (primary) side can be connected to standard 5-V logic. The high-voltage (secondary) side is in the DC-link voltage domain.

Internally, the data transfers are ensured by two independent communication channels. One channel is dedicated to transferring only the ON and OFF information of the PWM input signal. This channel is unidirectional (from the primary to the secondary side). Because this channel is dedicated to the PWM information, latency time and PWM distortion are minimized. The second channel is bidirectional and is used for all other data transfers (for example, status information).

The 1EDI2010AS supports advanced functions, such as two-level turn-on and two-level turn-off, in order to optimize the switching behavior of the IGBT. Furthermore, it supports several protection functions such as DESAT, overcurrent protection, etc.

1.2 Pin configuration and functionality

1.2.1 Pin configuration

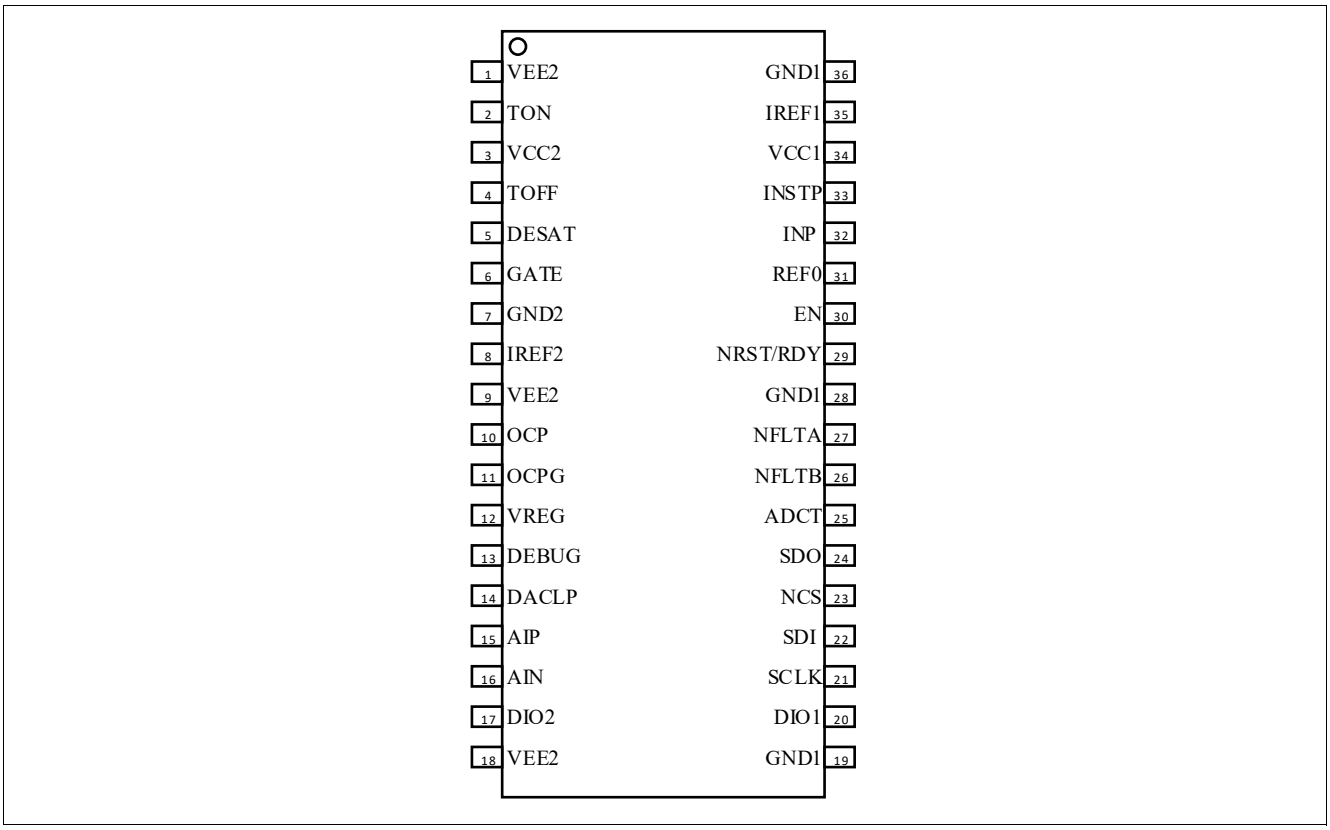


Figure 1 EiceSENSE pin configuration

Table 1 Pin configuration

Pin number	Symbol	I/O	Voltage class	Function
1,9,18	VEE2	Supply	Supply	Negative power supply[1)]
2	TON	Output	15 V secondary	Turn-on output
3	VCC2	Supply	Supply	Positive power supply
4	TOFF	Output	15 V secondary	Turn-off output
5	DESAT	Input	15 V secondary	Desaturation protection input
6	GATE	Input	15 V secondary	Gate monitoring input
7	GND2	Ground	Ground	Ground
8	IREF2	Input	5 V secondary	External reference input
10	OCP	Input	5 V secondary	Overcurrent protection
11	OCPG	Ground	Ground	Ground for the OCP function
12	VREG	Output	5 V secondary	Reference output voltage
13	DEBUG	Input	5 V secondary	Debug input
14	DACLP	Output	5 V secondary	Active clamping disable output

Table 1 Pin configuration (cont'd)

Pin number	Symbol	I/O	Voltage class	Function
15	AIP	Input	5 V analog secondary	ADC positive analog input
16	AIN	Input	5 V analog secondary	ADC negative analog input
17	DIO2	Input/output	5 V secondary	Digital I/O
19, 28, 36	GND1	Ground	Ground	Ground[2)]
20	DIO1	Input/output	5 V primary	Digital I/O
21	SCLK	Input	5 V primary	SPI serial clock input
22	SDI	Input	5 V primary	SPI serial data input
23	NCS	Input	5 V primary	SPI chip select input (low-active)
24	SDO	Output	5 V primary	SPI serial data output
25	ADCT	Input	5 V primary	ADC trigger input
26	NFLTB	Output	5 V primary	Fault B output (low-active, open drain)
27	NFLTA	Output	5 V primary	Fault A output (low-active, open drain)
29	NRST/RDY	Input/output	5 V primary	Reset input (low-active, open drain). This signal notifies that the device is "ready".
30	EN	Input	5 V primary	Enable input
31	REF0	Ref. ground	Ground	Reference ground for signals **INP**, **INSTP**, **EN**
32	INP	Input	5 V primary	Positive PWM input
33	INSTP	Input	5 V primary	Monitoring PWM input
34	VCC1	Supply input	Supply	Positive power supply
35	IREF1	Input	5 V primary	External reference input

1) All **VEE2** pins must be connected together.
2) All **GND1** pins must be connected together.

1.2.2 Pin functionality

1.2.2.1 Primary side

GND1

Ground connection for the primary side.

VCC1

5-V power supply for the primary side (referring to GND1).

INP

Non-inverting PWM input of the driver. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to V_{REF0} drives this input to low-state in case the pin is floating.

INSTP

Monitoring PWM input for shoot-through protection. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to V_{REF0} drives this input to the low state in case the pin is floating.

REF0

Reference ground signal for the signals **INP**, **INSTP**, and **EN**. This pin must be connected to the ground signal of the logic issuing those signals.

EN

Enable input signal. This signal allows the logic on the primary side to turn off and deactivate the device. An internal weak pull-down resistor to V_{REF0} drives this input to the low state in case the pin is floating.

NFLTA

Open-drain output signal used to report major failure events (Class A event). In case of an error event, **NFLTA** is driven to the low state. This pin must be connected externally to V_{CC1} with a pull-up resistance.

NFLTB

Open-drain output signal used to report major failure events (Class B event). In case of an error event, **NFLTB** is driven to the low state. This pin must be connected externally to V_{CC1} with a pull-up resistance.

SCLK

Serial clock input for the SPI interface. An internal weak pull-up device to V_{CC1} drives this input to high state in case the pin is floating.

SDO

Serial data output (push-pull) or the SPI interface.

SDI

Serial data input for the SPI interface. An internal weak pull-up device to V_{CC1} drives this input to high state in case the pin is floating.

NCS

Chip select input for the SPI interface. This signal is low-active. An internal weak pull-up device to V_{CC1} drives this input to the high state in case the pin is floating.

IREF1

Reference input of the primary chip. This pin must be connected to V_{GND1} via an external resistor.

NRST/RDY

Open-drain reset input. This signal is low-active. When a valid signal is received on this pin, the device is put into its default state. This signal is also used as a “ready” notification. A high level on this pin indicates that the primary chip is functional.

DIO1

I/O for the digital channel. Depending of the chosen configuration of the device, this pin can be an input or an output (push-pull). An internal weak pull-down resistor to V_{GND1} drives this input to the low state in case the pin is floating.

ADCT

ADC trigger input. An internal weak pull-down device to VGND1 drives this input to the low state in case the pin is floating.

1.2.2.2 Secondary side

VEE2

Negative power supply for the secondary side, referring to V_{GND2}.

VCC2

Positive power supply for the secondary side, referring to V_{GND2}.

GND2

Reference ground for the secondary side.

DESAT

Desaturation protection input pin. The function associated with this pin monitors the V_{CE} voltage of the IGBT. The detection threshold is programmable. An internal pull-up resistor to V_{CC2} drives this signal to the high level in case it is floating.

OCP

Overcurrent protection input pin. The function associated with this pin monitors the voltage across a sensing resistance located on the auxiliary path of a current-sense IGBT. An internal weak pull-up resistor to the internal 5-V reference drives this input to the high state in case the pin is floating.

OCPG

Overcurrent protection ground.

TON

Output pin for turning on the IGBT.

TOFF

Output pin for turning off the IGBT.

GATE

Input pin used to monitor the IGBT gate voltage.

DEBUG

Debug input pin. This pin is latched at power-up. When a high level is detected on this pin, the device enters a special mode where it can be operated without SPI interface. This feature is provided for development purpose only. This pin should normally be tied to V_{GND2}. An internal weak pull-down resistor to V_{GND2} drives this input to the low state in case the pin is floating.

IREF2

Reference input of the secondary chip. This pin must be connected to V_{GND2} via an external resistor.

VREG

Reference output voltage. This pin must be connected to an external capacitance to V_{GND2}.

DACLP

Output pin used to disable the active clamping function of the booster.

DIO2

I/O for the digital channel. Depending of the chosen configuration of the device, this pin can be an input or an output (push-pull). An internal weak pull-down resistor to V_{GND2} drives this input to the low state in case the pin is floating.

AIP

ADC positive analog input.

AIN

ADC negative analog input.

1.2.2.3 Pull devices

Some of the pins are connected internally to pull-up or pull-down devices. This is summarized in **Table 2**.

Table 2 Internal pull devices

Signal	Device
INP	Weak pull-down to V_{REF0}
INSTP	Weak pull-down to V_{REF0}
EN	Weak pull-down to V_{REF0}
SCLK	Weak pull-up to V_{CC1}
SDI	Weak pull-up to V_{CC1}

Table 2 Internal pull devices (cont'd)

Signal	Device
NCS	Weak pull-up to V_{CC1}
ADCT	Weak pull-down to V_{GND1}
DIO1	Weak pull-down to V_{GND1}
DESAT	Weak pull-up to V_{CC2}
DIO2	Weak pull-down to V_{GND2}
OCP	Weak pull-up to 5-V internal reference
DEBUG	Weak pull-down to V_{GND2}

1.3 Block diagram

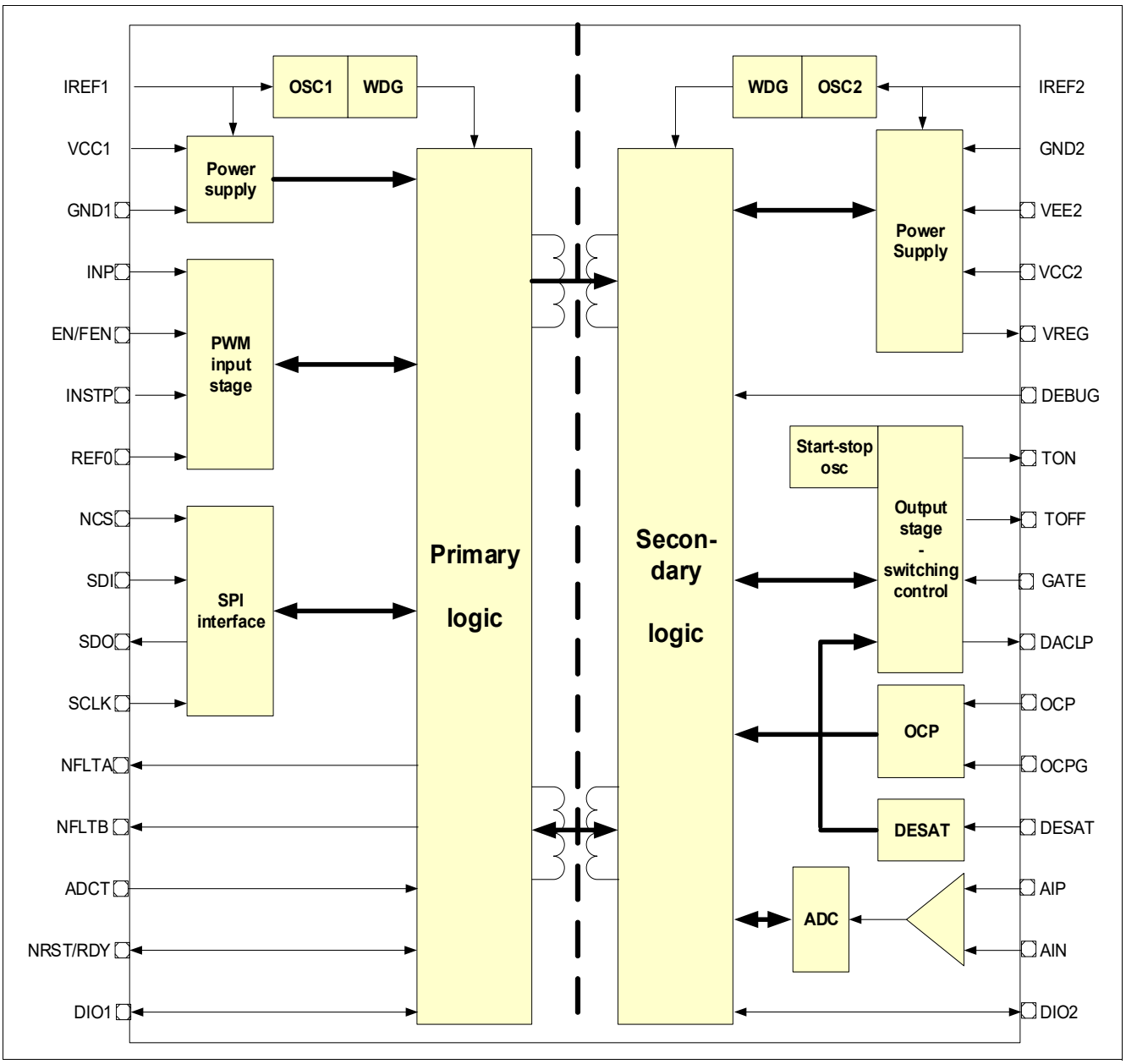


Figure 2 Block diagram

1.4 Functional block description

1.4.1 Power supplies

On the primary side, the 1EDI2010AS needs a single 5-V supply source V_{CC1} for proper operation. This makes the device compatible with most of the microcontrollers available for automotive applications.

On the secondary side, the 1EDI2010AS needs two power supplies for proper operation:

- The positive power supply V_{CC2} is typically set to 15 V (referring to V_{GND2}).
- Optionally, a negative supply V_{EE2} (typically set to -8 V referring to V_{GND2}) can be used. If no negative supply is needed, V_{EE2} must be connected to V_{GND2}.

Undervoltage monitoring on V_{CC1} and V_{CC2} is performed continuously during operation of the device (see **Chapter 2.3.1**).

A 5-V supply for the digital domain on the secondary side is generated internally (present at the **VREG** pin).

1.4.2 Clock domains

The clock system of the 1EDI2010AS is based on three oscillators defining each a clock domain:

- One RC oscillator (OSC1) for the primary chip.
- One RC oscillator (OSC2) for the secondary chip excepting the output stage.
- One start-stop oscillator (SSOSC2) for the output stage on the secondary side.

The two RC oscillators are running constantly. They are also monitored constantly, and large deviations from the nominal frequency are identified as a system failure (Class B event, see **Chapter 1.4.9.2**).

The start-stop oscillator is controlled by the PWM command.

1.4.3 PWM input stage

The PWM input stage generates the turn-on and turn-off commands for the secondary side from the external signals **INP**, **INSTP**, and **EN**. The general structure of the PWM input block is shown **Figure 3**.

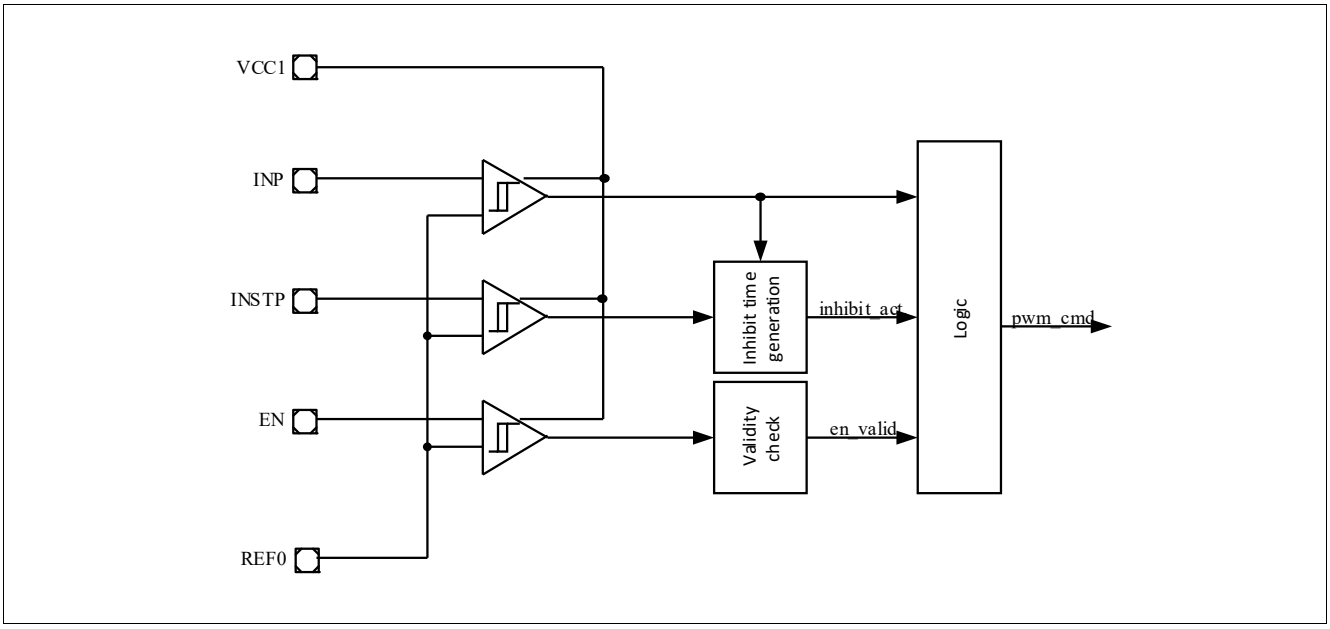


Figure 3 PWM input stage

The signals **INP**, **INSTP**, and **EN** are pseudo-differential, in the sense that they are not referenced to the common ground **GND1** but to the **REF0** signal. This is intended to make the device more robust against ground-bouncing effects.

*Note: Glitches shorter than t_{INPR1} occurring on signal **INP** are filtered internally.*

*Note: Pulses on **INP** shorter than t_{INPPD} might be distorted or suppressed.*

The 1EDI2010AS supports only non-inverted PWM signals. When a high level on the **INP** pin is detected while signals **INSTP** and **EN** are valid, a turn-on command is issued to the secondary chip. A low level on **INP** issues a turn-off command to the secondary chip.

The **EN** signal can inhibit turn-on commands received on **INP**. A valid **EN** signal is required in order to have turn-on commands issued to the secondary chip. If an invalid signal is provided, the PWM input stage constantly issues turn-off commands to the secondary chip. The functionality of the **EN** signal is detailed in **Chapter 1.4.8**.

*Note: After an invalid-to valid transition of the **EN** signal, a minimum delay of t_{INPEN} should be inserted before turning **INP** on.*

As shown in **Figure 4**, the **INSTP** signal provides shoot-through protection (STP) to the system. When the signal on the **INSTP** pin is at the high level, the internal signal `inhibit_act` is activated. The inhibition time is defined as the pulse duration of `inhibit_act`. It corresponds to the pulse duration of the **INSTP** signal to which a minimum dead time is added. During the inhibition time, rising edges of the **INP** signal are inhibited. The **PSTAT2**.**STP** bit is set for the duration of the inhibition time.

The deadtime is programmable through the **PCFG2**.**STPDEL** bit field.

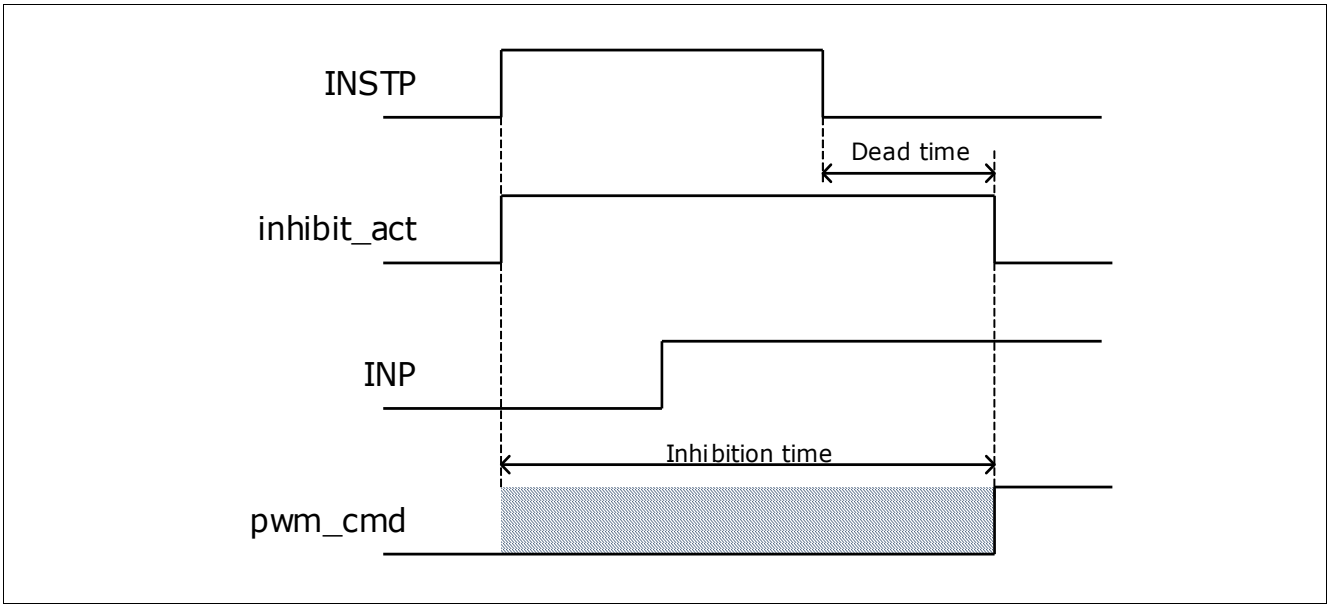


Figure 4 STP: Inhibition time definition

During the inhibition time, the pwm_cmd signal is not forced to low. It means that if the device is already turned on when **INSTP** is high, it stays on until the signal on the **INP** pin goes low. This is shown in **Figure 5**.

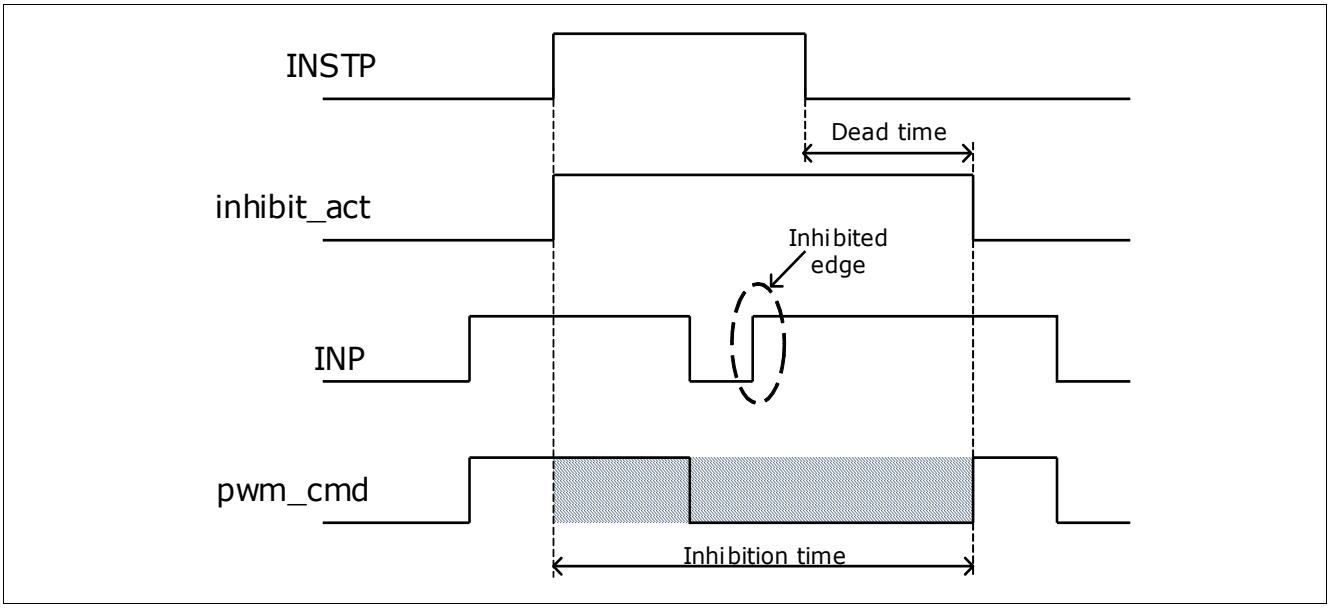


Figure 5 STP: Example of operation

When a condition occurs that inhibits a rising edge of the **INP** signal, an error notification is issued. See **Chapter 2.4.1** for details.

*Note: The failure notification via the **PER.STPER** bit is filtered internally for times shorter than one OSC1 clock cycle. No notification is raised but the INP signal may be delayed.*

1.4.4 SPI interface

This chapter describes the functionality of the SPI block.

1.4.4.1 Overview

The standard SPI interface implemented on the 1EDI2010AS is compatible with most of the microcontrollers available for automotive and industrial applications. The following features are supported by the SPI interface:

- Full-duplex bidirectional communication link
- SPI slave mode (only)
- 16-bit frame format
- Daisy-chain capability
- MSB first
- Parity check (optional) and parity-bit generation (LSB)

The SPI interface of the 1EDI2010AS provides a standardized bidirectional communication interface to the main microcontroller. From the architectural point of view, it fulfills the following functions:

- Initialization of the device
- Configuration of the device (static and runtime)
- Reading of the status of the device (static and runtime)
- Operation of the verification modes of the device

The purpose of the SPI interface is to exchange data which have relaxed timing constraints compared to the PWM signals (from the point of view of the motor-control algorithm). The IGBT switching behavior is, for example, controlled directly by the PWM input. Similarly, critical application failures requiring fast reaction are notified on the primary side via the feedback signals **NFLTA**, **NFLTB**, and **NRST/RDY**.

In order to minimize the complexity of the application and to optimize the microcontroller's resources, the implemented interface supports daisy-chaining. Several (typically six) 1EDI2010AS devices can be combined into a single SPI bus.

1.4.4.2 General operation

The SPI interface of the 1EDI2010AS supports full-duplex operation. The interface relies on four communication signals:

- **NCS**: (Not) chip select
- **SCLK**: Serial clock
- **SDI**: Serial data in
- **SDO**: Serial data out

The SPI interface of the 1EDI2010AS supports slave operation only. An SPI master (typically, the main microcontroller) is connected to one or several 1EDI2010AS devices, forming an SPI bus. Several bus topologies are supported.

A regular SPI bus topology can be used where each of the slaves is controlled by an individual chip-select signal (**Figure 6**). In this case, the number of slaves on the bus is limited only by the application's constraints.

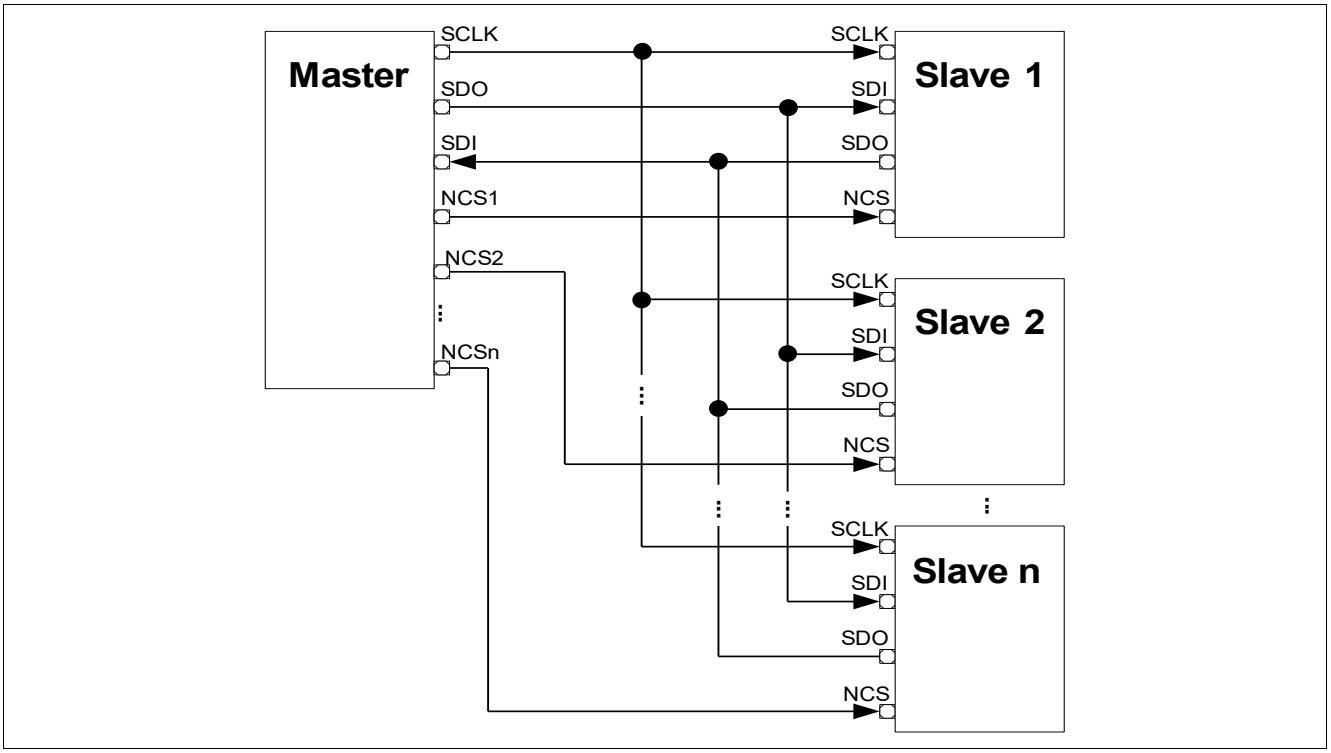


Figure 6 SPI regular bus topology

In order to simplify the layout of the PCB and to reduce the number of pins used on the microcontroller's side, a daisy-chain topology can also be used. The chain's length is not limited by the 1EDI2010AS itself. A possible topology is shown **Figure 7**.

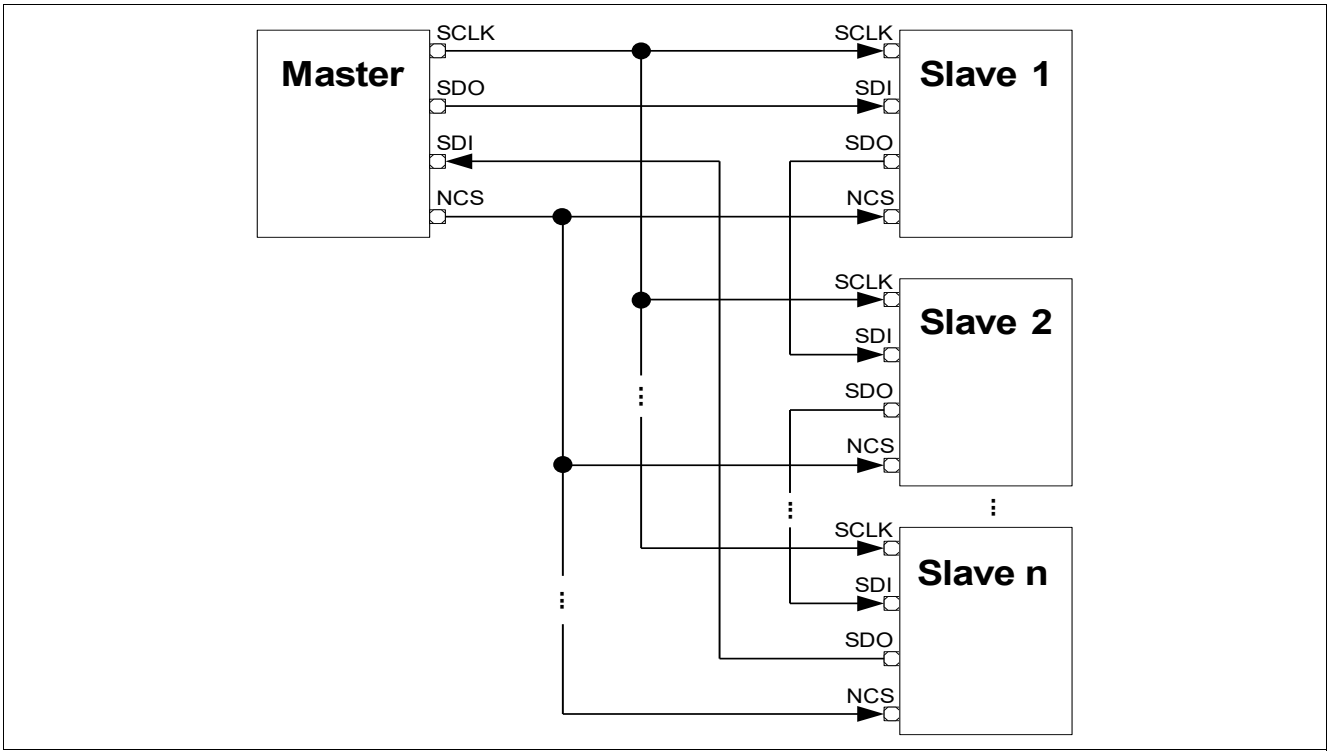


Figure 7 SPI daisy-chain bus topology

Physical layer

The SPI interface relies on two shift registers:

- An output shift register, reacting on the rising edges of **SCLK**.
- An input shift register, reacting on the falling edges of **SCLK**.

When the **NCS** is inactive, the signals on the **SCLK** and **SDI** pins are ignored. The **SDO** output is in tristate.

When **NCS** is activated, the output shift register is updated internally with the value requested by the previous SPI access.

On each rising edge of the **SCLK** signal (while **NCS** is active), one bit of the output shift register is serially shifted out on the **SDO** pin (MSB first). On each falling edge of the clock pulse, the data bit available at the **SDI** input is latched and serially shifted into the input shift register.

When **NCS** is deactivated, the SPI logic checks how many rising and falling edges of the **SCLK** signal have been received. In case both counts differ and / or are not a multiple of 16, an SPI error is generated. If no error was generated, the SPI block checks the validity of the received 16-bit word. In case of invalid data, an SPI error is generated. If no error is detected, the data is decoded by the internal logic.

The **NCS** signal is active low.

Input debouncing filters

The input stages of the **SDI**, **SCLK**, and **NCS** signals include each a debouncing filter which filters glitches and noise out of the input signals.

The **SDI** and **SCLK** input signals are analyzed at each edge of the internal clock derived from OSC1. If the same external signal value is sampled three times consecutively, the signal is considered valid and is processed by the SPI logic. Otherwise, the transition is considered as glitch and is discarded.

The **NCS** input signal is sampled at a rate corresponding to the period of the internal clock derived from OSC1. If the same external signal value is sampled two times consecutively, the signal is considered valid and is processed by the SPI logic. Otherwise, the transition is considered a glitch and is discarded.

1.4.4.3 Definitions

Command

A command is a high-level instruction issued by the SPI master which aims at generating a specific reaction in the addressed slave. The command is physically translated into a request message by the SPI master. The correct reception of the request message by the SPI slave leads to a specific action inside the slave and to the emission of an answer message by the slave.

Example: The READ command leads to the transfer of the value of the specified register from the device to the SPI master.

Word

A word is a 16-bit sequence of data bits.

Transfer

A transfer is defined as the SPI data transmissions (in both directions) occurring between a falling edge of **NCS** and the next consecutive rising edge of **NCS**.

Request message

A request message is a word issued by the SPI master that is addressing a single slave. A request message relates to a specific command.

Answer message

An answer message is a well-defined word issued by a single SPI slave as a response to a request message.

Transmit frame

A transmit frame is a sequence of one or several words sent by the SPI master within one SPI transfer. In regular SPI topologies, a transmit frame is in practice identical to a data word. In daisy-chain topologies, a transmit frame is a sequence of data words belonging to different request messages.

Receive frame

A receive frame is a sequence of one or several words received by the SPI master within one SPI transfer. In regular SPI topologies, a receive frame is in practice identical to a data word. In daisy-chain topologies, a receive frame is a sequence of data words belonging to different answer messages.

The SPI protocol supported by the 1EDI2010AS is based on the request-answer principle. The master sends a defined request message to which the slave replies with the corresponding answer message (**Figure 8**, **Figure 9**). Due to the nature of the SPI interface, the answer message is shifted, compared to the request message, by one SPI transfer. It means, for example, that the last word of the answer message n is being transmitted by the slave while the master is sending the first word of request message n+1.

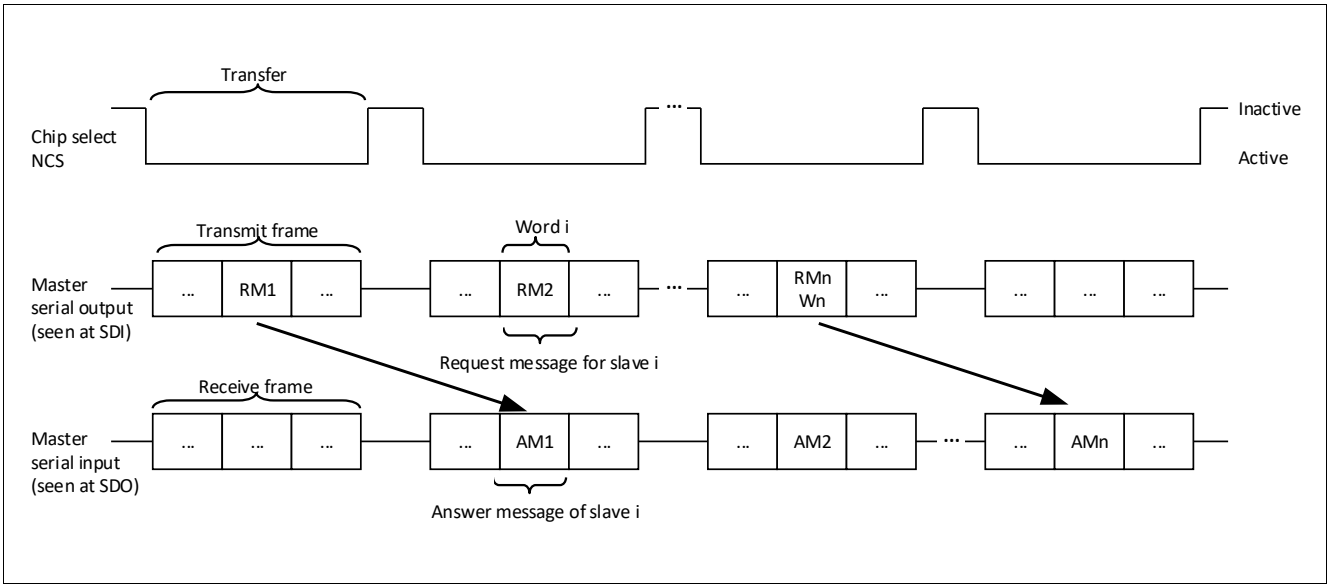


Figure 8 Request-answer principle – daisy-chain topology

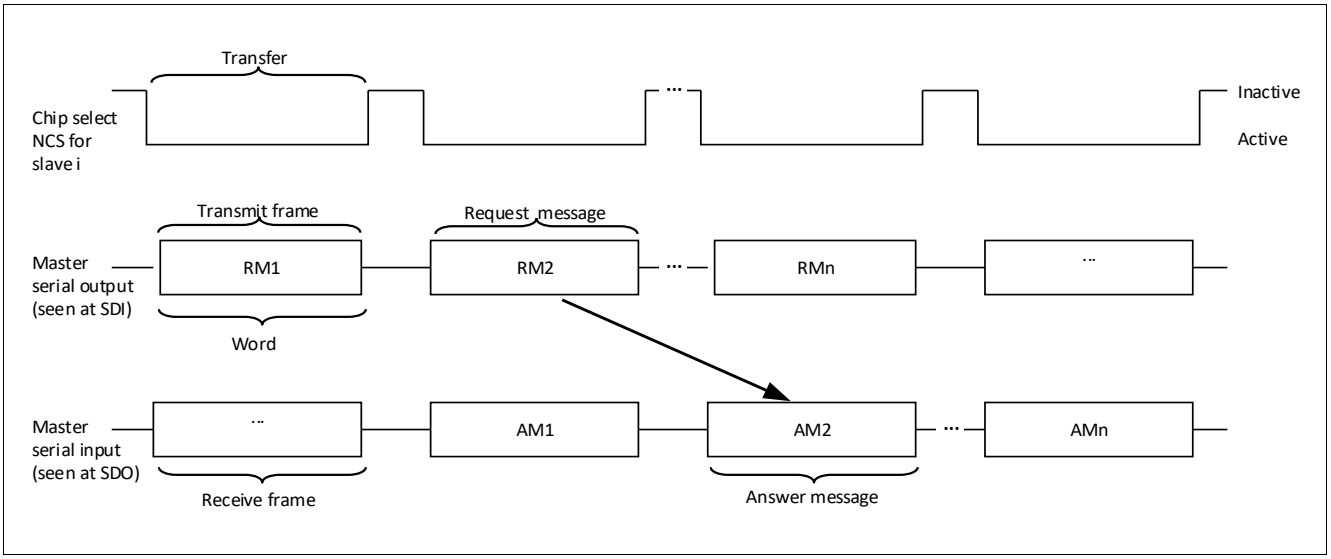


Figure 9 Request-answer principle – regular topology

The first word transmitted by the device after power-up is the content of the **PSTAT** register.

1.4.4.4 SPI data integrity support

1.4.4.4.1 Parity bit

By default, the SPI link relies on an odd-parity protection scheme for each transmitted or received 16-bit word in SPI messages. The parity bit corresponds to the LSB of the 16-bit word. Therefore, the effective payload of a 16-bit word is 15 data bits (plus one parity bit). The parity-bit check (on the received data) can be disabled by clearing the **PCFG.PAREN** bit. In that case, the parity bit is considered as “don’t care”. The generation of the parity bit by the driver for transmitted words cannot be disabled (but can be considered as “don’t care” by the SPI master).

Note: For fixed-value commands (ENTER_CMODE, ENTER_VMODE, EXIT_CMODE, NOP), the value of the parity bit must be correct even if parity checking is disabled. Otherwise, an SPI error is generated.

1.4.4.4.2 SPI error

When the device is unable to process an incoming request message, an SPI error is generated: The received message is discarded by the driver, the **PER.SPIER** bit is set, and the erroneous message is answered with an error notification (**LMI** bit set).

Several failures generate an SPI error:

- A parity error is detected on the received word.
- An invalid data word format is received (for example, not a 16-bit word).
- A word is received which does not corresponding to a valid request message.
- A command is received which cannot be processed. For example, the driver receives in Active mode a command which is only valid in other operating modes. Another typical example is a read access to the secondary side while the previous read access is not yet completed (device “busy”).
- An SPI access to an invalid address.

1.4.4.5 Protocol description

1.4.4.5.1 Command catalog

Table 3 gives an overview of the command catalog supported by the device. The full description of the commands and of the corresponding request and answer messages is provided in the following sections.

Table 3 SPI command catalog

Acronym	Short description	Valid in mode
ENTER_CMODE	Enters Configuration mode.	OPM0, OPM1
ENTER_VMODE	Enters Verification mode.	OPM2
EXIT_CMODE	Leaves Configuration mode to enter Configured mode.	OPM2
READ	Reads the register value at the specified address.	All
NOP	Triggers no action in the device (equivalent to a “nop”).	All
WRITEH	Updates the most significant byte of the internal write buffer.	All
WRITEL	Updates the least significant byte of the internal write buffer and copies the complete contents of the buffer into the addressed register. The write buffer is cleared afterwards.	All (with restrictions)

An overview of the commands is given **Figure 10**.

Message	Command				Data											P
ENTER_CMODE	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0
ENTER_VMODE	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
EXIT_CMODE	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0
NOP	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0
READ	0	0	0	0	A4	A3	A2	A1	A0	0	1	0	1	0	1	X
WRITEH	0	1	0	0	0	1	0	D15	D14	D13	D12	D11	D10	D9	D8	X
WRITEL	1	0	1	0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	X

Figure 10 SPI commands overview

1.4.4.5.2 Word convention

In order to simplify the description of the SPI commands, the following conventions are used (**Table 4**).

Table 4 Word convention

Symbol	Value
Va(REGISTER)	Value of register REGISTER
P_B	Parity bit
<<n	Left-shift operation of n bits.
$x_H \mid y_H$	Result of the operation: x_H OR y_H

1.4.4.5.3 ENTER_CMODE command

This command puts the device into Configuration mode (OPM2). It is only valid in Default mode (OPM0 and OPM1). If the request message is received while neither OPM0 nor OPM1 is active, the command is discarded and an SPI error occurs.

Table 5 describes the request message and the corresponding answer message.

Table 5 ENTER_CMODE request and answer messages

	Transfer 1	Transfer 2
Request message	1880_H	n/a
Answer message	n/a	Va(**PSTAT**)

1.4.4.5.4 ENTER_VMODE command

This command puts the device into Verification mode (OPM5). It is only valid in Configuration mode (OPM2). If the request message is received while OPM2 is not active, the command is discarded and an SPI error occurs.

Table 6 describes the request message and the corresponding answer message.

Table 6 ENTER_VMODE request and answer messages

	Transfer 1	Transfer 2
Request message	1140_H	n/a
Answer message	n/a	Va(**PSTAT**)

1.4.4.5.5 EXIT_CMODE command

When a valid EXIT_CMODE command is received by the device, it transitions from Configuration mode to Configured mode (OPM3). This command is only valid in Configuration mode (OPM2). If the request message is received while OPM2 is not active, the command is discardedand an SPI error occurs.

Table 7 describes the request message and the corresponding answer message.

Table 7 EXIT_CMODE request and answer messages

	Transfer 1	Transfer 2
Request message	1220_H	n/a
Answer message	n/a	Va(**PSTAT**)

1.4.4.5.6 NOP command

This command triggers no specific action in the driver (equivalent to a “nop”). However, the mechanisms verifying the validity of the word are active. This command is valid in all operating modes.

Table 8 describes the request message and the corresponding answer message.

Table 8 NOP request and answer messages

	Transfer 1	Transfer 2
Request message	1410_H	n/a
Answer message	n/a	Va(**PSTAT**)

1.4.4.5.7 READ command

This command reads the value of the register whose address is specified in the request message. This command is valid in all operating modes. However, in OPM4 and OPM6, the use of the READ command is restricted (see **Table 29**). If an access outside the allowed address range is performed, the access is discarded as invalid and an SPI error occurs.

Table 9 describes the request message and the corresponding answer message.

Table 9 READ request and answer messages

	Transfer 1	Transfer 2
Request message	See below	n/a
Answer message	n/a	Va(Register)

Request message words

Word 1: (ADDRESS_5BIT << 7)] | $002A_H$ | P_B.

Answer message words

Word 1: Value of REGISTER.

1.4.4.5.8 WRITEH

This command writes the specified value into the upper byte of the internal write buffer. It has no other effect on the functionality of the device. This command is valid in all operating modes.

Table 10 describes the request message and the corresponding answer message.

Table 10 WRITEH request and answer messages

	Transfer 1	Transfer 2
Request message	See below	n/a
Answer message	n/a	Va(**PSTAT**)

Request message words

Word 1: 4400_H | (DATA_8BIT << 1) | P_B

1.4.4.5.9 WRITEL

This command updates the value of the register whose address is specified in the request message. It is valid in all operating modes. However, depending on the active Operating mode, this command is restricted to a specific address range or specific registers (see **Table 30**). If an access outside the permitted address range is performed, the access is discarded as invalid and an SPI error occurs.

At the reception of this command, the specified value is written into the least significant byte of the internal buffer, the contents of the buffer are copied to the register at the specified address, and the entire write buffer is cleared.

Table 11 describes the request message and the corresponding answer message.

Table 11 WRITEL request and answer messages

	Transfer 1	**Transfer 2**
Request message	See below	n/a
Answer message	n/a	Va(**PSTAT**)

Request message words

Word 1: $A000_H$ | (ADDRESS_5BIT << 7) | (DATA_6BIT << 1) | P_B.

1.4.5 Operating modes

1.4.5.1 General operation

At any time, the driver can be in one of seven possible operating modes:

- OPM0: Default mode (default after reset, device is disabled).
- OPM1: Error mode (reached after a Class B event, device is disabled).
- OPM2: Configuration mode (device is disabled, configuration of the device can be modified).
- OPM3: Configured mode (device is configured and disabled).
- OPM4: Active mode (normal operation).
- OPM5: Verification mode (intrusive diagnostic functions can be triggered).
- OPM6: Weak Active mode (the device can be turned on but with restrictions)

The current Active mode of the device is stored in the bit field **PSTAT2.OPMP**.

The concept of the device is based on the following general ideas:

- The driver can only switch the IGBT on when OPM4 mode is active (exception: weak-turn on in OPM6).
- Starting from the OPM0 or OPM1 modes, the Active mode (OPM4) can only be activated through a dedicated SPI command sequence and the activation of the hardware signal **EN**. As a result, the probability that the device goes to OPM4 mode due to random signals is negligible.
- Differentiations of errors: Different classes of errors are defined, leading to different behavior of the device.

The state diagram for the operating modes is given in **Figure 11**:

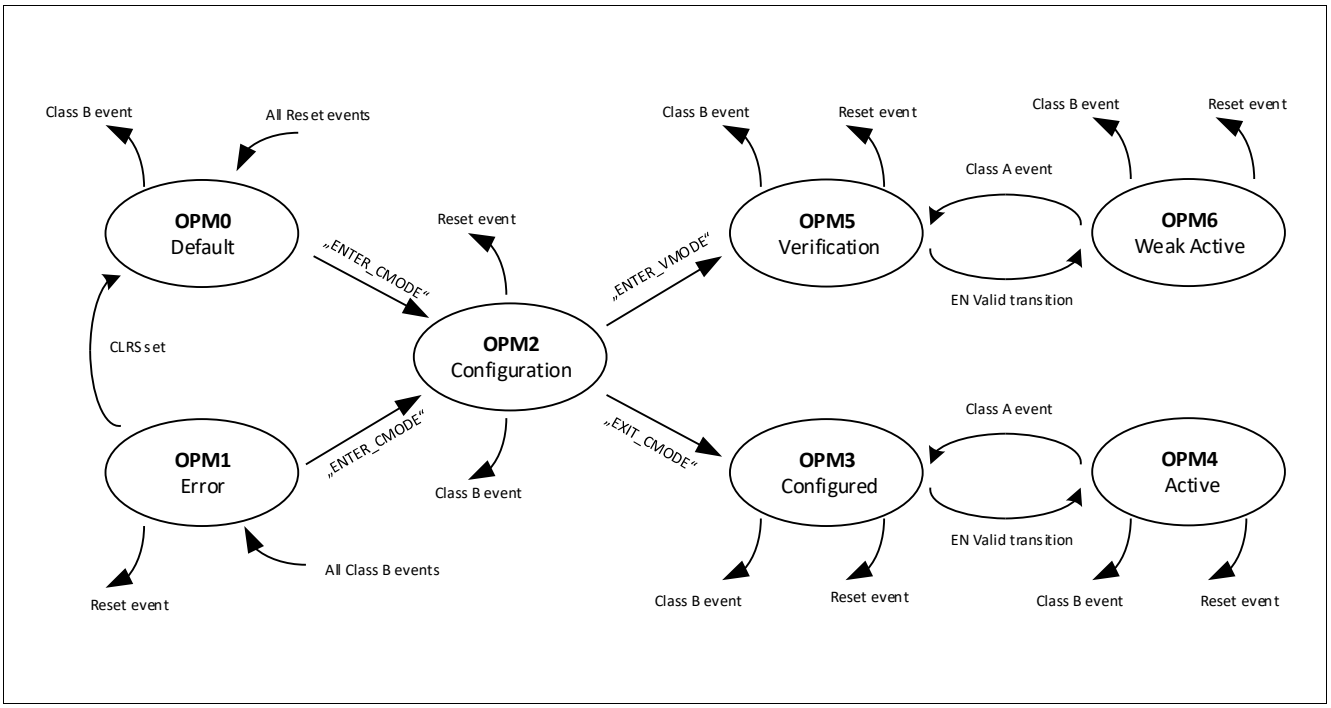


Figure 11 Operating modes state diagram

1.4.5.2 Definitions

1.4.5.2.1 Events and state transitions

The transitions from one state to another are based on events, SPI commands, or both. Events are grouped into several classes, as described below.

Class A events

The following is an (exhaustive) list of events that are defined as Class A events:

- DESAT event (leads to a safe turn-off sequence).
- OCP event (leads to a safe turn-off sequence).
- Valid-to-invalid transition of the **EN** signal (leads to a regular turn-off sequence).
- ADC Boundary Check Violation event (optional, can be disabled).

When a Class A event occurs, the output stage initiates either a safe turn-off sequence (DESAT, OCP) or a regular turn-off sequence (all other events). The event is notified via an error bit in the corresponding register.

Note: In contrast to a Reset event, a Class A event does not affect the contents of the configuration registers.

When a Class A event occurs, the device may change its operating mode, depending on which mode is active when the event occurs:

- If it was in OPM4, it goes in OPM3.
- If it was in OPM6, it goes in OPM5.

In all other cases, the mode is unaffected. A state transition due to a Class A event activates the **NFLTA** signal. If no state transition occurs (for example, if the device was not in OPM4 or OPM6), **NFLTA** is not activated (exception: ADC boundary check event - see **Chapter 1.4.7** for more details on failure notifications).

Class B events

The following is an (exhaustive) list of events that are defined as Class B events:

- UVLO2 event.
- Verification mode Time-Out error.

When a Class B event occurs, the output stage initiates a regular turn-off sequence. The event is notified via an error bit in the corresponding register and (possibly) via the **NFLTB** signal.

Note: Class B events may affect the contents of the configuration registers.

When a Class B event occurs, the device may change its operating mode, depending on which mode is active when the event occurs: If it was not in OPM1, it goes to OPM1. It is otherwise unaffected.

A state transition due to a Class B event activates the **NFLTB** signal. If no state transition occurs (for example, if the device was already in OPM1), **NFLTB** is not activated. See **Chapter 1.4.7** for more details on failure notifications.

Class C events

Generally speaking, Class C events are error events that do not lead to a change of the operating mode of the device. The following is a (non-exhaustive) list of Class C events:

- SPI error
- Shoot-Through Protection error

SPI commands

The following SPI commands have an impact on the device's operating mode. The SPI commands are described in **Chapter 1.4.4.5**.

- ENTER_CMODE
- ENTER_VMODE
- EXIT_CMODE
- Setting the **PCTRL.CLRS** bit (by writing to the **PCTRL** register).

Reset events

A reset puts the device (or part of the device) into its default state. Reset events are described in **Chapter 1.4.10**.

Internal supervision errors cause a Reset event, for example.

1.4.5.2.2 Emergency turn-off sequence

The emergency turn-off sequence (ETO) is the sequence of actions executed by the output stage of the device when Class A, Class B, or Reset event is detected.

An ETO includes these actions:

- A turn-off sequence is initiated. In case of a DESAT or OCP event, a safe turn-off sequence is initiated. For the other events, a regular turn-off sequence is initiated.
- The device enters the corresponding operating mode. As a consequence, the device is disabled.

Once an ETO has been initiated, the device cannot be reenabled for a maximum duration consisting of 256 OSC2 clock cycles. Consequently, you must wait for this duration before reenabling the device and sending a PWM turn-on command.

1.4.5.2.3 Ready, Disabled, Enabled, and Active states

The device is in the Ready state when no Reset event is active on the primary chip. When the device is ready, the **NRST/RDY** signal is at the high level.

When the device is in the Disabled state, PWM turn-on commands are ignored. This means that whatever the input signal **INP** is, the output stage (if not tristated) delivers a constant turn-off signal to the IGBT. Unless otherwise stated, all other functions of the device work normally.

When the device is not in the Disabled state, it is said to be in the Enabled state. In this case, PWM signal commands are processed normally (if the output stage is not tristated). In practice, the device is in the Enabled state when either OPM4 or OPM6 is active.

The Active state is the normal operating state of the device. The device is in the Active state when OPM4 is active.

Note: When the device is in the Active state, it also is in the Enabled state.

1.4.5.3 Operation modes description

Default mode (OPM0)

OPM0 is the default operating mode of the device after power-up or after a Reset event. In OPM0, the device is in the Disabled state.

The following exhaustive list of events brings the device into the OPM0 mode:

- Reset event.
- Bit **PCTRL.CLRS** set while the device is in OPM1.

Error mode (OPM1)

OPM1 is the operating mode of the device after a Class B event.

The following exhaustive list of events brings the device into the OPM1 mode:

- Any Class B event.

In OPM1, when the **PCTRL.CLRS** bit is set via the corresponding SPI command, the device normally goes to OPM0. However, if the conditions for a Class B event are met at that moment, no state transition occurs and the device stays in OPM1. **PCTRL.CLRS** operates normally on the secondary sticky bits.

In OPM1, when a valid ENTER_CMODE command is received, the device normally goes to OPM2. However, if the conditions for a Class B event are met at that moment, no state transition occurs and the device stays in OPM1 for the duration of the event. The state transition to OPM2 is executed as soon as the conditions resulting in a Class B event disappear. No LMI error notification is issued.

Configuration mode (OPM2)

OPM2 is the mode in which the configuration of the device can be modified. When OPM2 is active, the device is in the Disabled state.

The following exhaustive list of events brings the device into Configuration mode:

- Reception of a valid ENTER_CMODE command while OPM0 or OPM1 is active.

Configured mode (OPM3)

OPM3 is the mode in which the device is ready to be enabled. When OPM3 is active, the device is in the Disabled state.

The following exhaustive list of events brings the device into Configured mode:

- Reception of a valid EXIT_CMODE command while OPM2 is active.
- Class A event while OPM4 is active.

Active mode (OPM4)

OPM4 is the normal operating mode of the device. When OPM4 is active, the device is in the Active state. The following exhaustive list of event brings the device into Active mode:

- Invalid-to-valid transition on the **EN** signal while OPM3 is active.

Verification mode (OPM5)

OPM5 is the mode in which intrusive verification functions can be started. When OPM5 is active, the device is in the Disabled state.

The following exhaustive list of event brings the device into Verification mode:

- Reception of a valid ENTER_VMODE command while OPM2 is active.
- Any Class A event while mode OPM6 is active.

After a transition from OPM2 to OPM5, an internal watchdog timer is started. If, after time t_{VMTO}, the device is still in either OPM5 or OPM6, a time-out event occurs and a Class B event is generated.

Weak Active mode (OPM6)

OPM6 is the mode in which the device can be activated to run diagnostic tests at the system level. When OPM6 is active, the device is in the Enabled state. In this state a PWM turn-on command issues a weak turn-on on the secondary side.

The following exhaustive list of event brings the device into Weak Active mode:

- Invalid-to-valid transition on the **EN** signal while OPM5 is active.

The watchdog timer started when OPM5 is entered is not reset by entering OPM6.

Implementation notes related to state transitions

- A Class A or Class B event detected on the secondary side leads to an immediate reaction of the device's output stage. Due to the latency of the inter-chip communication, the notification on the primary side is slightly delayed.
- The **NFLTA** or **NFLTB** signal is activated simultaneously with the corresponding state transition on the primary side.
- The operating mode can be changed while a failure condition is present. This may, however, immediately lead to a new error notification and state transition.

1.4.5.4 Activating the device after a reset

After a Reset event, the device is in the OPM0 mode and disabled. In order to become active, the device needs to enter the Configuration mode with the ENTER_CMODE command. Once the device has been configured, the Configuration mode has to be exited with an EXIT_CMODE command. Once this is done, the device enters the Active mode when an invalid-to-valid transition on the **EN** pin is detected.

1.4.5.5 Activating the device after a Class A or Class B event

If during operation, a Class A event occurs, the device enters OPM3 (or OPM5). The **PSTAT2.OPMP** bit field is updated accordingly. In order to reactivate the device, an invalid-to-valid transition has to be applied to the **EN** signal. It means, for example, in EN mode that a low level and then a high level is applied to **EN**. If no Class A event is active, the device enters OPM4 (or, respectively, OPM6).

If a Class B event occurs during the device operation, the device enters the Default mode (OPM1). The **PSTAT2.OPMP** bit field is updated accordingly. In order to reactivate the device, the steps defined in **Chapter 1.4.5.4** need to be performed.

1.4.5.6 Debug mode

The **DEBUG** pin makes is possible to operate the device in the Debug mode, in which the device can be operated without an SPI interface. This mode should be used for development purposes only and is not intended to be used in final applications.

At V_{CC2} power-on, the level on the **DEBUG** pin is latched. In case a high level is detected, the device enters the Debug mode and the **SSTAT**.**DBG** bit is set.

In Debug mode, the regular operation of the internal state machine is modified, so that the device can only enter OPM3 or OPM4. As a result, the OPM0, OPM1, OPM2, OPM5, and OPM6 modes are completely bypassed. In case of a Reset event, the device goes to OPM3 (instead of OPM0). In addition, in Debug mode events leading normally to a Class B event instead result in a Class A event and the activation of the **NFLTA** signal. Class B events are therefore not generated by the device in Debug mode (and the **NFLTB** signal is not used).

The configuration of the device in Debug mode corresponds to the default settings and cannot be changed.

In Debug mode, the operation of the device is otherwise similar to the regular operation. In particular, the **EN** signal has to be managed properly: When the device is in OPM3, a transition from a low to a high level has to be applied to the device in order to enter OPM4 (Active mode).

*Note: Once it has been latched at power-on, the level on the **DEBUG** pin has no impact on the device until the next power-on event on the secondary side.*

1.4.6 Driver functionality

The structure of the output stage and the associated external booster of the device is shown in **Figure 12**:

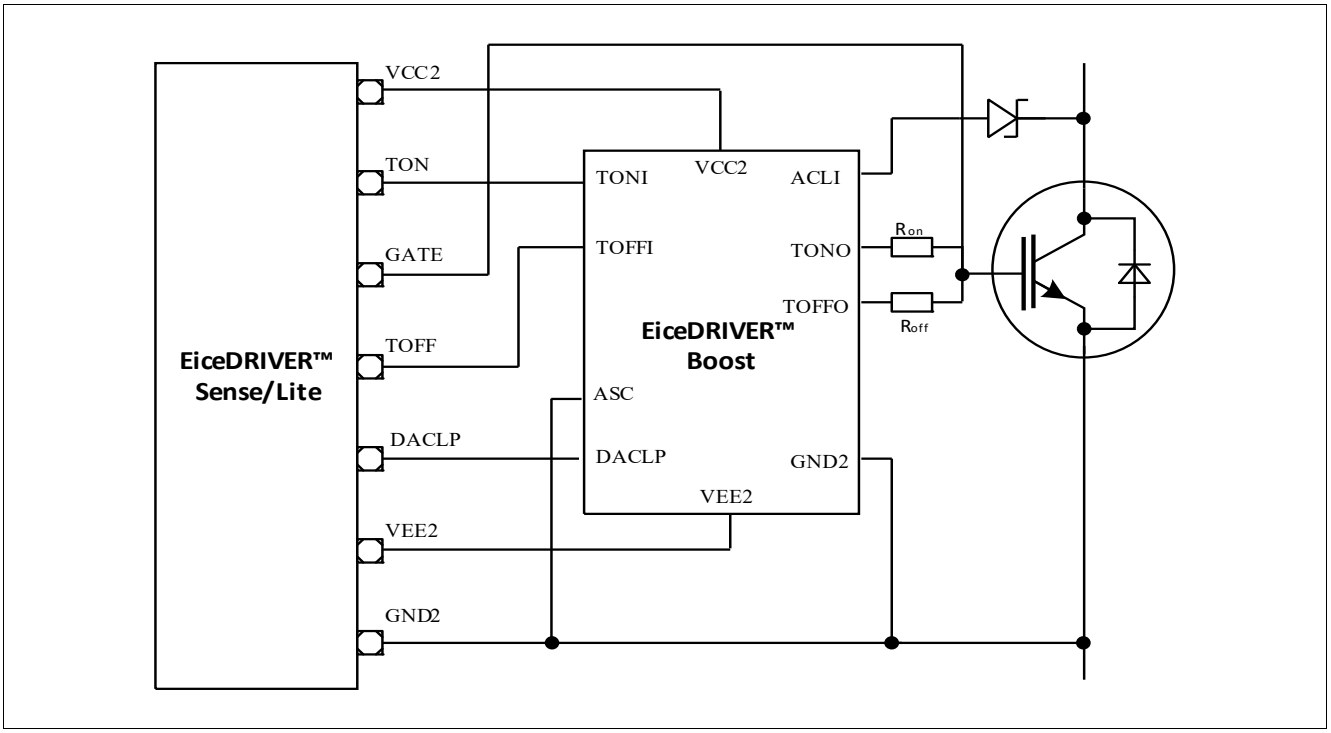


Figure 12 Output stage diagram of principle

1.4.6.1 Overview

Two turn-off behaviors are supported by the device, depending on the event causing the turn-off action.

- Regular turn-off
- Safe turn-off

A safe turn-off sequence uses the timing and plateau-level parameters defined in the **SSTTOF** register. It is triggered only by a DESAT or OCP event. A turn-off sequence which is not “safe” is “regular”. A regular turn-off sequence uses the timing parameters defined in the **SRTTOF** register and the plateau level defined by **PCTRL2**.**GPOF**.

Two-level turn-off (TTOFF)

Because a hard turn-off may generate a critical overvoltage on the IGBT, possibly causing its destruction, the 1EDI2010AS supports two-level turn-off functionality (TTOFF). The TTOFF function consists in switching the IGBT off in three steps in such a way that:

1. The IGBT gate voltage is first decreased with a reduced slew rate until a specific (and programmable) voltage is reached by the **TOFF** signal.
2. The **TOFF** (and **TON**) voltage is stabilized at this level. The IGBT gate voltage thus forms a plateau.
3. Finally, the switch-off sequence is resumed using hard commutation.

The TTOFF delays and plateau voltage are fully programmable using the corresponding SPI commands. For a regular turn-off sequence, the TTOFF delay is defined by the **SRTTOF**.**RTVAL** bit field. Setting this field to 00_H completely disables the TTOFF function for all regular turn-off sequences (but has no effect on safe turn-off sequences). The plateau level is defined by **PCTRL2**.**GPOF**. If this function is to be activated, a minimum value

for the delay time has to be programmed. Too-small delays are not visible as plateaus on the output signal, but they still affect the slew rate away from V_{CC2}.

For a safe turn-off sequence, the TTOFF delay is defined by the **SSTTOF**.**STVAL** bit field. Setting this field to 00_H completely disables the TTOFF function for all safe turn-off sequences (but has no effect on regular turn-off sequences). If this function is to be activated, a minimum value for the delay time has to be programmed. The plateau level is defined by **SSTTOF**.**GPS**.

The timing of a safe turn-off event is in the clock domain of the main secondary oscillator (OSC2). The timing of a regular turn-off event is in the clock domain of the start-stop oscillator (SSOSC2), leading to high accuracy and low PWM distortion.

When using the TTOFF function (with a non-zero delay), the PWM command that is received on the **INP** pin is delayed by the programmed delay time (**Figure 13**). For pulses larger than the TTOFF delay ($t_{PULSE} > t_{TTOFF}$ + two SSOSC cycles), the output pulse width is kept identical to the input pulse width. For smaller pulses ($t_{PULSE} < t_{TTOFF}$ + 2 two SSOSC cycles), the output pulse is identical to the programmed delay. The minimum pulse width delivered by the device to the IGBT is therefore the programmed delay time extended by two SSOSC cycles.

The device allows for external booster voltage compensation at the IGBT gate. When the **SCFG**.**VBEC** bit is cleared, the plateau voltage at **TOFF** corresponds to the programmed value. When the **SCFG**.**VBEC** bit is set, an additional V_{BE} (base emitter junction voltage of an internal p-n diode) is substracted from the programmed voltage at **TOFF** in order to compensate for the V_{BE} of an external booster.

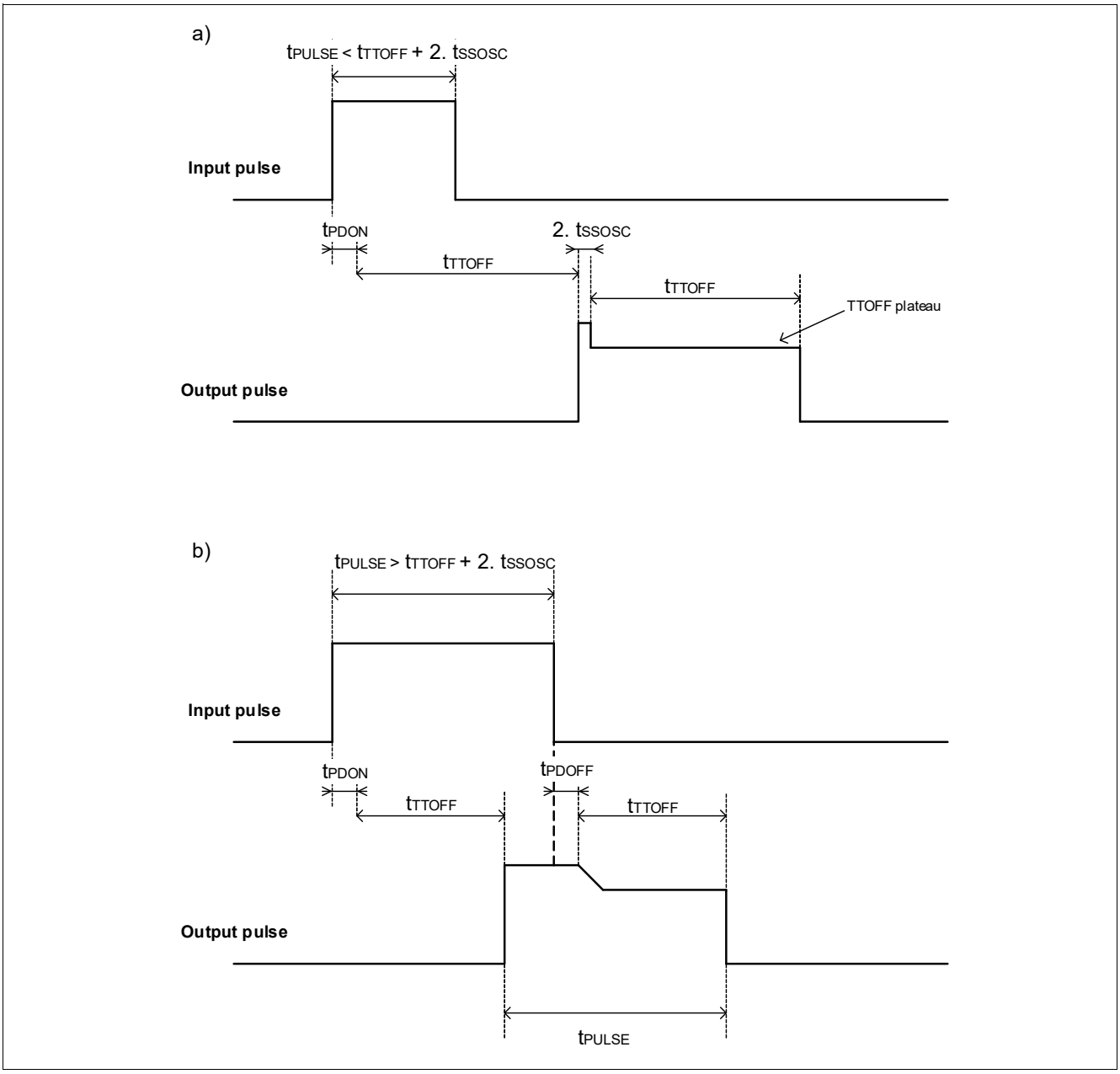


Figure 13 TTOFF: Principle of operation

Two-level turn-on (TTON)

In order to increase EM compatibility and the efficiency of the whole system, the 1EDI2010AS supports two-level turn-on functionality (TTON). The TTON function consists of switching the IGBT on in three steps in such a way that:

1. The IGBT gate voltage is first increased until a specific (and programmable) voltage is reached by the **TON** signal.
2. The **TON** (and **TOFF**) voltage is stabilized at this level. The IGBT gate voltage thus forms a plateau.
3. Finally, the switch-on sequence is resumed up to the maximum output voltage.

The TTON feature needs to be activated by configuring the delay in the **STTON.TTONVAL** bit field.

The plateau voltage level can be configured at runtime by updating the **PCTRL.GPON** bit field. This bit field can also be programmed to a value generating a hard turn-on.

When using the TTON function (with a non-zero delay), the PWM command that is received on the **INP** pin is **not** delayed by the programmed TTON delay time (**Figure 14**). However, the minimum pulse width that can be generated corresponds to the programmed TTON delay. Thus, for input pulses smaller than the TTON delay ($t_{PULSE} < t_{TTON}$), the output pulse width is extended.

The device allows for external booster voltage compensation at the IGBT gate. When the **SCFG.VBEC** bit is cleared, the plateau voltage at **TON** corresponds to the programmed value. When the **SCFG.VBEC** bit is set, an additional V_{BE} (base emitter junction voltage of an internal p-n diode) is added to the programmed voltage at **TON** in order to compensate for the V_{BE} of an external booster.

The TON and TTOFF functions can be used simultaneously.

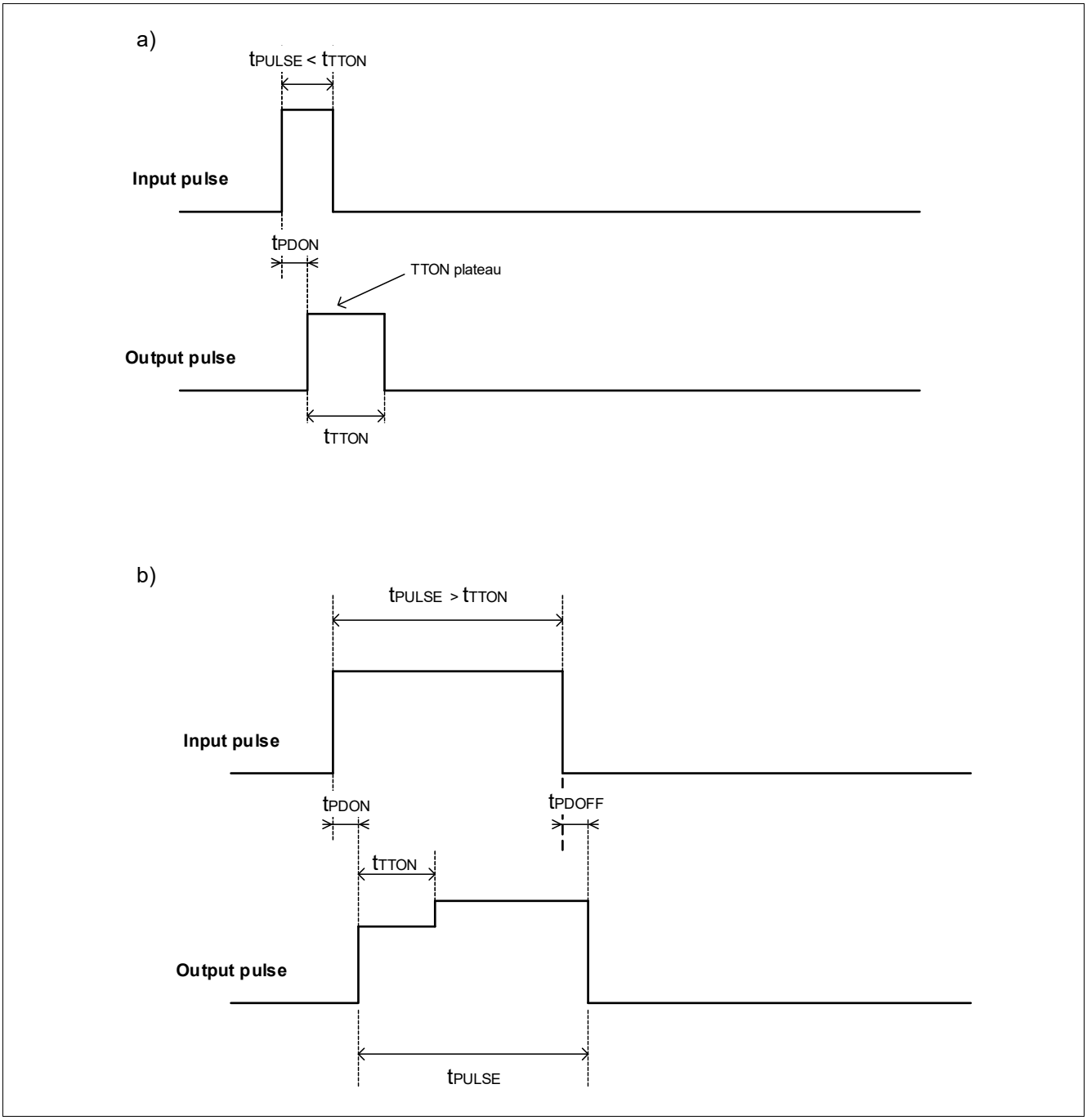


Figure 14 TTON: Principle of operation

Pulse suppressor

In order to increase the device's robustness against external disturbances, a pulse suppressor can be enabled by setting the **SCFG.PSEN** bit. The **SRTTOF** register should also programmed with a value higher than 2_H. When a PWM turn-on sequence occurs, the activation of the output stage is delayed by the programmed TTOFF number of cycles, as for a normal TTOFF sequence. However, the PWM command received by the secondary chip signal is internally sampled at every SSOSC cycle before the actual turn-on command is executed by the output stage. If at least one of the sampling points does not detect a High level, the turn-on sequence is aborted and the device is not switched on.

If a valid PWM ON command is detected by the secondary side after the decision point at which the previous sequence has been aborted, a new turn-on sequence is initiated.

One of the consequence of activating the pulse suppressor is that all PWM pulses shorter than the programmed TTOFF plateau time are filtered out (**Figure 15**).

Note: The pulse suppressor only acts on turn-on pulses, not on turn-off pulses.

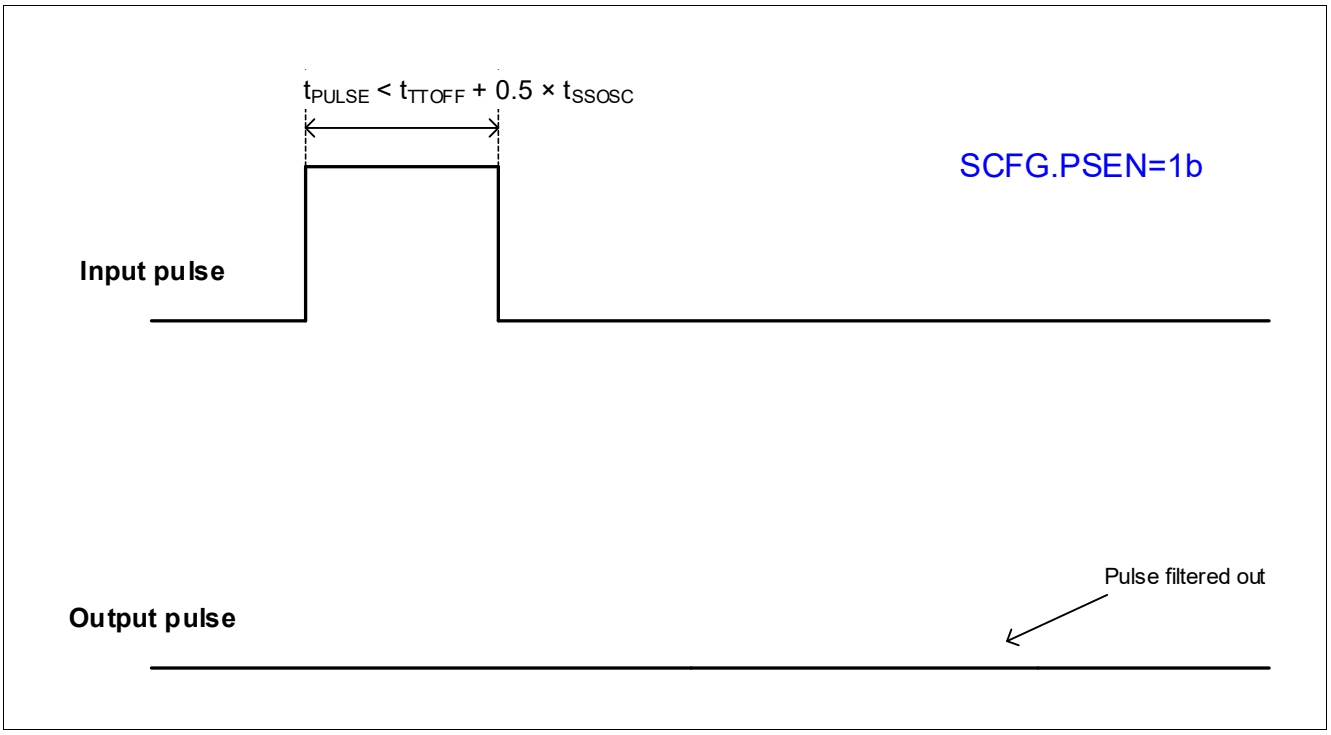


Figure 15 TTOFF: Pulse suppressor aborting a turn-on sequence

1.4.6.2 Switching sequence description

Figure 16 shows a schematic switching sequence. When a valid turn-on command is detected, a certain propagation time t_{PDON} is needed by the logic to transfer the PWM command to the secondary side. At this point, the TTOFF delay time t_{TTOFF} defined by the **SRTTOF**.**RTVAL** bit field is added before the turn-on command is executed. The **TON** signal is then activated, while the **TOFF** signal is deactivated.

If the two-level turn-on function is active, TON is increased up to the plateau voltage defined by the **PCTRL**.**GPON** bit field. The duration t_{TTON} between the beginning of the turn-on sequence and the moment where the switching sequence is resumed is defined by the **STTON**.**TTONVAL** bit field.

When a valid turn-off command is detected, a certain propagation time t_{DOFF} is needed by the command to be processed by the logic on the secondary side. This propagation time depends on the event having generated the turn-off action (non-exhaustive list):

- PWM turn-off command at pin **INP**: $t_{DOFF} = t_{PDOFF}$
- DESAT event: $t_{DOFF} = t_{OFFDESAT2}$
- OCP event: $t_{DOFF} = t_{OFFOCP2}$
- Class A event on the primary side: $t_{DOFF} = t_{OFFCLA}$
- Class B event on the secondary side: $t_{DOFF} = t_{OFFCLB2}$

When the turn-off command is processed by the logic, the **TON** and **TOFF** signals are decreased with the slew rate t_{SLEW} fixed by hardware. Once the voltage at the **TOFF** pin has reached the value defined by the **PCTRL2**.**GPOF** bit field (or **SSTTOF**.**GPS**, in case of a safe turn-off), the turn-off sequence is interrupted. Time t_{TTOFF} is defined as the moment when the device starts turning off the **TOFF** signal, and the moment in which the turn-off sequence is resumed. Depending on the event that triggered the turn-off sequence, t_{TTOFF} is taken from either the **SRTTOF**.**RTVAL** or the **SSTTOF**.**STVAL** bit field. Once the TTOFF time has elapsed, a hard commutation takes place, and the **TON** and **TOFF** signals are driven to V_{EE2}.

Note: Once a turn-off sequence has been started, it is completed with the same delay parameters.

The **DACLP** signal can be activated by configuring the **SCFG**.**DACLC** bit field. From the moment when the hard commutation takes place, the **DACLP** signal remains deactivated for a time t_{ACL} fixed by hardware. When this time has elapsed, the **DACLP** signal is reactivated (that is, active clamping is disabled). The voltage level at the **DACLP** pin can be read at the **SSTAT2**.**DACL** bit.

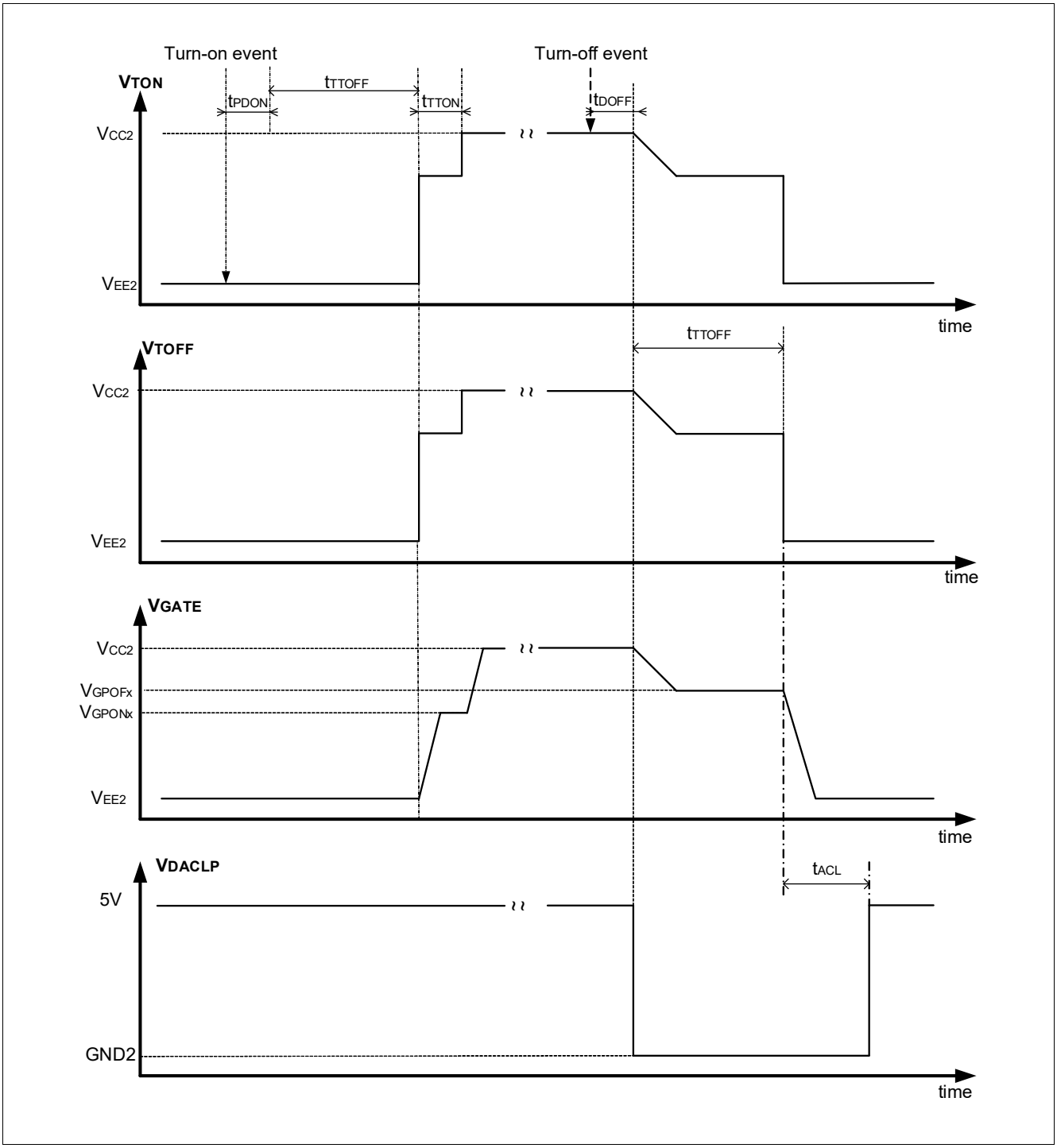


Figure 16 Schematic switching sequence

1.4.6.3 Passive clamping

When the secondary chip is not supplied, the **TOFF**, **TON**, and **GATE** signals are clamped to V_{EE2}. The **GATE** pin is the sensing pin for this clamping and should not be overstressed. See **Chapter 5** for the electrical capability of this feature.

1.4.7 Fault notifications

The device provides two kinds of fault notification mechanisms:

- The **NFLTA**, **NFLTB**, and **NRST/RDY** pins allow for fast error notification to the main microcontroller. All signals are active low.
- Error bits can be read by SPI.

The activation of the **NRST/RDY** signal is associated with Reset events (see **Chapter 1.4.10**). The activation of the **NFLTA** signal is associated with Class A events. The activation of the **NFLTB** signal is associated with Class B events. In general, the activation of **NFLTA** or **NFLTB** is linked to a state transition of the device.

Handling Class A and B events

If a Class A event occurs that leads to a state transition (from OPM4 to OPM3 or OPM6 to OPM5), the **NFLTA** signal is activated. If a Class A event occurs that does not lead to a state transition, **NFLTA** is not activated (exception: ADC Boundary Check events). However, the corresponding error bit in the **PER** or **SER** register is set.

ADC boundary check events are handled in a special way: If the **SCFG2.ACAEN** bit is set, an ADC boundary check event leads to a Class A event, an emergency (regular) turn-off sequence is issued, and possibly there is a state transition and **NFLTA** is activated. The **PSTAT2.FLTAP** bit is set if the **SADC.AOVS** bit or the **SADC.AUVS** bit is set.

If the **SCFG2.ACAEN** bit is cleared, an ADC boundary check event does not lead to a state transition (**NFLTA** is not activated and no emergency turn-off sequence is initiated). However, the **SER.AUVER** bit, the **SER.AOVER** bit or both are set. Therefore, when **SCFG2.ACAEN** is cleared, the ADC Boundary Check event behaves like a Class C event.

Additionally, the **NFLTA** signal can be activated directly by setting the status bits related to boundary checks on the primary side. This lets **NFLTA** be activated in case of ADC Boundary Check events in any operating mode. If the **PCFG.ADAEN** bit is set, **NFLTA** is activated at the transition of bit **PSTAT2.AXVP** from 0_B to 1_B.

If a Class B event occurs that leads to a state transition (to OPM1), the **NFLTB** signal is activated. If a Class B event occurs that does not lead to a state transition, **NFLTB** is not activated. However, the corresponding error bit in the **PER** or **SER** register is set.

The level issued by the device on the **NFLTA** and **NFLTB** pins is specified by the **PSTAT2.FLTA** and **PSTAT2.FLTB** bits. The levels read by the device at those pins is specified by the **PPIN.NFLTAL** and **PPIN.NFLTBL** bits. If a condition leading to a Class A event is detected by the device, the **PSTAT2.FLTAP** bit is set. If a condition leading to a Class B event is detected by the device, the **PSTAT2.FLTBP** bit is set.

*Note: In case of short events (for example, DESAT or OCP events), it might not be possible to observe a change of the states of the **PSTAT2.FLTAP** or **FLTBP** bits.*

Clearing fault notifications

Table 12 summarizes how fault notifications are cleared:

Table 12 Failure notification clearing

	NFLTA and NFLTB signals	**Primary sticky bits**	**Secondary sticky bits**
PCTRL.CLRP set	De-assertion	Cleared	-
PCTRL.CLRS set[1)]	-	-	Cleared
EN invalid-to-valid transition	De-assertion[2)]	-	-

1) If the device is in OPM1, setting the **PCTRL.CLRS** bit leads to a transition to OPM0.

2) Only in OPM3 and OPM5. In other operating modes, no de-assertion is performed.

A CLRP command (that is, setting the **PCTRL.CLRP** bit) clears all sticky bits on the primary side. A CLRS command (that is, setting the **PCTRL.CLRS** bit) clears all sticky bits on the secondary side.

The **NFLTA** and **NFLTB** signals are de-asserted with an invalid-to-valid transition of the **EN** signal. They can also be de-asserted by a CLRP command, depending on the device's status.

1.4.8 EN signal pin

The **EN** signal allows the logic on the primary side to directly control on the state of the device. A valid signal has to be provided on the **EN** pin. A valid-to-invalid transition of the signal on the **EN** pin generates a Class A event.

The **EN** pin should be driven actively by the external circuit. If this pin is floating, an internal weak pull-down resistor ensures that the signal is low.

*Note: Even if the signal at the **EN** pin is valid, the device can still be in the Disabled state. This may happen, for example, if another error is being detected.*

A valid **EN** signal is defined as a digital high level. When **EN** is at the low level, the signal is considered not valid, and the device is in the Disabled state. In case of a high-to-low transition, a Class A event is generated.

An Invalid-to-valid transition of the **EN** signal deactivates the **NFLTA** and **NFLTB** signals (only when the device is in OPM3 or OPM5).

The levels read by the device at the **EN** pin are specified by the **PPIN.ENL** bit. The validity status of the **EN** signal is stored in the **PSTAT2.ENVAL** bit.

1.4.9 Internal supervision

The internal supervision functionality is summarized in **Table 13**:

Table 13 System supervision overview

Parameter	Short description
Function	Monitoring of the key internal functions of the chip.
Periodicity	Continuous.
Action in case of a failure event	See below.
Programmable	No.

The primary and secondary chips are equipped with internal verification mechanisms ensuring that the key functions of the device are operating correctly. The internal blocks which are supervised are listed below:

- Lifesign watchdog: mutual verification of the response of both chips (both primary and secondary).
- Oscillators (both primary and secondary, including open and short detection on the **IREF1** and **IREF2** pins).
- Memory (both primary and secondary).

1.4.9.1 Lifesign watchdog

The primary and the secondary chips monitor each other by means of a lifesign signal. The periodicity of the signal is typically t_{LS}. Each chip expects a lifesign from its counterpart within a given time window. If a lifesign error is detected by a chip, a Reset event is generated on both sides (which causes a transition to OPM0) and the **NFLTB** pin is set. Due to the communication loss on both sides, both the **PER.CERP** bit and the **SER.CERS** bit are set.

*Note: The **PER.CERP** and **SER.CERS** bits indicate a loss-of-communication event. The current status of the internal communication is indicated by the **PSTAT.SRDY** bit.*

1.4.9.2 Oscillator monitoring

The main oscillators on the primary and on the secondary side are monitored continuously. Two distinct mechanisms are used for this purpose:

- The lifesign watchdog enables the detection of significant deviations from the nominal frequency (both primary and secondary, see above).
- Open and short detection on the **IREF1** pin.

If a failure is detected on the **IREF1** pin, the primary chip is kept in reset state for the duration of the failure and the **NRST/RDY** signal is asserted. This leads to the detection of a lifesign error by the secondary chip, which generates a Reset event.

1.4.9.3 Memory supervision

The configuration parameters of the device, stored in the registers, are protected with a parity-bit protection mechanism. Both the primary and the secondary chip are protected. (See **Chapter 3**.)

If a failure is detected on the primary chip, that side is kept in reset state, and both the **NRST/RDY** and the **NFLTB** signals are asserted. The secondary side initiates an emergency (regular) turn-off sequence.

If a memory failure is detected by the secondary chip, an emergency (regular) turn-off sequence is initiated. The secondary chip is kept in reset state for the duration of the failure. This leads to the detection of a lifesign error by the primary chip, which generates a Reset event.

1.4.9.4 Hardware failure behavior

The internal supervision function can detect several failures which could lead to the primary or secondary chip hold on (staying in reset). Failures which can be detected are mentioned in the table below. The failures are detected by the supervision function described in the previous sections.

Table 14 Failure events summary

Failure event	Primary	Secondary	Notification (primary)	Notification (secondary)
OSC1 not starting at power-up	Reset	Soft reset	• **NRST/RDY** low (driven by device during event). • **PER.RSTP** bit set (once OSC1 valid again). • **PER.CERP** bit **not** set. • **NFLTB** activated at the end of the Reset event.	• **SER.CERS** bit set (if the lifesign is lost). • Output stage issues a PWM OFF command.
IREF1 shorted to ground or open	Reset	Soft reset	• **NRST/RDY** low (driven by device during event). • **PER.RSTP** bit set (once **IREF1** is valid again). • **PER.CERP** bit **not** set. • **NFLTB** activated at the end of the Reset event.	• **SER.CERS** bit set (if the lifesign is lost). • Output stage issues a PWM OFF command.
Memory error on primary side	Reset	Soft reset	• **NRST/RDY** low (driven by device during event). • **PER.RSTP** bit set (when failure condition is removed). • **PER.CERP** bit **not** set. • **NFLTB** activated at the end of the Reset event.	• **SER.CERS** bit set (if the lifesign is lost). • Output stage issues a PWM OFF command.
OSC2 not starting at power-up	-	Hard reset	• **NFLTB** activated. • **PER.CERP** bit set. • Bit **PSTAT.SRDY** cleared	• Output stage issues a PWM OFF command.
OSC2 misfunction during operation	-	Soft reset	• **NFLTB** activated. • **PER.CERP** bit set. • **PSTAT.SRDY** bit cleared for the duration of the failure.	• Output stage issues a PWM OFF command.
VREG shorted to ground	-	Hard reset	• **NFLTB** activated. • **PER.CERP** bit set. • **PSTAT.SRDY** bit cleared.	• Output stage issues a PWM OFF command. • **SER.RSTS** bit (once V_{CC2} is valid again).
Memory error on secondary side	-	Hard reset	• **NFLTB** activated. • **PER.CERP** bit set. • **PSTAT.SRDY** bit cleared.	• Output stage issues a PWM OFF command.

1.4.10 Reset events

A Reset event sets the device and its internal logic in the default configuration. All user-defined settings are overwritten with the default values. The list of Reset events and their effect is summarized in **Table 15**.

Table 15 Reset events summary

Reset event	Primary	Secondary	Notification (primary)	Notification (secondary)
NRST/RDY input signal active (driven externally)	Reset	Soft reset	• **NRST/RDY** low (during event). • **PER.RSTEP** bit and **PER.RSTP** set. • **PER.CERP** bit **not** set. • **NFLTB** activated at the end of the Reset event.	• **SER.CERS** bit set (if the lifesign is lost). • Output stage issues a PWM OFF command.
UVLO1 event	Reset	Soft reset	• **NRST/RDY** low (driven by device during event). • **PER.RSTP** bit set (once V_{CC1} valid again). • **PER.CERP** bit **not** set. • **NFLTB** activated at the end of the Reset event.	• **SER.CERS** bit set (if the lifesign is lost). • Output stage issues a PWM OFF command.
V_{CC2} Reset event (communication loss due to voltage breakdown on V_{CC2})	-	Hard reset	• **NFLTB** activated. • **PER.CERP** bit set. • **PSTAT.SRDY** bit cleared for the duration of the failure.	• **SER.RSTS** bit set (once V_{CC2} is valid again). • Output stage issues a PWM OFF command.

All Reset events put the device in the OPM0 mode. During a soft reset, the device logic continues to work, but the registers use the default values.

Table 16 describes the behavior of the device pins in case of a hard reset condition on the primary side.

Table 16 Pin behavior (primary side) in case of reset condition

Pin	Output level	Comments
SDO	Tristate	–
NFLTB	Low	–
NFLTA	Low	–
NRST/RDY	Low (GND1)	–

Table 17 describes the behavior of the device pins in case of a hard reset condition on the secondary side.

Table 17 Pin behavior (secondary side) in case of reset condition

Pin	Output level	Comments
TON	Low (V_{EE2})	Passive clamping
TOFF	Low (V_{EE2})	Passive clamping
DESAT	Low (GND2)	Clamped

Table 17 Pin behavior (secondary side) in case of reset condition (cont'd)

Pin	Output level	Comments
GATE	Low (V_{EE2})	Passive clamping
DACLP	High (5 V)	–

1.4.11 Operation in Configuration mode

This section describes the mechanisms for configuring the device.

1.4.11.1 Static configuration parameters

When the device is in the OPM2 mode, static parameters can be configured by writing the appropriate configuration register.

Once OPM2 is left with the SPI command EXIT_CMODE, the configuration parameters are fixed on both the primary and the secondary chip. In particular, this means that write accesses to the corresponding registers are invalid. This prevents static configurations from being modified during runtime. In addition, the configuration parameters on the primary and secondary side are protected with a memory protection mechanism. When the values are not consistent, a Reset event, a Class B event, or both are generated.

1.4.11.1.1 Configuration of the SPI parity check

By default, the SPI interface supports odd-parity checks. The parity-checking mechanism (active on the reception of an SPI word) can be disabled by setting the **PCFG**.**PAREN** bit to 0_B. Setting **PAREN** to 1_B enables the parity check.

The generation of parity bits for the transmitter cannot be disabled.

1.4.11.1.2 Configuration of NFLTA activation in case of boundary check events

The **NFLTA** signal is normally activated by a state transition. However, it can also be configured to be activated by a transition in the **PSTAT2**.**AXVP** bit. This is configured by setting the **PCFG**.**ADAEN** bit.

1.4.11.1.3 Configuration of the ADCT pin

The **ADCT** signal can be used as a trigger source for the ADC on the secondary side. If **PCFG**.**ADTEN** is cleared, the voltage read on the pin is ignored by the device. If **PCFG**.**ADTEN** is set, an ADC conversion is triggered by a rising edge detected on **ADCT** pin.

1.4.11.1.4 Configuration of the STP minimum dead time

The minimum dead time for the shoot-through protection can be specified in the **PCFG2**.**STPDEL** bit field. The value is specified as a number of OSC1 clock cycles.

1.4.11.1.5 Configuration of the digital channel

The direction of the **DIO1** pin can be set by writing bit field **PCFG2**.**DIO1**. The direction of the **DIO2** pin can be set by writing the **SCFG**.**DIO2C** bit field.

1.4.11.1.6 Configuration of the V_{BE} compensation

The V_{BE} compensation of the **TON** and **TOFF** signals can be activated or deactivated by writing the **SCFG**.**VBEC** bit. See **Chapter 1.4.6** for details.

1.4.11.1.7 Clamping of DESAT pin

By setting the **SCFG**.**DSTCEN** bit, the DESAT signal is clamped to V_{GND2} while the output stage of the device issues a PWM OFF command and during blanking time periods. When **SCFG**.**DSTCEN** bit is cleared, the DESAT clamping is only activated during blanking time periods.

1.4.11.1.8 Activation of the pulse suppressor

The pulse suppressor function is associated with the TTOFF function and can be activated by setting the **SCFG**.**PSEN** bit. When pulse suppression is activated, **SRTTOF**.**RTVAL** should be set to its minimum value.

1.4.11.1.9 Configuration of the Verification mode time-out duration

The length of the time-out in Verification mode is selectable via the **SCFG**.**TOSEN** bit.

1.4.11.1.10 DESAT threshold level configuration

The detection level of the **DESAT** comparator is selectable via the **SCFG**.**DSATLS** bit.

1.4.11.1.11 UVLO2 threshold level configuration

The detection levels of the UVLO2 comparators are selectable via the **SCFG**.**UVLO2S** bit.

1.4.11.1.12 DACLP Operating mode configuration

The Operating mode of the **DACLP** pin is selectable via the **SCFG**.**DACLC** bit field.

1.4.11.1.13 Configuration of the ADC

The ADC can be configured by writing the **SCFG2** register. The limits of the boundary checker are selectable by writing the **SBC** register.

*Note: **SCFG2** and **SBC** can only be written when the **SCFG**.**CFG2** bit is set to 1_B.*

1.4.11.1.14 Configuration of the DESAT blanking time

The blanking time for the DESAT protection can be configured by writing the **SDESAT**.**DSATBT** bit field. A minimum value for the blanking time has to be specified.

Note: The specified OCP blanking time should be smaller than the programmed DESAT blanking time.

1.4.11.1.15 Configuration of the OCP function

The blanking time for the OCP protection can be configured by writing the **SOCP**.**OCPBT** bit field. Programming 0_H deactivates the blanking time feature. If a blanking time is required, a minimum value for the delay has to be programmed. The detection level of the OCP comparator is selectable via the **SCFG**.**OCPLS** bit.

Note: The programmed OCP blanking time should be smaller than the programmed DESAT blanking time.

1.4.11.1.16 Configuration of the TTOFF sequences

The TTOFF delays for regular and safe turn-off sequences can be programmed separately by writing, respectively, the **SRTTOF** or **SSTTOF** registers. The delay for the regular turn-off can also be configured using the timing calibration feature.

Programming 0_H as a delay value disables the TTOFF for the respective turn-off sequence. Hard turn-offs are performed instead. If the TTOFF function is desired, a minimum value for the delay has to be programmed.

When safe two-level turn-off is used (non-zero delay) in normal Operating mode (OPM4), the programmed safe turn-off delay value should be higher than the programmed regular two-level turn of delay.

The plateau level for safe two-level turn-off sequences can be specified in the **SSTTOF.GPS** bit field. The plateau level value for safe turn-off sequences should be lower than the one selected for regular turn-off sequences.

The regular TTOFF delay can be calibrated using the TCF feature of the device.

1.4.11.1.17 Configuration of the TTON delay

The TTON delay can be configured by writing the **STTON.TTONVAL** bit field. Programming 0_H as a delay value disables the TTON for all turn-on sequences. Hard turn-ons are performed instead. If the TTON function is desired, a minimum value for the delay has to be programmed.

The TTON delay can be calibrated using the TCF feature of the device.

1.4.11.2 Dynamic configuration

The TTOFF (regular turn-off only) plateau level can be modified at runtime by writing the **PCTRL2.GPOF** bit field. The value of this bit field is periodically transferred to the secondary side. The last valid value received by the primary side is available in the **PSTAT.GPOFP** bit field.

Similarly, the WTO and the TTON plateau level can be configured by writing **PCTRL.GPON** bit field. The value of this bit field is periodically transferred to the secondary side. The last valid value received by the primary side is available in the **PSTAT.GPONP** bit field.

A plateau voltage value written to the device is latched and becomes active two switching sequences later. (That is, when a new value is written, the next sequence still uses the old value and the one after that uses the new value.).

1.4.11.3 Delay calibration

In order to compensate for timing errors caused by variations between parts, a dedicated timing calibration feature (TCF) is available. The TCF works in such a way that the PWM input signal is used to start and stop a counter clocked by the start-stop oscillator of the output stage. This can be used to configure the following delays:

- TTOFF delay for regular turn-off
- TTON delay

Using the TCF, part-to-part variations of the frequency of the start-stop oscillator can be compensated for. This results in better accuracy for application critical timing. Device-specific variations, for example, related to temperature, are however not compensated for. The TCF can be activated or deactivated in the Configuration mode by writing the **SSCR.VFS2** bit field. The device should then be put into OPM6 and the PWM signal applied. Details about the TCF operation are provided in **Chapter 2.5.3**.

1.4.12 Low-latency digital channel

The low-latency digital channel provides an alternative to discrete galvanic isolators. Digital signals can be transmitted through the **DIO1** and **DIO2** pins. The direction of the channel is specified by the **PCFG2**.**DIO1** and **SCFG**.**DIO2C** bit fields. The functionality of the channel is shown **Figure 17**.

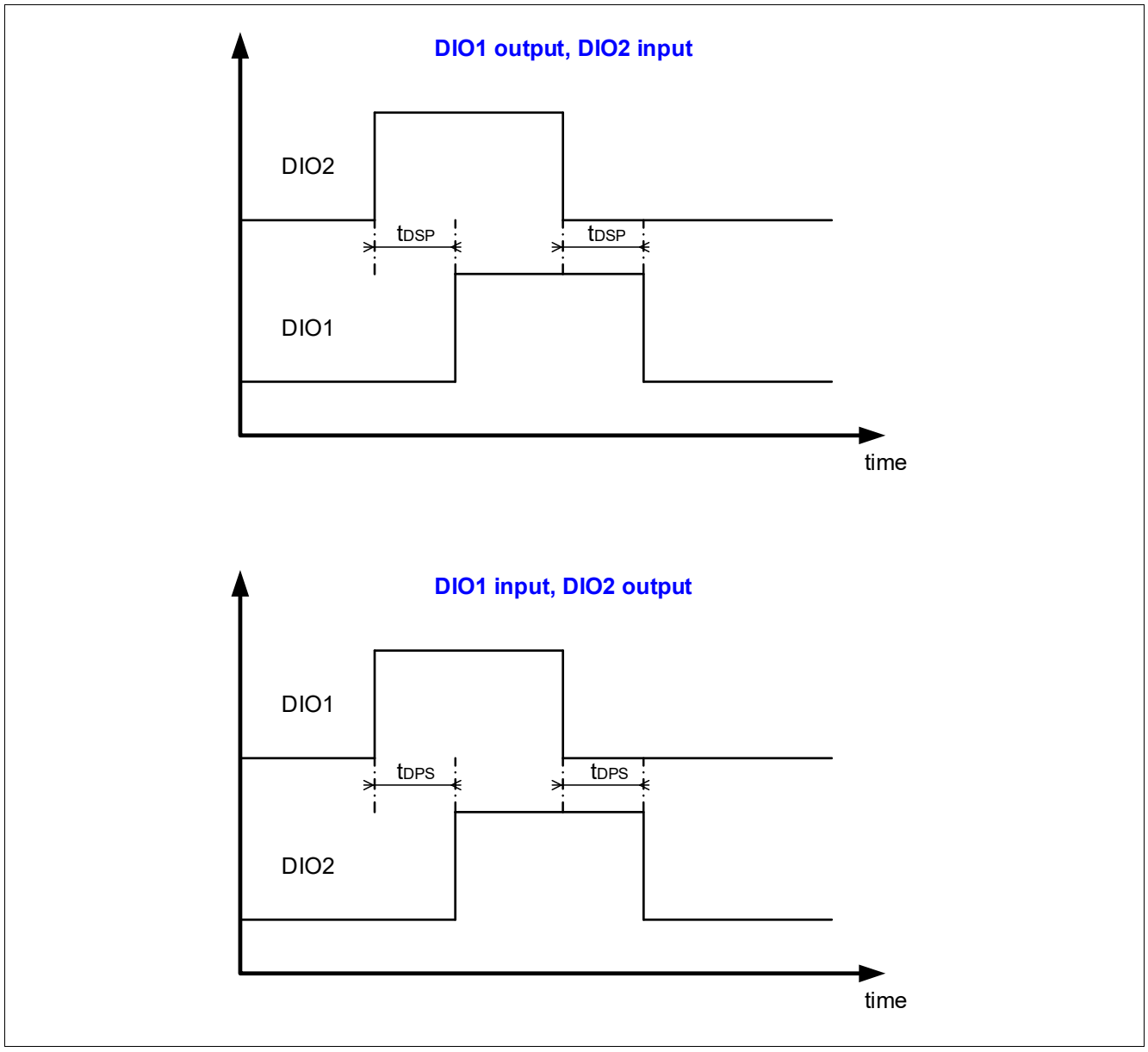


Figure 17 Low-latency digital channel

The voltage level at the **DIO1** pin can be read from the **PPIN**.**DIO1L** bit. The voltage level at **DIO2** can be read from **SSTAT2**.**DIO2L**.

The input stages of the **DIO1** and **DIO2** signals both include a debouncing filter that filters glitches and noises from the input signals.

1.4.13 Analog-to-digital converter

1.4.13.1 Overview

The key properties of the built-in ADC on the secondary side are:

- Successive approximation method
- 0-V to 5-V input signal (input buffer)
- 8-bit resolution
- Fast conversion time
- Preamplifier with programmable gain
- Selectable offset

The ADC operates based on successive approximation. It offers flexible analog measuring capabilities, among them (non-exhaustive list):

- Measuring an NTC resistor located on the power module (**Figure 18**)
- Measuring a temperature diode integrated into the IGBT (**Figure 19**)
- Measuring the high-voltage DC link or phase voltage (**Figure 20**)

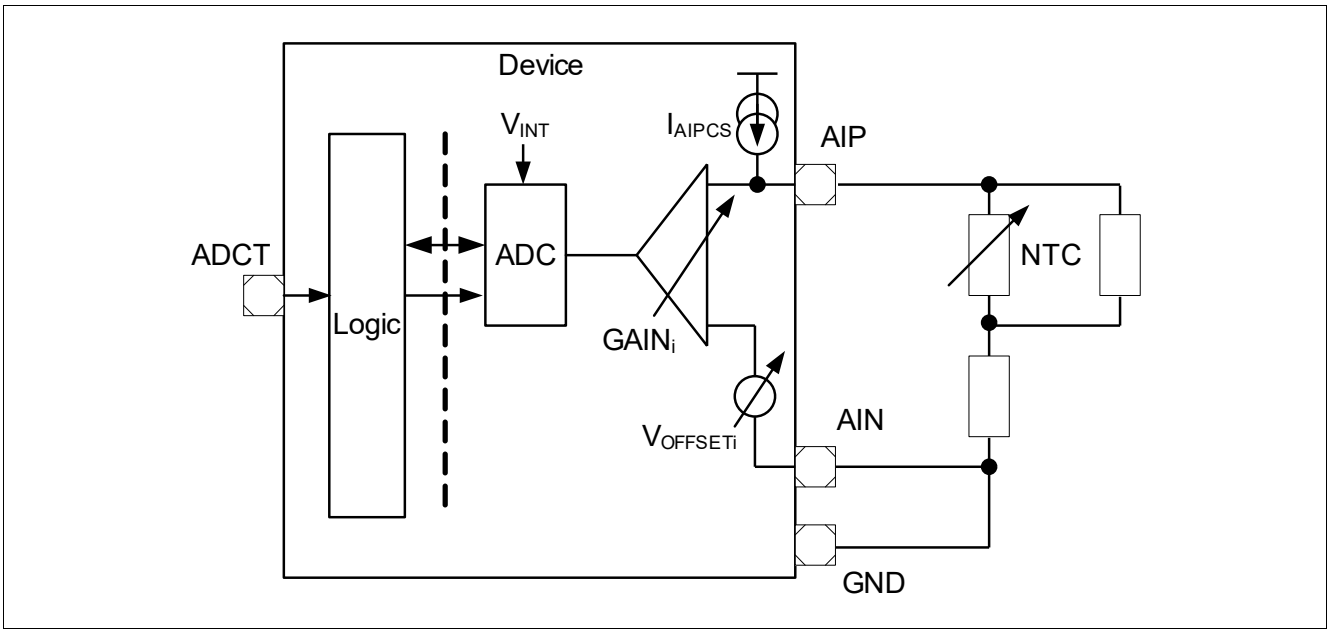


Figure 18 Application example: NTC measurement

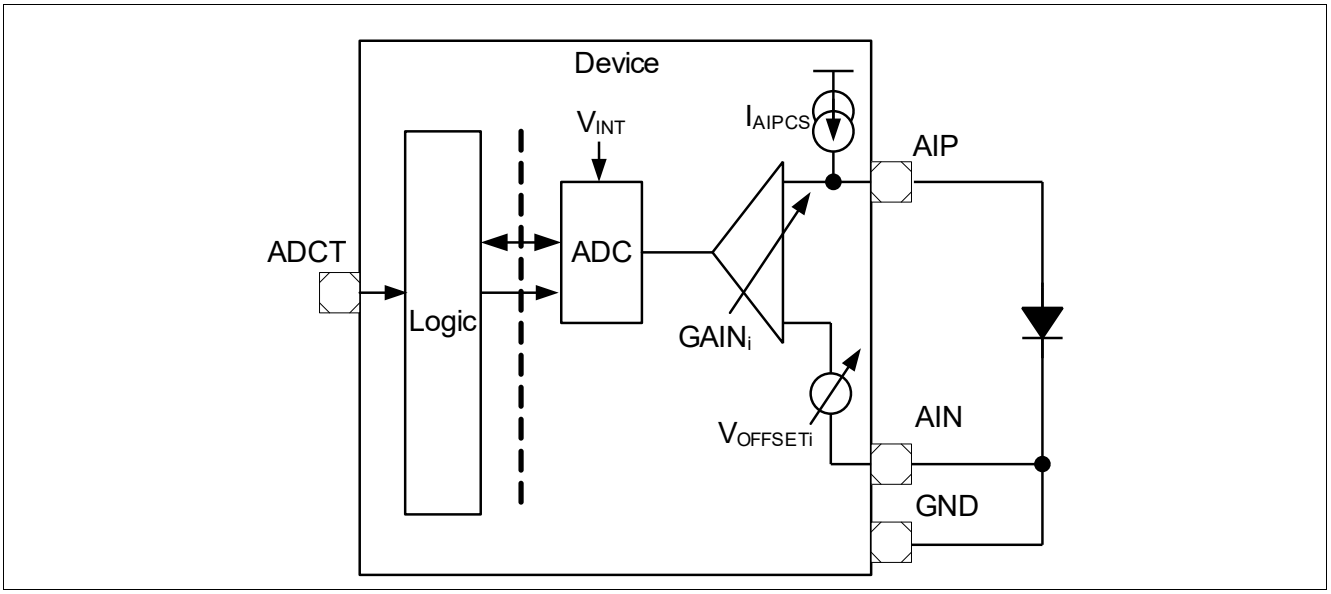


Figure 19 Application example: Diode measurement

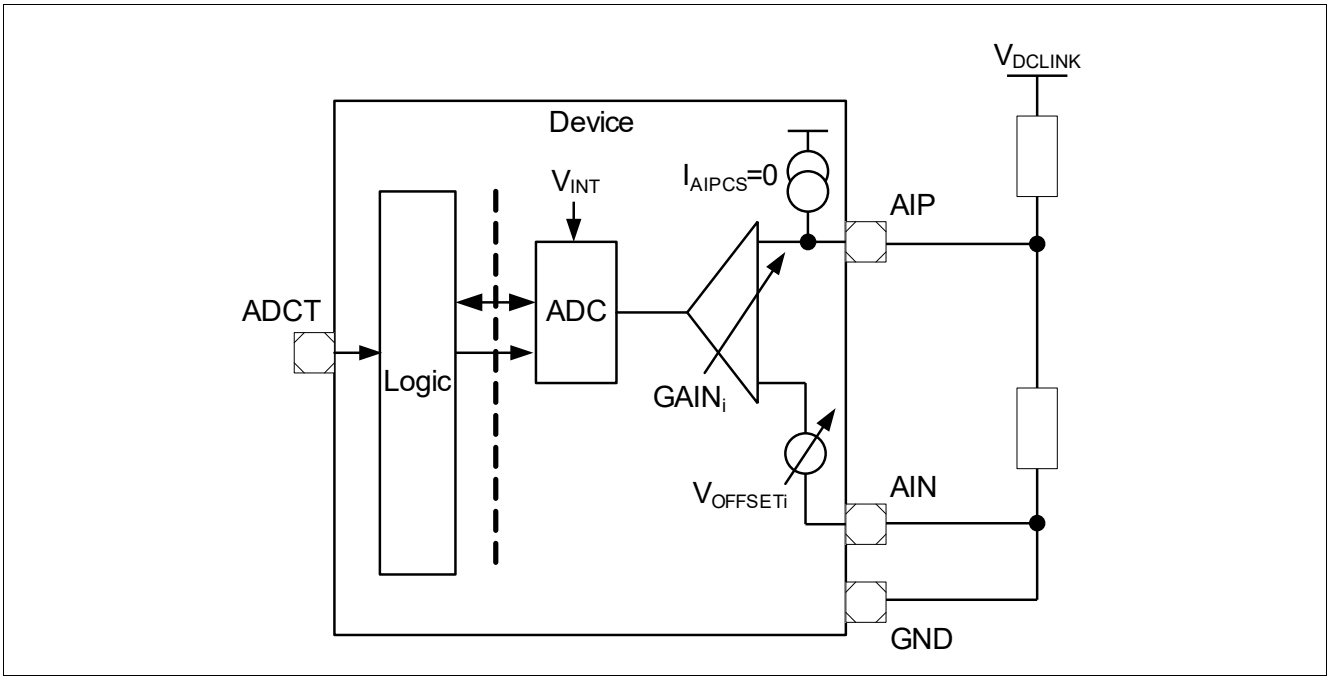


Figure 20 Application example: V_{DCLINK} measurement

*Note: The internal current source can be disabled by writing 0 to the **SCFG2.ACSS** bit.*

1.4.13.2 General operation

When the ADC receives a valid trigger, it samples the voltage provided by the input buffer. The result of the conversion is stored as an 8-bit value.

The input buffer captures the voltage V_{AIP} - V_{AIN}. 0 V (V_{AIP} = V_{AIN}) is converted to the digital value 00_H by the ADC. The conversion voltage range depends on the specified gain of the input buffer. For example, if GAIN = 1 and V_{OFFi} = 0 V is programmed, V_{AIP} - V_{AIN} = 2.75 V corresponds to the digital value FF_H.

Once the conversion is completed, the **SADC.ADCVAL** bit field is updated and the **SADC.AVFS** bit is set. This valid flag can be cleared by SPI with a CLRS command.

If a trigger is received while a conversion is already in progress, any new conversion request is ignored until the running conversion is completed.

Since the ADC can be assigned (statically) to different functions by the application, several operating modes can be chosen from in order to suit each of those specific roles. The operating mode is configured via the SPI interface.

Trigger sources

Several trigger sources are available for starting a conversion. These are the trigger sources for the conversion on the primary side:

- Direct SPI write command.
- **ADCT** pin.

In addition, trigger sources can be activated on the secondary side depending on the configuration of the **SCFG2.ATS** bit field:

- Periodic Trigger mode: In this mode, conversions are started automatically by the ADC at a fixed periodical rate (parameter t_{ATRIG}).
- PWM Trigger mode: In this mode, conversions are triggered by a PWM edge (rising or falling, selectable). When the corresponding PWM signal is detected on the secondary side, the ADC is triggered after the delay programmed in the **SCFG2.PWMD** bit field. The reference point that starts the delay is the hard transition (ON or OFF).

Operation mode

By setting the **SCFG2.ACSS** bit, a current source can be activated that delivers a fixed current to pin **AIP**.

Gain and offset configuration

The gain and offset of the differential input buffer is configurable statically with bit fields **SCFG2.AGS** and **SCFG2.AOS**.

Mathematical model

The following equation can be used to calculate a converted digital value from the voltage at the ADC input pins:

$$V_{ALDIG} = (V_{AIP} - V_{AIN} - V_{OFFi}) \times GAIN_i \times 255/V_{INT}, \text{ where:} \quad (1.1)$$

- V_{INT} is the internal ADC voltage.
- V_{ALDIG} is the digital value calculated by the ADC (from 0 to 255).
- V_{AIP} is the voltage at the **AIP** pin.
- V_{AIN} is the voltage at the **AIN** pin.
- V_{OFFi} is the offset value specified in the **SCFG2.AOS** bit field.

- $GAIN_i$ is the gain value specified in the **SCFG2.AGS** bit field.

1.4.13.3 Boundary checks

The boundary check mechanism automatically compares each conversion result to two boundary values, the limits specified, respectively, in the **SBC.LCB1A** (lower limit) and **SBC.LCB1B** (upper limit) bit fields.

When a new conversion result is available, it is compared with the boundary values stored in the **SBC** register. The values used for the comparison are respectively **SBC.LCB1A** extended by the LSBs 0_B0_B (that is, (**LCB1A** <<2) and FC_H) and **SBC.LCB1B** extended by the LSBs 1_B1_B (that is, (**LCB1B** << 2) | 03_H).

If the conversion result lies below both boundaries, the **SER.AUVER** error flag is set. In case the conversion result lies above boundaries, the **SER.AOVER** error flag is set. If the conversion result is above or equal to one boundary and below or equal to the other boundary, no flag is set. Do not specify a lower limit that is above the upper limit. In that case, the SER.AUVER and SER.AOVER flags may be set unexpectedly.

The default limits are chosen such that the flags are never set, regardless of the conversion result (equivalent to disabling the limit check).

The reaction of the device to a boundary check event can be configured by setting the **SCFG2.ADAEN** bit.

2 Protection and diagnostics

This section describes the safety-related functions of the 1EDI2010AS.

2.1 Supervision overview

The 1EDI2010AS driver provides extended supervision functions, in order to support safety strategies on the system level. **Table 18** gives an overview of the available functions.

Table 18 Safety-related functions

Protection feature	Description	Category	Details
DESAT	Monitoring the collector-emitter voltage of the IGBT in ON state.	A	**Chapter 2.2.1**
OCP	Monitoring the current on the IGBT's auxiliary emitter path.	A	**Chapter 2.2.2**
External enable	Fast deactivation via an external enable signal on the primary.	A	**Chapter 2.2.3**
ADC boundary check	ADC boundary check.	A	**Chapter 1.4.13.3**
Power supply monitoring	Undervoltage lock-out function on V_{CC1}, and V_{CC2}.	B	**Chapter 2.3.1**
STP	Shoot-through protection.	C	**Chapter 2.4.1**
SPI error detection	SPI error detection.	C	**Chapter 2.4.2**
WTO	Weak turn-on functionality.	D	**Chapter 2.5.2**
Internal clock supervision	Plausibility check of the frequency of the internal oscillator.	D	**Chapter 2.5.3**
TTOFF	Two-level turn-off.	E	**Chapter 1.4.6**
SPI communication	SPI communication (using the **PRW** register).	E	**Chapter 3.1.1**
Overvoltage robustness	Robustness against transient overvoltage on the power supply.	E	**Chapter 5.1**

From the conceptual point of view, the protection functions can be grouped into five categories.

- Category A: The device "decides on its own", after the detection of a Class A event, to change the state of the output stage and to disable itself. A dedicated action from the user is needed to reactivate the device (fast reactivation).
- Category B: The device "decides on its own", after the detection of a Class B event, to change the state of the output stage and to disable itself. A complete reinitialization from the user is needed to reactivate the device (slow reactivation).
- Category C: Only a notification is issued when an error is detected.
- Category D: Intrusive supervision functions, aimed at being started when the application is not running.
- Category E: Functions or capabilities supported by the device whose use can enhance the overall safety coverage of the application.

2.2 Protection functions: Category A

2.2.1 Desaturation protection

The integrated desaturation (DESAT) functionality is summarized in **Table 19**:

Table 19 DESAT protection overview

Parameter	Short description
Function	Monitoring the V_{CE} voltage of the IGBT.
Periodicity	Continuous while device issues a PWM ON command.
Action in case of failure event	1. Emergency (safe) turn-off sequence. 2. **SER.DESATER** error flag is set. 3. Assertion of the **NFLTA** signal.
Programmable	Yes (blanking time and threshold level).

The DESAT function aims at protecting the IGBT in case of short circuit. The voltage drop V_{CE} over the IGBT is monitored via the **DESAT** pin while the device issues a PWM ON command. The voltage at the **DESAT** pin is externally filtered by an RC filter, and decoupled by an external diode (see **Figure 21**). The DESAT voltage is compared to an internal reference voltage. The result of this comparison is available by reading the **SSTAT2.DSATC** bit.

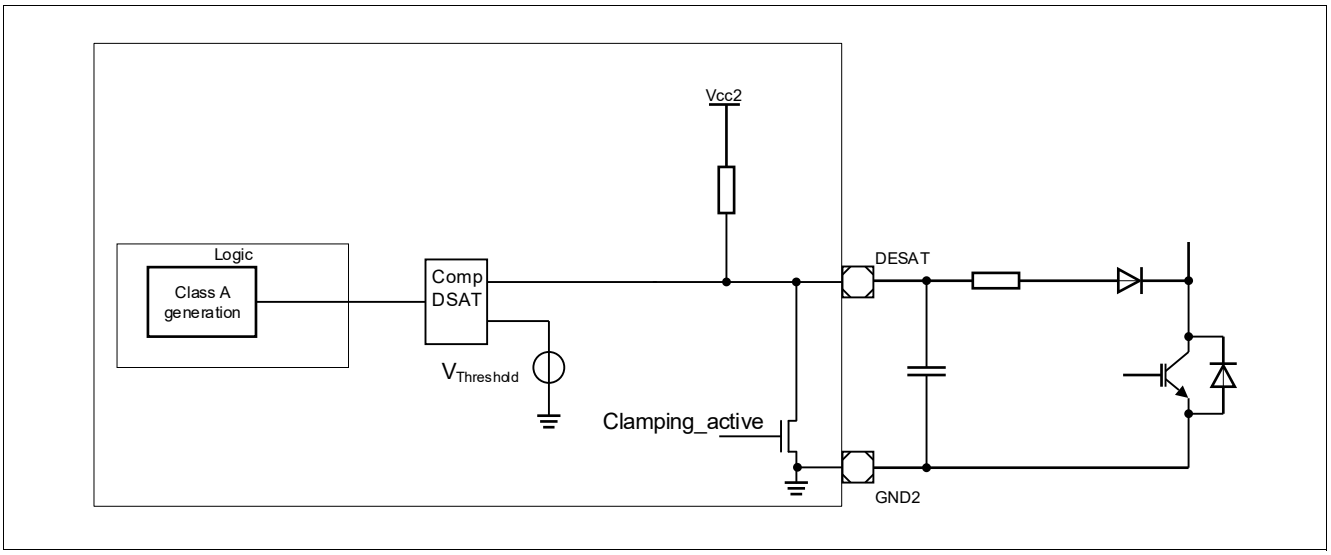


Figure 21 DESAT function: diagram of principle

At the beginning of a turn-on sequence, the voltage at the **DESAT** pin is forced to the low level for the duration of the blanking time specified in the **SDESAT** register. Once the blanking time has elapsed, the voltage at **DESAT** is released and is compared to an internal reference voltage. Depending on the value of the decoupling capacitance, an additional “analog” blanking time is added which corresponds to the charging of the capacitance through the internal pull-up resistance (**Figure 22**).

If the measured voltage is higher than the selected internal threshold, an emergency (safe) turn-off sequence is initiated, the **SER.DESATER** bit is set, and a fault notification is issued on the **NFLTA** pin (if there is a transition to another operating state – see **Chapter 1.4.7**). The threshold can be selected in OPM2 by writing to **SCFG.DSATLS**. Writing 1 to **DSATLS** selects the **DESAT reference Level** V_{DESAT1}; otherwise V_{DESAT0} is selected.

The DESAT function is not active while the output stage is in the PWM OFF state.

The blanking time needs to be chosen carefully, since the DESAT protection may be *de facto* inhibited if the PWM ON-time is too short compared to the chosen blanking time.

At turn-off, the DESAT signal is pulled down for the duration of the TTOFF plateau time, extended by the blanking time once the hard turn-off sequence is initiated.

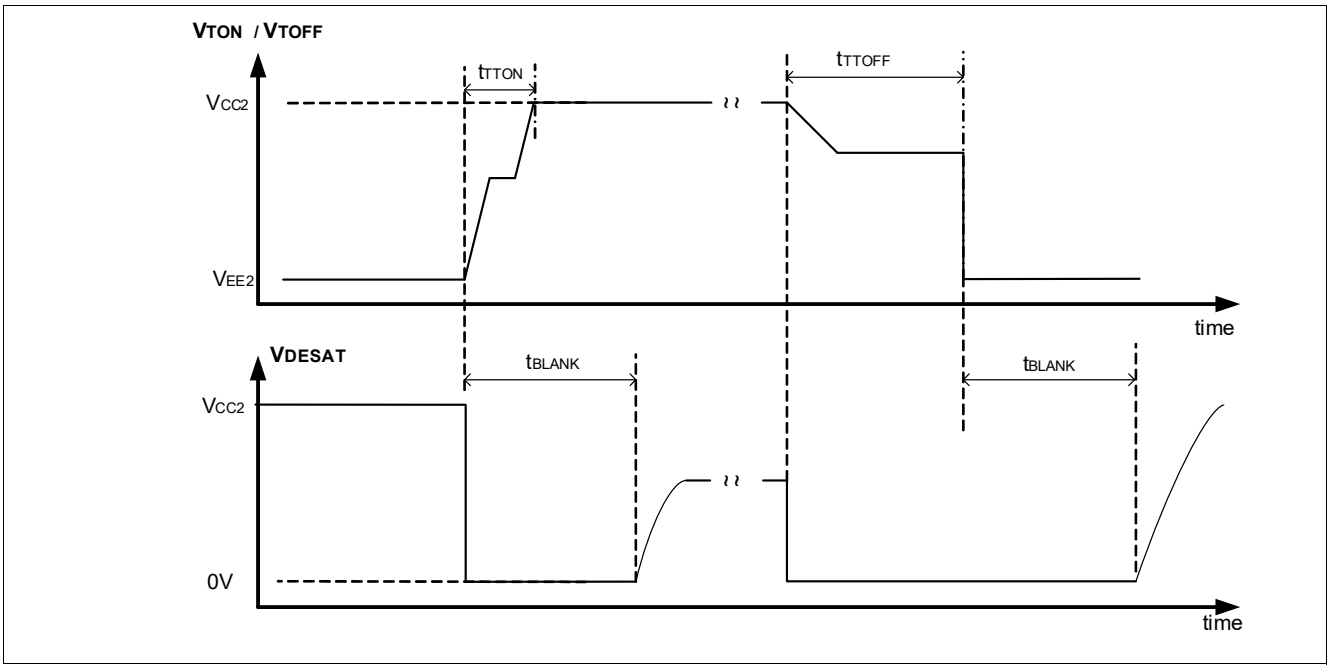


Figure 22 DESAT operation

*Note: If the **DESAT** pin is open, the pull-up resistance ensures that a DESAT event is generated at the next PWM turn-on command.*

DESAT clamping during turn-off

The internal pull-up resistance may lead to the unwanted charging of the DC link capacitance via the DESAT pin. To avoid this, the DESAT function needs to be activated by clearing the **SCFG.DSTCEN** bit. When that bit is set, the **DESAT** pin is internally clamped to GND2 when a PWM OFF command is issued by the device.

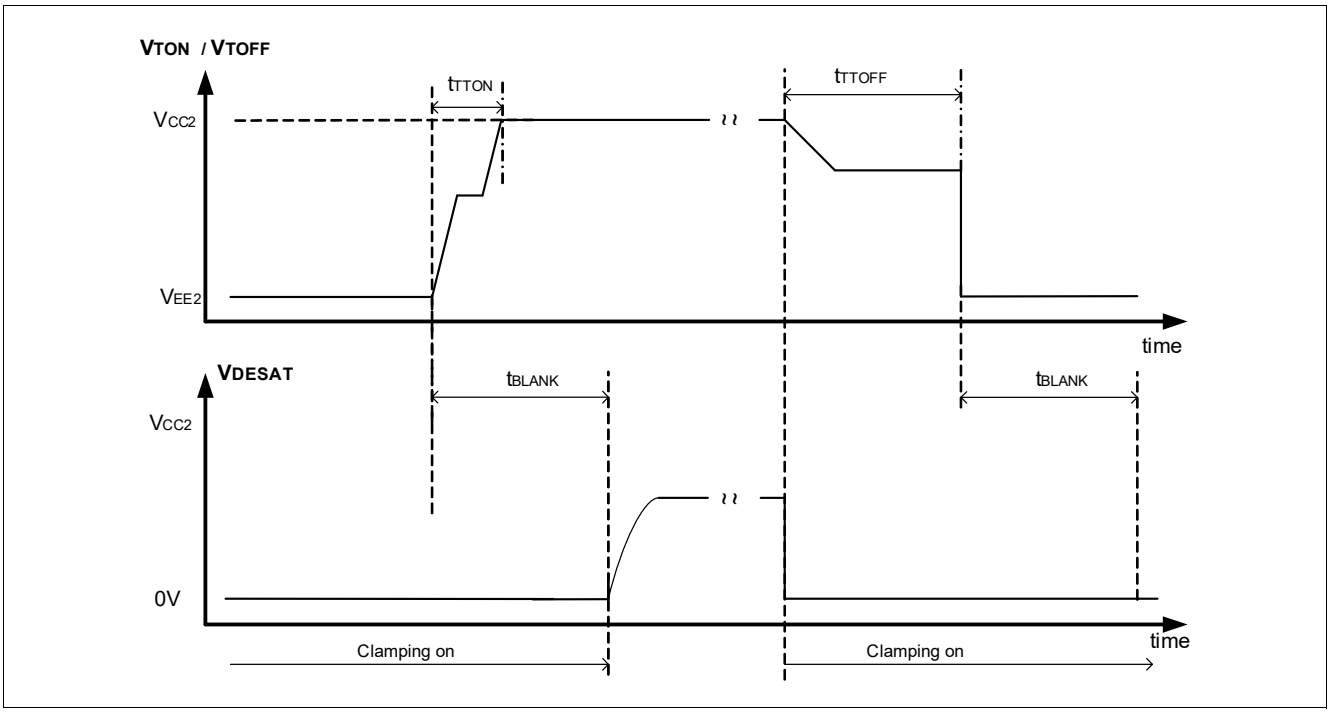


Figure 23 DESAT operation with DESAT clamping enabled

2.2.2 Overcurrent protection

The integrated overcurrent protection (OCP) functionality is summarized in **Table 20**:

Table 20 OCP function overview

Parameter	Short description
Function	Monitoring the voltage drop over an external resistor located on the auxiliary emitter path of the IGBT.
Periodicity	Continuous while the device issues a PWM ON command.
Action in case of failure event	1. Emergency (safe) turn-off sequence. 2. **SER.OCPER** error flag is set. 3. Assertion of the **NFLTA** signal.
Programmable	Yes (blanking time and threshold level).

The integrated overcurrent protection (OCP) function aims at protecting the IGBT from overcurrent and short-circuit conditions. The voltage drop over a sense resistor located on the auxiliary emitter path of the IGBT is monitored via the **OCP** pin while the device issues a PWM ON command. The voltage at **OCP** is externally filtered by an (optional) RC filter and compared to the internal reference threshold (see **Figure 24**). The result of these comparisons is available by reading the **SSTAT2.OCPC** bit.

*Note: **SSTAT2.OCPC** is blanked by the selected blanking time.*

At the beginning of a turn-on sequence, the internal evaluation of the voltage at **OCP** is inhibited for the duration of the blanking time defined by the **SOCP** register. Once the blanking time has elapsed, the voltage at **OCP** is compared to an internal reference voltage.

If the voltage measured at **OCP** is higher than the internal threshold V_{OCP}, an emergency (safe) turn-off sequence is initiated, the **SER.OCPER** bit is set, and a fault notification is issued on the **NFLTA** pin (if there is a transition to another operating state – see **Chapter 1.4.7**). The OCP function is not active while the output stage is in the PWM OFF state. The detection threshold can be selected by configuring the **SCFG.OCPLS** bit field.

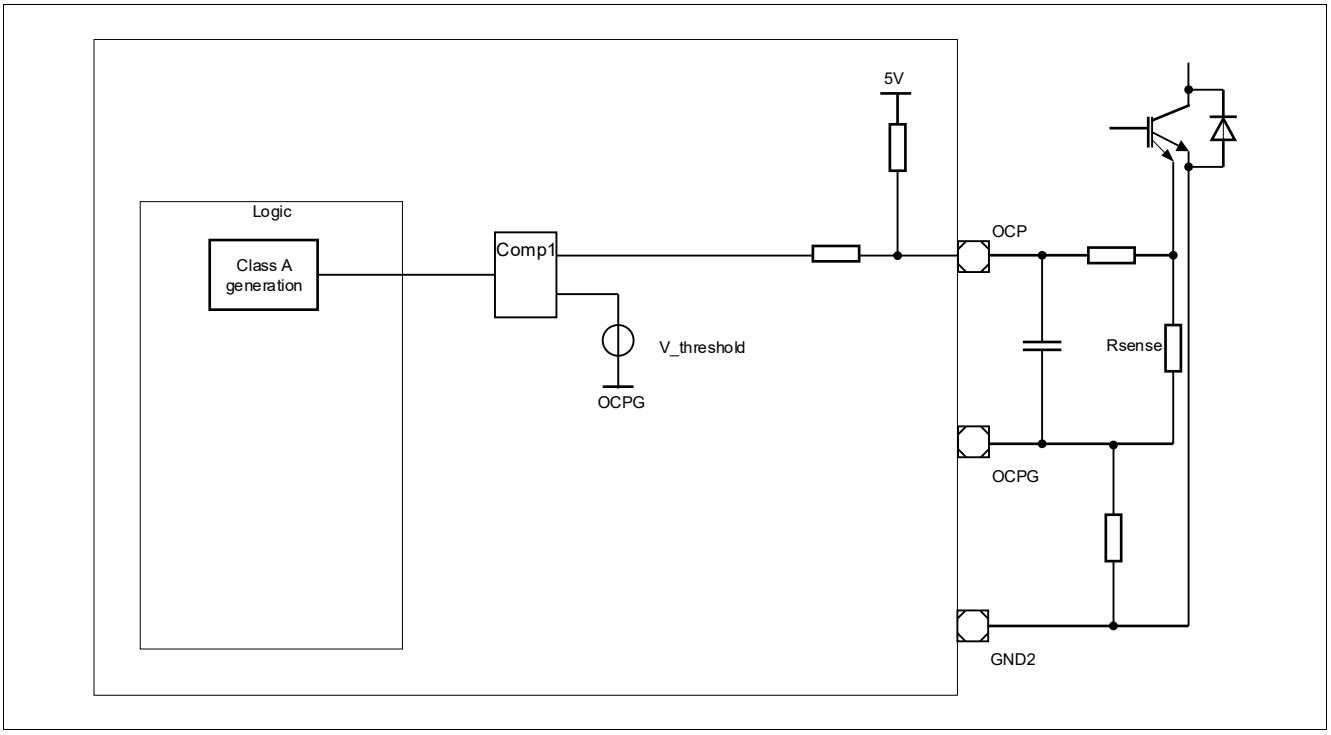


Figure 24 OCP function: Principle of operation

Notes

1. *Both DESAT and OCP protection mechanisms can be used simultaneously.*
2. *When the **OCP** pin is open, the pull-up resistance ensures that an OCP event is generated.*
3. *If TLTO or TLTOFF times are used, these times should be taken into consideration for the blanking time as well to reach valid voltage levels.*

2.2.3 External enable

The external enable functionality is summarized in **Table 21**:

Table 21 External enable function overview

Parameter	Short description
Function	External enable.
Periodicity	Invalid signal on the **EN** pin.
Action in case of failure event	1. Emergency (regular) turn-off sequence. 2. **PER.ENER** error flag is set. 3. Assertion of the **NFLTA** signal.
Programmable	No

The functionality of the signal on the **EN** pin is described in **Chapter 1.4.8**. In case of a valid-to-invalid signal transition, an error is detected. In that case, an emergency (regular) turn-off sequence is initiated, the **PER.ENER** bit is set, and a fault notification is issued on the **NFLTA** pin (if there is a transition to another operating state – see **Chapter 1.4.7**). The current validity state of the signal on **EN** is stored in the **PSTAT2.ENVAL** bit.

2.3 Protection functions: Category B

2.3.1 Power supply voltage monitoring

The power supply voltage monitoring functionality is summarized in **Table 22**:

Table 22 Power supply voltage monitoring overview

Parameter	Short description
Function	Monitoring V_{CC1}, and V_{CC2}.
Periodicity	Continuous.
Action in case of failure event	1. Emergency (regular) turn-off sequence. 2. The **PER**.**RSTP** (UVLO1) or **SER**.**UVLO2ER** (UVLO2) error flags are set. 3. Assertion of signal **NRST/RDY** (UVLO1) or **NFLTB** (UVLO2).
Programmable	Yes (UVLO2 threshold level).

In order to ensure correct switching of the IGBT, the device supports an undervoltage lockout (UVLO) function for V_{CC1} and V_{CC2}.

The V_{CC1} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{CC1} of the primary chip drops below V_{UVLO1L}, an error is detected. In that case, an emergency (regular) turn-off sequence is initiated and the **NRST/RDY** signal goes low. If V_{CC1} subsequently reaches a level higher than V_{UVLO1H}, the error condition is removed and **NRST/RDY** is deasserted. In addition, the **PER**.**RSTP** bit is set.

The V_{CC2} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{CC2} of the secondary chip drops below V_{UVLO2L}, an error is detected. In that case, an emergency (regular) turn-off sequence is initiated, the **SER**.**UVLO2ER** bit is set, and the **NFLTB** signal is activated (if there is a transition to another operating state – see **Chapter 1.4.7**). If V_{CC2} subsequently reaches a level higher than V_{UVLO2H}, the error condition is removed and the device can be reenabled. The level of UVLO2 can be adjusted by configuring **SCFG**.**UVLO2S** to adapt to a lower supply voltage.

The current status of the error detection of UVLO2 mechanism is available in the **SSTAT2**.**UVLO2M** bit.

Note: If V_{CC2} goes below V_{RST2}, the secondary chip is kept in reset.

2.4 Protection functions: Category C

2.4.1 Shoot-through protection function

The shoot-through protection (STP) functionality is summarized in **Table 23**:

Table 23 STP overview

Parameter	Short description
Function	Prevents the high-side and low-side switches from activating simultaneously.
Periodicity	Continuous.
Action in case of failure event	1. The signal at the **INP** pin is inhibited. 2. **PER.STPER** error flag is set.
Programmable	No.
Programmable	Yes (minimum dead time).

With the implemented STP function, a low-side device can monitor the status of its high-side counterpart and vice versa. The input pin **INSTP** provides an input for the PWM signal of the driver's counterpart (**Figure 25**).

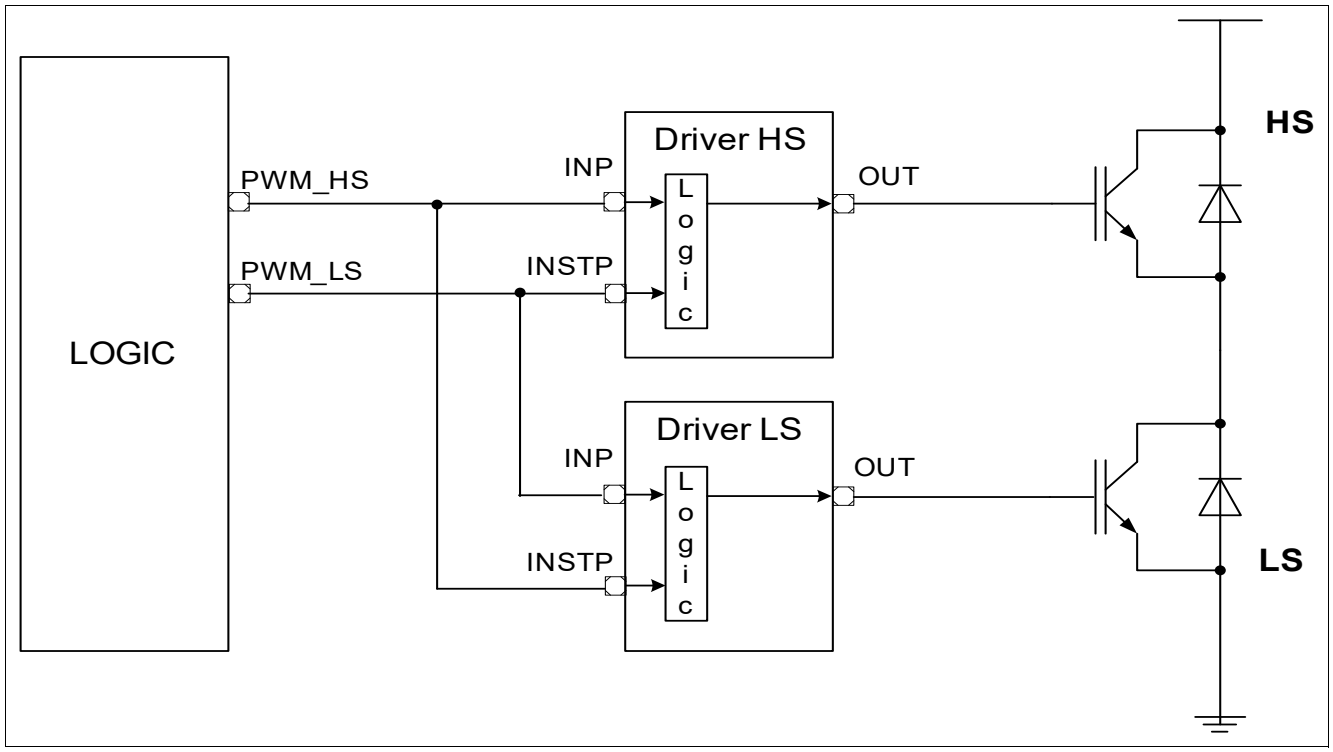


Figure 25 Shoot-through protection: Principle of operation

If one of the driver is in the ON state, the driver's counterpart PWM input is inhibited, preventing it from turning on (see **Chapter 1.4.3**). A minimum dead time is defined by the hardware. This dead time is configurable via the **PCFG2.STPDEL** bit field. Conceptually, the STP aims at providing an additional "line of defense" for the system in case erroneous PWM commands are issued by the primary logic. In normal operation, dead-time management must be performed at the microcontroller level.

If a PWM ON command is received on the **INP** pin during the inhibition time, a failure event is detected. In this case, the high level at **INP** is ignored and the **PER.STPER** bit is set.

Note: An internal filter ensures that STPER is not set for glitches shorter than approximately 50 ns.

The STP can be tested by applying invalid INSTP and INP and then checking the **PSTAT2.STP** bit.
The STP cannot be disabled. However, setting the **INSTP** pin to V_{GND1} in practice deactivates the function.

2.4.2 SPI error detection

The SPI error-detection mechanisms are summarized in **Table 24**:

Table 24 SPI error detection overview

Parameter	Short description
Function	Detection of invalid SPI commands and notification.
Periodicity	Continuous.
Action in case of failure event	**PER.SPIER** flag is set.
Programmable	Yes (parity can be disabled).

For details, see **Chapter 1.4.4.4**.
The SPI error-detection mechanism can be tested by inserting a known error and then verifying that the device's reaction conforms to the specification.

2.5 Protection functions: Category D

2.5.1 Operation in Verification mode and Weak Active mode

Verification mode and Weak Active mode are used to start intrusive test functions on the device and system levels, in order to verify safety relevant functions at runtime. The following functions are supported in the Verification and Weak Active modes:

- Weak turn-on
- Internal clock supervision
- Timing calibration

Intrusive test functions can only be started once a correct sequence of SPI commands has been received after reset. The device prevents intrusive function from being started while it is normally active.

A time-out function ensures that the device transitions from OPM5 or OPM6 to OPM1 after a hardware-defined time.

The verification functions are triggered by setting the corresponding bit fields in **PSCR** or **SSCR** registers while the device is in OPM2. The settings are then activated in OPM5. Only one verification function should be active at a time.

*Note: In OPM5 and OPM6 mode, it is recommended to set the **SSTTOF.STVAL** bit field to 0_H.*

2.5.2 Weak turn-on

The weak turn-on (WTO) corresponds to the operation when OPM6 is active.

The purpose of the weak turn-on functionality is to perform a test of the IGBT, by switching it on with reduced gate voltage, in order to limit the current through it in case of overcurrent conditions. This avoids high currents when the system has no memory of the previous state. **Figure 26** shows a schematic weak turn-on sequence.

The device allows for external booster voltage compensation at the IGBT gate. When the **SCFG.VBEC** bit is cleared, the plateau voltage at **TON** corresponds to the programmed value. When **SCFG.VBEC** is set, V_{BE} (base emitter junction voltage of an internal p-n diode) is substracted from the programmed voltage at **TON** in order to compensate for the V_{BE} of an external booster.

Note: When using WTO, it is recommended to set the plateau of the selected TTOFF (if active) to a smaller voltage than the WTO voltage.

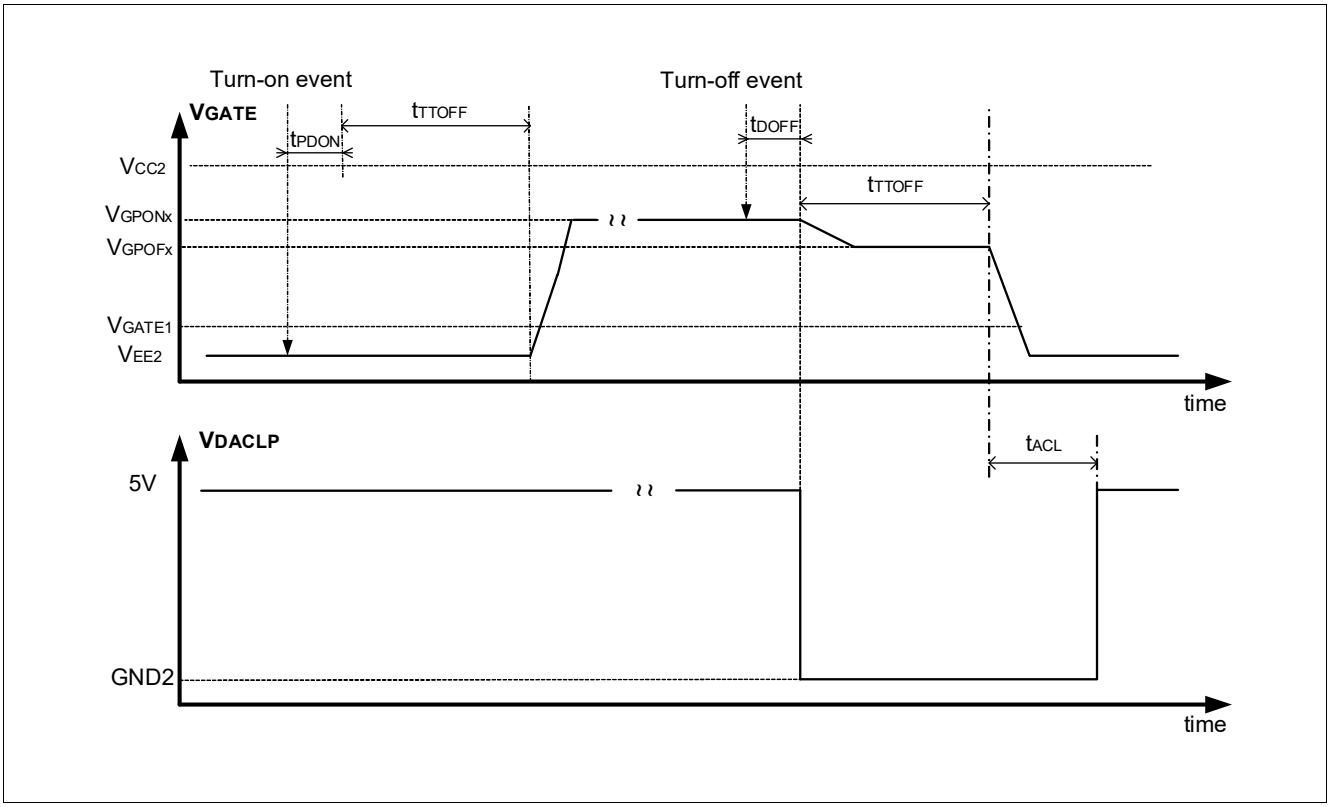


Figure 26 Schematic weak turn-on sequence

Note: The V_{GPOFx} voltages must be smaller than V_{GPONx} to achieve a lower plateau.

2.5.3 Internal clock supervision

The primary clock supervision functionality is summarized in **Table 25**:

Table 25 Primary clock supervision overview

Parameter	Short description
Function	Supervision of the frequencies of OSC1 and SSOSC2.
Periodicity	On request.
Action in case of event	n/a
Programmable	No

The clock supervision function consists on the primary clock supervision and the TCF feature.

Primary clock supervision

This supervision function measures the frequency of the OSC1 oscillator. It works in such a way that the PWM input signal is used to start and stop a counter clocked by OSC1. The function is activated when the device is in OPM5 or OPM6. The counter is incremented for the duration of the high level at the **INP** pin. A high-to-low transition on INP stops the counter and its content is transferred to the **PCS**.**CSP** bit field. A plausibility check can then be made by the logic. In case of a long **INP** pulse, the counter does not overflow but stays at the maximum value until cleared. **PCS**.**CSP** is cleared by setting the **PCTRL**.**CLRP** bit.

The **INP** signal is not issued at the output stage.

Note: OSC2 is indirectly monitored by the lifesign mechanism.

Timing calibration feature

This function measures the frequency of the SSOC2 oscillator. The PWM input signal is used to start and stop a counter clocked by SSOSC2. The function is activated when the device is in OPM6. The counter is incremented for the duration of the high level on the **INP** pin. A high-to-low transition on **INP** stops the counter and its content is transferred to the **SCS**.**SCSS** bit field. A plausibility check can then be made by the logic. In case of a long **INP** pulse, the counter does not overflow but stays at the maximum value until cleared. **SCS**.**SCSS** is cleared by a Reset event or a Verification mode time-out.

The **INP** signal is not issued at the output stage.

3 Registers

3.1 Register descriptions

This chapter describes the internal registers of the device. **Table 27** provides an overview of the implemented registers. The abbreviations shown in **Table 28** are used throughout the section.

Table 26 Register Address Space

Module	Base Address	End Address	Note
SPI	00_H	$1F_H$	

Table 27 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
Register descriptions, Primary register description			
PID	Primary ID Register	00_H	4911_H
PSTAT	Primary Status Register	01_H	$0F54_H$
PSTAT2	Primary Second Status Register	02_H	0010_H
PER	Primary Error Register	03_H	$x80x_H$
PCFG	Primary Configuration Register	04_H	0004_H
PCFG2	Primary Second Configuration Register	05_H	0045_H
PCTRL	Primary Control Register	06_H	$001C_H$
PCTRL2	Primary Second Control Register	07_H	0015_H
PSCR	Primary Supervision Function Control Register	08_H	0001_H
PRW	Primary Read/Write Register	09_H	0001_H
PPIN	Primary Pin Status Register	$0A_H$	$0xxx_H$
PCS	Primary Clock Supervision Register	$0B_H$	0001_H
Register descriptions, Secondary registers description			
SID	Secondary ID Register	10_H	8921_H
SSTAT	Secondary Status Register	11_H	0001_H
SSTAT2	Secondary Second Status Register	12_H	$0xxx_H$
SER	Secondary Error Register	13_H	$xxxx_H$
SCFG	Secondary Configuration Register	14_H	$C111_H$
SCFG2	Secondary Second Configuration Register	15_H	0800_H
SSCR	Secondary Supervision Function Control Register	17_H	0001_H
SDESAT	Secondary DESAT Blanking Time Register	18_H	2000_H
SOCP	Secondary OCP Blanking Time Register	19_H	0001_H
SRTTOF	Secondary Regular TTOFF Configuration Register	$1A_H$	0001_H
SSTTOF	Secondary Safe TTOFF Configuration Register	$1B_H$	2081_H
STTON	Secondary TTON Configuration Register	$1C_H$	0001_H

Table 27 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
SADC	Secondary ADC Result Register	$1D_H$	0001_H
SBC	Secondary ADC Boundary Register	$1E_H$	$FC01_H$
SCS	Secondary Clock Supervision Register	$1F_H$	0001_H

The registers are addressed wordwise.

Table 28 Bit access terminology

Basic access types	Symbol	Description
read/write	rw	This bit or bit field can be written or read.
read	r	This bit or bit field is read only.
write	w	This bit or bit field is write only (read as 0_H).
read/write hardware-affected	rwh	As rw, but the bit or bit field can also be modified by hardware.
read hardware-affected	rh	As r, but the bit or bit field can also be modified by hardware.
sticky	s	Sticky bits have a base state, the so-called reset state (for example, 0) and a modified state (for example, 1). After a system reset, they are always in their reset state. If a write changes the bit to its modified state, it cannot be changed back except through a system reset. It is not possible to return them to their reset state with a write operation. A bit can be sticky in addition to having other attributes (such as "rh").

3.1.1 Primary register description

Primary ID Register

This register contains the identification number of the primary chip version.

PID
Primary ID Register **(00_H)** **Reset value: 4911_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PVERS												Res		LMI	P
r												r		rh	rh

Field	Bits	Type	Description
PVERS	15:4	r	**Primary Chip Identification** The version of the primary chip. This bit field is hardcoded. 491_H **a11**, A11 step.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Status Register

This register contains information on the status of the device.

PSTAT
Primary Status Register **(01_H)** **Reset Value: $0F54_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				ERR	GPONP			ACT	SRDY	AVFP	GPOFP			LMI	P
r				rh	rh			rh	rh	rh	rh			rh	rh

Field	Bits	Type	Description
Res	15:12	r	**Reserved** Read as 0_B.
ERR	11	rh	**Error Status** The OR-combination of all bits of the **PER** register. 0_B **noError**, No error has been detected. 1_B **error**, An error has been detected.
GPONP	10:8	rh	**Gate TTON Plateau Level Configuration Status** The latest turn-on plateau level configuration request (WTO, TTON) received by the primary side via the SPI interface. The encoding is identical to the **PCTRL.GPON** bit field.
ACT	7	rh	**Active State Status** Whether the device is in Active mode (OPM4). 0_B **notActive**, The device is not in Active mode. 1_B **active**, The device is in Active mode.
SRDY	6	rh	**Secondary Ready Status** Whether the secondary chip is ready for operation. 0_B **notReady**, Secondary chip is not ready. 1_B **ready**, Secondary chip is ready.
AVFP	5	rh	**ADC Result Valid Flag** Whether a valid ADC result is available in **SADC**. *Note: This bit field is a mirror of **SADC.AVFS***
GPOFP	4:2	rh	**Gate Regular TTOFF Plateau Level Configuration Status** The latest turn-off plateau level configuration request (regular TTOFF) received by the primary side via the SPI interface. Coding is identical to the **PCTRL2.GPOF** bit field.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.

Field	Bits	Type	Description
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Second Status Register

This register contains information on the status of the device.

PSTAT2
Primary Second Status Register **(02_H)** **Reset value: 0010_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				AXVP	STP	FLTBP	FLTAP	OPMP			FLTB	FLTA	ENVAL	LMI	P
r				rh	rh	rh	rh	rh			rhs	rhs	rh	rh	rh

Field	Bits	Type	Description
Res	15:12	r	**Reserved** Read as 0_B.
AXVP	11	rh	**ADC Under- Or Overvoltage Error Status** Whether a violation of a boundary condition was detected. *Note: This bit is a mirror of the OR-combination of the **SADC.AUVS** and **SADC.AOVS** bits.* 0_B **noError**, No error condition is being detected. 1_B **error**, An error condition is being detected
STP	10	rh	**Shoot-Through Protection Status** Whether the inhibition time for the shoot-through protection is active (for example, to inhibit a PWM rising edge). 0_B **inhibitionNotActive**, STP inhibition is not active. 1_B **inhibitionActive**, STP inhibition is active.
FLTBP	9	rh	**Class B Event Status** Whether the conditions for a Class B event are met. 0_B **noError**, The conditions for a Class B event are not present. 1_B **error**, The conditions for a Class B event are present.
FLTAP	8	rh	**Class A Event Status** This bit indicates if the conditions leading to a Class A event are met. 0_B **noError**, The conditions for a Class A event are not present. 1_B **error**, The conditions for a Class A event are present.

Field	Bits	Type	Description
OPMP	7:5	rh	**Operating Mode** The active operating mode. 000_B **opm0**, Mode OPM0 is active . 001_B **opm1**, Mode OPM1 is active . 010_B **opm2**, Mode OPM2 is active. 011_B **opm3**, Mode OPM3 is active. 100_B **opm4**, Mode OPM4 is active. 101_B **opm5**, Mode OPM5 is active. 110_B **opm6**, Mode OPM6 is active. 111_B Reserved.
FLTB	4	rhs	**NFLTB Pin Driver Request** The output state that is being driven by the device on the **NFLTB** pin. This bit is sticky. 0_B **tristate**, **NFLTB** is in tristate. 1_B **lowLevel**, A low level is present on **NFLTB**.
FLTA	3	rhs	**NFLTA Pin Driver Request** The output state that is being driven by the device on the **NFLTA** pin. This bit is sticky. 0_B **tristate**, **NFLTA** is in tristate. 1_B **lowLevel**, A low level is present on **NFLTA**.
ENVAL	2	rh	**EN Valid Status** Whether the signal received on the **EN** pin is valid. 0_B **notValid**, An invalid signal has been detected. 1_B **valid**, A valid signal has been detected.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Error Register

This register provides information on the error status of the device.

PER
Primary Error Register **(03_H)** **Reset Value: $x80x_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			RSTEP	RSTP	ENER	STPER	SPIER	Res	ADER	Res			CERP	LMI	P
r			rhs	rhs	rhs	rhs	rhs	rh	rhs	r			rhs	rh	rh

Field	Bits	Type	Description
Res	15:13	r	**Reserved** Read as 0_B.
RSTEP	12	rhs	**Primary External Hard Reset flag** Whether a Reset event has been detected on the primary chip due to the activation of the **NRST/RDY** pin. This bit is sticky. 0_B **notSet**, No external hard-Reset event has been detected. 1_B **set**, An external hard-Reset event has been detected.
RSTP	11	rhs	**Primary Reset Flag** Whether a Reset event has been detected on the primary chip. This bit is sticky. 0_B **notSet**, No Reset event has been detected. 1_B **set**, A Reset event has been detected.
ENER	10	rhs	**EN Signal Invalid Flag** Whether an invalid-to-valid transition on the **EN** signal has been detected. This bit is sticky. 0_B **notSet**, No valid-to-invalid transition has been detected. 1_B **set**, A valid-to-invalid transition has been detected.
STPER	9	rhs	**Shoot-Through Protection Error Flag** Whether a shoot-through protection error event has been detected. This bit is sticky. *Note: This bit cannot be cleared while an error condition is present (that is, while the **PSTAT2.STP** bit is set).* 0_B **notSet**, No event has been detected. 1_B **set**, An event has been detected.

Field	Bits	Type	Description
SPIER	8	rhs	**SPI Error Flag** Whether an SPI error event has been detected. This bit is sticky. 0_B **notSet**, No error event has been detected. 1_B **set**, An error event has been detected.
Res	7	rh	**Reserved** This bit field is reserved.
ADER	6	rhs	**ADC Error Flag** Whether a boundary condition violation has been detected. This bit is sticky. *Note: This bit cannot be cleared while an error condition is active (that is, while the **PSTAT2.AXVP** bit is set).* 0_B **notSet**, No error condition has been detected. 1_B **set**, An error condition has been detected has been detected.
Res	5:3	r	**Reserved** Read as 0_B.
CERP	2	rhs	**Primary Communication Error Flag** Whether a loss of communication[1)] with the secondary chip has been detected by the primary chip. This bit is sticky. *Note: This bit cannot be cleared while an error condition is active (that is, while the **PSTAT2.SRDY** bit is cleared).* 0_B **notSet**, No loss-of-communication event has been detected. 1_B **set**, A loss-of-communication event has been detected.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

1) This bit is not set after a Reset event.

Registers

Primary Configuration Register

This register is used to configure the device.

PCFG
Primary Configuration Register **(04_H)** **Reset Value: 0004_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res									ADTEN	ADAEN	Res		PAREN	LMI	P
r									rw	rw	rw		rw	rh	rh

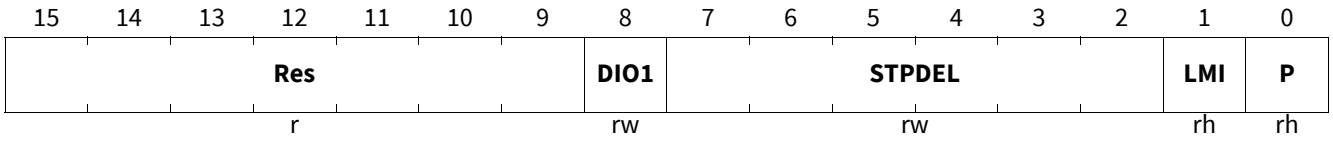
Field	Bits	Type	Description
Res	15:7	r	**Reserved** Read as 0_B.
ADTEN	6	rw	**ADC Trigger Input Enable** Whether an ADC trigger is generated by a transition from low to high on the **ADCT** pin. 0_B **disabled**, **ADCT** pin is disabled. 1_B **enabled**, **ADCT** pin is enabled.
ADAEN	5	rw	**NFLTA Pin Activation on Boundary Check Event Enable** Whether the **NFLTA** signal is activated by a transition from 0_B to 1_B of the **PSTAT2**. **AXVP** bit. 0_B **disabled**, **NFLTA** activation is disabled. 1_B **enabled**, **NFLTA** activation is enabled
Res	4:3	rw	**Reserved** This bit field is reserved and shall be written with 0_B.
PAREN	2	rw	**SPI Parity Enable** Whether the SPI parity error detection is active (reception only). 0_B **disabled**, Parity checking is disabled. 1_B **enabled**, Parity checking is enabled.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Second Configuration Register

This register is used to configure the device.

PCFG2
Primary Second Configuration Register **(05_H)** **Reset Value: 0045_H**



Field	Bits	Type	Description
Res	15:9	r	**Reserved** Read as 0_B.
DIO1	8	rw	**DIO1 Pin Mode** The direction of the **DIO1** pin. 0_B **input**, **DIO1** is an input. 1_B **output**, **DIO1** is an output.
STPDEL	7:2	rw	**Shoot-Through Protection Delay** The dead time for the shoot-through protection (as a number of OSC1 clock cycles). 00_H **0**, 0 clock cycles. 01_H **01**, 1 clock cycle. ... $3F_H$ **3F**, 63 clock cycles.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Control Register

This register is used to control the device at runtime.

PCTRL
Primary Control Register **(06_H)** **Reset Value: $001C_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res									CLRS	CLRP	GPON			LMI	P
r									rwh	rwh	rw			rh	rh

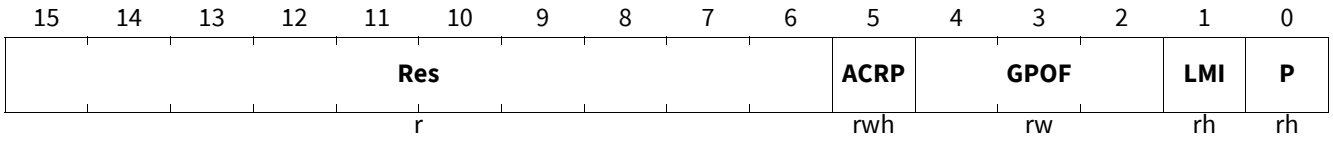
Field	Bits	Type	Description
Res	15:7	r	**Reserved** Read as 0_B.
CLRS	6	rwh	**Clear Secondary Sticky Bits** Setting this bit clears the sticky bits on the secondary side. This bit is automatically cleared by hardware. 0_B **noAction**, No action. 1_B **clear**, Clear sticky bits.
CLRP	5	rwh	**Clear Primary Sticky Bits** Setting this bit clears the sticky bits on the primary side. This bit is automatically cleared by hardware. 0_B **noAction**, No action. 1_B **clear**, Clear sticky bits and deassert the **NFLTA** and **NFLTB** signals.
GPON	4:2	rw	**Gate TTON Plateau Level** The plateau voltage during weak turn-on and two-level turn-on. For the voltage levels see **Table 45**. 0_H **gpon0**, V_{GPON0} selected. 1_H **gpon1**, V_{GPON1} selected. 2_H **gpon2**, V_{GPON2} selected. 3_H **gpon3**, V_{GPON3} selected. 4_H **gpon4**, V_{GPON4} selected. 5_H **gpon5**, V_{GPON5} selected. 6_H **gpon6**, V_{GPON6} selected. 7_H **gpon6WtoOrHardSwitching**, V_{GPON6} (WTO) or hard switching (TTON).
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Second Control Register

This register is used to control the device at runtime.

PCTRL2
Primary Second Control Register **(07_H)** **Reset Value: 0015_H**

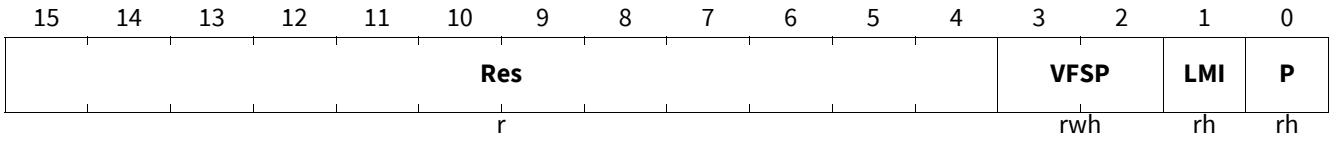


Field	Bits	Type	Description
Res	15:6	r	**Reserved** Read as 0_B.
ACRP	5	rwh	**ADC Conversion Request** This bit triggers an ADC conversion. It can be set by a direct write or via the **ADCT** pin. 0_B **none**, No conversion request is pending. 1_B **pending**, A conversion request is pending.This bit is automatically cleared by hardware.
GPOF	4:2	rw	**Gate Regular TTOFF Plateau Level** The two-level turn-off plateau voltage (regular turn-off). For voltage levels see **Table 45**. 0_H **gpof0**, V_{GPOF0} selected. 1_H **gpof1**, V_{GPOF1} selected. 2_H **gpof2**, V_{GPOF2} selected. 3_H **gpof3**, V_{GPOF3} selected. 4_H **gpof4**, V_{GPOF4} selected. 5_H **gpof5**, V_{GPOF5} selected. 6_H **gpof6**, V_{GPOF6} selected. 7_H **gpof7**, V_{GPOF7} selected.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Primary Supervision Function Control Register

This register is used to trigger the verification functions on the primary side.

PSCR
Primary Supervision Function Control Register (08$_H$) **Reset Value: 0001$_H$**



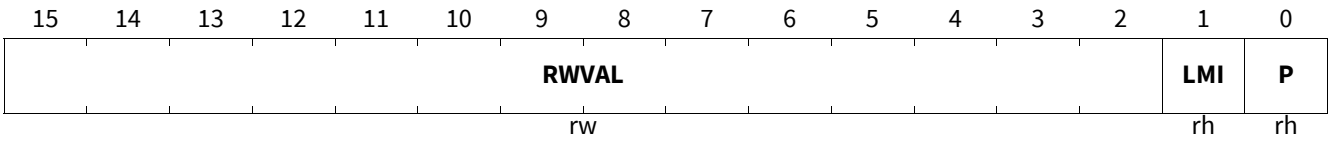
Field	Bits	Type	Description
Res	15:4	r	**Reserved** Read as 0_B.
VFSP	3:2	rwh	**Primary Verification Function** This bit field activates the primary verification functions. *Note: The selection defined by this bit field is only effective when the device enters OPM5. This bit field is automatically cleared when entering OPM1.* 00_B **disabled**, No function activated. 01_B Reserved. 10_B **primaryClockSupervision**, Primary clock supervision is active. 11_B Reserved.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Read/Write Register

This register provides a readable and writable address space for data integrity tests at runtime. It is not associated with any hardware functions.

PRW
Primary Read/Write Register **(09_H)** **Reset Value: 0001_H**



Field	Bits	Type	Description
RWVAL	15:2	rw	**Data Integrity Test Register** This bit field is ignored by the device.
LMI	1	rh	**Last Message Invalid Flag** Whether the last-received SPI message was correctly processed by the device. 0_B **noError**, Most recent message was processed correctly. 1_B **error**, Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Pin Status Register

This register provides status information on the I/Os of the primary chip.

PPIN
Primary Pin Status Register **($0A_H$)** **Reset Value: $0xxx_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							DIO1L	ADCTL	NFLTBL	NFLTAL	ENL	INSTPL	INPL	LMI	P
r							rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Res	15:9	r	**Reserved** Read as 0_B.
DIO1L	8	rh	**DIO1 Pin Level** The logical level read on the **DIO1** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.
ADCTL	7	rh	**ADC Trigger Input Level** The logical level read on the **ADCT** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.
NFLTBL	6	rh	**NFLTB Pin Level** The logical level read on the **NFLTB** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.
NFLTAL	5	rh	**NFLTA Pin Level** The logical level read on the **NFLTA** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.
ENL	4	rh	**EN Pin Level** The logical level read on the **EN** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.
INSTPL	3	rh	**INSTP Pin Level** The logical level read on the **INSTP** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.
INPL	2	rh	**INP Pin Level** The logical level read on the **INP** pin. 0_B **low**, Low level is detected. 1_B **high**, High level is detected.

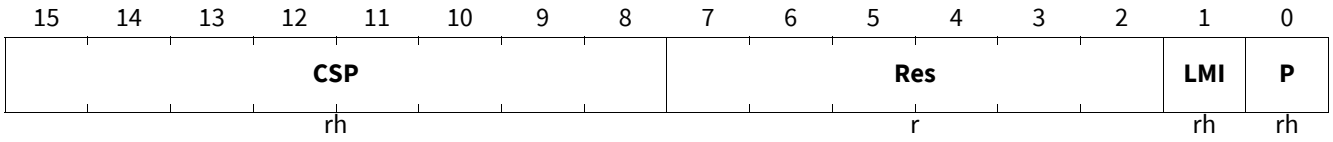
Field	Bits	Type	Description
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B **noError**, Most recent message was processed correctly. 1_B **error**, Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Primary Clock Supervision Register

This register contains the results of the primary clock supervision function.

PCS
Primary Clock Supervision Register **($0B_H$)** **Reset Value: 0001_H**



Field	Bits	Type	Description
CSP	15:8	rh	**Primary Clock Supervision** This bit field is written by hardware when the primary clock supervision function is active and contains the number of measured OSC1 clock cycles. *Note: This bit field can be cleared by setting the **PCTRL.CLRP** bit.*
Res	7:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

3.1.2 Secondary registers description

Secondary ID Register

This register contains the identification number of secondary chip version.

SID
Secondary ID Register **(10_H)** **Reset Value: 8921_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVERS												Res		LMI	P
r												r		rh	rh

Field	Bits	Type	Description
SVERS	15:4	r	**Secondary Chip Identification** The version number of the secondary chip. This bit field is hard-coded.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary Status Register

This register contains information on the status of the device.

SSTAT
Secondary Status Register **(11_H)** **Reset Value: 0001_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**Res**				**DBG**	**Res**					**PWM**	**Res**		**LMI**	**P**
rh	r				rh	rh					rh	r		rh	rh

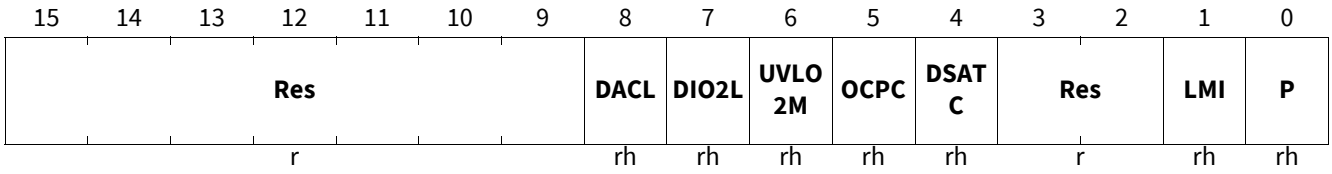
Field	Bits	Type	Description
Res	15	rh	**Reserved**
Res	14:11	r	**Reserved** Read as 0_B.
DBG	10	rh	**Debug Mode Active Flag** Whether the Debug mode is active. 0_B **notSet**, Debug mode is not active. 1_B **set**, Debug mode is active.
Res	9:5	rh	**Reserved**
PWM	4	rh	**PWM Command Status** The status of the PWM command received from the primary side. 0_B **off**, PWM OFF command was detected. 1_B **on**, PWM ON command was detected.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary Second Status Register

This register contains information on the status of the device.

SSTAT2
Secondary Second Status Register **(12_H)** **Reset Value: $0xxx_H$**



Field	Bits	Type	Description
Res	15:9	r	**Reserved** Read as 0_B.
DACL	8	rh	**DACLP Pin output level** The level read at the **DACLP** pin. 0_B **low**, **DACLP** level is low. 1_B **high**, **DACLP** level is high.
DIO2L	7	rh	**DIO2 Pin Level** The level read at the **DIO2** pin. 0_B **low**, **DIO2** level is low. 1_B **high**, **DIO2** level is high.
UVLO2M	6	rh	**UVLO2 Event** The result of the UVLO2 monitoring function. 0_B **noError**, No failure condition was detected. 1_B **error**, A failure condition was detected.
OCPC	5	rh	**OCP Comparator Result** The (blanked) output of the first comparator of the OCP function. 0_B **belowThreshold**, **OCP** voltage is below the internal threshold. 1_B **aboveThreshold**, **OCP** voltage is above the internal threshold.
DSATC	4	rh	**DESAT Comparator Result** The output of the comparator of the DESAT function. 0_B **belowThreshold**, **DESAT** voltage is below the internal threshold. 1_B **aboveThreshold**, **DESAT** voltage is above the internal threshold.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.

Field	Bits	Type	Description
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary Error Register

This register provides information on the error status of the device.

SER
Secondary Error Register **(13_H)** **Reset Value: $xxxx_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSTS	OCPER	DESATER	UVLO2ER	Res		VMTO	Res		AOVER	AUVER	CERS	Res		LMI	P
rhs	rhs	rhs	rhs	r		rhs	r		rhs	rhs	rhs	r		rh	rh

Field	Bits	Type	Description
RSTS	15	rhs	**Secondary Hard-Reset Flag** Whether a hard Reset event has been detected on the secondary chip (due to a V_{CC2} power-up). This bit is sticky. 0_B **notSet**, No hard-Reset event has been detected. 1_B **set**, A hard-Reset event has been detected.
OCPER	14	rhs	**OCP Error Flag** Whether an OCP event has been detected. This bit is sticky. *Note: This bit cannot be cleared while an error condition is active (that is, while the **SSTAT2.OCPC** bit is set).* 0_B **notSet**, No event has been detected. 1_B **set**, An event has been detected.
DESATER	13	rhs	**DESAT Error Flag** Whether a DESAT event has been detected. This bit is sticky. 0_B **notSet**, No event has been detected. 1_B **set**, An event has been detected.
UVLO2ER	12	rhs	**UVLO2 Error Flag** Whether an undervoltage lockout event (on V_{CC2}) has been detected. This bit is sticky. *Note: This bit cannot be cleared while an error condition is active (that is, while the **SSTAT2.UVLO2M** bit is set).* 0_B **notSet**, No event has been detected. 1_B **set**, An event has been detected.
Res	11:10	r	**Reserved** Read as 0_B.

Field	Bits	Type	Description
VMTO	9	rhs	**Verification Mode Time-Out Event Flag** Whether a time-out event in Verification mode has been detected. This bit is sticky. 0_B **notSet**, No event has been detected. 1_B **set**, An event has been detected.
Res	8:7	r	**Reserved** Read as 0_B.
AOVER	6	rhs	**ADC Overvoltage Error Flag** Whether an overvoltage boundary violation was detected. This bit is sticky. 0_B **notSet**, No error condition has been detected. 1_B **set**, An error condition has been detected.
AUVER	5	rhs	**ADC Undervoltage Error Flag** Whether an undervoltage boundary violation was detected. This bit is sticky. 0_B **notSet**, No error condition has been detected. 1_B **set**, An error condition has been detected.
CERS	4	rhs	**Communication Error Secondary Flag** Whether a loss of communication with the primary chip has been detected by the secondary chip. This bit is sticky. 0_B **notSet**, No loss of communication has been detected. 1_B **set**, A loss of communication has been detected.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary Configuration Register

This register is used to configure the device.

SCFG
Secondary Configuration Register **(14_H)** **Reset Value: $C111_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACLC		OCPLS	UVLO2S	DSATLS	TOSEN	PSEN	DSTCEN	DIO2C		CFG2	VBEC	Res		LMI	P
rw		rw	rw	rw	rw	rw	rw	rw		rwh	rw	r		rh	rh

Field	Bits	Type	Description
DACLC	15:14	rw	**DACLP Pin clamping output** The function of the **DACLP** pin. 00_B **low**, The pin delivers a constant low level. 01_B **high**, The pin delivers a constant high level. 10_B **daclpSafe**, **DACLP** function selected. The signal is active only in case of a safe turn-off sequence. 11_B **daclpRegular**, **DACLP** function selected. The signal is active for both regular and safe turn-off sequences.
OCPLS	13	rw	**OCP Threshold Level** The threshold level of the OCP function. 0_B **vocp0**, Threshold V_{OCP0} selected. 1_B **vocp1**, Threshold V_{OCP1} selected.
UVLO2S	12	rw	**UVLO2 Threshold Level** The threshold level of the UVLO2 function. 0_B **uvlo2l0**, Threshold $V_{UVLO2L0}$ selected. 1_B **uvlo2l1**, Threshold $V_{UVLO2L0}$ selected.
DSATLS	11	rw	**DESAT Threshold Level** The threshold level of the DESAT function. 0_B **vdesat0**, Threshold V_{DESAT0} selected. 1_B **vdesat1**, Threshold V_{DESAT1} selected.
TOSEN	10	rw	**Verification Mode Time-Out Duration** The duration of the Verification mode time-out. 0_B **regular**, Regular time-out value (typ. 15 ms). 1_B **slow**, Long time-out value (typ. 60 ms).
PSEN	9	rw	**Pulse Suppressor Enable** Whether the internal pulse suppressor is enabled. 0_B **disabled**, Pulse suppressor is disabled. 1_B **enabled**, Pulse suppressor is enabled.
DSTCEN	8	rw	**DESAT Clamping Enable** Whether the internal clamping (to GND2) of the DESAT pin during PWM OFF commands is enabled. 0_B **disabled**, DESAT clamping is disabled. 1_B **enabled**, DESAT clamping is enabled.

Field	Bits	Type	Description
DIO2C	7:6	rw	**DIO2 Pin Mode** The function of the **DIO2** pin. 00_B **input**, **DIO2** is an input. 01_B **output**, **DIO2** is an output transferring the signal from **DIO1**. 10_B Reserved. 11_B Reserved.
CFG2	5	rwh	**Secondary Advanced Configuration Enable** Whether write accesses to the **SCFG2** and **SBC** registers are enabled. This bit is automatically cleared when mode OPM2 is left. 0_B **disabled**, Write accesses to **SCFG2** and **SBC** are discarded. 1_B **enabled**, Write accesses to **SCFG2** and **SBC** are executed normally.
VBEC	4	rw	**VBE Compensation Enable** Whether the V_{BE} compensation of the TTOFF, TTON, and WTO plateau levels is enabled. 0_B **disabled**, V_{BE} Compensation is disabled. 1_B **enabled**, V_{BE} Compensation is enabled.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Secondary Second Configuration Register

This register is used to configure the device. It can only be written if **SCFG.CFG2** is set.

SCFG2
Secondary Second Configuration Register **(15_H)** **Reset Value: 0800_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCEN	ACAEN	ACSS	AOS			AGS		ATS		PWMD		Res		LMI	P
rw	rw	rw	rw			rw		rw		rw		r		rh	rh

Field	Bits	Type	Description
ADCEN	15	rw	**ADC Enable** Whether the ADC function is enabled: 0_B **disabled**, ADC disabled. 1_B **enabled**, ADC enabled.
ACAEN	14	rw	**ADC Class A Event Enable** Whether boundary check violations generate Class A events: 0_B **disabled**, No Class A event is generated. 1_B **enabled**, A Class A event is generated.
ACSS	13	rw	**ADC Current Source** Whether the internal current source is enabled. 0_B **disabled**, Current source is disabled. 1_B **enabled**, Current source I_{AIPCS} is selected.
AOS	12:10	rw	**ADC Offset** The offset value of the ADC. For voltage levels see **Table 51**. 0_H **ofst0**, V_{OFF0} selected. 1_H **ofst1**, V_{OFF1} selected. 2_H **ofst2**, V_{OFF2} selected. 3_H **ofst3**, V_{OFF3} selected. 4_H **ofst4**, V_{OFF4} selected. 5_H Reserved. 6_H Reserved. 7_H Reserved.
AGS	9:8	rw	**ADC Gain** The gain value of the ADC. 00_B **gain0**, $GAIN_0$ selected. 01_B **gain1**, $GAIN_1$ selected. 10_B **gain2**, $GAIN_2$ selected. 11_B **gain3**, $GAIN_3$ selected.

Field	Bits	Type	Description
ATS	7:6	rw	**ADC Secondary Trigger Mode** The trigger mode of the ADC on the secondary side. 00_B **disabled**, No secondary trigger source active. 01_B **periodic**, Periodic trigger selected. 10_B **risingPwm**, PWM trigger selected (rising edge). 11_B **fallingPwm**, PWM trigger selected (falling edge).
PWMD	5:4	rw	**ADC PWM Trigger Delay** The offset value of the delay between PWM edge and ADC when the PWM Trigger mode is selected. 00_B **delay0**, 16 OSC2 cycles selected. 01_B **delay1**, 32 OSC2 cycles selected. 10_B **delay2**, 48 OSC2 cycles selected. 11_B **delay3**, 64 OSC2 cycles selected.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary Supervision Function Control Register

This register is used to trigger the verification functions on the secondary side.

SSCR

Secondary Supervision Function Control Register(17_H) **Reset Value: 0001_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res										VFS2		Res		LMI	P
r										rwh		r		rh	rh

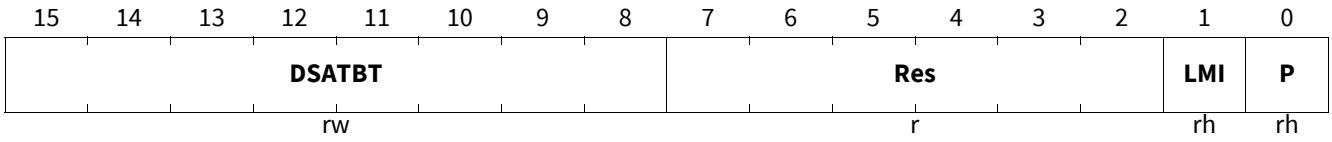
Field	Bits	Type	Description
Res	15:6	r	**Reserved** Read as 0_B.
VFS2	5:4	rwh	**Secondary Verification Function** Whether the secondary verification function is activated. All bit combinations that are not listed below are reserved. *Note: The selection defined by this bit field is only effective when the device enters OPM5. This bit field is automatically cleared when entering OPM1.* 00_B **disabled**, No secondary verification function activated. 01_B **tcf**, TCF function active.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary DESAT Blanking Time Register

This register configures the blanking time of the DESAT function.

SDESAT
Secondary DESAT Blanking Time Register (18_H) Reset Value: 2000_H



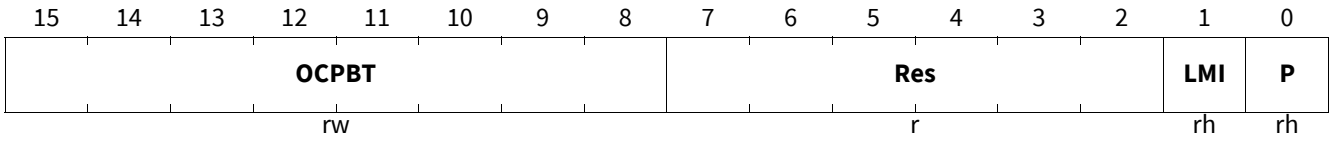
Field	Bits	Type	Description
DSATBT	15:8	rw	**DESAT Blanking Time** The blanking time of the DESAT function (in OSC2 clock cycles). A minimal value of at least A_H has to be programmed.
Res	7:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary OCP Blanking Time Register

This register configures the blanking time of the OCP function.

SOCP
Secondary OCP Blanking Time Register **(19_H)** **Reset Value: 0001_H**



Field	Bits	Type	Description
OCPBT	15:8	rw	**OCP Blanking Time** The blanking time of the OCP function (in OSC2 clock cycles). Writing 0_H to this field deactivates the digital blanking-time generation. If used, a minimal value of at least A_H has to be programmed.
Res	7:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Secondary Regular TTOFF Configuration Register

This register contains the configuration of the TTOFF function for regular turn-off.

SRTTOF

Secondary Regular TTOFF Configuration Register($1A_H$) **Reset Value: 0001_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTVAL								Res						LMI	P
rw								r						rh	rh

Field	Bits	Type	Description
RTVAL	15:8	rw	**Gate Regular TTOFF delay** The TTOFF delay for a regular turn-off (in SSOSC2 clock cycles). Writing 00_H to this field deactivates the TTOFF function for regular turn-off. If used, a value greater then 02_H has to be programmed.
Res	7:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary Safe TTOFF Configuration Register

This register contains the configuration of the TTOFF function for safe turn-off.

SSTTOF
Secondary Safe TTOFF Configuration Register (1B$_H$) **Reset Value: 2081$_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STVAL								GPS			Res			LMI	P
rw								rw			r			rh	rh

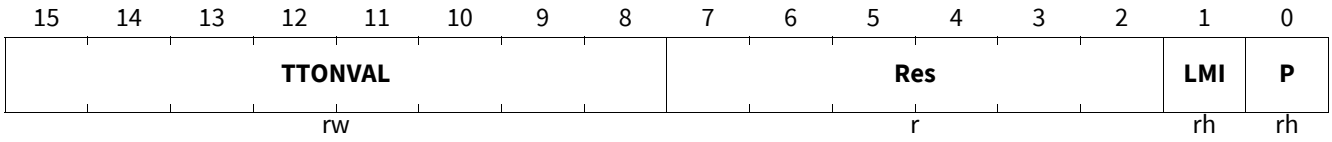
Field	Bits	Type	Description
STVAL	15:8	rw	**Gate Safe TTOFF delay** The TTOFF delay for a safe turn-off (in OSC2 clock cycles). Writing 00$_H$ to this field deactivates the TTOFF function for regular turn-off. If used, a minimal value of at least 0A$_H$ has to be programmed. **Notes** 1. *In OPM5 and OPM6, it is recommended to have this bit field set to 0$_H$.* 2. *In OPM4, this bit field should be programmed with a higher value than **SRTTOF.RTVAL**.*
GPS	7:5	rw	**Gate Safe TTOFF Plateau Voltage** The TTOFF plateau voltage for safe turn-off sequences. The encoding is identical to **PCTRL2.GPOF**. *Note: In OPM4, this bit field should be programmed with a value smaller than or equal to **PCTRL2.GPOF**.*
Res	4:2	r	**Reserved** Read as 0$_B$.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0$_B$ Most recent message was processed correctly. 1$_B$ Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary TTON Configuration Register

This register contains the configuration of the TTON function for regular turn-on.

STTON
Secondary TTON Configuration Register **($1C_H$)** **Reset Value: 0001_H**



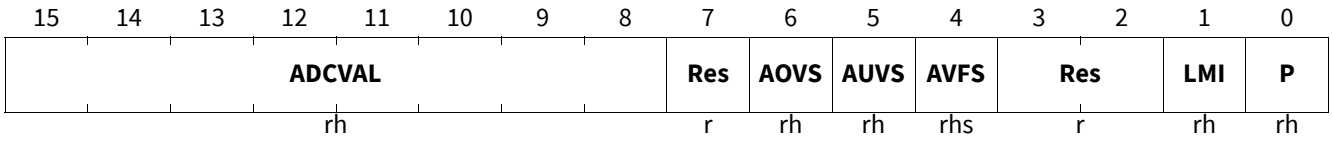
Field	Bits	Type	Description
TTONVAL	15:8	rw	**Gate TTON Delay** The TTON delay (in SSOSC2 clock cycles). Writing 00_H to this field deactivates the TTON function. If used, a minimal value of at least A_H has to be programmed.
Res	7:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Secondary ADC Result Register

This register contains the status of the ADC channel.

SADC

Secondary ADC Result Register **($1D_H$)** **Reset Value: 0001_H**



Field	Bits	Type	Description
ADCVAL	15:8	rh	**ADC Result** The results of the last conversion of the ADC channel. It is automatically updated every time a new conversion result is available.
Res	7	r	**Reserved** Read as 0_B.
AOVS	6	rh	**ADC Overvoltage Error Status** Whether a boundary condition violation is occurring (overvoltage). 0_B **noError**, No error condition is being detected. 1_B **error**, An error condition is being detected.
AUVS	5	rh	**ADC Undervoltage Error Status** Whether a boundary condition violation is occurring (undervoltage). 0_B **noError**, No error condition is being detected. 1_B **error**, An error condition is being detected.
AVFS	4	rhs	**ADC Result Valid Flag** Whether a new conversion result is available. This bit is set every time the **ADCVAL** bit field is updated with a new value. This bit is sticky. 0_B **notValid**, No conversion result is available. 1_B **valid**, A conversion result is available.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Registers

Secondary ADC Boundary Register

This register contains the values for the ADC boundary check. It can only be written if **SCFG.CFG2** is set.

SBC

Secondary ADC Boundary Register **($1E_H$)** **Reset Value: $FC01_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCB1B						**LCB1A**						**Res**		**LMI**	**P**
rw						rw						r		rh	rh

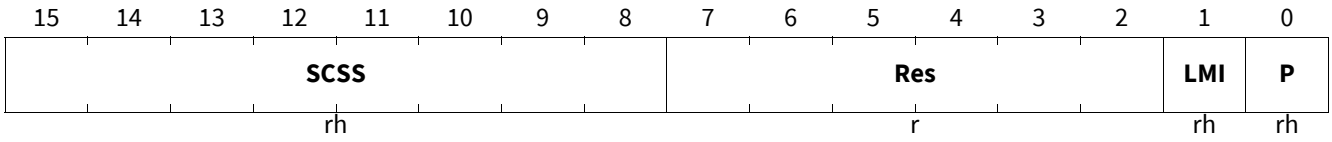
Field	Bits	Type	Description
LCB1B	15:10	rw	**ADC Limit Checking Boundary B** Second boundary used for the limit-checking mechanism. Should contain the upper limit.
LCB1A	9:4	rw	**ADC Limit Checking Boundary A** First boundary used for the limit-checking mechanism. Should contain the lower limit.
Res	3:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

Secondary Clock Supervision Register

This register contains the results of the secondary clock supervision function.

SCS

Secondary Clock Supervision Register **($1F_H$)** **Reset Value: 0001_H**



Field	Bits	Type	Description
SCSS	15:8	rh	**Secondary Supervision Oscillator Clock Cycles** The number of measured start-stop oscillator clock cycles. This field is written by the hardware's TCF function.
Res	7:2	r	**Reserved** Read as 0_B.
LMI	1	rh	**Last Message Invalid Notification** Whether the last-received SPI message was correctly processed by the device. 0_B Most recent message was processed correctly. 1_B Most recent message was discarded.
P	0	rh	**Parity Bit** Odd parity bit.

3.1.3 Read/write address ranges

Table 29 summarizes which register can be accessed with READ commands in the different operating modes.

Table 29 Read access validity

	OPM0, OPM1	OPM2	OPM3	OPM4	OPM5	OPM6
PID	X	X	X	X	X	X
PSTAT	X	X	X	X	X	X
PSTAT2	X	X	X	X	X	X
PER	X	X	X	X	X	X
PCFG	X	X	X	X	X	X
PCFG2	X	X	X	X	X	X
PCTRL	X	X	X	X	X	X
PCTRL2	X	X	X	X	X	X
PSCR	X	X	X	X	X	X
PRW	X	X	X	X	X	X
PPIN	X	X	X	X	X	X
PCS	X	X	X	X	X	X
SID	X	X	X	X 1)	X	X 1)
SSTAT	X	X	X	X 1)	X	X 1)
SSTAT2	X	X	X	X 1)	X	X 1)
SER	X	X	X	X 1)	X	X 1)
SCFG	X	X	X	X 1)	X	X 1)
SCFG2	X	X	X	X 1)	X	X 1)
SSCR	X	X	X	X 1)	X	X 1)
SDESAT	X	X	X	X 1)	X	X 1)
SOCP	X	X	X	X 1)	X	X 1)
SRTTOF	X	X	X	X 1)	X	X 1)
SSTTOF	X	X	X	X 1)	X	X 1)
STTON	X	X	X	X 1)	X	X 1)
SADC	X	X	X	X 1)	X	X 1)
SBC	X	X	X	X 1)	X	X 1)
SCS	X	X	X	X 1)	X	X 1)

1) This read access has increased latency.

Table 30 summarizes which register can be accessed with WRITEL commands in the different operating modes.

Table 30 Write access validity

	OPM0, OPM1	OPM2	OPM3	OPM4	OPM5	OPM6
PID						
PSTAT						
PSTAT2						
PER						
PCFG		X				
PCFG2		X				
PCTRL	X	X	X	X	X	X
PCTRL2	X	X	X	X	X	X
PSCR		X				
PRW	X	X	X	X	X	X
PPIN						
PCS						
SID						
SSTAT						
SSTAT2						
SER						
SCFG		X				
SCFG2 [1)]		X				
SSCR		X				
SDESAT		X				
SOCP		X				
SRTTOF		X				
SSTTOF		X				
STTON		X				
SADC [1)]						
SBC		X				
SCS						

1) Write access is possible only if the SCFG.CFG2 bit is set.

4 Application information

4.1 Typical application circuit

Table 31 Component values

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Decoupling capacitance (between VEE2 and GND2)	C_d	2 × 0.5	11	–	µF	10 µF capacitance next to the power supply source (for example, flyback converter). 1 µF close to the device. It is strongly recommended to have at least two capacitances close to the device (for example, 2 × 500 nF)	P_4.1.1
Decoupling capacitance (between VCC2 and GND2)	C_d	–	11	–	µF	10 µF capacitance next to the power supply source (for example, flyback converter). 1 µF close to the device	P_4.1.2
Decoupling capacitance (between VCC1 and GND1)	C_d	–	11	–	µF	10 µF capacitance next to the power supply source (for example, flyback converter). 1 µF close to the device	P_4.1.3
Series resistance	R_{s1}	0	1	–	kΩ	–	P_4.1.4
Pull-up resistance	R_{pu1}	–	10	–	kΩ	–	P_4.1.5
Filter resistance	R_1	–	1	–	kΩ	–	P_4.1.6
Filter capacitance	C_1	–	47	–	pF	–	P_4.1.7
Reference resistance	R_{ref1}	–	26.7[1)]	–	kΩ	High-accuracy, as close as possible to the device	P_4.1.8
Reference capacitance	C_{ref1}	–	100	–	pF	As close as possible to the device	P_4.1.9
Pull-up resistance	R_{pu2}	–	10	–	kΩ	–	P_4.1.10
Reference resistance	R_{ref2}	–	23.7[1)]	–	kΩ	High-accuracy, as close as possible to the device	P_4.1.11
Reference capacitance	C_{ref2}	–	100	–	pF	As close as possible to the device	P_4.1.12
DESAT filter resistance	R_{desat}	1	3	–	kΩ	Depends on the required response time	P_4.1.13
DESAT filter capacitance	C_{desat}	–	n/a	–	pF	Depends on the required response time	P_4.1.14

Table 31 Component values (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
DESAT diode	D_{desat}	–	n/a	–	–	HV diode	P_4.1.15
Sense resistance	R_{sense}	–	n/a	–	Ω	Depends on the IGBT specification	P_4.1.16
OCP filter capacitance	C_{ocp}	–	n/a	–	pF	Depends on the required response time	P_4.1.17
OCP and OCPG resistance	R_{ocp}, R_{ocpg}	0	–	100	Ω	Depends on the required response time	P_4.1.18
DACLP filter resistance	R_{daclp}	–	1	–	kΩ	–	P_4.1.19
DACLP filter capacitance	C_{daclp}	–	470	–	pF	–	P_4.1.20
Active clamping resistance	R_{acl1}	–	n/a	–	Ω	Depends on the application requirements	P_4.1.21
Active clamping resistance	R_{acl2}	–	n/a	–	kΩ	Depends on the application requirements	P_4.1.22
Active clamping capacitance	C_{acli}	–	n/a	–	nF	Depends on the application requirements	P_4.1.23
TVS diode	$D_{tvsacl1}$, $D_{tvsacl2}$	–	n/a	–	–	Depends on the application requirements	P_4.1.24
Active clamping diode	D_{acl}	–	n/a	–	–	Depends on the application requirements	P_4.1.25
ACLI clamping diode	D_{acl2}	–	n/a	–	–	Depends on the application requirements	P_4.1.26
VREG capacitance	C_{vreg}	–	1	–	µF	As close as possible to the device	P_4.1.27
GATE resistance	R_{gon}	0.5	–	–	Ω	–	P_4.1.28
GATE resistance	R_{goff}	0.5	–	–	Ω	–	P_4.1.29
GATE clamping diode	D_{gcl1}	–	n/a	–	–	2)	P_4.1.30
GATE clamping diode	D_{gcl2}	–	n/a	–	–	For example, Schottky diode2)	P_4.1.31
GATE series resistance	R_{gate}	0	10	–	Ω	Optional component	P_4.1.32
VEE2 clamping diode	D_{gcl3}	–	n/a	–	–	For example, Schottky diode2)	P_4.1.33
ADC filter resistance	R_{adc}	–	10	–	Ω	–	P_4.1.34
ADC filter capacitance	C_{adc}	–	1	–	nF	–	P_4.1.35

1) If other values are used, the functionality of IC cannot be guaranteed.
2) Characteristics of this component are application specific.

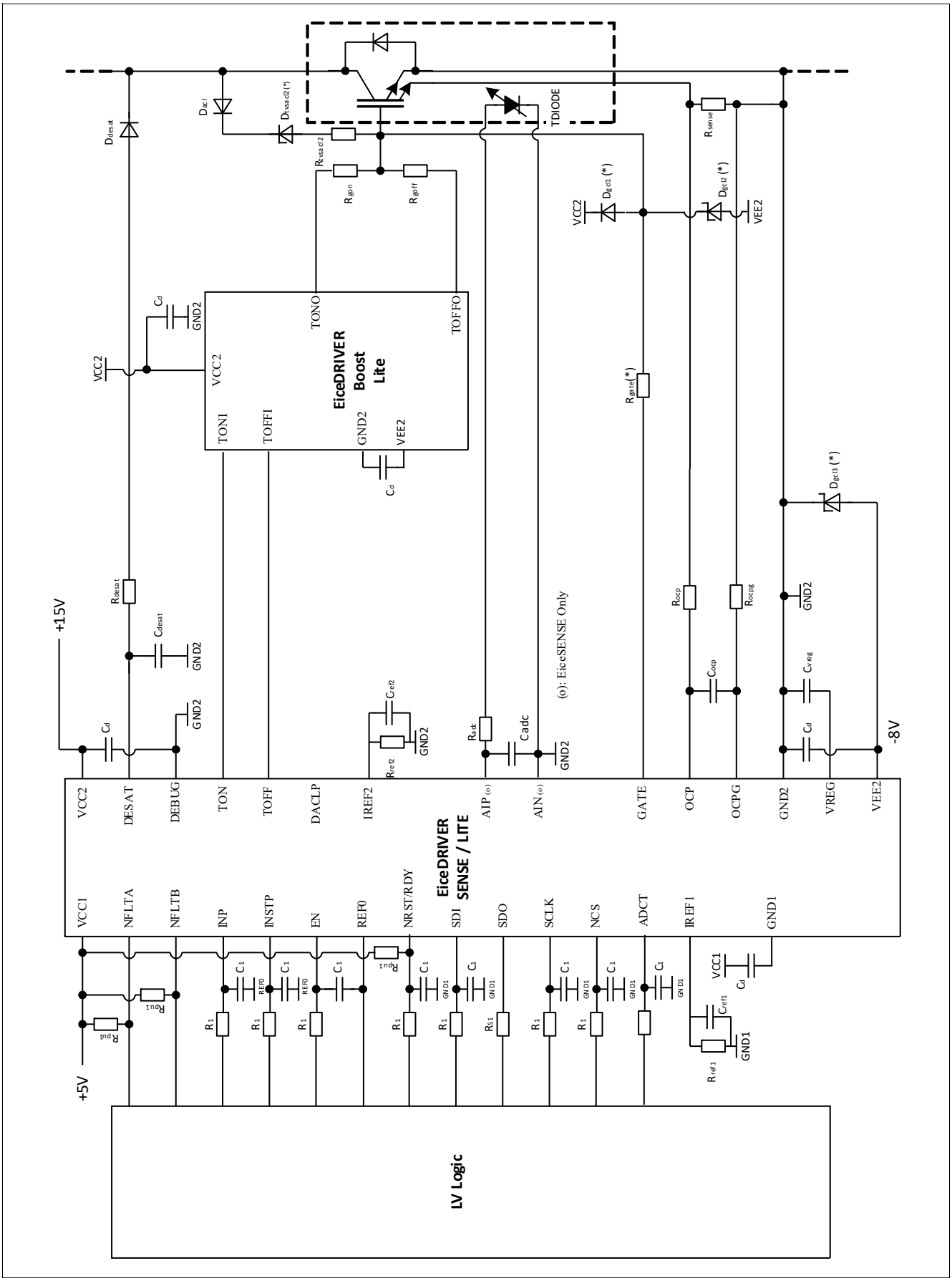


Figure 27 Typical application example

5 General product characteristics

5.1 Absolute maximum ratings

Stress above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect the device reliability.

Table 32 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction temperature	T_{JUNC}	-40	–	150	°C	–	P_5.1.1
Storage temperature	T_{STO}	-55	–	150	°C	–	P_5.1.2
Positive power supply (primary)	V_{CC1}	-0.3	–	6.0	V	Referenced to **GND1**	P_5.1.3
Positive power supply (secondary)	V_{CC2}	-0.3	–	28	V	Referenced to **GND2**	P_5.1.4
Negative power supply	V_{EE2}	-13	–	0.3	V	Referenced to **GND2**	P_5.1.5
Power supply voltage difference (secondary) V_{CC2} - V_{EE2}	V_{DS2}	–	–	40	V	–	P_5.1.6
Voltage on any I/O pin on primary side except **INP**, **INSTP**, **EN**	V_{IN1}	-0.3	–	6.0	V	Referenced to **GND1**	P_5.1.7
Voltage on **INP**, **INSTP**, **EN** pins	V_{INR1}	-0.3	–	6.0	V	Referenced to **REF0**[2)]	P_5.1.8
Voltage difference between **REF0** and **GND1**	V_{DG1}	-4	–	4	V	–	P_5.1.9
Voltage difference between **OCPG** and **GND2**	V_{OCPG2}	-0.3	–	0.3	V	–	P_5.1.10
Output current on push-pull I/O on primary side	I_{OUTPP1}	–	–	20	mA	–	P_5.1.11
Output current on push-pull I/O on secondary side	I_{OUTPP2}	–	–	5	mA	–	P_5.1.12
Output current on open-drain I/O on primary side	I_{OUTOD1}	–	–	20	mA	–	P_5.1.13
VREG output DC current	I_{REG2}	–	–	525	µA	C_{LOAD} = 1 µF	P_5.1.14
Voltage on 5-V pin on secondary side	V_{IN52}	-0.3	–	6.0	V	Referenced to **GND2**	P_5.1.15
Voltage on 15-V pin on secondary side	V_{IN152}	V_{EE2} - 0.3	–	V_{CC2} + 0.3	V	Referenced to **GND2**, except **DESAT**	P_5.1.16
Voltage on **DESAT** pin	$V_{INDESAT}$	-0.3	–	V_{CC2} + 0.3	V	Referenced to **GND2**	P_5.1.17
Power dissipation, primary chip	$P_{DISMAX1}$	–	–	100	mW	T_{AMB} = 125°C	P_5.1.18

Table 32 Absolute maximum ratings[1] (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power dissipation, secondary chip	$P_{DISMAX2}$	–	–	600	mW	T_{AMB} = 125°C	P_5.1.19
ESD immunity	V_{ESD}	–	–	2	kV	HBM[3]	P_5.1.20
		–	–	750	V	CDM[4], pins 1, 18, 19, 36	P_5.1.21
		–	–	500	V	CDM[4], all other pins	P_5.1.22
MSL level	MSL	n/a	3	n/a	–	–	P_5.1.23

1) Not subject to production test, specified by design.
2) Maximum voltage of V_{INR1} + V_{DG1} should be below 7 V.
3) According to EIA/JESD22-A114-B.
4) According to JESD22-C101-C.

5.2 Operating range

To ensure correct operation of the 1EDI2010AS, the following operating conditions must not be exceeded. All parameters specified in the following sections assume these operating conditions, unless otherwise noted.

Table 33 Operating conditions

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Ambient temperature	T_{amb}	-40	–	125	°C	–	P_5.2.1
Positive power supply (primary)	V_{CC1}	4.65	5.0	5.5	V	Referenced to **GND1**[1]	P_5.2.2
Positive power supply (secondary)	V_{CC2}	13.0	15.0	18.0	V	Referenced to **GND2**[2]	P_5.2.3
Negative power supply	V_{EE2}	-10.0	-8.0	0	V	Referenced to **GND2**[3]	P_5.2.4
PWM switching frequency	f_{sw}	–	–	30	kHz	[4]	P_5.2.5
Common-mode transient immunity	$\Delta V_{ISO}/\Delta t$	-100	–	100	kV/µs	At 1000 V[5]	P_5.2.6
Pulsed magnetic field transient immunity	H_{ISO}	-1000	–	1000	A/m	t_r = 10 s[5][6]	P_5.2.7

1) Deterministic and correct operation of the device is guaranteed down to V_{UVLO1L}.
2) Deterministic and correct operation of the device is guaranteed down to V_{UVLO2L}.
3) Deterministic and correct operation of the device is guaranteed up to 0.3 V.
4) Maximum junction temperature of the device must not be exceeded.
5) Not subject to production test, specified by design.
6) As per IEC 61000-4-9.

5.3 Thermal characteristics

The indicated thermal parameters apply to the full operating range, unless otherwise specified.

Table 34 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance junction to ambient	R_{THJA}	–	60	–	K/W	T_{amb} = 125°C[1)2)]	P_5.3.1
Thermal resistance junction to case	R_{THJC}	–	–	41	K/W	T_{amb} = 125°C[1)]	P_5.3.2

1) Not subject to production test, specified by design.

2) The thermal characteristics are determined with a six-layer board with the dimensions 30 mm × 40 mm × 1.5 mm and a Cu thickness of 35 µm per layer. (Cooling areas should be provided on the top and the bottom, but should not cover the isolation area of the IC.)

5.4 Electrical characteristics

The indicated electrical parameters apply to the full operating range, unless otherwise specified.

5.4.1 Power supply

Table 35 Power supplies characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
UVLO1 threshold high	V_{UVLO1H}	4.20	4.47	4.65	V	Referenced to **GND1**	P_5.4.1
UVLO1 threshold low	V_{UVLO1L}	4.20	4.40	4.60	V	Referenced to **GND1**	P_5.4.2
UVLO1 hysteresis	$V_{UVLO1HYS}$	40	70	–	mV	–	P_5.4.3
UVLO2 threshold high	$V_{UVLO2H0}$	11.5	12.5	13.0	V	Referenced to **GND2**	P_5.4.4
	$V_{UVLO2H1}$	9.5	10.25	11	V	Referenced to **GND2**	P_5.4.5
UVLO2 threshold low	$V_{UVLO2L0}$	11.0	11.7	12.5	V	Referenced to **GND2**	P_5.4.6
	$V_{UVLO2L1}$	9	9.75	10.5	V	Referenced to **GND2**	P_5.4.7
UVLO2 hysteresis	$V_{UVLO2HY0}$	500	850	–	mV	$V_{UVLO2H0}$ or $V_{UVLO2L0}$ selected	P_5.4.8
	$V_{UVLO2HY1}$	400	500	–	mV	$V_{UVLO2H1}$ or $V_{UVLO2L1}$ selected	P_5.4.9
V_{CC2} reset level	V_{RST2}	7.9	8.3	8.8	V	Referenced to **GND2**	P_5.4.11
Quiescent current input chip	I_{Q1}	–	7.5	10	mA	V_{CC1} = 5 V, all I/Os inactive	P_5.4.12
Quiescent current output chip VCC2	I_{QVCC2}	–	11	13	mA	V_{CC2} = 15 V, V_{EE2} = -8 V, all I/Os inactive	P_5.4.13
Quiescent current output chip VEE2	I_{QVEE2}	–	1	2	mA	V_{CC2} = 15 V, V_{EE2} = -8 V, all I/Os inactive	P_5.4.14
VCC1 ramp-up or ramp-down time	t_{RP1}	–	–	0.5	V/ms	Absolute value	P_5.4.15
VCC2 ramp-up or ramp-down time	t_{RP2}	–	–	1.5	V/ms	Absolute value	P_5.4.16
VEE2 ramp-up or ramp-down time	t_{RP3}	–	–	0.8	V/ms	Absolute value	P_5.4.17
Power dissipation, primary chip	P_{DIS1}	–	37.5	–	mW	T_{AMB} = 25°C	P_5.4.18
Power dissipation, secondary chip	P_{DIS2}	–	175	–	mW	T_{AMB} = 25°C, idle mode	P_5.4.19

5.4.2 Internal oscillators

Table 36 Internal oscillators

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Primary and secondary main oscillator frequency	f_{clk1}	14.0	16.6	19.1	MHz	Resistances on pin **IREF1** nominal	P_5.4.20
Start-stop oscillator frequency	f_{clk2}, f_{clkst2}	15.0	17.1	19.0	MHz	Resistances on pin **IREF2** nominal	P_5.4.21

5.4.3 Primary I/O electrical characteristics

Table 37 Electrical characteristics for pins INP, INSTP, EN

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low input voltage	V_{INPRL1}	0	–	0.3 × V_{CC1}	V	Referenced to **REF0**	P_5.4.24
High input voltage	V_{INPRH1}	0.7 × V_{CC1}	–	V_{CC1}	V	Referenced to **REF0**	P_5.4.25
Weak pull-down resistance	R_{PDIN1}	20	–	100	kΩ	Referenced to **REF0**	P_5.4.26
Input current	I_{INPR1}	–	–	300	µA	–	P_5.4.27
Input pulse suppression	t_{INPR1}	–	20	–	ns	1)	P_5.4.28
Time between **EN** valid and **INP** high level	t_{INPEN}	8	–	–	µs	2)	P_5.4.29
INP high or low duration	t_{INPPD}	250	–	–	ns	–	P_5.4.30
INSTP high or low duration	$t_{INSTPPD}$	250	–	–	ns	–	P_5.4.31
EN high or low duration	t_{ENDC}	10	–	–	µs	2)	P_5.4.32

1) Not subject to production test, specified by design.
2) Timing is given for hard ON/OFF switching condition only.

Table 38 Electrical characteristics for pins NRST/RDY, SCLK, SDI, NCS, DIO1 (input), ADCT

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low input voltage	V_{INPL1}	0	–	0.3 × V_{CC1}	V	Referenced to **GND1**	P_5.4.33
High input voltage	V_{INPH1}	0.7 × V_{CC1}	–	V_{CC1}	V	Referenced to **GND1**	P_5.4.34
Weak pull-up resistance **SCLK**, **SDI**, **NCS**	R_{PUSPI1}	25	–	100	kΩ	Referenced to **VCC1**	P_5.4.35
Weak pull-down resistance **DIO1**, **ADCT**	$R_{PDADDI1}$	25	–	100	kΩ	Referenced to **GND1**	P_5.4.36
Input current	I_{INP1}	–	–	400	µA	–	P_5.4.37
NRST/RDY output voltage in non-ready conditions	V_{OUTNR}	–	–	1	V	V_{cc1} = 5 V, I_{load} = 2 mA	P_5.4.38
		–	0.7	1	V	V_{cc1} = 0 V, I_{load} = 500 µA	P_5.4.39
NRST/RDY driven-active time after power supplies are within operating range	t_{RST}	–	15.4	–	µs	1)	P_5.4.40
NRST/RDY minimum activation time	t_{RSTAT}	10	–	–	µs	–	P_5.4.41
Minimum **DIO1** high or low duration	t_{DIO1DC}	10	–	–	µs	When configured as input	P_5.4.42
Minimum **ADCT** high or low duration	t_{ADCTDC}	20	–	–	µs	–	P_5.4.43

1) Not subject to production test, specified by design.

Table 39 Electrical characteristics for pins SDO, DIO1 (output)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low output voltage	V_{OUTPL1}	–	–	0.5	V	I_{load} = 5 mA	P_5.4.44
High output voltage	V_{OUTPH1}	3.85	–	–	V	I_{load} = 5 mA	P_5.4.45

Table 40 Electrical characteristics for pins NFLTA, NFLTB

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low output voltage	V_{OUTDL1}	–	–	0.5	V	I_{SINK} = 5 mA	P_5.4.46

5.4.4 Secondary I/O electrical characteristics

Table 41 Electrical characteristics for pins TON, TOFF and GATE

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TON, **TOFF** high output voltage	V_{15OH2}	V_{CC2} - 1	–	V_{CC2} + 0.3	V	Referenced to **GND2**	P_5.4.47
TON, **TOFF** low output voltage	V_{15OL2}	V_{EE2} - 0.3	–	V_{EE2} + 1	V	Referenced to **GND2**	P_5.4.48
TON, **TOFF** source and sink current	I_{15O2}	1	–	–	A	1)2)	P_5.4.49
GATE input voltage range	V_{15GATE}	V_{EE2}	–	V_{CC2}	V	Referenced to **GND2**	P_5.4.50
Passive clamping voltage	V_{PCLP}	–	–	V_{EE2} + 1	V	Secondary chip not supplied; **TON**, **TOFF** and **GATE** shorted, I_{CLAMP} = 10 mA	P_5.4.51
Passive clamp current	I_{PCLP}	5	–	–	mA	Secondary chip not supplied; **TON**, **TOFF** and **GATE** shorted, $V_{GATE} = V_{EE2}$ + 2 V	P_5.4.52

1) Not subject to production test, specified by design.
2) Thermally limited.

Table 42 Electrical characteristics for pins DEBUG, DIO2 (input)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low input voltage	V_{5INL2}	0	–	1.5	V	Referenced to **GND2**	P_5.4.53
High input voltage	V_{5INH2}	3.5	–	5.5	V	Referenced to **GND2**	P_5.4.54
Weak pull-down resistance	R_{PDIN2}	20	–	80	kΩ	Connected to **GND2**	P_5.4.55

Table 43 Electrical characteristics for pins DIO2, DACLP (output)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High output voltage	V_{5OH2}	4.0	–	5.25	V	Referenced to **GND2**, I_{load} = 2 mA, V_{REG2} = typ.	P_5.4.56
Low output voltage	V_{5OL2}	0	–	0.5	V	Referenced to **GND2**, I_{load} = 2 mA	P_5.4.57
Minimum **DIO2** high or low duration	t_{DIO2DC}	10	–	–	µs	When configured as input	P_5.4.58

Table 44 Electrical characteristics for pin AIP

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage range for current source	V_{AIP}	0	–	4.5	V	I_{AIPCS} = typ.	P_5.4.60
Current source	I_{AIPCS}	–	1.05	–	mA	R_{ref2} = 23.7 kΩ[1)]	P_5.4.61
Output current source error	$I_{AIPCSER}$	-3	–	3	%	Deviation from nominal value	P_5.4.62

1) Recommended resistance for specified limits. Other values may cause the device to malfunction.

5.4.5 Switching characteristics

Table 45 Switching characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input-to-output propagation delay ON	t_{PDON}	175	215	255	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V[1)]	P_5.4.63
Input-to-output propagation delay OFF	t_{PDOFF}	175	215	255	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V[1)]	P_5.4.64
Input-to-output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-50	0	50	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V	P_5.4.65
Input-to-output propagation delay distortion variation for two consecutive pulses	$t_{PDISTOV}$	–	25	–	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V, T_{JUNC} = 25°C[2)]	P_5.4.66
Rise time	t_{RISE}	–	120	205	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V, C_{LOAD} = 10 nF, 10%-90%	P_5.4.67
		–	30	50	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V, no load, 10%-90%	P_5.4.68
Fall time	t_{FALL}	–	150	235	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V, C_{LOAD} = 10 nF, 90%-10%	P_5.4.69
		–	60	100	ns	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{EE2} = -8 V, no load, 90%-10%	P_5.4.70
TTOFF plateau voltage, without V_{BE} compensation	V_{GPOF0}	5.4	6.0	6.3	V	Referenced to **GND2**, measured at pin **TON** shorted with **TOFF**, V_{CC2} = 15 V, T_{JUNC} = 25°C	P_5.4.71
	V_{GPOF1}	6.4	7.0	7.3	V		P_5.4.72
	V_{GPOF2}	7.3	8.0	8.4	V		P_5.4.73
	V_{GPOF3}	8.2	9.0	9.4	V		P_5.4.74
	V_{GPOF4}	9.2	10.0	10.5	V		P_5.4.75
	V_{GPOF5}	10.1	11.0	11.5	V		P_5.4.76
	V_{GPOF6}	11.1	12.0	12.6	V		P_5.4.77
	V_{GPOF7}	12.1	13.0	13.6	V		P_5.4.78

Table 45 Switching characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TTOFF plateau voltage, with V_{BE} compensation	V_{GPOF0}	4.7	5.3	5.6	V	Referenced to **GND2**, measured at pin **TON** shorted with **TOFF**, V_{CC2} = 15 V, T_{JUNC} = 25°C	P_5.4.79
	V_{GPOF1}	5.7	6.3	6.6	V		P_5.4.80
	V_{GPOF2}	6.6	7.3	7.7	V		P_5.4.81
	V_{GPOF3}	7.6	8.3	8.7	V		P_5.4.82
	V_{GPOF4}	8.5	9.3	9.8	V		P_5.4.83
	V_{GPOF5}	9.5	10.3	10.8	V		P_5.4.84
	V_{GPOF6}	10.5	11.3	11.9	V		P_5.4.85
	V_{GPOF7}	11.5	12.3	12.9	V		P_5.4.86
Temperature variation from configured V_{TTOFF}(25°C) at T_J = - 40°C	ΔV_{Tm40}	–	-110	–	mV	1)3)	P_5.4.87
Temperature variation from configured V_{TTOFF}(25°C) at T_J = 150°C	ΔV_{T150}	–	110	–	mV	1)3)	P_5.4.88
TTOFF decrease rate	t_{SLEW}	–	9	–	V/µs	–	P_5.4.89
TTOFF delay deviation from nominal value	$t_{DEVTTOFF}$	-100	0	100	ns	For a target time of 2 µs, using the TCF1)2)	P_5.4.90
TTOFF plateau time	t_{TTOFF}	–	2.6	–	µs	**SRTTOF.RTVAL** = 26_H	P_5.4.91
TTON or WTO plateau voltage, without V_{BE} compensation	V_{GPON0}	5.6	6.0	6.4	V	Referenced to **GND2**, measured at pin **TON** shorted with **TOFF**, V_{CC2} = 15 V, T_{JUNC} = 25°C	P_5.4.92
	V_{GPON1}	6.5	7.0	7.5	V		P_5.4.93
	V_{GPON2}	7.45	8.0	8.5	V		P_5.4.94
	V_{GPON3}	8.4	9.0	9.6	V		P_5.4.95
	V_{GPON4}	9.35	10.0	10.6	V		P_5.4.96
	V_{GPON5}	10.3	11.0	11.7	V		P_5.4.97
	V_{GPON6}	11.25	12.0	12.75	V	Referenced to **GND2**, measured at pin **TON** shorted with **TOFF**, V_{CC2} = 16.5 V, T_{JUNC} = 25°C	P_5.4.98

Table 45 Switching characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TTON or WTO plateau voltage, with V_{BE} compensation	V_{GPON0}	6.2	6.7	7.1	V	Referenced to **GND2**, measured at pin **TON** shorted with **TOFF**, V_{CC2} = 15 V, T_{JUNC} = 25°C	P_5.4.99
	V_{GPON1}	7.15	7.7	8.15	V		P_5.4.100
	V_{GPON2}	8.1	8.7	9.2	V		P_5.4.101
	V_{GPON3}	9.0	9.7	10.3	V		P_5.4.102
	V_{GPON4}	10.0	10.7	11.2	V		P_5.4.103
	V_{GPON5}	10.7	11.4	12	V		P_5.4.104
	V_{GPON6}	11.55	12.4	13.1	V	Referenced to **GND2**, measured at pin **TON** shorted with **TOFF**, V_{CC2} = 16.5 V, T_{JUNC} = 25°C	P_5.4.105
TTON delay	t_{TTON}	–	8	–	µs	**SCFG.TTONVAL** = $7F_H$	P_5.4.106
DACLP delay	t_{ACL}	–	5	–	µs	4)	P_5.4.107

1) Values are valid only for stand-alone switching transitions.
2) Not subject to production test, specified by design.
3) Measured without V_{BE} compensation.
4) If a subsequent switching sequence is turning off during this time, the delay will be extended.

5.4.6 Desaturation protection

Table 46 DESAT characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
DESAT input voltage range	$V_{15DESAT}$	0	–	V_{CC2}	V	Referenced to **GND2**	P_5.4.108
DESAT reference Level	V_{DESAT0}	8.5	9	9.5	V	V_{CC2} = 15 V, V_{EE2} = -8 V	P_5.4.109
	V_{DESAT1}	2.9	3	3.1	V		P_5.4.110
DESAT pull-up resistance	R_{DSATPU}	19	30	44	kΩ	V_{CC2} = 15V, V_{EE2} = -8 V, V_{DESAT} = 2 V	P_5.4.111
DESAT low voltage	V_{DESATL}	–	200	–	mV	Referenced to **GND2**, desat clamping enabled, I_{sink} = 5 mA	P_5.4.112
DESAT blanking time deviation from programmed value	$\Delta t_{DESATBL}$	-20	–	20	%	After transition of the PWM command, assuming a programmed blanking time of 1 µs[1)]	P_5.4.113

1) Not subject to production test, specified by design.

5.4.7 Overcurrent protection

Table 47 OCP characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overcurrent error detection threshold	V_{OCP0}	277	300	318	mV	Referenced to **OCPG**	P_5.4.114
	V_{OCP1}	564	600	630	mV	Referenced to **OCPG**	P_5.4.115
OCP blanking time deviation from programmed value	Δt_{OCPBL}	-20	–	20	%	After transition of the PWM command, assuming a programmed blanking time of 1 µs[1)]	P_5.4.116
OCP pull-up resistance	R_{PUOCP2}	40	100	175	kΩ	To internal 5 V reference	P_5.4.117

1) Not subject to production test, specified by design.

5.4.8 Low-latency digital channel

Table 48 Digital channel characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input-to-output propagation time, primary to secondary	t_{DPS}	–	2	4.5	µs	1)	P_5.4.118
Input-to-output propagation time, secondary to primary	t_{DSP}	–	2	4.5	µs	1)	P_5.4.119

1) Single events only. If other communication events occur simultaneously, the maximum propagation time increases.

5.4.9 Error-detection timing

Table 49 Error-detection timing

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Dead time for shoot-through protection	t_{DEAD}	800	–	1200	ns	Default value[2]	P_5.4.120
Class A event detection to **NFLTA** activation	t_{AFLTA}	–	2	4.5	µs	V_{CC2} = typ., V_{CC1} = typ., V_{EE2} = typ.[2]	P_5.4.121
Class A event detection to turn-off sequence activation	t_{OFFCLA}	–	–	400	ns	V_{TOFF} = V_{CC2} - 1 V, V_{CC2} = typ., V_{CC1} = typ., V_{EE2} = typ.[2]	P_5.4.122
DESAT event detection to turn-off sequence activation	$t_{OFFDESAT2}$	–	–	430	ns	V_{TOFF} = V_{CC2} - 1 V, after blanking time elapsed, V_{CC2} = typ., V_{CC1} = typ., V_{EE2} = typ.[2]	P_5.4.123
OCP event occurrence to turn-off sequence activation	$t_{OFFOCP2}$	–	–	150	ns	V_{TOFF} = V_{CC2} - 1 V, after blanking time elapsed, V_{CC2} = typ., V_{CC1} = typ., V_{EE2} = typ.[2]	P_5.4.124
Class B event detection to **NFLTB** activation	t_{BFLTB}	–	2	4.5	µs	V_{CC2} = typ., V_{CC1} = typ., V_{EE2} = typ.[2]	P_5.4.125
Class B event detection to turn-off sequence activation	$t_{OFFCLB2}$	–	–	400	ns	V_{TOFF} = V_{CC2} - 1 V, V_{CC2} = typ., V_{CC1} = typ., V_{EE2} = typ.[1)2)]	P_5.4.126
Verification mode time-out	t_{VMTO}	–	15	–	ms	After a transition from OPM2 to OPM5, **SCFG.TOSEN** = 0_B[1)2)]	P_5.4.127
		–	60	–	ms	After a transition from OPM2 to OPM5, **SCFG.TOSEN** = 1_B[1)2)]	P_5.4.128
Lifesign error detection time	t_{LS}	–	5	–	µs	After error condition detected by logic	P_5.4.129

1) Not subject to production test, specified by design.
2) The deviation of the clock needs to be considered.

5.4.10 SPI interface

Table 50 SPI interface characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI frame size	N_{bit}	n/a	N × 16	n/a	bit	N is the length of the daisy chain	P_5.4.130
Baud rate	f_{CLK}	0.1	–	2	MHz	1)2)	P_5.4.131
Serial clock period	t_{SCLKp}	0.5	–	–	µs	3)	P_5.4.132
SCLK duty cycle	D_{SCLK}	45	–	55	%	3)	P_5.4.133
SDI set-up time	t_{SDIsu}	65	–	–	ns	3)	P_5.4.134
SDI hold time	t_{SDIh}	100	–	–	ns	3)	P_5.4.135
NCS lead time	t_{CSlead}	1	–	–	µs	3)	P_5.4.136
NCS trail time	$t_{CStrail}$	1	–	–	µs	3)	P_5.4.137
NCS inactive time	$t_{CSinact}$	10	–	–	µs	3)	P_5.4.138
SDO enable time	t_{SDOen}	–	–	500	ns	C_{load} = 20 pF 3)	P_5.4.139
SDO disable time	t_{SDOdis}	–	–	1	µs	C_{load} = 20 pF 3)	P_5.4.140
SDO valid time	t_{SDOv}	10	–	185	ns	C_{load} = 20 pF 3)	P_5.4.141

1) Not subject to production test, low limit specified by design.
2) In a daisy chain configuration the maximum baud rate is 1.8 MHz.
3) Not subject to production test, specified by design.

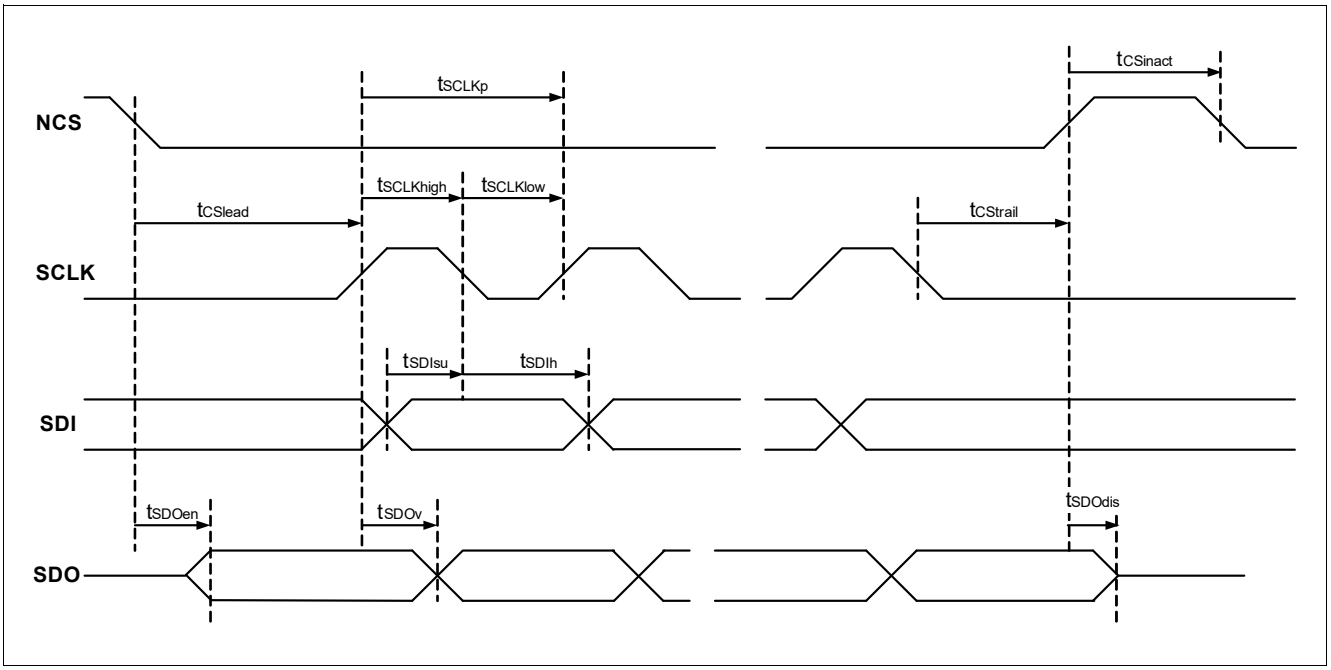


Figure 28 SPI interface timing

5.4.11 ADC parameters

Table 51 ADC parameters

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ADC resolution	*Res*	n/a	8	n/a	bit	[1]	P_5.4.142
Sampling time	t_{SMPL}	–	120	–	clock	From ADC trigger active to end of sampling phase, in OSC2 domain[1]	P_5.4.143
Conversion time	t_{CONV}	–	211	–	clock	From ADC trigger active to result available in the register, in OSC2 domain[1]	P_5.4.144
ADCT trigger signal propagation time	t_{PTRIG}	–	2	–	µs	From valid signal on the **ADCT** pin to start of conversion, external trigger mode only[1]	P_5.4.145
Internal voltage range ADC	V_{INT}	–	2.75	–	V	Resulting in 93 LSB/V	P_5.4.146
Preamplifier gain	$GAIN_0$, $GAIN_1$	–	0.67	–	–	Resulting in 62 LSB/V	P_5.4.147
	$GAIN_2$	–	1	–	–	Resulting in 93 LSB/V	P_5.4.148
	$GAIN_3$	–	2	–	–	Resulting in 186 LSB/V	P_5.4.149
ADC offset	V_{OFF0}	–	0.0	–	V	–	P_5.4.150
	V_{OFF1}	–	0.5	–	V	–	P_5.4.151
	V_{OFF2}	–	1.0	–	V	–	P_5.4.152
	V_{OFF3}	–	1.5	–	V	–	P_5.4.153
	V_{OFF4}	–	2.0	–	V	–	P_5.4.154
Offset error	ER_{OFF}	-3.1	–	3.1	LSB	Negative errors result in the minimum offset[2]	P_5.4.158
Gain error	ER_{GAIN}	-5	–	5	–	Negative errors result in the minimum gain[2]	P_5.4.159
INL	*INL*	–	1	1.6	LSB	[2]	P_5.4.160
DNL	*DNL*	–	0.4	0.75	LSB	[2]	P_5.4.161
Accuracy[3]	*TUE*	-	–	6.5	LSB	Negative errors result in the minimum value[2]	P_5.4.162
Automatic trigger period	t_{ATRIG}	–	4	–	ms	[1]	P_5.4.163

1) Not subject to production test, specified by design.
2) Accuracy-related parameters do not apply while the device is not switching a PWM signal.
3) Total unadjusted error is the square sum of all worst RMS errors (*DNL*, *INL*, ER_{OFF} and ER_{GAIN}).

5.4.12 Insulation characteristics

Table 52 Insulation characteristics in compliance with DIN V VDE 0884 - 10 : 2006-12, expired on December 31st, 2019

Description	Symbol	Characteristic	Unit
Installation classification per EN60664-1, Table 1: Rated main voltage less than 150 V_{rms} Rated main voltage less than 300 V_{rms} Rated main voltage less than 600 V_{rms}	–	 I-IV I-III I-II	–
Climatic classification	–	40 / 125 / 21	–
Pollution degree (EN 60664-1)	–	2	–
Minimum external clearance	CLR	8.12	mm
Minimum external creepage	CPG	8.24	mm
Minimum comparative tracking index	CTI	400	–
Maximum repetitive insulation voltage	V_{IORM}	1420	V_{PEAK}
Highest allowable overvoltage	V_{IOTM}	6000	V_{PEAK}
Maximum surge insulation voltage	V_{IOSM}	4615	V_{PEAK}
Surge insulation test voltage $V_{IOSM,test} = V_{IOSM} \times 1.3$	$V_{IOSM,test}$	6000	V_{PEAK}
Input to output test voltage, method b[1)] $V_{pd(m)} = V_{IORM} \times 1.875$, 100% production test with t_m = 1 sec, partial discharge charge < 5 pC	$V_{pd(m)}$	2663	V_{PEAK}
	$V_{ini(b)}$	6000	V_{PEAK}
Input to output test voltage, method a[1)] $V_{pd(m)} = V_{IORM} \times 1.6$, 100% sample test with t_m = 60 sec, partial discharge charge < 5 pC	$V_{pd(m)}$	2272	V_{PEAK}
	$V_{ini(a)}$	6000	V_{PEAK}
Insulation resistance at T_s = 150°C , V_{IO} = 500 V	R_{IO}	> 10^9	Ω
Insulation resistance at 100°C ≤ T_{amb} ≤ 125°C, V_{IO} = 500 V	R_{IO}	> 10^{12}	Ω

1) Refer to VDE 0884 - 10 for a detailed description of Method a and b partial discharges.

Table 53 Isolation characteristics according to UL 1577

Description	Symbol	Characteristic	Unit
Insulation test voltage / 1 min	V_{ISO}	3750	V_{rms}
Insulation test voltage / 1 sec	V_{ISO}	4500	V_{rms}

6 Package information

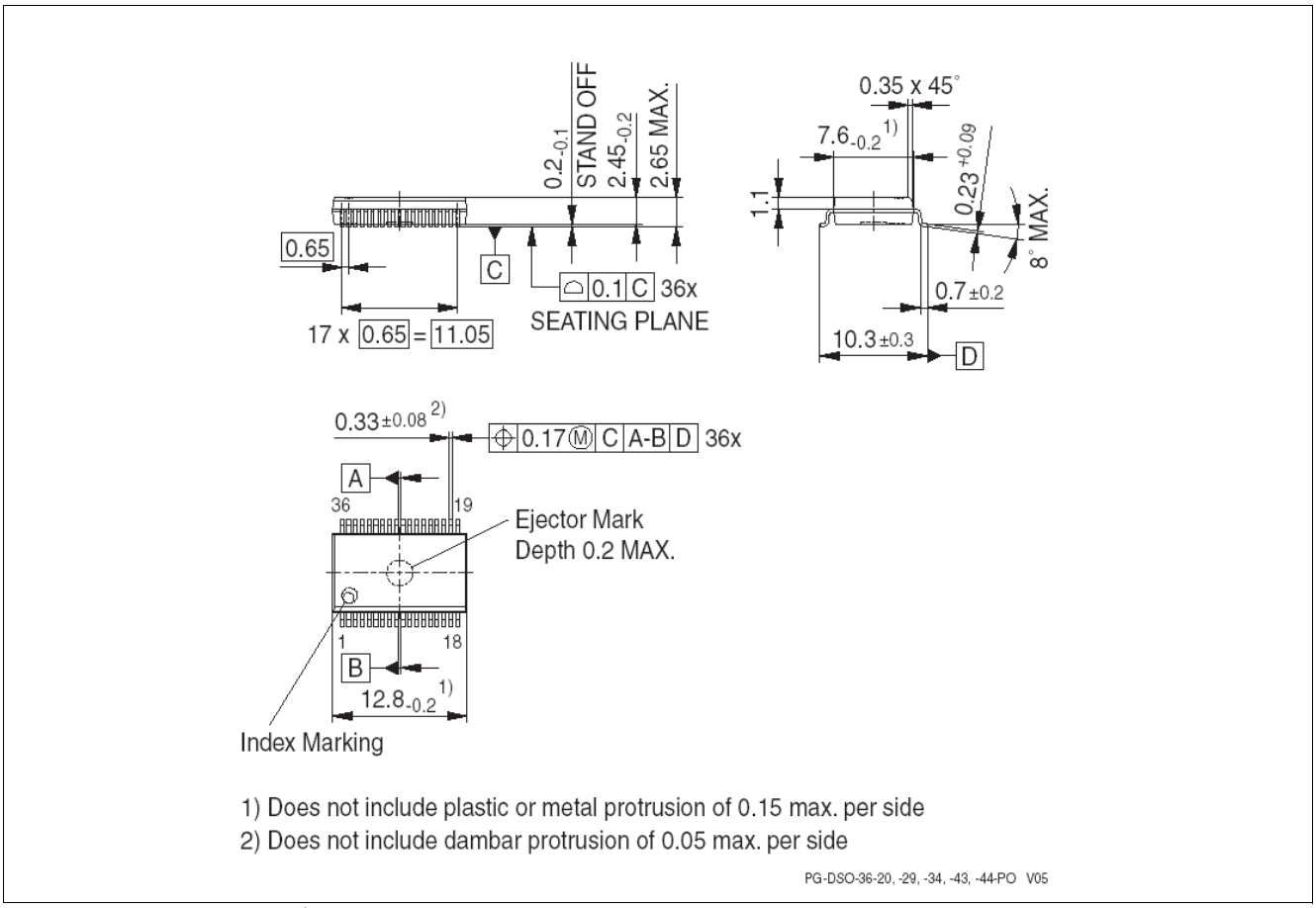


Figure 29 PG-DSO-36[1)]

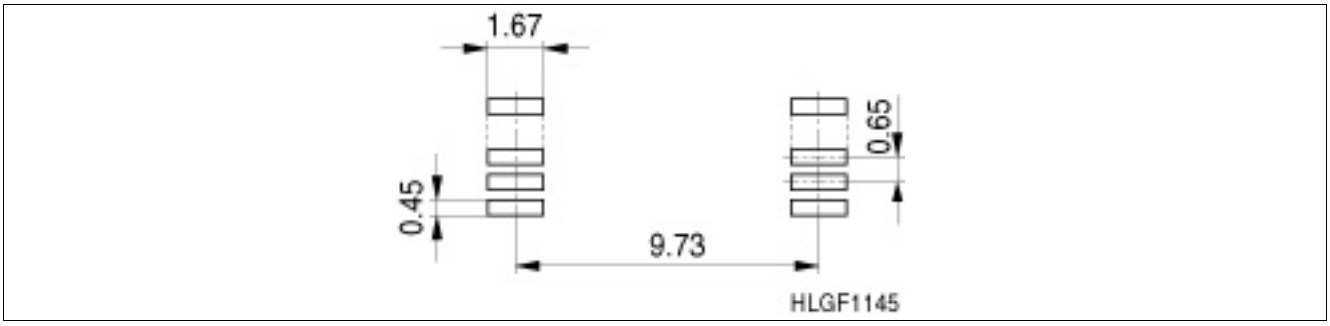


Figure 30 Recommended Footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
Rev 2.1	2021-12-09	• Editorial changes • Added info that DIN V VDE 0884-10:2006-12 expired on December 31st, 2019 V_{IOSM} updated to reflect actual rated value instead of test voltage. Added specification for isolation resistance and partial discharge • Typo fixed in ESD immunity rating – corner pins are 1, 18, 19, 36
Rev 2.0	2017-06-19	–
1.33	2017-01-27	New chapter with failure behavior 2.4.9.4 (former reset events)
		Reset events summary table updated due to new chapter 2.4.9.4 Table 2-15
		Updated figure 2-7.
		GATE pin characteristics merged in Table 5-11 with TON/TOFF characteristics.
		Added test conditions in Table 5-11 for TON/TOFF and GATE pins.
		Merged V_{PCLPG} and V_{PCLP} in Table 5-11 due to test conditions. Same for I_{PCLP}.
		Removed unprecise footnote in Table 5-11.
		Updated values for weak pull-down in Table 5-12.
		Moved DESAT input voltage range to DESAT characteristics in Table 5-16.
		Updated links of registers in chapter 2.4.6.1 and 2.4.6.2.

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