

# EiceDRIVER™ SIL

1EDI2002AS



ISO26262  
compliant

## Features

### Functional Features

- Single Channel IGBT Driver.
- On-chip galvanic insulation (up to 6 kV).
- Support of 600 V and 1200 V IGBT technologies.
- Low propagation delay and minimal PWM distortion.
- Support of 5 V logic levels (primary side).
- 16-bit Standard SPI interface (up to 2 Mbaud) with daisy chain support (primary side).
- Enable input pin (primary side).
- Pseudo-differential inputs for critical signals (primary side).
- Power-On Reset pin (primary side).
- Debug mode.
- Pulse Suppressor.
- Fully Programmable Active Clamping Inhibit signal (secondary side).
- Fully programmable Two-Level Turn On (TTON).
- Low latency digital channel.
- Optimal support of EiceBoost functions.
- 36-pin PG-DSO-36 green package.
- Automotive qualified (as per AEC Q100).

### Safety Relevant Features

- Programmable Desaturation monitoring.
- Overcurrent protection.
- Fully programmable Two-Level Turn-Off.
- Automatic Emergency Turn-Off in failure case.
- Automatic or externally triggered disabling of the output stage (tristate).
- Under- and over-voltage supervision of all the power supplies (both primary and secondary sides).
- NFLTA and NFLTB notification pins for fast system response time (primary side).
- Safe internal state machine.
- Weak Turn-On functionality.
- Internal overtemperature sensor (secondary side).
- Internal clock monitoring.



- Gate signal monitoring.
- IGBT state monitoring.
- Individual error and status flags readable via SPI.
- Support for Active Short Circuit strategies.
- Full diagnosticability.
- In-application testability of safety critical functions.
- Suitable for systems up to ASIL D requirements (as per ISO 26262).

## Potential applications

- Inverters for automotive Hybrid Electric Vehicles (HEV) and Electric Vehicles (EV).
- High Voltage DC/DC converter.
- Industrial Drive.

## Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

## Description

Type	Package	Ordering Code	Marking
1EDI2002AS	PG-DSO-36	SP001362894	1EDI2002AS

## Table of Contents

<b>1</b>	<b>Product Definition</b>	<b>9</b>
1.1	Overview	9
<b>2</b>	<b>Functional Description</b>	<b>10</b>
2.1	Introduction	10
2.2	Pin Configuration and Functionality	11
2.2.1	Pin Configuration	11
2.2.2	Pin Functionality	13
2.2.2.1	Primary Side	13
2.2.2.2	Secondary Side	14
2.2.2.3	Pull Devices	16
2.3	Block Diagram	17
2.4	Functional Block Description	18
2.4.1	Power Supplies	18
2.4.2	Clock Domains	18
2.4.3	PWM Input Stage	19
2.4.4	SPI Interface	21
2.4.4.1	Overview	21
2.4.4.2	General Operation	22
2.4.4.3	Definitions	24
2.4.4.4	SPI Data Integrity Support	26
2.4.4.5	Protocol Description	27
2.4.5	Operating Modes	31
2.4.5.1	General Operation	31
2.4.5.2	Definitions	32
2.4.5.3	Operation Modes Description	34
2.4.5.4	Activating the device after reset	36
2.4.5.5	Activating the device after an Event Class A or B	36
2.4.5.6	Debug Mode	36
2.4.6	Driver Functionality	37
2.4.6.1	Overview	37
2.4.6.2	Switching Sequence Description	42
2.4.6.3	Disabling the output stage	43
2.4.6.4	Passive Clamping	44
2.4.7	Fault Notifications	45
2.4.8	EN Signal Pin	46
2.4.9	Reset Events	46
2.4.10	Operation in Configuration Mode	49
2.4.10.1	Static Configuration Parameters	49
2.4.10.2	Dynamic Configuration	53
2.4.10.3	Delay Calibration	53
2.4.11	Low Latency Digital Channel	54
<b>3</b>	<b>Protection and Diagnostics</b>	<b>55</b>
3.1	Supervision Overview	55
3.2	Protection Functions: Category A	57
3.2.1	Desaturation Protection	57
3.2.2	Overcurrent Protection	59

3.2.3	External Enable .....	61
3.2.4	Output Stage Monitoring .....	62
3.3	Protection Functions: Category B .....	63
3.3.1	Power Supply Voltage Monitoring .....	63
3.3.2	Internal Supervision .....	64
3.3.2.1	Lifesign watchdog .....	65
3.3.2.2	Oscillator Monitoring .....	65
3.3.2.3	Memory Supervision .....	65
3.4	Protection Functions: Category C .....	66
3.4.1	Shoot Through Protection function .....	66
3.4.2	Gate Monitoring .....	67
3.4.3	Temperature Monitoring .....	68
3.4.4	SPI Error Detection .....	68
3.4.5	Active Short Circuit Support .....	69
3.4.6	IGBT State Monitoring .....	70
3.5	Protection Functions: Category D .....	71
3.5.1	Operation in Verification Mode and Weak Active Mode .....	71
3.5.2	Weak Turn On .....	71
3.5.3	DESAT Supervision Level 1 .....	72
3.5.4	DESAT Supervision Level 2 .....	73
3.5.5	DESAT Supervision Level 3 .....	74
3.5.6	OCP Supervision Level 1 .....	74
3.5.7	OCP Supervision Level 3 .....	75
3.5.8	Power Supply Monitoring Supervision .....	75
3.5.9	Internal Clock Supervision .....	77
3.5.10	DIO Supervision .....	77
<b>4</b>	<b>Register Description .....</b>	<b>79</b>
4.1	Primary Register Description .....	81
4.2	Secondary Registers Description .....	100
4.3	Read / Write Address Ranges .....	124
<b>5</b>	<b>Specification .....</b>	<b>126</b>
5.1	Typical Application Circuit .....	126
5.2	Absolute Maximum Ratings .....	129
5.3	Operating range .....	130
5.4	Thermal Characteristics .....	130
5.5	Electrical Characteristics .....	131
5.5.1	Power Supply .....	131
5.5.2	Internal Oscillators .....	132
5.5.3	Primary I/O Electrical Characteristics .....	133
5.5.4	Secondary I/O Electrical Characteristics .....	135
5.5.5	Switching Characteristics .....	137
5.5.6	Desaturation Protection .....	139
5.5.7	Overcurrent Protection .....	139
5.5.8	Low Latency Digital Channel .....	140
5.5.9	DOUT .....	140
5.5.10	Over temperature Warning .....	140
5.5.11	Error Detection Timing .....	141



5.5.12	SPI Interface .....	142
5.5.13	Insulation Characteristics .....	143
<b>6</b>	<b>Package Information .....</b>	<b>144</b>
<b>7</b>	<b>Revision History .....</b>	<b>145</b>

## List of Tables

Table 1	Pin Configuration .....	11
Table 2	Internal pull devices .....	16
Table 3	SPI Command Catalog .....	27
Table 4	Word Convention .....	28
Table 5	ENTER_CMODE request and answer messages .....	28
Table 6	ENTER_VMODE request and answer messages .....	28
Table 7	EXIT_CMODE request and answer messages .....	29
Table 8	NOP request and answer messages .....	29
Table 9	READ request and answer messages .....	29
Table 10	WRITEH request and answer messages .....	30
Table 11	WRITEL request and answer messages .....	30
Table 12	Failure Notification Clearing .....	45
Table 13	Reset Events Summary .....	47
Table 14	Pin behavior (primary side) in case of reset condition .....	48
Table 15	Pin behavior (secondary side) in case of reset condition .....	49
Table 16	Safety Related Functions .....	55
Table 17	DESAT Protection Overview .....	57
Table 18	OCF Function Overview .....	59
Table 19	External Enable Function Overview .....	61
Table 20	Output Stage Monitoring Overview .....	62
Table 21	Power Supply Voltage Monitoring Overview .....	63
Table 22	System Supervision Overview .....	64
Table 23	STP Overview .....	66
Table 24	Gate Monitoring Overview .....	67
Table 25	Temperature Monitoring Overview .....	68
Table 26	SPI Error Detection Overview .....	68
Table 27	Active Short Circuit Support Overview .....	69
Table 28	IGBT State Monitoring Overview .....	70
Table 29	DESAT Supervision Level 1 Overview .....	73
Table 30	DESAT Supervision Level 2 Overview .....	73
Table 31	DESAT Supervision Level 3 Overview .....	74
Table 32	OCF Supervision Level 1 Overview .....	74
Table 33	OCF Supervision Level 3 Overview .....	75
Table 34	Power Supply Monitoring Supervision Overview .....	75
Table 35	Primary Clock Supervision Overview .....	77
Table 36	DIO Supervision Overview .....	77
Table 37	Register Overview .....	79
Table 38	Bit Access Terminology .....	80
Table 39	Read Access Validity .....	124
Table 40	Write Access Validity .....	125
Table 41	Component Values .....	126
Table 42	Absolute Maximum Ratings .....	129
Table 43	Operating Conditions .....	130
Table 44	Thermal Characteristics .....	130
Table 45	Power Supplies Characteristics .....	131
Table 46	Internal Oscillators .....	132

Table 47	Electrical Characteristics for Pins: <b>INP</b> , <b>INSTP</b> , <b>EN/FEN</b> .....	133
Table 48	Electrical Characteristics for Pins: <b>NRST/RDY</b> , <b>SCLK</b> , <b>SDI</b> , <b>NCS</b> , <b>DIO1</b> (input) .....	133
Table 49	Electrical Characteristics for Pins: <b>SDO</b> , <b>DOUT</b> , <b>DIO1</b> (output) .....	134
Table 50	Electrical Characteristics for Pins: <b>NFLTA</b> , <b>NFLTb</b> .....	134
Table 51	Electrical Characteristics for Pins: <b>TON</b> , <b>TOFF</b> & <b>GATE</b> .....	135
Table 52	Electrical Characteristics for Pins: <b>OSD</b> , <b>DEBUG</b> , <b>DIO2</b> (input) .....	135
Table 53	Electrical Characteristics for Pin: <b>NUV2</b> .....	135
Table 54	Electrical Characteristics for Pins: <b>DACLp</b> , <b>DIO2</b> (output) .....	136
Table 55	Electrical Characteristics for Pin: <b>VREG</b> .....	136
Table 56	Switching Characteristics .....	137
Table 57	<b>DESAT</b> characteristics .....	139
Table 58	<b>OCP</b> characteristics .....	139
Table 59	Digital channel characteristics .....	140
Table 60	Data Out characteristics .....	140
Table 61	Over temperature Warning Characteristics .....	140
Table 62	Error Detection Timing .....	141
Table 63	SPI Interface Characteristics .....	142
Table 64	Insulation Characteristics in compliance with DIN V VDE 0884 - 10 : 2006-12, expired on December 31st, 2019	143
Table 65	Isolation Characteristics referring to UL 1577 .....	143

## List of Figures

Figure 1	Pin Configuration .....	11
Figure 2	Block Diagram .....	17
Figure 3	PWM Input Stage .....	19
Figure 4	STP: Inhibition Time Definition .....	20
Figure 5	STP: Example of Operation .....	20
Figure 6	SPI Regular Bus Topology .....	22
Figure 7	SPI Daisy Chain Bus Topology .....	23
Figure 8	Response Answer Principle - Daisy Chain Topology .....	25
Figure 9	Response Answer Principle - Regular Topology .....	25
Figure 10	SPI Commands Overview .....	27
Figure 11	Operating Modes State Diagram .....	31
Figure 12	Output Stage Diagram of Principle .....	37
Figure 13	TTOFF: Principle of Operation .....	39
Figure 14	TTON: Principle of Operation .....	40
Figure 15	TTOFF: pulse suppressor aborting a turn-on sequence .....	41
Figure 16	Idealized Switching Sequence .....	43
Figure 17	Output Stage Disable: Principle of Operation .....	44
Figure 18	Low Latency Digital Channel .....	54
Figure 19	DESAT Function: Diagram of Principle .....	57
Figure 20	DESAT Operation .....	58
Figure 21	DESAT Operation with DESAT clamping enabled .....	59
Figure 22	OCP Function: Principle of Operation .....	60
Figure 23	Power Supply Supervision Function .....	63
Figure 24	Shoot Through Protection: Principle of Operation .....	66
Figure 25	Gate Monitoring Function: Timing Definition .....	68
Figure 26	ASC Strategy Support .....	69
Figure 27	Idealized Weak Turn-On Sequence .....	72
Figure 28	Typical Application Example .....	128
Figure 29	SPI Interface Timing .....	142
Figure 30	Package Dimensions .....	144
Figure 31	Recommended Footprint .....	144



## **1 Product Definition**

### **1.1 Overview**

The 1EDI2002AS is a high-voltage IGBT gate driver designed for automotive motor drives above 5 kW. The 1EDI2002AS is based on Infineon's Coreless Transformer (CLT) technology, providing galvanic insulation between low voltage and high voltage domains. The device has been designed to support 400 V, 600 V and 1200 V IGBT technologies.

The 1EDI2002AS can be connected on the low voltage side ("primary" side) to 5 V logic. A standard SPI interface allows the logic to configure and to control the advanced functions implemented in the driver.

On the high voltage side ("secondary" side), the 1EDI2002AS is dimensioned to drive an external booster stage. Short propagation delays and controlled internal tolerances lead to minimal distortion of the PWM signal.

A large panel of safety-related functions has been implemented in the 1EDI2002AS, in order to support functional safety requirements at system level (as per ISO 26262). Besides, those integrated features ease the implementation of Active Short Circuit (ASC) strategies.

The 1EDI2002AS can be used optimally with Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage family.

## **2 Functional Description**

### **2.1 Introduction**

The 1EDI2002AS is an advanced single channel IGBT driver that can also be used for driving power MOS devices. The device has been developed in order to optimize the design of high performance safety relevant automotive systems.

The device is based on Infineon's Coreless Transformer Technology and consist of two chips separated by a galvanic isolation. The low voltage (primary) side can be connected to a standard 5 V logic. The high voltage (secondary) side is in the DC-link voltage domain.

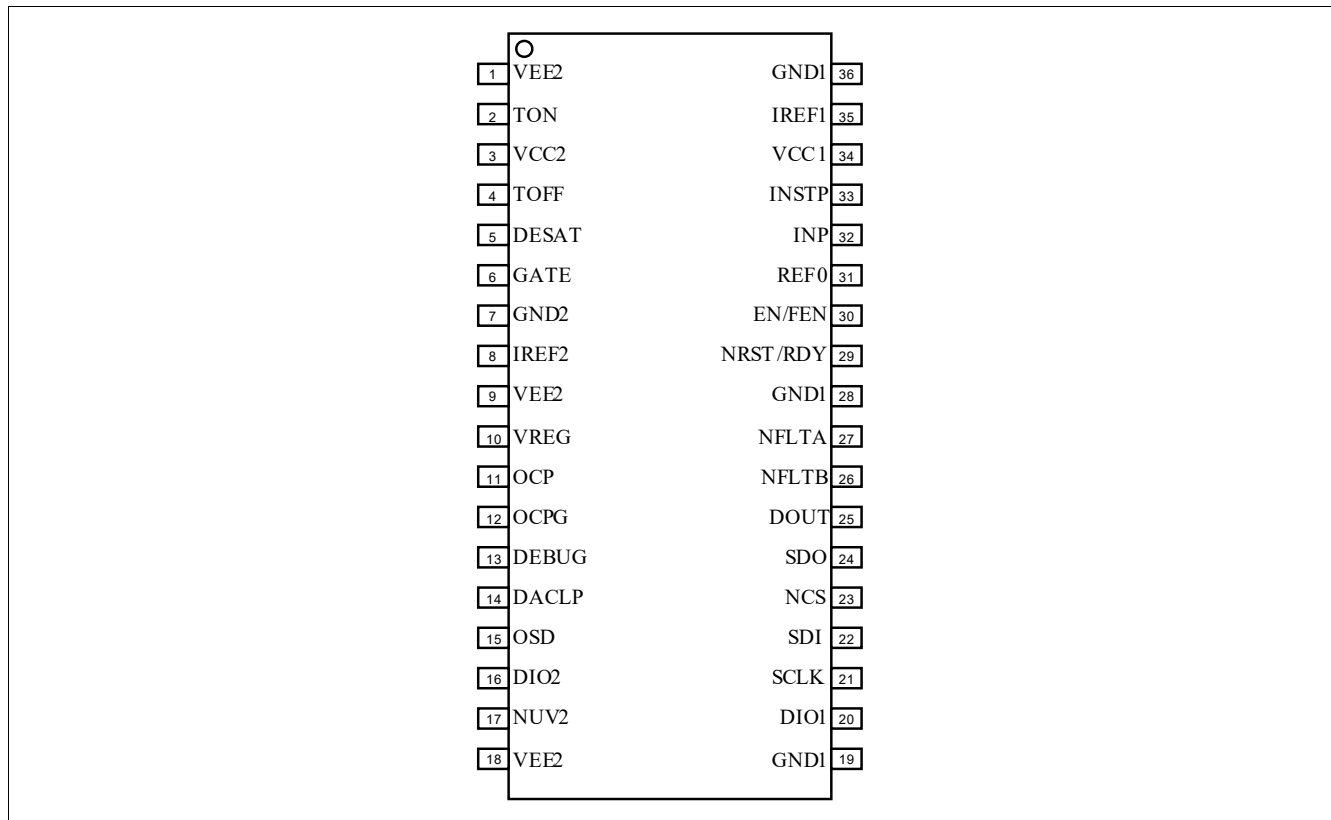
Internally, the data transfers are ensured by two independent communication channels. One channel is dedicated to transferring the ON and OFF information of the PWM input signal only. This channel is unidirectional (from primary to secondary). Because this channel is dedicated to the PWM information, latency time and PWM distortion are minimized. The second channel is bidirectional and is used for all the other data transfers (e.g. status information, etc).

The 1EDI2002AS supports advanced functions in order to optimize the switching behavior of the IGBT. Furthermore, it supports several monitoring and protection functions, making it suitable for systems having to fulfill ASIL requirements (as per ISO 26262).

## Functional Description

## 2.2 Pin Configuration and Functionality

### 2.2.1 Pin Configuration



**Figure 1 Pin Configuration**

**Table 1 Pin Configuration**

Pin Number	Symbol	I/O	Voltage Class	Function
1,9,18	VEE2	Supply	Supply	Negative Power Supply <sup>1)</sup> .
2	TON	Output	15V Secondary	Turn-On Output.
3	VCC2	Supply	Supply	Positive Power Supply.
4	TOFF	Output	15V Secondary	Turn-Off Output.
5	DESAT	Input	15V Secondary	Desaturation Protection Input.
6	GATE	Input	15V Secondary	Gate Monitoring Input.
7	GND2	Ground	Ground	Ground.
8	IREF2	Input	5V Secondary	External Reference Input.
10	VREG	Output	5V Secondary	Reference Output Voltage.
11	OCP	Input	5V Secondary	Over Current Protection.
12	OCPG	Ground	Ground	Ground for the OCP function,
13	DEBUG	Input	5V Secondary	Debug Input.

## Functional Description

**Table 1 Pin Configuration (cont'd)**

Pin Number	Symbol	I/O	Voltage Class	Function
14	DACLP	Output	5V Secondary	Active Clamping Disable Output.
15	OSD	Input	5V Secondary	Output Stage Disable Input.
16	DIO2	Input / Output	5V Secondary	Digital I/O.
17	NUV2	Output	5V Secondary	V <sub>CC2</sub> not valid notification output.
19, 28, 36	GND1	Ground	Ground	Ground <sup>2)</sup> .
20	DIO1	Input / Output	5V Primary	Digital I/O.
21	SCLK	Input	5V Primary	SPI Serial Clock Input.
22	SDI	Input	5V Primary	SPI Serial Data Input.
23	NCS	Input	5V Primary	SPI Chip Select Input (low active).
24	SDO	Output	5V Primary	SPI Serial Data Output.
25	DOUT	Output	5V Primary	<b>DESAT</b> comparator output.
26	NFLT B	Output	5V Primary	Fault B Output (low active, open drain).
27	NFLT A	Output	5V Primary	Fault A Output (low active, open drain).
29	NRST/RDY	Input/Output	5V Primary	Reset Input (low active, open drain). This signal notifies that the device is “ready”.
30	EN/FEN	Input	5V Primary	Enable Input.
31	REF0	Ref. Ground	Ground	Reference Ground for signals <b>INP</b> , <b>INSTP</b> , <b>EN/FEN</b> .
32	INP	Input	5V Primary	Positive PWM Input.
33	INSTP	Input	5V Primary	Monitoring PWM Input.
34	VCC1	Supply Input	Supply	Positive Power Supply.
35	IREF1	Input	5V Primary	External Reference Input.

1) All **VEE2** pins must be connected together.

2) All **GND1** pins must be connected together.

## Functional Description

### 2.2.2 Pin Functionality

#### 2.2.2.1 Primary Side

##### **GND1**

Ground connection for the primary side.

##### **VCC1**

5 V power supply for the primary side (referring to GND1).

##### **INP**

Non-inverting PWM input of the driver. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to  $V_{REF0}$  drives this input to Low state in case the pin is floating.

##### **INSTP**

Monitoring PWM input for shoot through protection. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to  $V_{REF0}$  drives this input to Low state in case the pin is floating.

##### **REF0**

Reference Ground signal for the signals **INP**, **INSTP**, **EN/FEN**. This pin should be connected to the ground signal of the logic issuing those signals.

##### **EN/FEN**

Enable Input Signal. This signal allows the logic on the primary side to turn-off and deactivate the device. An internal weak pull-down resistor to  $V_{REF0}$  drives this input to Low state in case the pin is floating. This pin reacts on logic level or on a periodic signal, depending on the device's configuration.

##### **NFLTA**

Open-Drain Output signal used to report major failure events (Event Class A). In case of an error event, **NFLTA** is driven to Low state. This pin shall be connected externally to  $V_{CC1}$  with a pull-up resistance.

##### **NFLT B**

Open-Drain Output signal used to report major failure events (Event Class B). In case of an error event, **NFLT B** is driven to Low state. This pin shall be connected externally to  $V_{CC1}$  with a pull-up resistance.

##### **SCLK**

Serial Clock Input for the SPI interface. An internal weak pull-up device to  $V_{CC1}$  drives this input to high state in case the pin is floating.

##### **SDO**

Serial Data Output (push-pull) or the SPI interface.

## Functional Description

### SDI

Serial Data Input for the SPI interface. An internal weak pull-up device to  $V_{CC1}$  drives this input to high state in case the pin is floating.

### NCS

Chip Select input for the SPI interface. This signal is low active. An internal weak pull-up device to  $V_{CC1}$  drives this input to High state in case the pin is floating.

### IREF1

Reference input of the primary chip. This pin shall be connected to  $V_{GND1}$  via an external resistor.

### NRST/RDY

Open drain reset input. This signal is low-active. When a valid signal is received on this pin, the device is brought in its default state. This signal is also used as a “ready notification”. A high level on this pin indicates that the primary chip is functional.

### DOUT

Enhanced DESAT functionality comparator status output. This signal allows real-time monitoring of the IGBT state.

### DIO1

I/O for the digital channel. Depending of the chosen configuration of the device, this pin can be an input or an output (push-pull). An internal weak pull-down resistor to  $V_{GND1}$  drives this input to Low state in case the pin is floating.

## 2.2.2.2 Secondary Side

### VEE2

Negative power supply for the secondary side, referring to  $V_{GND2}$ .

### VCC2

Positive power supply for the secondary side, referring to  $V_{GND2}$ .

### GND2

Reference ground for the secondary side.

### DESAT

Desaturation Protection input pin. The function associated with this pin monitors the  $V_{CE}$  voltage of the IGBT. The detection threshold is programmable. An internal pull-up resistor to  $V_{CC2}$  drives this signal to High level in case it is floating.

## Functional Description

### OCP

Over Current Protection input pin. The function associated with this pin monitors the voltage across a sensing resistance located on the auxiliary path of a Current Sense IGBT. An internal weak pull-up resistor to the internal 5V reference drives this input to High state in case the pin is floating.

### OCPG

Over Current Protection Ground.

### TON

Output pin for turning on the IGBT.

### TOFF

Output pin for turning off the IGBT.

### GATE

Input pin used to monitor the IGBT gate voltage.

### OSD

Output Stage Disable input. A High Level on this pin tristates the output stage. An internal weak pull-down resistor to  $V_{GND2}$  drives this input to Low state in case the pin is floating.

### DACLP

Output pin used to disable the active clamping function of the booster.

### DEBUG

Debug input pin. This pin is latched at power-up. When a High level is detected on this pin, the device enters a special mode where it can be operated without SPI interface. This feature is for development purpose only. This pin should normally be tied to  $V_{GND2}$ . An internal weak pull-down resistor to  $V_{GND2}$  drives this input to Low state in case the pin is floating.

### IREF2

Reference input of the secondary chip. This pin shall be connected to  $V_{GND2}$  via an external resistor.

### VREG

Reference Output voltage. This pin shall be connected to an external capacitance to  $V_{GND2}$ .

### NUV2

$V_{CC2}$  not valid notification signal (Open Drain). This signal drives a low level when  $V_{CC2}$  is not valid or when the internal 5V digital supply is not valid. When both supplies are valid, this pin is in high impedance state. This pin shall be connected externally to a 5 V reference with a pull-up resistance.

### DIO2

I/O for the digital channel. Depending of the chosen configuration of the device, this pin can be an input or an output (push-pull). An internal weak pull-down resistor to  $V_{GND2}$  drives this input to Low state in case the pin is floating.

## Functional Description

### 2.2.2.3 Pull Devices

Some of the pins are connected internally to pull-up or pull-down devices. This is summarized in [Table 2](#).

**Table 2 Internal pull devices**

Signal	Device
<b>INP</b>	Weak pull down to $V_{REF0}$
<b>INSTP</b>	Weak pull down to $V_{REF0}$
<b>EN/FEN</b>	Weak pull down to $V_{REF0}$
<b>SCLK</b>	Weak pull up to $V_{CC1}$
<b>SDI</b>	Weak pull up to $V_{CC1}$
<b>NCS</b>	Weak pull up to $V_{CC1}$
<b>DIO1</b>	Weak pull down to $V_{GND1}$
<b>DESAT</b>	Weak pull up to $V_{CC2}$
<b>DIO2</b>	Weak pull down to $V_{GND2}$
<b>OSD</b>	Weak pull down to $V_{GND2}$
<b>OCP</b>	Weak pull up to 5 V internal reference
<b>DEBUG</b>	Weak pull down to $V_{GND2}$



Functional Description

2.3 Block Diagram

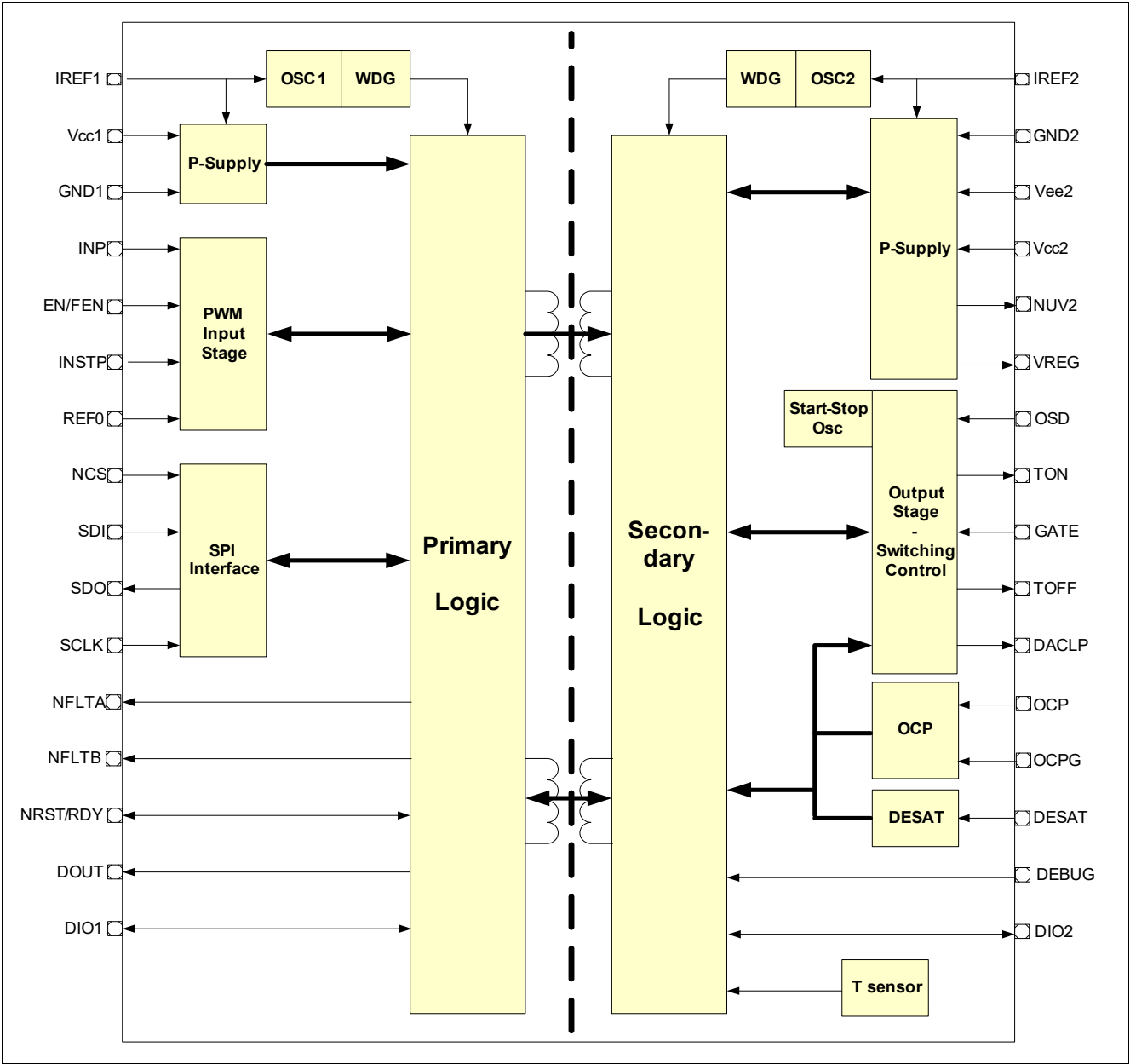


Figure 2 Block Diagram

## **2.4 Functional Block Description**

### **2.4.1 Power Supplies**

On the primary side, the 1EDI2002AS needs a single 5 V supply source  $V_{CC1}$  for proper operation. This makes the device compatible to most of the microcontrollers available for automotive applications.

On the secondary side, the 1EDI2002AS needs two power supplies for proper operation.

- The positive power supply  $V_{CC2}$  is typically set to 15 V (referring to  $V_{GND2}$ ).
- The negative supply  $V_{EE2}$  is typically set to -8 V (referring to  $V_{GND2}$ ).

Under- and over-voltage monitoring is performed continuously during operation of the device (see [Chapter 3.3.1](#)).

A 5 V supply for the digital domain on the secondary side is generated internally (present at pin **VREG**).

### **2.4.2 Clock Domains**

The clock system of the 1EDI2002AS is based on three oscillators defining each a clock domain:

- One RC oscillator (OSC1) for the primary chip.
- One RC oscillator (OSC2) for the secondary chip excepting the output stage.
- One Start-Stop oscillator (SSOSC2) for the output stage on the secondary side.

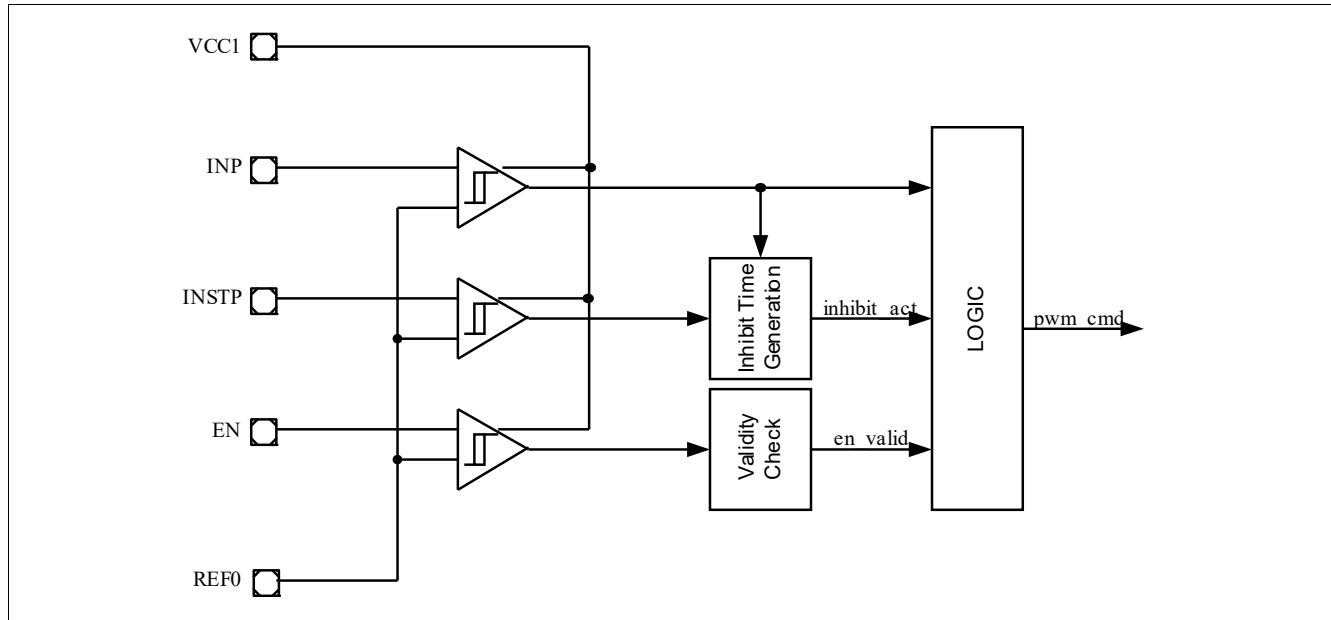
The two RC oscillators are running constantly. They are also monitored constantly, and large deviations from the nominal frequency are identified as a system failure (Event Class B, see [Chapter 3.3.2.2](#)).

The Start Stop oscillator is controlled by the PWM command.

## Functional Description

### 2.4.3 PWM Input Stage

The PWM input stage generates from the external signals **INP**, **INSTP** and **EN/FEN** the turn-on and turn-off commands to the secondary side. The general structure of the PWM input block is shown **Figure 3**.



**Figure 3** PWM Input Stage

Signals **INP**, **INSTP** and **EN/FEN** are pseudo-differential, in the sense that they are not referenced to the common ground **GND1** but to signal **REF0**. This is intended to make the device more robust against ground bouncing effects.

*Note:* Glitches shorter than  $t_{INPR1}$  occurring at signal **INP** are filtered internally.

*Note:* Pulses at **INP** below  $t_{INPPD}$  might be distorted or suppressed.

The 1EDI2002AS supports non-inverted PWM signals only. When a High level on pin **INP** is detected while signals **INSTP** and **EN/FEN** are valid, a turn-on command is issued to the secondary chip. A Low level at pin **INP** issues a turn-off command to the secondary chip.

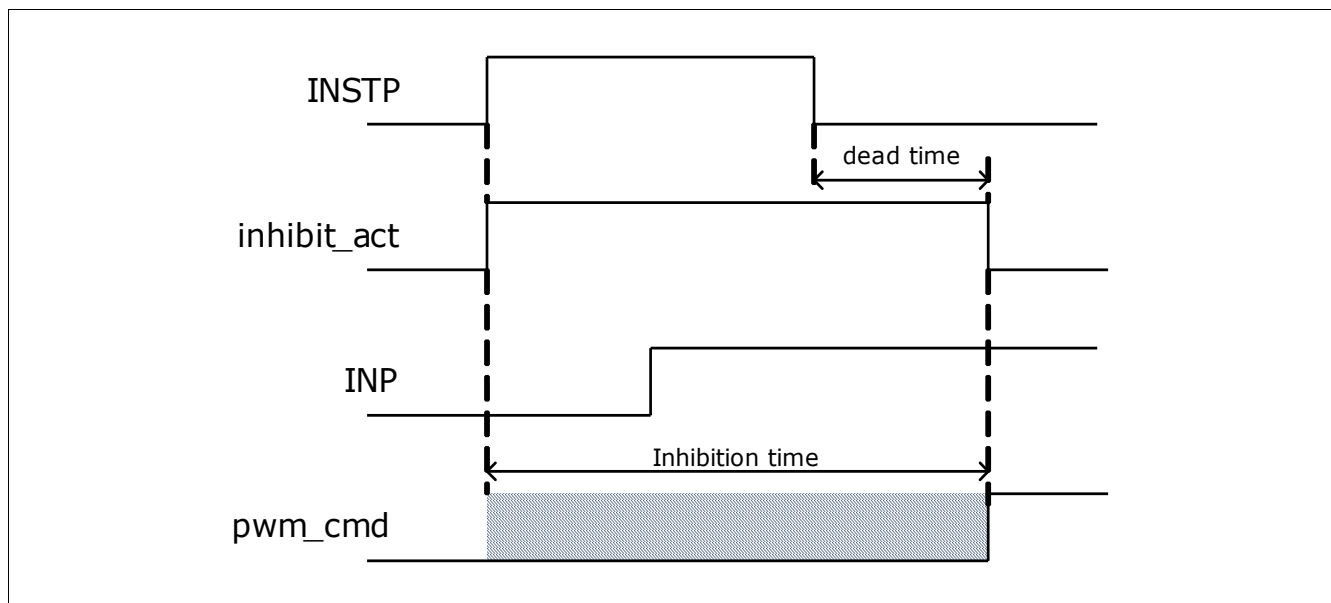
Signal **EN/FEN** can inhibit turn-on commands received at pin **INP**. A valid signal **EN/FEN** is required in order to have turn-on commands issued to the secondary chip. If an invalid signal is provided, the PWM input stage issues constantly turn-off commands to the secondary chip. The functionality of signal **EN/FEN** is detailed in **Chapter 2.4.8**.

*Note:* After an invalid-to valid-transition of signal **EN/FEN**, a minimum delay of  $t_{INPEN}$  should be inserted before turning **INP** on.

As shown in **Figure 4**, signal **INSTP** provides a Shoot-Through Protection (STP) to the system. When signal at pin **INSTP** is at High level, the internal signal `inhibit_act` is activated. The inhibition time is defined as the pulse duration of signal `inhibit_act`. It corresponds to the pulse duration of signal **INSTP** to which a minimum dead time is added. During the inhibition time, rising edges of signal **INP** are inhibited. Bit **PSTAT2.STP** is set for the duration of the inhibition time.

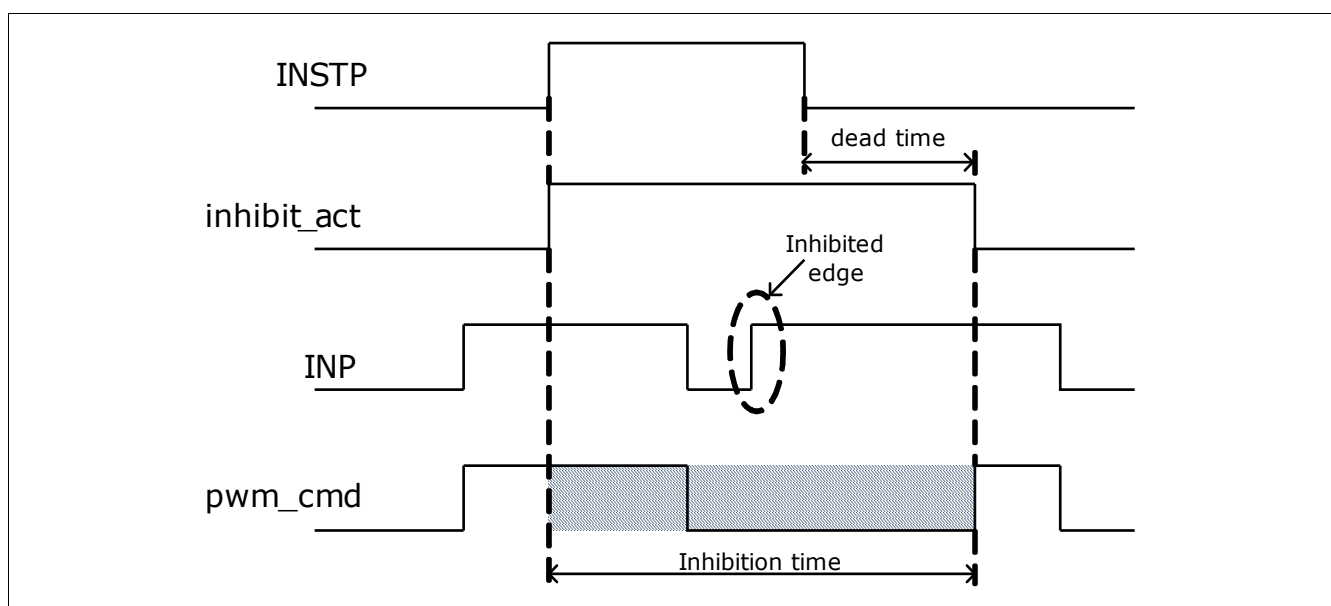
The deadtime is programmable with bit field **PCFG2.STPDEL**.

## Functional Description



**Figure 4 STP: Inhibition Time Definition**

It shall be noted that during the inhibition time, signal `pwm_cmd` is not forced to Low. It means that if the device is already turned-on when **INSTP** is High, it stays turned-on until the signal at pin **INP** goes Low. This is depicted in [Figure 5](#).



**Figure 5 STP: Example of Operation**

When a condition occurs where a rising edge of signal **INP** is inhibited, an error notification is issued. See [Chapter 3.4.1](#) for more details.

## **Functional Description**

### **2.4.4 SPI Interface**

This chapter describes the functionality of the SPI block.

#### **2.4.4.1 Overview**

The standard SPI interface implemented on the 1EDI2002AS is compatible with most of the microcontrollers available for automotive and industrial applications. The following features are supported by the SPI interface:

- Full-duplex bidirectional communication link.
- SPI Slave mode (only).
- 16-bit frame format.
- Daisy chain capability.
- MSB first.
- Parity Check (optional) and Parity Bit generation (LSB).

The SPI interface of the 1EDI2002AS provides a standardized bidirectional communication interface to the main microcontroller. From the architectural point of view, it fulfills the following functions:

- Initialization of the device.
- Configuration of the device (static and runtime).
- Reading of the status of the device (static and runtime).
- Operation of the verification modes of the device.

The purpose of the SPI interface is to exchange data which have relaxed timing constraints compared to the PWM signals (from the point of view of the motor control algorithm). The IGBT switching behavior is for example controlled directly by the PWM input. Similarly, critical application failures requiring fast reaction are notified on the primary side via the feedback signals **NFLTA**, **NFLTb** and **NRST/RDY**.

In order to minimize the complexity of the end-application and to optimize the microcontroller's resources, the implemented interface has daisy chain capability. Several (typically 6) 1EDI2002AS devices can be combined into a single SPI bus.

## Functional Description

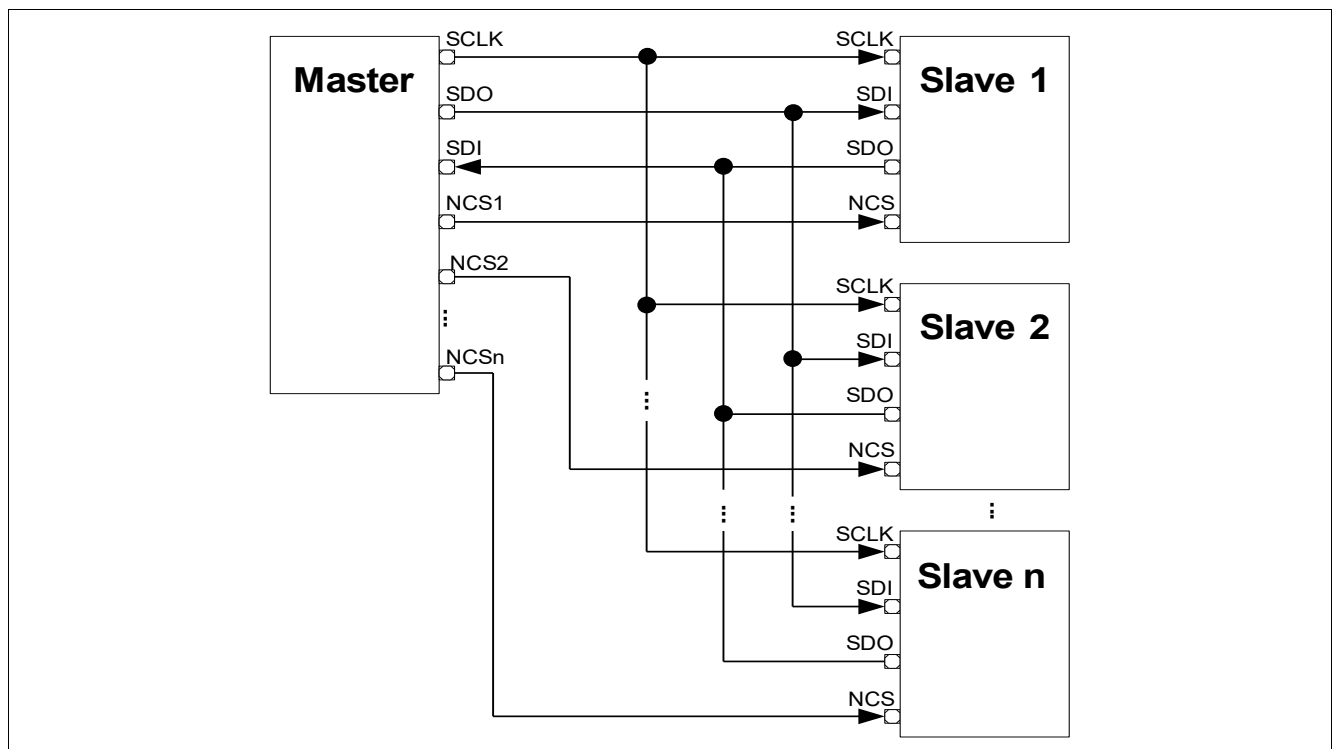
### 2.4.4.2 General Operation

The SPI interface of the 1EDI2002AS supports full duplex operation. The interface relies on four communication signals:

- **NCS**: (Not) Chip Select.
- **SCLK**: Serial Clock.
- **SDI**: Serial Data In.
- **SDO**: Serial Data Out.

The SPI interface of the 1EDI2002AS supports slave operation only. An SPI master (typically, the main microcontroller) is connected to one or several 1EDI2002AS devices, forming an SPI bus. Several bus topologies are supported.

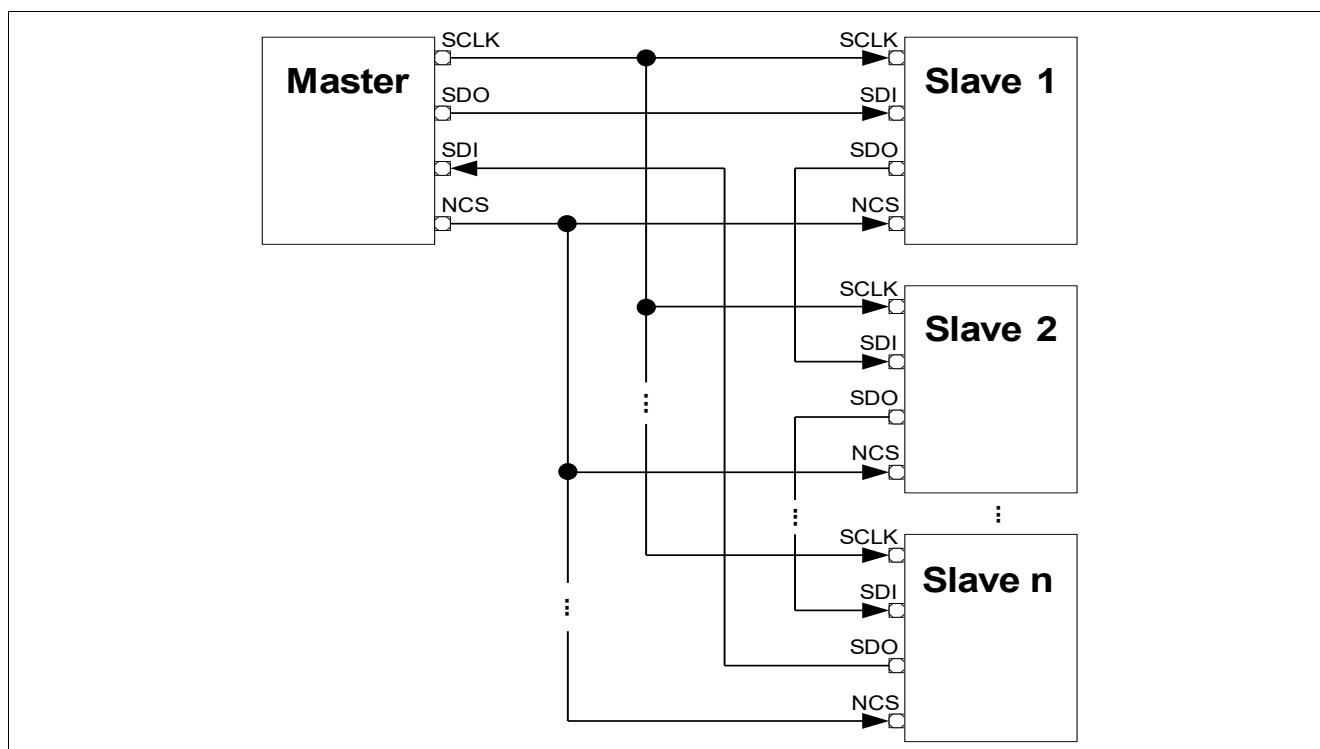
A regular SPI bus topology can be used where each of the slaves is controlled by an individual chip select signal (**Figure 6**). In this case, the number of slaves on the bus is only limited by the application's constraints.



**Figure 6 SPI Regular Bus Topology**

In order to simplify the layout of the PCB and to reduce the number of pins used on the microcontroller's side, a daisy chain topology can also be used. The chain's depth is not limited by the 1EDI2002AS itself. A possible topology is shown **Figure 7**.

## Functional Description



**Figure 7 SPI Daisy Chain Bus Topology**

### Physical Layer

The SPI interface relies on two shift registers:

- A shift output register, reacting on the rising edges of **SCLK**.
- A shift input register, reacting on the falling edges of **SCLK**.

When signal **NCS** is inactive, the signals at pins **SCLK** and **SDI** are ignored. The output **SDO** is in tristate.

When **NCS** is activated, the shift output register is updated internally with the value requested by the previous SPI access.

At each rising edge of the **SCLK** signal (while **NCS** is active), the shift output register is serially shifted out by one bit on the **SDO** pin (MSB first). At each falling edge of the clock pulse, the data bit available at the input **SDI** is latched and serially shifted into the shift input register.

At the deactivation of **NCS**, the SPI logic checks how many rising and falling edges of the **SCLK** signal have been received. In case both counts differ and / or are not a multiple of 16, an SPI Error is generated. The SPI block then checks the validity of the received 16-bit word. In case of a non valid data, an SPI error is generated. In case no error is detected, the data is decoded by the internal logic.

The **NCS** signal is active low.

### Input Debouncing Filters

The input stages of signals **SDI**, **SCLK**, and **NCS** include each a Debouncing Filter. The input signals are that way filtered from glitches and noise.

The input signals **SDI** and **SCLK** are analyzed at each edge of the internal clock derived from OSC1. If the same external signal value is sampled three times consecutively, the signal is considered as valid and is processed by the SPI logic. Otherwise, the transition is considered as a glitch and is discarded.

## **Functional Description**

The input signal **NCS** is sampled at a rate corresponding to the period of the internal clock derived from OSC1. If the same external signal value is sampled two times consecutively, the signal is considered as valid and is processed by the SPI logic. Otherwise, the transition is considered as a glitch and is discarded.

### **2.4.4.3 Definitions**

#### **Command**

A command is a high-level command issued by the SPI master which aims at generating a specific reaction in the addressed slave. The command is physically translated into a Request Message by the SPI master. The correct reception of the Request Message by the SPI slave leads to a specific action inside the slave and to the emission of an Answer Message by the slave.

Example: the READ command leads to the transfer of the value of the specified register from the device to the SPI master.

#### **Word**

A word is a 16-bit sequence of shifted data bits.

#### **Transfer**

A transfer is defined as the SPI data transfers (in both directions) occurring between a falling edge of **NCS** and the next consecutive rising edge of **NCS**.

#### **Request Message**

A request message is a word issued by the SPI master and addressing a single slave. A request message relates to a specific command.

#### **Answer Message**

An answer message is a well-defined word issued by a single SPI slave as a response to a request message.

#### **Transmit Frame**

A transmit frame is a sequence of one or several words sent by the SPI Master within one SPI transfer. In regular SPI topologies, a transmit frame is in practice identical to a data word. In daisy chain topologies, a transmit frame is a sequence of data words belonging to different request messages.

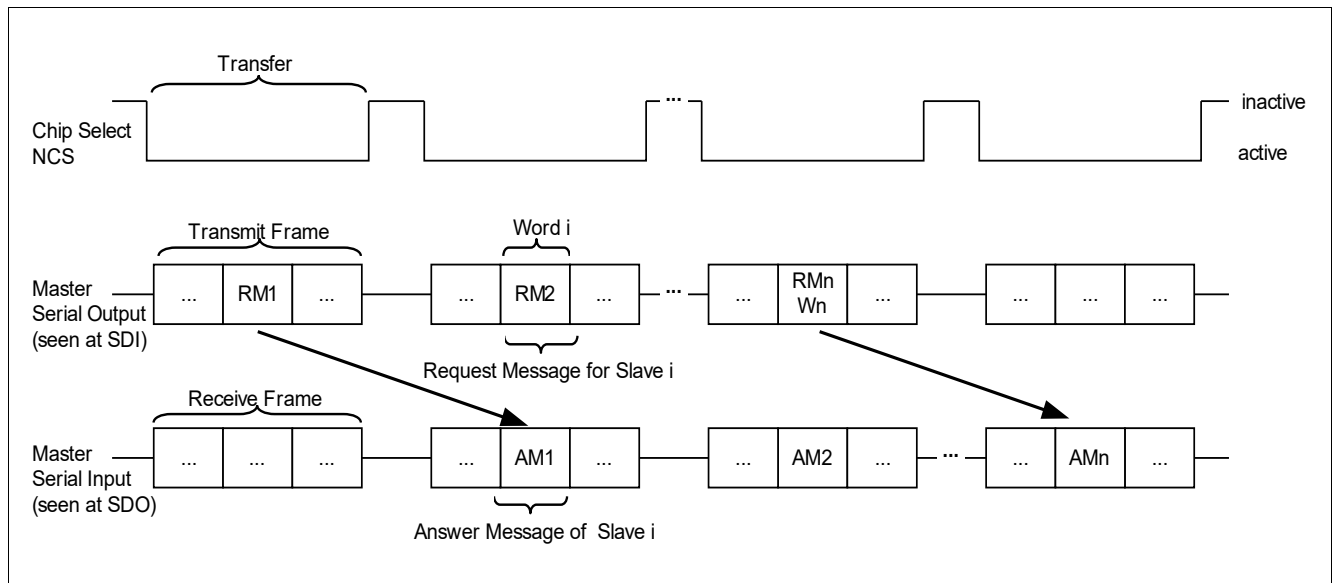
#### **Receive Frame**

A receive frame is a sequence of one or several words received by the SPI Master within one SPI transfer. In regular SPI topologies, a receive frame is in practice identical to a data word. In daisy chain topologies, a receive frame is a sequence of data words belonging to different Answer Messages.

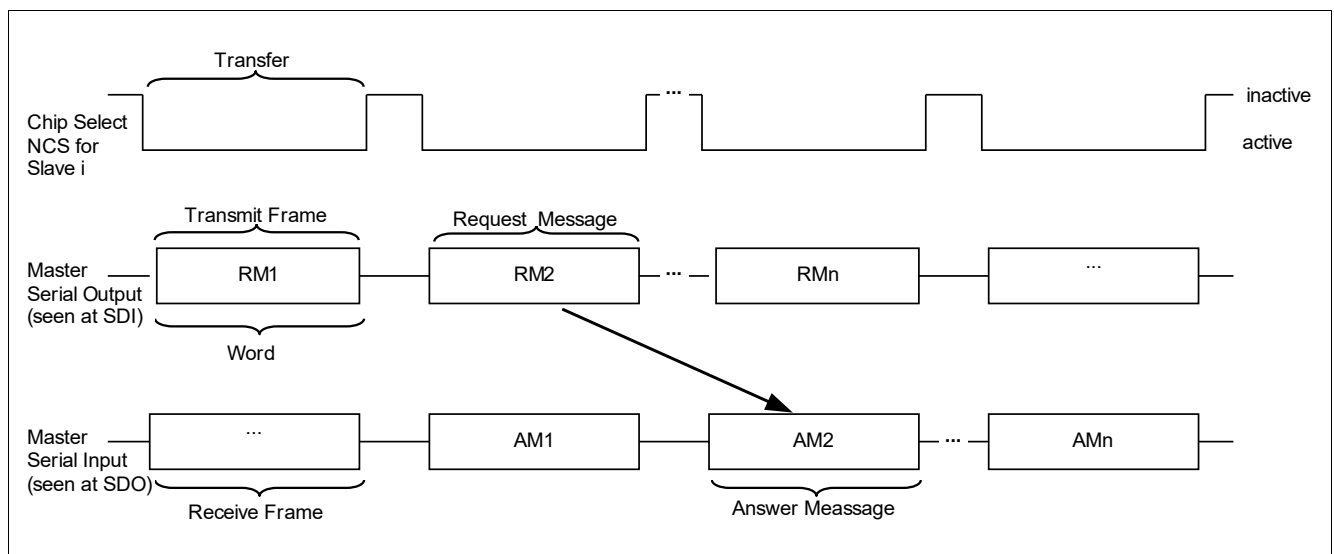
The SPI protocol supported by the 1EDI2002AS is based on the Request / Answer principle. The master sends a defined request message to which the slave answers with the corresponding answer message (**Figure 8**, **Figure 9**). Due to the nature of the SPI interface, the Answer Message is shifted, compared to the Request Message, by one SPI transfer. It means, for example, that the last word of answer message  $n$  is transmitted by the slave while the master sends the first word of request message  $n+1$ .



## Functional Description



**Figure 8 Response Answer Principle - Daisy Chain Topology**



**Figure 9 Response Answer Principle - Regular Topology**

The first word transmitted by the device after power-up is the content of register **PSTAT**.

## Functional Description

### 2.4.4.4 SPI Data Integrity Support

#### 2.4.4.4.1 Parity Bit

By default, the SPI link relies on an odd parity protection scheme for each transmitted or received 16-bit word of the SPI message. The parity bit corresponds to the LSB of the 16-bit word. Therefore, the effective payload of a 16-bit word is 15 data bit (plus one parity bit). The parity bit check (on the received data) can be disabled by clearing bit **PCFG.PAREN**. In this case, the parity bit is considered as “don’t care”. The generation of the parity bit by the driver for transmitted words can not be disabled (but can be considered as “don’t care” by the SPI master).

*Note: For fixed value commands (ENTER\_CMODE, ENTER\_VMODE, EXIT\_CMODE, NOP), it has to be ensured that the value of the parity bit is correct even if parity check is disabled. Otherwise, an SPI error will be generated.*

#### 2.4.4.4.2 SPI Error

When the device is not able to process an incoming request message, an SPI error is generated: the received message is discarded by the driver, bit **PER.SPIER** is set and the erroneous message is answered with an error notification (bit **LMI** set).

Several failures generate an SPI error:

- A parity error is detected on the received word.
- An invalid data word format is received (e.g. not a 16 bit word).
- A word is received, which does not corresponding to a valid Request Message.
- A command is received which can not be processed. For example, the driver receives in Active Mode a command which is only valid in other operating modes. Another typical example is a read access to the secondary while the previous read access is not yet completed (device “busy”).
- An SPI access to an invalid address.

*Note: the content of a frame with LMI bit set is the value of register **PSTAT**.*

*Note: In case of permanent LMI error induced by system failures, it is recommended to apply a reset via pin **NRST/RDY**.*

## Functional Description

### 2.4.4.5 Protocol Description

#### 2.4.4.5.1 Command Catalog

**Table 3** gives an overview of the command catalog supported by the device. The full description of the commands and of the corresponding request and answer messages is provided in the following sections.

**Table 3 SPI Command Catalog**

Acronym	Short Description	Valid in Mode
ENTER_CMODE	Enters into Configuration Mode.	OPM0, OPM1
ENTER_VMODE	Enters into Verification Mode.	OPM2
EXIT_CMODE	Leaves Configuration Mode to enter into Configured Mode.	OPM2
READ	Reads the register value at the specified address.	All
NOP	Triggers no action in the device (equivalent to a “nop”).	All
WRITEH	Update the most significant byte of the internal write buffer.	All
WRITEL	Updates the least significant byte of the internal write buffer, and copies the contents of the complete buffer into the addressed register. The write buffer is cleared afterwards.	All (with restrictions)

An overview of the commands is given **Figure 10**.

Message	Command				Data												P
ENTER_CMODE	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
ENTER_VMODE	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0
EXIT_CMODE	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0
NOP	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0
READ	0	0	0	0	A4	A3	A2	A1	A0	0	1	0	1	0	1	X	X
WRITEH	0	1	0	0	0	1	0	D15	D14	D13	D12	D11	D10	D9	D8	X	X
WRITEL	1	0	1	0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	X	X

**Figure 10 SPI Commands Overview**

#### 2.4.4.5.2 Word Convention

In order to simplify the description of the SPI commands, the following conventions are used (**Table 4**).

## Functional Description

**Table 4 Word Convention**

Acronym	Value
Va(REGISTER)	Value of register REGISTER
P <sub>B</sub>	Parity Bit
<<n	Left shift operation of n bits.
x <sub>H</sub>   y <sub>H</sub>	Result of the operation: x <sub>H</sub> OR y <sub>H</sub>

### 2.4.4.5.3 ENTER\_CMODE Command

The goal of this function is to set the device into Configuration Mode. After reception of a valid ENTER\_CMODE command, mode OPM2 is active. This command is only valid in Default Mode (OPM0 and OPM1). In case the request message is received while OPM1 is not active, the complete command is discarded and an SPI error occurs.

**Table 5** describes the request message and the corresponding answer message.

**Table 5 ENTER\_CMODE request and answer messages**

	Transfer 1	Transfer 2
Request message	1880 <sub>H</sub>	N.a.
Answer message	N.a.	Va( <b>PSTAT</b> )

### 2.4.4.5.4 ENTER\_VMODE Command

The goal of this function is to set the device into Verification Mode. After reception of a valid ENTER\_VMODE command, mode OPM5 is active. This command is only valid in Configuration Mode (OPM2). In case the request message is received while OPM2 is not active, the complete command is discarded and an SPI error occurs.

**Table 6** describes the request message and the corresponding answer message.

**Table 6 ENTER\_VMODE request and answer messages**

	Transfer 1	Transfer 2
Request message	1140 <sub>H</sub>	N.a.
Answer message	N.a.	Va( <b>PSTAT</b> )

### 2.4.4.5.5 EXIT\_CMODE Command

When a valid EXIT\_CMODE is received by the device, the Configuration Mode is left to Configured Mode (Mode OPM3 active). This command is only valid in Configuration Mode (OPM2). In case the request message is received while OPM2 is not active, the complete command is discarded and an SPI error occurs.

**Table 7** describes the request message and the corresponding answer message.

## Functional Description

**Table 7 EXIT\_CMODE request and answer messages**

	Transfer 1	Transfer 2
Request message	1220 <sub>H</sub>	N.a.
Answer message	N.a.	Va( <b>PSTAT</b> )

### 2.4.4.5.6 NOP Command

This command triggers no specific action in the driver (equivalent to a “nop”). However, the mechanisms verifying the validity of the word are active. This command is valid in all operating modes.

**Table 8** describes the request message and the corresponding answer message.

**Table 8 NOP request and answer messages**

	Transfer 1	Transfer 2
Request message	1410 <sub>H</sub>	N.a.
Answer message	N.a.	Va( <b>PSTAT</b> )

### 2.4.4.5.7 READ Command

This command aims at reading the value of the register whose address is specified in the request message. This command is valid in all operating modes. However, in OPM4 and OPM6, the use of the READ command is restricted (see **Table 39**). If an access outside the allowed address range is performed, the access is discarded as invalid and an SPI error occurs.

**Table 9** describes the request message and the corresponding answer message.

**Table 9 READ request and answer messages**

	Transfer 1	Transfer 2
Request message	See below	N.a.
Answer message	N.a.	Va(Register)

#### Request message words

Word 1: ( ADDRESS\_5BIT << 7 ) | 002A<sub>H</sub> | P<sub>B</sub>.

#### Answer message words

Word 1: Value of REGISTER.

### 2.4.4.5.8 WRITEH

This command aims at writing the upper byte of the internal write buffer with the specified value. This command has no other effect on the functionality of the device. This command is valid in all operating modes.

**Table 10** describes the request message and the corresponding answer message.

## Functional Description

**Table 10 WRITEH request and answer messages**

	Transfer 1	Transfer 2
Request message	See below	N.a.
Answer message	N.a.	Va( <b>PSTAT</b> )

### Request message words

Word 1:  $4400_H \mid (DATA\_8BIT \ll 1) \mid P_B$

### 2.4.4.5.9 WRITEL

This command aims at updating the value of the register whose address is specified in the request message. This command is valid in all operating modes. However, depending on the active operating mode, this command is restricted to a given address range or specific registers (see [Table 40](#)). If an access outside the allowed address range is performed, the access is discarded as invalid and an SPI error occurs.

At the reception of this command, the least significant byte of the internal buffer is written with the specified value, the contents of the buffer is copied to the register at the specified address and the complete write buffer is cleared.

[Table 11](#) describes the request message and the corresponding answer message.

**Table 11 WRITEL request and answer messages**

	Transfer 1	Transfer 2
Request message	See below	N.a.
Answer message	N.a.	Va( <b>PSTAT</b> )

### Request message words

Word 1:  $A000_H \mid (ADDRESS\_5BIT \ll 7) \mid (DATA\_6BIT \ll 1) \mid P_B$ .

## Functional Description

### 2.4.5 Operating Modes

#### 2.4.5.1 General Operation

At any time, the driver can be in one out of seven possible operating modes:

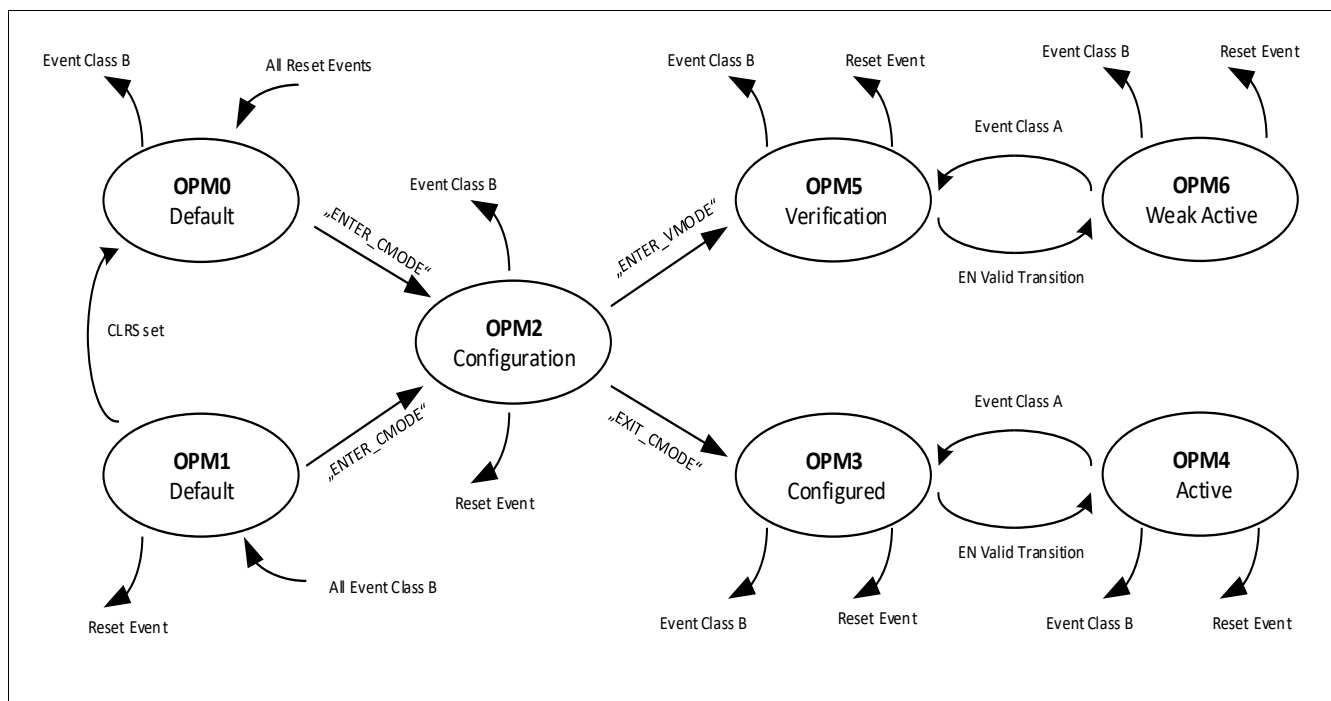
- OPM0: Default Mode (default after reset, device is disabled).
- OPM1: Error Mode (reached after Event Class B, device is disabled).
- OPM2: Configuration Mode (device is disabled, configuration of the device can be modified).
- OPM3: Configured Mode (device is configured and disabled).
- OPM4: Active Mode (normal operation).
- OPM5: Verification mode (intrusive diagnostic functions can be triggered).
- OPM6: Weak active mode (the device can be turned on but with restrictions)

The current active mode of the device is given by bit field **SSTAT.OPM**.

The concept of the device is based on the following general ideas:

- The driver can only switch the IGBT on when OPM4 mode is active (exception: weak-turn on in OPM6).
- Starting from Mode OPM0 or OPM1, the Active Mode OPM4 can only be activated through a dedicated SPI command sequence and the activation of the hardware signal **EN/FEN**. As a result, the probability that the device goes to OPM4 mode due to random signals is negligible.
- Differentiations of errors: different classes of errors are defined, leading to different behavior of the device.

The state diagram for the operating modes is given in **Figure 11**:



**Figure 11 Operating Modes State Diagram**

## Functional Description

### 2.4.5.2 Definitions

#### 2.4.5.2.1 Events and State Transitions

The transitions from one state to the other are based on “events” and / or SPI commands. The following classification is chosen for defining the events.

##### Events Class A

The following (exhaustive) list of events are defined as Events Class A:

- Occurrence of a DESAT event (leads to a safe turn-off sequence).
- Occurrence of an OCP event (leads to a safe turn-off sequence).
- Valid to Invalid transition on **EN/FEN** signal (leads to a regular turn-off sequence).
- Tristate event due to an Output Stage Monitoring event.
- Tristate event due to the activation of signal **OSD**.

When an Event Class A occurs, the output stage either initiates either a safe turn-off sequence (DESAT, OCP, or a regular turn-off sequence (**EN/FEN** event) or goes in tristate (tristate event). The event is notified via an error bit in the corresponding register.

*Note: Contrarily to a reset event, an Event Class A does not affect the contents of the configuration registers.*

When an Event Class A occurs, the device may change its operating mode depending on which mode is active when the event occurs:

- If it was in OPM4, it goes in OPM3.
- If it was in OPM6, it goes in OPM5.

In all other cases, the OPM is unaffected. A state transition due to an Event Class A leads to the activation of signal **NFLTA**. If no state transition occurs (if for example the device was not in OPM4 or OPM6), **NFLTA** is not activated (exception: tristate event - see **Chapter 2.4.7** for more details on failure notifications).

##### Events Class B

The following (exhaustive) list of events are defined as Events Class B:

- Occurrence of a UVLO2 event.
- Occurrence of a OVLO2 event.
- Occurrence of a UVLO3 event.
- Occurrence of a OVLO3 event (with bit **SCFG2.OVLO3D** set).
- Internal Supervision Error.
- Verification Mode Time Out Error

When an Event Class B occurs, the output stage initiates a regular turn-off sequence. The event is notified via an error bit in the corresponding register and (possibly) via the signal **NFLT B**.

*Note: Events Class B may affect the contents of the configuration registers.*

When an Event Class B occurs, the device may change its operating mode depending on which mode is active when the event occurs: if it was not in OPM1, it goes to OPM1. It is unaffected otherwise



## Functional Description

A state transition due to an Event Class B leads to the activation of signal **NFLT B**. If no state transition occurs (if for example the device was already in OPM1), **NFLT B** is not activated. See [Chapter 2.4.7](#) for more details on failure notifications.

*Note: Events class A and class B can occur quasi simultaneously, in both orders. Hence, in case an event A and an event B occur while one is not finally processed, an emergency turn-off is triggered accordingly.*

### Events Class C

Generally speaking, Events Class C are error events that do not lead to a change of the operating mode of the device. The following (non-exhaustive) list of events is comprised within the Event Class C:

- Over Temperature Warning.
- SPI Error.
- Shoot Through Protection error.
- Etc.

### SPI Commands

The following SPI commands have an impact on the device's operating mode. The SPI commands are described in [Chapter 2.4.4.5](#).

- ENTER\_CMODE.
- ENTER\_VMODE.
- EXIT\_CMODE.
- Setting of bit **SCTRL.CLRS** (by writing register **PCTRL**)

### Reset Events

A reset sets the device (or part of the device) in its default state. Reset events are described in [Chapter 2.4.9](#).

#### 2.4.5.2.2 Emergency Turn-Off Sequence

The denomination "Emergency Turn-Off Sequence" (ETO) is used to describe the sequence of actions executed by the output stage of the device when an Event Class A (exception: tristate event), Class B or a Reset Event is detected.

An ETO sequence is described by the following set of actions:

- A Turn-Off sequence is initiated. In case of DESAT or OCP event, a safe turn-off sequence is initiated. For the other events, a regular turn-off sequence is initiated.
- The device enters the corresponding OPM mode. As a consequence, the device is disabled.

Once an ETO has been initiated, the device can not be reenabled for a maximum duration consisting of 256 OSC2 clock cycles. Consequently, the user shall wait for this duration before reenabling the device and sending PWM turn-on command.

## Functional Description

### 2.4.5.2.3 Ready, Disabled, Enabled and Active State

The device is said to be in Ready state in case no reset event is active on the primary chip. When the device is Ready, signal **NRST/RDY** is at High level.

When the device is in Disabled State, the PWM turn-on commands are ignored. This means that whatever the input signal **INP** is, the output stage (if not tristated) delivers a constant turn-off signal to the IGBT. Unless otherwise stated, all other functions of the device work normally.

When the device is not in Disabled State, it is said to be in Enabled State. In this case, the PWM signal command is processed normally (if the output stage is not tristated). Practically, the device is in Enabled State when either Mode OPM4 or Mode OPM6 is active.

Active State corresponds to the normal operating state of the device. Practically, the device is in Active State when Mode OPM4 is active.

*Note: When the device is in Active State, it implicates it is in Enabled state.*

### 2.4.5.3 Operation Modes Description

#### Default Mode (OPM0)

Mode OPM0 is the default operating mode of the device after power up or after a rest event. In OPM0, the device is in Disabled State.

The following exhaustive list of events bring the device in OPM0 Mode:

- Occurrence of a Reset Event.
- Bit **SCTRL.CLRS** set while the device was in OPM1.

#### Error Mode (OPM1)

Mode OPM1 is the operating mode of the device after an Event Class B.

The following exhaustive list of events bring the device in OPM1 Mode:

- Occurrence of an Event Class B.

In OPM1, when bit **SCTRL.CLRS** is set via the corresponding SPI command, the device shall normally jump to OPM0. However, in case the conditions for an Event Class B are met at that moment, no state transition occurs and the device stays in OPM1. The operation of bit **SCTRL.CLRS** on the secondary sticky bits works normally.

In OPM1, when a valid ENTER\_CMODE command is received, the device shall normally jump to OPM2. However, in case the conditions for an Event Class B are met at that moment, no state transition occurs and the device stays in OPM1 for the duration of the event. The state transition to OPM2 is executed as soon as the conditions leading to the Event Class B disappear. It shall be noted that no LMI error notification is issued.

#### Configuration Mode (OPM2)

Configuration Mode is the mode where the configuration of the device can be modified. When OPM2 is active, the device is in Disabled State.

The following exhaustive list of events bring the device in Configuration Mode:

- Reception of a valid ENTER\_CMODE command **while** Mode OPM0 or OPM1 active.

## Functional Description

### Configured Mode (OPM3)

Configured Mode is the mode where the device is ready to be enabled. When OPM3 is active, the device is in Disabled State.

The following exhaustive list of events bring the device in Mode OPM3:

- Reception of a valid EXIT\_CMODE command **while** Mode OPM2 active.
- Event Class A **while** Mode OPM4 active.

### Active Mode (OPM4)

The Active Mode corresponds to the normal operating mode of the device. When OPM4 is active, the device is in Active State. The following exhaustive list of event bring the device in Active Mode:

- Invalid to Valid Transition on signal **EN/FEN** **while** Mode OPM3 active.

### Verification Mode (OPM5)

Verification Mode is the mode where intrusive verification functions can be started. When OPM5 is active, the device is in disabled state.

The following exhaustive list of event bring the device in Verification Mode:

- Reception of a valid ENTER\_VMODE command **while** Mode OPM2 active.
- Occurrence of an Event Class A **while** Mode OPM6 active.

After a transition from Mode OPM2 to OPM5, an internal watchdog timer is started. If after time  $t_{VMTO}$ , the device has not left both modes OPM5 or OPM6, a time-out event occurs and an Event Class B is generated.

### Weak Active Mode (OPM6)

Weak Active Mode is the mode where the device can be activated to run diagnosis tests at system level. When OPM6 is active, the device is in Enabled State. A PWM turn-on command issues a Weak Turn-On on the secondary side.

The following exhaustive list of event bring the device in Weak Active Mode:

- Invalid to Valid Transition on signal **EN/FEN** **while** Mode OPM5 active.

The watchdog counter started when entering Mode OPM5 is not reset when entering OPM6.

### Implementation Notes related to State Transitions

- An Event Class A or Class B detected on the secondary side lead to an immediate reaction of the device's output stage. Due to the latency of the inter-chip communication, the notification on the primary side is slightly delayed.
- The activation of signal **NFLTA** or **NFLTB** is simultaneous to the corresponding state transition on the primary side.
- It is possible to change the operating mode while a failure condition is present. This may however lead to a new immediate error notification and state transition.

## Functional Description

### 2.4.5.4 Activating the device after reset

After a reset event, the device is in Mode OPM0 and disabled. In order to be active, the device needs to enter Configuration Mode with the ENTER\_CMODE command. Once all the configurations have been performed, the Configuration Mode has to be exited with an EXIT\_CMODE command. Once this is done, the device can enter the Active Mode when Invalid to Valid transition on pin **EN/FEN** is detected.

### 2.4.5.5 Activating the device after an Event Class A or B

If during operation, an Event Class A occurs, the device enters the OPM3 (or OPM5). Bit field **SSTAT.OPM** is updated accordingly. In order to reactivate the device, an invalid-to-valid transition has to be applied to signal **EN/FEN**. It means for example in EN Mode, that a Low-level and then a High level is applied to **EN/FEN**. If no Event Class A event is active, the device will enter OPM4 (respectively OPM6).

If during operation, an Event Class B occurs, the device enters the Default Mode OPM1. Bit field **SSTAT.OPM** is updated accordingly. In order to reactivate the device, the steps defined in [Chapter 2.4.5.4](#) need to be performed.

### 2.4.5.6 Debug Mode

The **DEBUG** pin gives the possibility to operate the device in the so-called Debug Mode. The goal of the Debug Mode is to operate the device without SPI interface. This mode should be used for development purpose only and is not intended to be used in final applications.

At  $V_{CC2}$  power-on, the level at pin **DEBUG** is latched. In case a High level is detected, the device enters the Debug Mode. Bit **SSTAT.DBG** is then set.

In Debug Mode, the regular operation of the internal state machine is modified, so that the device can only enter OPM3 or OPM4. As a result Modes OPM0, OPM1, OPM2, OPM5 and OPM6 are completely bypassed. In case of a Reset event, the device goes to OPM3 (instead of OPM0). Besides, in Debug Mode, events leading normally to an Event Class B are replaced an Event Class A, resulting in the activation of signal **NFLTA**. Event Class B are therefore not generated by the device in Debug Mode (and signal **NFLTB** shall not be used).

It should be noted that the configuration of the device in Debug Mode corresponds to the default settings and can not be changed.

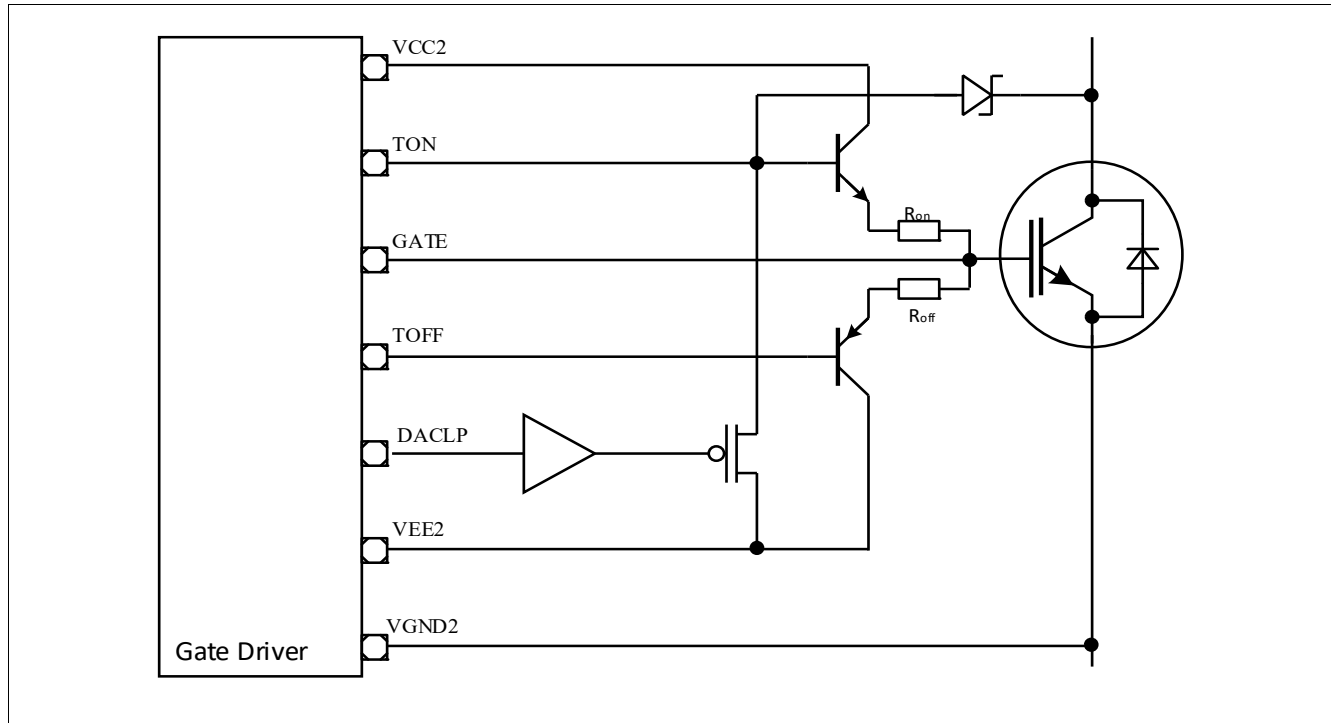
In Debug Mode, the operation of the device is otherwise similar to regular operation. It means in particular that the signal **EN/FEN** has to be managed properly: when the device is in OPM3, a Low to High level transition has to be applied to the device in order to enter OPM4 (Active Mode).

*Note: Once it has been latched at power-on, the level on the pin **DEBUG** has no impact on the device until the next power-on event on the secondary side.*

## Functional Description

### 2.4.6 Driver Functionality

The structure of the output stage and its associated external booster of the device is depicted **Figure 12**:



**Figure 12** Output Stage Diagram of Principle

#### 2.4.6.1 Overview

Two turn-off behaviors are supported by the device, depending on the event causing the turn-off action.

- Regular Turn-Off.
- Safe Turn-Off.

A Safe Turn-Off sequence uses the timing and plateau level parameters defined in register **SSTOF**. It is triggered by a DESAT or an OCP event only. A turn-off sequence which is not “Safe” is then “Regular”. A Regular Turn-Off sequence uses the timing parameters defined in register **SRTTOF** and the plateau level defined by **SCTRL.GPOFS**.

#### Two Level Turn-Off (TTOFF)

Because a hard turn-off may generate a critical overvoltage on the IGBT leading eventually to its destruction, the 1EDI2002AS supports the Two Level Turn-Off functionality (TTOFF). The TTOFF function consists in switching the IGBT off in three steps in such a way that:

1. The IGBT gate voltage is first decreased with a reduced slew rate until a specific (and programmable) voltage is reached by the **TOFF** signal.
2. **TOFF** (and **TON**) voltage is stabilized at this level. The IGBT Gate voltage forms thus a plateau.
3. Finally, the switch-off sequence is resumed using hard commutation.

The TTOFF delays and plateau voltage are fully programmable using the corresponding SPI commands. For a Regular Turn-Off sequence, the TTOFF delay is defined by bit field **SRTTOF.RTVAL**. Setting this field to 00<sub>H</sub> completely disables the TTOFF function for all Regular Turn-Off sequences (but this has no effect on Safe Turn-

## Functional Description

Off sequences). The plateau level is defined by **SCTRL.GPOFS**. If this function is to be activated, a minimum value for the delay time has to be programmed.

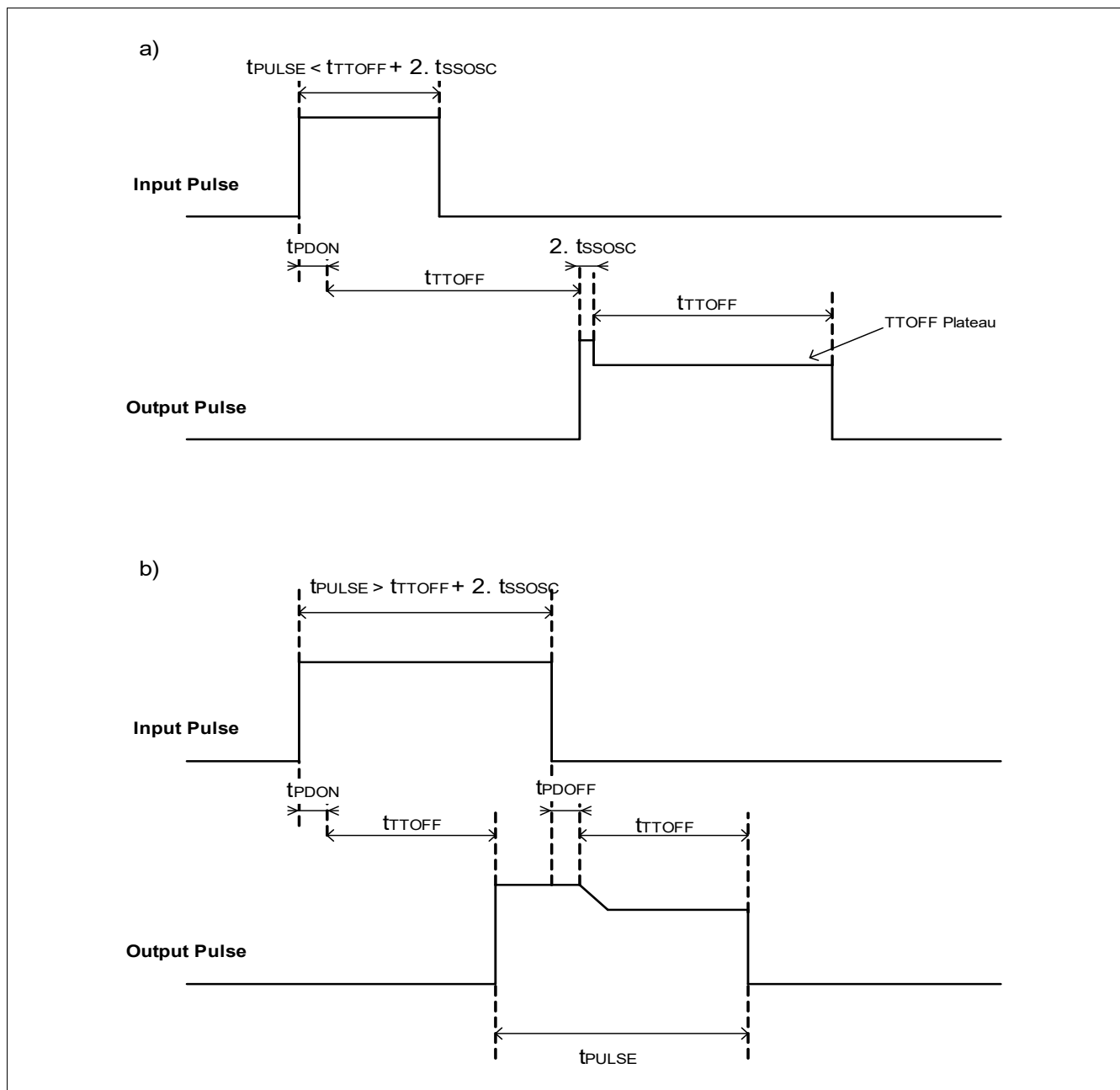
For a Safe Turn-Off sequence, the TTOFF delay is defined by bit field **SSTTOF.STVAL**. Setting this field to 00<sub>H</sub> completely disables the TTOFF function for all Safe Turn-Off sequences (but this has no effect on Regular Turn-Off sequences). If this function is to be activated, a minimum value for the delay time has to be programmed. The plateau level is defined by **SSTTOF.GPS**.

The timing of a Safe Turn-Off event is in the clock domain of the main secondary oscillator (OSC2). The timing of a Regular Turn-Off event is in the clock domain of the Start-Stop Oscillator (SSOSC2), leading to high accuracy and low PWM distortion

When using the TTOFF function (with a non-zero delay), the PWM command is received on pin **INP** is delayed by the programmed delay time (**Figure 13**). For pulses larger than the TTOFF delay ( $t_{\text{PULSE}} > t_{\text{TTOFF}} + 2 \times \text{SSOSC}$  cycles), the output pulse width is kept identical to the input pulse width. For smaller pulses ( $t_{\text{PULSE}} < t_{\text{TTOFF}} + 2 \times \text{SSOSC}$  cycles), the output pulse is identical to the programmed delay. The minimum pulse width delivered by the device to the IGBT is therefore the programmed delay time extended by two SSOSC cycles.

The device allows for external booster voltage compensation at the IGBT gate. When bit **SCFG.VBEC** is cleared, the voltage at **TOFF** at the plateau corresponds to the programmed value. When bit **SCFG.VBEC** is set, an additional  $V_{\text{BE}}$  (base emitter junction voltage of an internal pn diode) is subtracted from the programmed voltage at **TOFF** in order to compensate for the  $V_{\text{BE}}$  of an external booster.

## Functional Description



**Figure 13 TTOFF: Principle of Operation**

### Two Level Turn-On (TTON)

In order to increase EM compatibility and the efficiency of the whole system, the 1EDI2002AS supports the Two Level Turn-On functionality (TTON). The TTON function consists in switching the IGBT on in three steps in such a way that:

1. The IGBT gate voltage is first increased until a specific (and programmable) voltage is reached by the **TON** signal.
2. **TON** (and **TOFF**) voltage is stabilized at this level. The IGBT Gate voltage forms thus a plateau.
3. Finally, the switch-on sequence is resumed up to the maximum output voltage.

The TTON feature needs to be activated by configuring the delay with bit field **SCFG2.TTOND**.

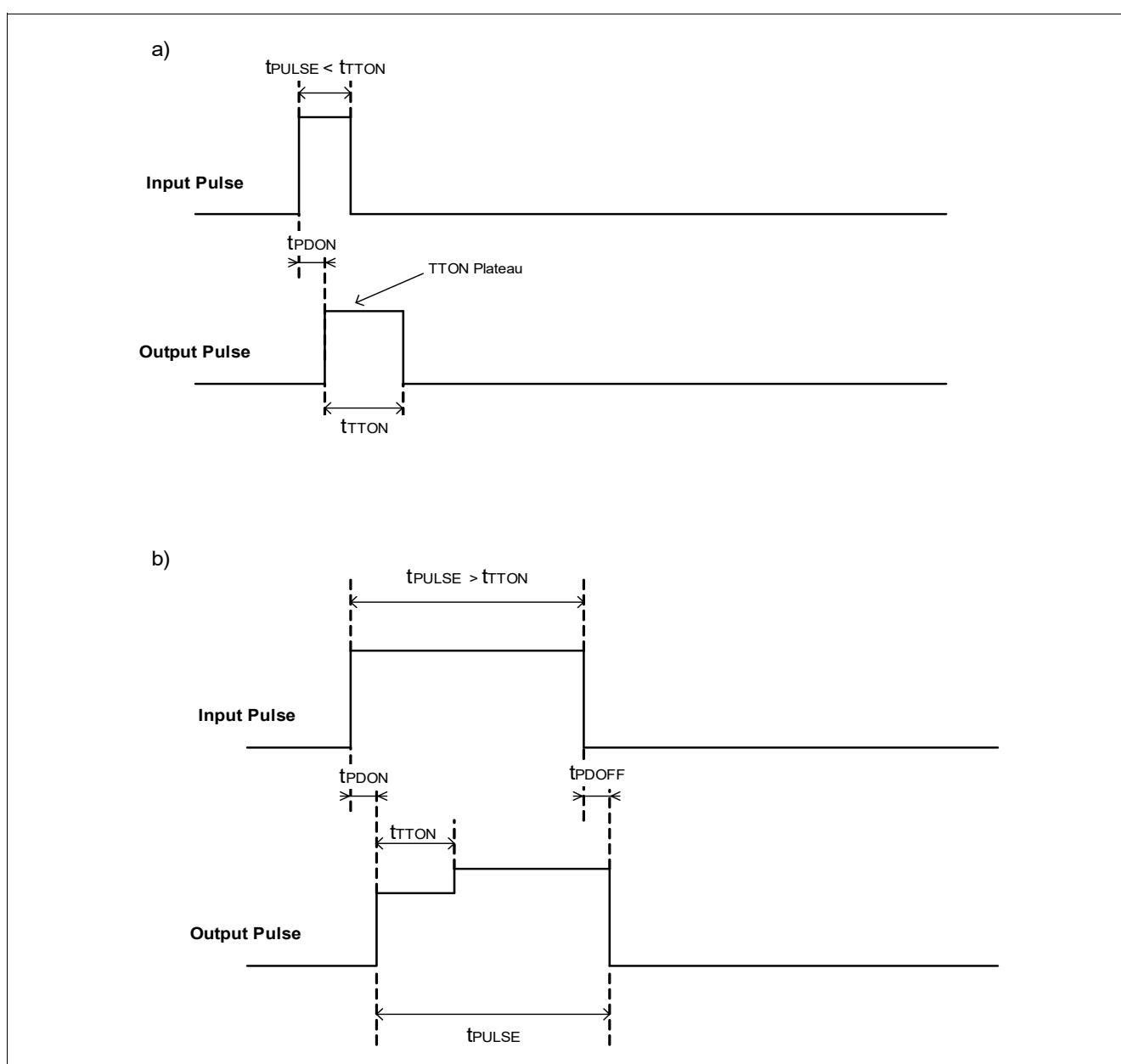
## Functional Description

The plateau voltage level can be configured during run time by updating bit field **SCTRL.GPONS**. This bit field can also be programmed to a value generating a hard turn-on.

When using the TTON function (with a non-zero delay), the PWM command is received on pin **INP** is **not** delayed by the programmed TTON delay time (**Figure 14**). However, the minimum pulse width that can be generated corresponds to the programmed TTON delay. Thus, for input pulses smaller than the TTON delay ( $t_{PULSE} < t_{TTON}$ ), the output pulse width is extended.

The device allows for external booster voltage compensation at the IGBT gate. When bit **SCFG2.VBEC** is cleared, the voltage at **TON** at the plateau corresponds to the programmed value. When bit **SCFG2.VBEC** is set, an additional  $V_{BE}$  (base emitter junction voltage of an internal pn diode) is **added** to the programmed voltage at **TON** in order to compensate for the  $V_{BE}$  of an external booster.

The TON and TTOFF functions can be used simultaneously.



**Figure 14 TTON: Principle of Operation**



## Functional Description

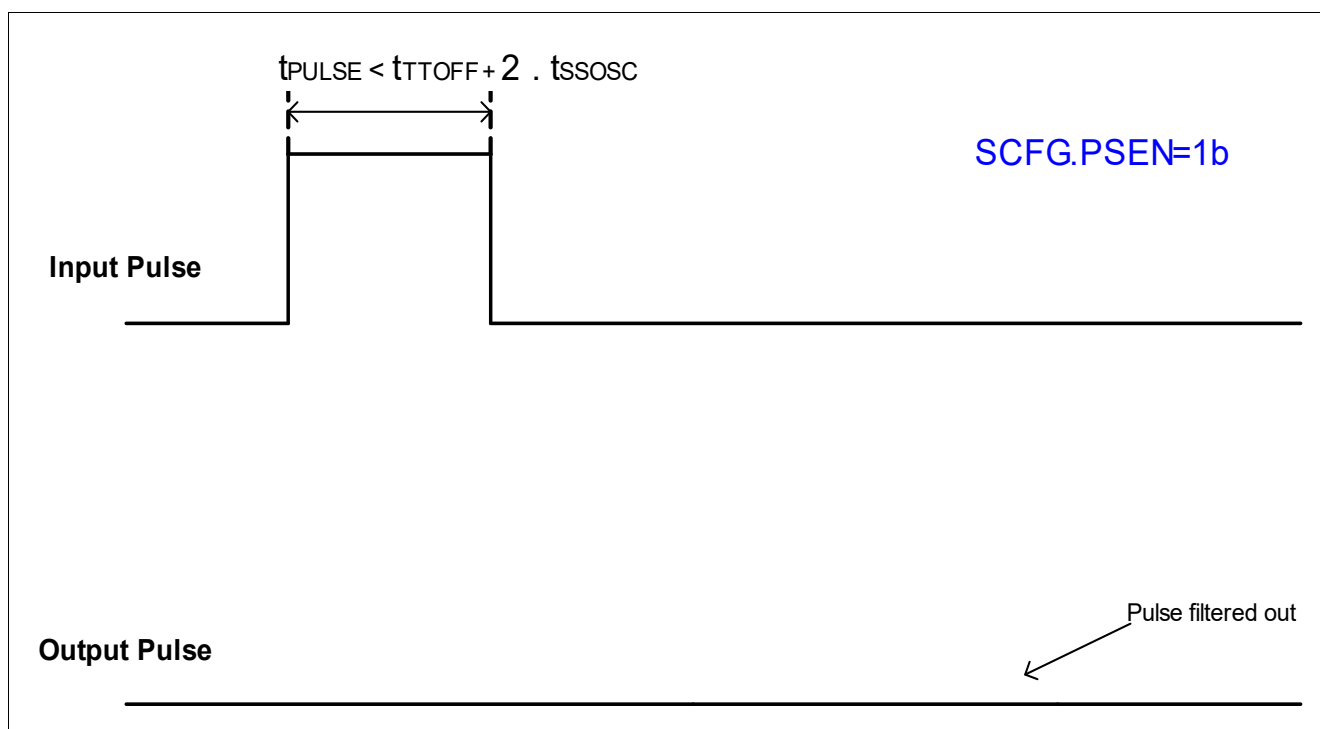
### Pulse Suppressor

In order to increase the device's robustness against external disturbances, a pulse suppressor can be enabled by setting bit **SCFG.PSEN**. Register **SRTTOF** shall also be programmed with a value higher than  $2_{H_1}$ . When a PWM turn-on sequence occurs, the activation of the output stage is delayed by the programmed TTOFF number of cycles, as for a normal TTOFF sequence. However, the PWM command received by the secondary chip signal is internally sampled at every SSOSC cycle before the actual turn-on command is executed by the output stage. If at least one of the sampling point does not detect a high level, the turn-on sequence is aborted and the device is not switched on.

In case a valid PWM ON command is detected by the secondary side after the decision point the previous sequence has been aborted, a new turn-on sequence is initiated.

One of the consequence of activating the pulse suppressor is that all PWM pulses shorter than the programmed TTOFF plateau time are filtered out (**Figure 15**).

*Note: The Pulse Suppressor only acts on turn-on pulses, not on turn-off pulses.*



**Figure 15 TTOFF: pulse suppressor aborting a turn-on sequence**

## Functional Description

### 2.4.6.2 Switching Sequence Description

**Figure 16** shows an idealized switching sequence. When a valid turn-on command is detected, a certain propagation time  $t_{PDON}$  is needed by the logic to transfer the PWM command to the secondary side. At this point the TTOFF delay time  $t_{TTOFF}$  defined by bit field **SRTTOF.RTVAL** is added before the turn-on command is executed. Signal **TON** is then activated, while signal **TOFF** is deactivated.

In case the two level turn-on function is active, signal **TON** is increased up to the plateau voltage defined by bit field **SCTRL.GPONS**. The duration  $t_{TTON}$  between the beginning of the turn-on sequence and the moment where the switching sequence is resumed is defined by bit field **SCFG2.TTOND**.

When a valid turn-off command is detected, a certain propagation time  $t_{DOFF}$  is needed by the command to be processed by the logic on the secondary side. This propagation time depends on the event having generated the turn-off action (non exhaustive list):

- In case of a PWM turn-off command at pin **INP**,  $t_{DOFF} = t_{PDOFF}$ .
- In case of a DESAT Event,  $t_{DOFF} = t_{OFFDESAT2}$ .
- In case of an OCP event,  $t_{DOFF} = t_{OFFOCP2}$ .
- In case of an Event Class A on the primary side:  $t_{DOFF} = t_{OFFCLA}$ .
- In case of an Event Class B on the secondary side:  $t_{DOFF} = t_{OFFCLB2}$ .

When the turn-off command is processed by the logic, signal **DACL** is deactivated (i.e. active clamping is enabled). Signal **TON** and **TOFF** are decreased with the slew rate  $t_{SLEW}$  fixed by hardware. Once the voltage at pin **TOFF** has reached the value defined by bit field **SCTRL.GPOFS** (or **SSTTOF.GPS** in the case of a safe turn-off), the turn-off sequence is interrupted. Time  $t_{TTOFF}$  is defined as the moment when the device starts turning off signal **TOFF**, and the moment where the turn-off sequence is resumed. Depending on the event that triggered the turn-off sequence,  $t_{TTOFF}$  is given by either bit field **SRTTOF.RTVAL** or **SSTTOF.STVAL**. Once the TTOFF time has elapsed, a hard commutation takes place, and signals **TON** and **TOFF** are driven to  $V_{EE2}$ .

*Note: Once a turn-off sequence is started, it is completed to the end with the same delay parameters.*

At the moment when the hard commutation takes place, signal **DACL** remains deactivated for time  $t_{ACL}$  defined by bit field **SACLT.AT**. When this time is elapsed, signal **DACL** is reactivated (i.e. active clamping is disabled).

When bit **SCFG2.ACLPM** is set, signal **DACL** is only deactivated in case of a safe turn-off sequence, for a total duration  $t_{ACL}$  (+  $t_{TTOFF}$ , if applicable).

In case **SACLT.AT** is set to  $0_H$ , **DACL** is constantly activated (constant High level). In case **SACLT.AT** is set to  $FF_H$ , **DACL** is constantly at Low level.

The Gate Monitoring function (time-out mechanism) is started at each turn-on and turn-off sequence. See **Chapter 3.4.2** for more details.

## Functional Description

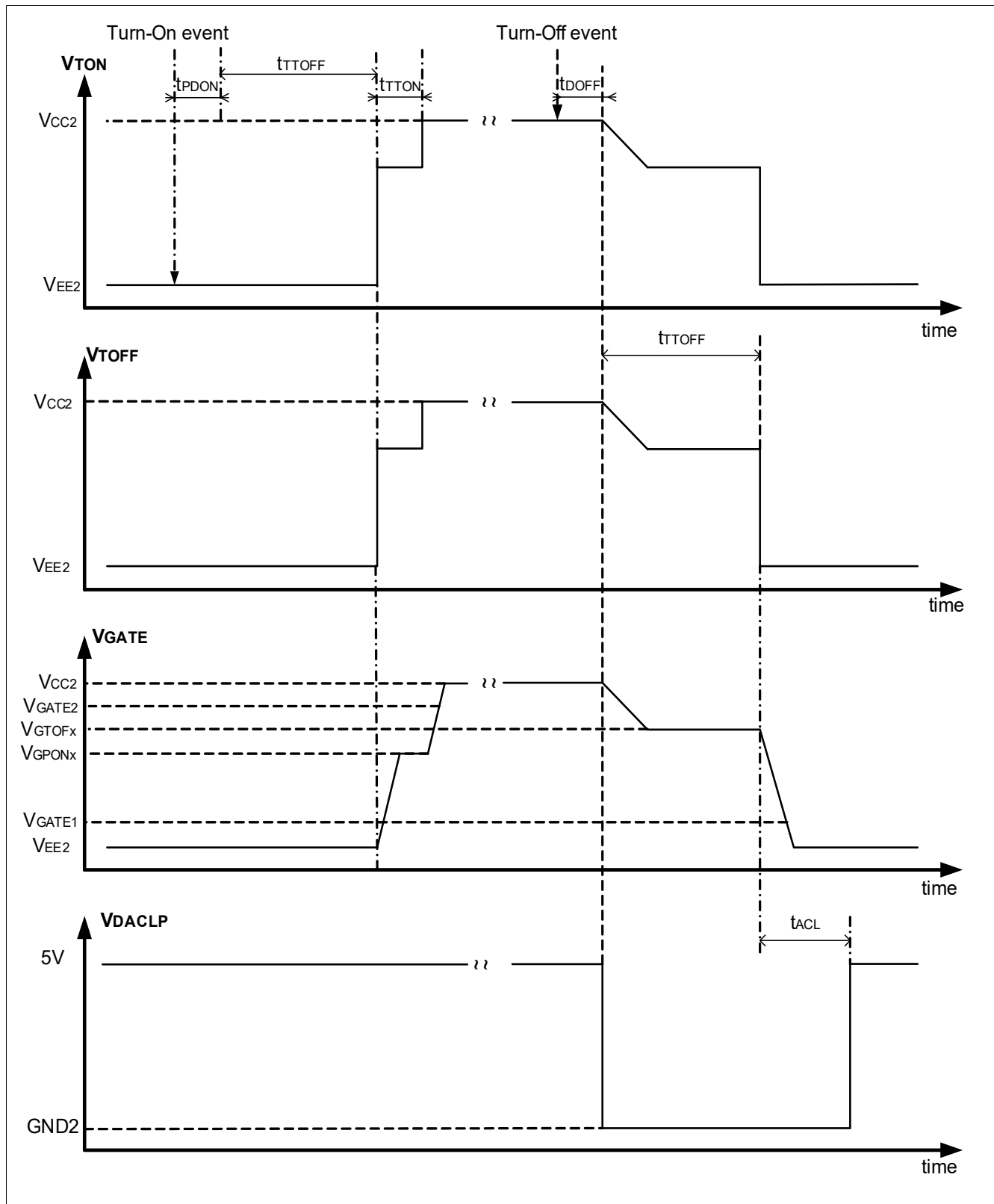


Figure 16 Idealized Switching Sequence

### 2.4.6.3 Disabling the output stage

The output stage of the device can be disabled, i.e. tristated. There are two ways to tristate the device: either via signal **OSD** or via the Output Stage Monitor (see [Chapter 3.2.4](#)).

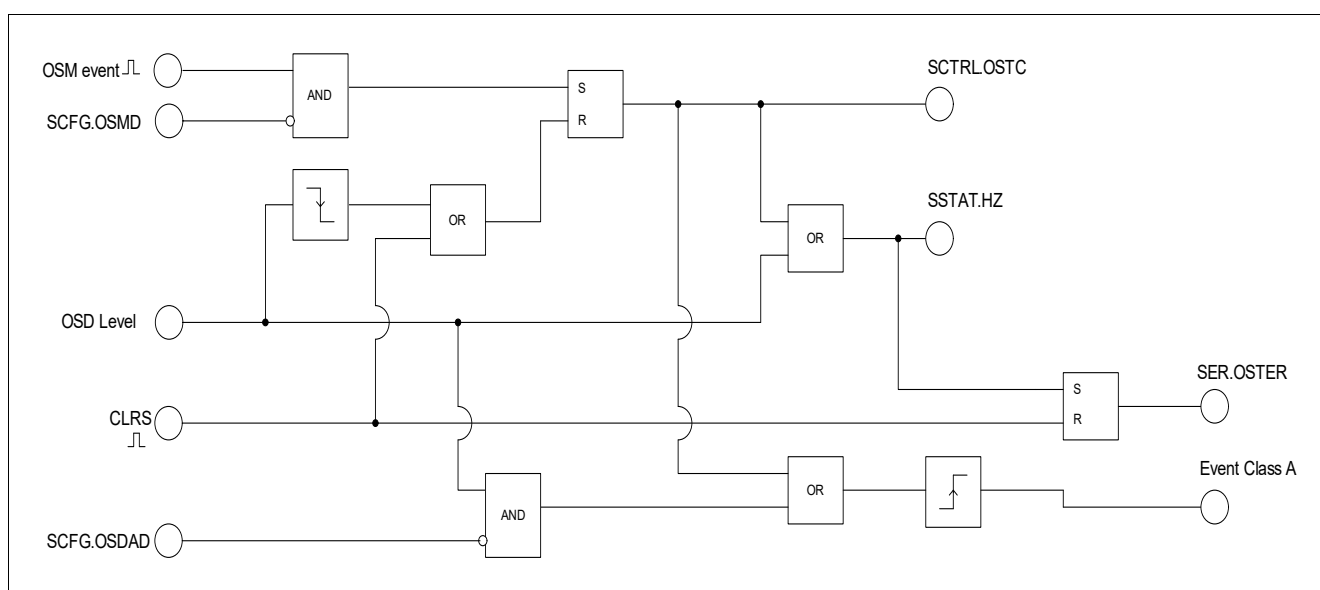
## Functional Description

The current state of the output stage is indicated by bit **SSTAT.HZ**. If the bit is cleared, the output stage operates normally and issues a High or a Low level. If it is set, signals **TON** and **TOFF** are tristated.

If the transition from normal operation to tristate is caused by the Output Stage Monitoring, an Event Class A is generated. If it is caused by a High Level detected on pin **OSD**, an Event Class A is generated only if bit **SCFG.OSDAD** is cleared. Otherwise, if **SCFG.OSDAD** is set, no event is generated (i.e OPM mode not changed). When bit **SSTAT.HZ** is set, sticky bit **SER.OSTER** is set (independently from the value of **SCFG.OSDAD**).

**Figure 17** shows the principle of operation of the Output Stage Disable mechanisms.

The activation of signal **NFLT** due to a tristate event depends on the configuration of the chip (see **Chapter 2.4.7**).



**Figure 17 Output Stage Disable: Principle of Operation**

**Note:** Bit **SSTAT.HZ** is the result of the logical operation of bit **SCTRL.OSTC** being ORed with bit **SSTAT2.OSDL**.

### OSD Signal

The input signal **OSD** is used as a control signal in order to tristate the output stage of the device. A Low level at pin **OSD** corresponds to the normal operation of the device. When signal **OSD** is at High level, the output stage is tristated. A High to Low transition of signal **OSD** clears bit **SCTRL.OSTC**.

The level read by the device at pin **OSD** is given by bit **SSTAT2.OSDL**.

### Output Stage Monitoring

The Output Stage Monitoring function is described in **Chapter 3.2.4**. In case the OSM detects an error condition, bit **SCTRL.OSTC** is set and the output stage is tristated.

The functionality of the OSM is controlled by bit **SCFG.OSMD**. When this bit is set, the OSM is inhibited.

#### 2.4.6.4 Passive Clamping

When the secondary chip is not supplied, signals **TOFF**, **TON** and **GATE** are clamped to  $V_{EE2}$ . See **Chapter 5.5.4** for the electrical capability of this feature.

## Functional Description

### 2.4.7 Fault Notifications

The device provides two kinds of fault notification mechanisms:

- Pins **NFLTA**, **NFLTB** and **NRST/RDY** allow for fast error notification to the main microcontroller. All signals are active low.
- Error bits can be read by SPI.

The activation of signal **NRST/RDY** is associated with Reset Events (see [Chapter 2.4.9](#)). The activation of signal **NFLTA** is associated with Class A Events. The activation of signal **NFLTB** is associated with Class B Events. In general the activation of signal **NFLTA** or **NFLTB** is linked to a state transition of the state machine. If an Event Class A occurs that leads to a state transition (from OPM4 to OPM3 or OPM6 to OPM5), signal **NFLTA** is activated. In case an Event Class A occurs that does not lead to a state transition, **NFLTA** is not activated (exception: tristate events). However, the corresponding error bit in register **PER** or **SER** is set.

Tristate events are handled in a special way. Tristate events can be generated either by the output stage monitoring (when enabled) or by a High Level at pin **OSD**.

In case bit **SCFG.OSMD** is set, the OSM is completely disabled and therefore can not generate any tristate events (and consequently it can not generate Events Class A).

In case bit **SCFG.OSDAD** is set, a transition to High Level of pin **OSD** does not generate any state transition. As a result, no Event Class A is generated. However, bit **SER.OSTER** is set and the output stage is in tristate for the duration for which pin **OSD** is at High Level.

Additionally, signal **NFLTA** can be activated directly by the status bits on the primary side. This allows to have signal **NFLTA** activated in any OPM mode in case of tristate events. If **PCFG.OSTAEN** is set, **NFLTA** is activated at the transition of bit **PER.OSTER** from 0<sub>B</sub> to 1<sub>B</sub>. If **PCFG.OSMAEN** is set, **NFLTA** is activated at the transition of bit **PSTAT2.OSTC** from 0<sub>B</sub> to 1<sub>B</sub>. In case both bits **PCFG.OSTAEN** and **PCFG.OSMAEN** are cleared, **NFLTA** is only activated in case of a state transition of the state machine.

If an Event Class B occurs that leads to a state transition (to OPM1), signal **NFLTB** is activated. In case an Event Class B occurs that does not lead to a state transition, **NFLTB** is not activated. However, the corresponding error bit in register **PER** or **SER** is set.

OVLO3 Events are handled in a special way. In case bit **SCFG2.OVLO3D** is set, an OVLO3 event does not lead to a transition of the state machine (**NFLTB** is not activated). Besides, no Emergency Turn-Off sequence is initiated. However, bit **SER.OVLO3ER** is set. Therefore, when bit **SCFG2.OVLO3D** is set, OVLO3 detection mechanism behaves like an Event Class C.

**Table 12** describes how failure notifications are cleared:

**Table 12 Failure Notification Clearing**

	<b>NFLTA / B signals</b>	<b>Primary Sticky Bits</b>	<b>Secondary Sticky Bits</b>
<b>PCTRL.CLRP</b> set	De-assertion	Cleared	-
<b>PCTRL.CLRS</b> set <sup>1)</sup>	-	-	Cleared
<b>EN/FEN</b> Invalid to Valid transition	De-assertion <sup>2)</sup>	-	-

1) If the device is in OPM1, setting bit **SCTRL.CLRS** leads to a transition to OPM0

2) Only in OPM3 and OPM5. In other Operating Modes, no de-assertion is done.

The level issued by the device on pins **NFLTA** and **NFLTB** is given by bits **PSTAT2.FLTA** and **PSTAT2.FLTB**. The levels read by the device at those pins is given by bits **PPIN.NFLTAL** and **PPIN.NFLTBL**.

## Functional Description

### 2.4.8 EN Signal Pin

The **EN/FEN** signal allows the logic on the primary side to have a direct control on the state of the device. A valid signal has to be provided on this pin. A valid to invalid transition of the signal on pin **EN/FEN** generates an Event Class A.

Pin **EN/FEN** should be driven actively by the external circuit. In case this pin is floating, an internal weak pull-down resistor ensures that the signal is low.

*Note: It should be noted that even if the signal at pin **EN/FEN** is valid, the device can still be in disabled state. This may happen for example if another error is being detected*

Depending on the value of bit **PCFG2.FEN**, two types of valid signals can be chosen from:

#### EN Mode

When the EN Mode is selected (bit **PCFG2.FEN** cleared), pin **EN/FEN** acts as an Enable pin. A valid **EN/FEN** signal is defined as a digital High level. When **EN/FEN** is at Low level, the signal is considered as not valid and the device is in Disabled State. In case of a High-to-Low transition, an Event Class A is generated.

#### FEN Mode

When the FEN Mode (bit **PCFG2.FEN** set) is selected, a valid signal is defined as a periodic clock signal. The signal is constantly monitored by a watchdog unit. The watchdog evaluates the signal as valid if two consecutive valid half-periods are detected.

If, after a valid signal has been recognized, a timing violation is detected by the watchdog, an Event Class A is generated.

Every time an edge (rising or falling) is received, a counter is started. The counter is incremented at a frequency of  $f_{OSC1}/8$ . The following edge is expected by the device during a window corresponding to the time between state 2 and state 6 of the counter. In case the edge comes too early or too late, an Event Class A is generated.

An Invalid to Valid transition of signal **EN/FEN** deactivates signals **NFLT A** and **NFLT B** (when the device is in OPM3 or OPM5 only).

The levels read by the device at pin **EN/FEN** is given by bits **PPIN.ENL**. The validity status of **EN/FEN** signal is given by bit **PSTAT2.ENVAL**.

### 2.4.9 Reset Events

A reset event sets the device and its internal logic in the default configuration. All user-defined settings are overwritten with the default values. The list of reset events and their effect is summarized in **Table 13**.

## Functional Description

**Table 13 Reset Events Summary**

Reset Event	Primary	Secondary	Notification (primary)	Notification (secondary)
<b>NRST/RDY</b> Input signal active (driven externally)	Reset	Soft Reset	<ul style="list-style-type: none"> <li>• <b>NRST/RDY</b> Low (during event).</li> <li>• Bit <b>PER.RSTE1</b> and <b>PER.RST1</b> set.</li> <li>• Bit <b>PER.CER1</b> is <b>not</b> set.</li> <li>• Event Class B (<b>NFLT B</b> activated) at the end of the reset event.</li> </ul>	<ul style="list-style-type: none"> <li>• Bit <b>SER.CER2</b> set (in case of lifesign lost).</li> <li>• Output Stage issues a PWM OFF command.</li> <li>• <b>OSD</b> pin functionality operational.</li> </ul>
UVLO1 Event	Reset	Soft Reset	<ul style="list-style-type: none"> <li>• <b>NRST/RDY</b> Low (driven by device during event).</li> <li>• Bit <b>PER.RST1</b> set (once <math>V_{CC1}</math> valid again).</li> <li>• Bit <b>PER.CER1</b> is <b>not</b> set.</li> <li>• Event Class B (<b>NFLT B</b> activated) at the end of the reset event.</li> </ul>	<ul style="list-style-type: none"> <li>• Bit <b>SER.CER2</b> set (in case of lifesign lost).</li> <li>• Output Stage issues a PWM OFF command.</li> <li>• <b>OSD</b> pin functionality operational.</li> </ul>
OSC1 not starting at power-up	Reset	Soft Reset	<ul style="list-style-type: none"> <li>• <b>NRST/RDY</b> Low (driven by device during event).</li> <li>• Bit <b>PER.RST1</b> set (once OSC1 valid again).</li> <li>• Bit <b>PER.CER1</b> is <b>not</b> set.</li> <li>• Event Class B (<b>NFLT B</b> activated) at the end of the reset event.</li> </ul>	<ul style="list-style-type: none"> <li>• Bit <b>SER.CER2</b> set (in case of lifesign lost).</li> <li>• Output Stage issues a PWM OFF command.</li> <li>• <b>OSD</b> pin functionality operational.</li> </ul>
IREF1 shorted to ground or open	Reset	Soft Reset	<ul style="list-style-type: none"> <li>• <b>NRST/RDY</b> Low (driven by device during event).</li> <li>• Bit <b>PER.RST1</b> set (once IREF1 valid again).</li> <li>• Bit <b>PER.CER1</b> is <b>not</b> set.</li> <li>• Event Class B (<b>NFLT B</b> activated) at the end of the reset event.</li> </ul>	<ul style="list-style-type: none"> <li>• Bit <b>SER.CER2</b> set (in case of lifesign lost).</li> <li>• Output Stage issues a PWM OFF command.</li> <li>• <b>OSD</b> pin functionality operational.</li> </ul>
Memory Error on Primary	Reset	Soft Reset	<ul style="list-style-type: none"> <li>• <b>NRST/RDY</b> Low (driven by device during event).</li> <li>• Bit <b>PER.RST1</b> set (when failure condition is removed).</li> <li>• Bit <b>PER.CER1</b> is <b>not</b> set.</li> <li>• Event Class B (<b>NFLT B</b> activated) at the end of the reset event.</li> </ul>	<ul style="list-style-type: none"> <li>• Bit <b>SER.CER2</b> set (in case of lifesign lost).</li> <li>• Output Stage issues a PWM OFF command.</li> <li>• <b>OSD</b> pin functionality operational.</li> </ul>

## Functional Description

**Table 13 Reset Events Summary**

Reset Event	Primary	Secondary	Notification (primary)	Notification (secondary)
UVLO2 Event	-	Hard Reset	<ul style="list-style-type: none"> <li>Event Class B (<b>NFLT</b> activated, bit <b>PER.CER1</b> set).</li> <li>Bit <b>PSTAT.SRDY</b> cleared for the duration of the failure.</li> </ul>	<ul style="list-style-type: none"> <li>Signal <b>NUV2</b> at Low level (if <math>V_{CC2} &lt; V_{UVLO2}</math>).</li> <li>Bit <b>SER.RST2</b> (once <math>V_{CC2}</math> valid again).</li> <li>Output Stage issues a PWM OFF command.</li> <li><b>OSD</b> pin functionality operational for: <math>V_{CC2} &gt; V_{RST2}</math>.</li> </ul>
OSC2 not starting at power-up	-	Hard Reset	<ul style="list-style-type: none"> <li>Event Class B (<b>NFLT</b> activated, bit <b>PER.CER1</b> set)</li> <li>Bit <b>PSTAT.SRDY</b> cleared</li> </ul>	<ul style="list-style-type: none"> <li>Output Stage issues a PWM OFF command.</li> <li><b>OSD</b> pin functionality operational.</li> </ul>
OSC2 misfunction during operation	-	Soft Reset	<ul style="list-style-type: none"> <li>Event Class B (<b>NFLT</b> activated, bit <b>PER.CER1</b> set)</li> <li>Bit <b>PSTAT.SRDY</b> cleared for the duration of the failure.</li> </ul>	<ul style="list-style-type: none"> <li>Output Stage issues a PWM OFF command.</li> <li><b>OSD</b> pin functionality operational.</li> </ul>
IREF2 open	-	Hard Reset	<ul style="list-style-type: none"> <li>Event Class B (<b>NFLT</b> activated, bit <b>PER.CER1</b> not)</li> <li>Bit <b>PSTAT.SRDY</b> cleared</li> </ul>	None.
VREG shorted to ground	-	Undefined	<ul style="list-style-type: none"> <li>Event Class B (<b>NFLT</b> activated, bit <b>PER.CER1</b> set)</li> <li>Bit <b>PSTAT.SRDY</b> cleared.</li> </ul>	<ul style="list-style-type: none"> <li>Signal <b>NUV2</b> at Low Level.</li> <li>Output Stage issues a PWM OFF command.</li> </ul>
Memory Error on Secondary	-	Hard Reset	<ul style="list-style-type: none"> <li>Event Class B (<b>NFLT</b> activated, bit <b>PER.CER1</b> set).</li> <li>Bit <b>PSTAT.SRDY</b> cleared.</li> </ul>	<ul style="list-style-type: none"> <li>Output Stage issues a PWM OFF command.</li> <li><b>OSD</b> pin functionality operational.</li> </ul>

All reset events set the device in Mode OPM0. In a soft reset, the logic works further, but the registers use the default values.

In case of a reset condition on the primary side, the behavior of the pin of the device is defined in [Table 14](#).

**Table 14 Pin behavior (primary side) in case of reset condition**

Pin	Output Level	Comments
SDO	Low	
DOUT	Tristate	
NFLT	Low	



## Functional Description

**Table 14 Pin behavior (primary side) in case of reset condition (cont'd)**

Pin	Output Level	Comments
NFLTA	High	
NRST/RDY	Low (GND1)	

In case of a hard reset condition on the secondary side, the behavior of the pin of the device is defined in [Table 15](#).

**Table 15 Pin behavior (secondary side) in case of reset condition**

Pin	Output Level	Comments
TON	Low ( $V_{EE2}$ )	Passive Clamping
TOFF	Low ( $V_{EE2}$ )	Passive Clamping
DESAT	Low (GND2)	Clamped.
GATE	Low ( $V_{EE2}$ )	Passive Clamping
DACL	High (5 V)	Active clamping disabled by default.
NUV2	Low (GND2)	

### 2.4.10 Operation in Configuration Mode

This section describes the mechanisms to configure the device.

#### 2.4.10.1 Static Configuration Parameters

Static parameters can be configured when the device is in Mode OPM2 by writing the appropriate register.

Once Mode OPM2 is left with the SPI Command EXIT\_CMODE, the configuration parameters are frozen on both primary and secondary chips. This means in particular that write accesses to the corresponding registers are invalidated. This prevents static configurations to be modified during runtime. Besides, the configuration parameters on the primary and secondary side are protected with a memory protection mechanism. In case the values are not consistent, a Reset Event and / or an Event Class B is generated.

##### 2.4.10.1.1 Configuration of the SPI Parity Check

The SPI interface supports by default an odd parity check. The Parity Check mechanism (active at the reception of an SPI word) can be disabled by setting bit **PCFG.PAREN** to 0<sub>B</sub>. Setting bit **PAREN** to 1<sub>B</sub> enables the Parity Check.

Parity Bit Generation for the transmitter can not be disabled.

##### 2.4.10.1.2 Configuration of NFLTA Activation in case of Tristate Event

Signal **NFLTA** is normally activated by a state transition of the internal state machine. However, it can be also configured to be activated in relation with the primary bits **PER.OSTER** or **PSTAT2.OSTC**. This is configured thanks to bits **PCFG.OSTAEN** and **PCFG.OSMAEN**.

## Functional Description

### 2.4.10.1.3 Configuration of the STP Minimum Dead Time

The minimum dead time for the Shoot-Through Protection can be programmed by writing bit field **PCFG2.STPDEL**. The value programmed corresponds to a number of OSC1 clock cycles.

*Note:* Register **PCFG2** can only be written if bit **PCFG.CFG1** is set.

### 2.4.10.1.4 Configuration of the EN/FEN Mode

The mode of operation of pin **EN/FEN** can be programmed by writing bit field **PCFG2.FEN**. The description of the operating modes is given in **Chapter 2.4.8**.

*Note:* Register **PCFG2** can only be written if bit **PCFG.CFG1** is set.

### 2.4.10.1.5 Configuration of the Digital Channel

The direction of pin **DIO1** can be programmed by writing bit field **PCFG2.DIO1**. The direction of pin **DIO2** can be programmed by writing bit field **SCFG2.DIO2**.

*Note:* Register **PCFG2** can only be written if bit **PCFG.CFG1** is set. Register **SCFG2** can only be written if bit **SCFG.CFG2** is set.

### 2.4.10.1.6 Configuration of DOUT Signal Activation

The signal at pin **DOUT** can be activated or deactivated by programming bit **PCFG2.DOEN1**. If deactivated, pin **DOUT** delivers a steady Low signal. The rest of the logic is not affected by this setting. Besides, bit **SCFG2.ISMEN** has to be set as well. Furthermore, permanent DESAT clamping shall be deactivated (**SCFG.DSTCEN** cleared).

*Note:* Register **PCFG2** can only be written if bit **PCFG.CFG1** is set. Register **SCFG2** can only be written if bit **SCFG.CFG2** is set

### 2.4.10.1.7 Configuration of the V<sub>BE</sub> Compensation

The V<sub>BE</sub> compensation of signal **TON** and **TOFF** can be activated or deactivated by writing bit **SCFG.VBEC**. See **Chapter 2.4.6** for more details.

### 2.4.10.1.8 Deactivation of Output Stage Monitoring

The OSM function can be disabled by setting bit **SCFG.OSMD**.

## Functional Description

### 2.4.10.1.9 Deactivation of Events Class A due to pin OSD

By setting bit **SCFG.OSDAD**, Event Class A are not issued in case of a Tristate event generated by pin **OSD**. Other actions such as tristating the output stage or setting bit **SER.OSTER** are performed normally.

### 2.4.10.1.10 Clamping of DESAT pin

By setting bit **SCFG.DSTCEN**, the DESAT signal is clamped to  $V_{GND2}$  while the output stage of the device issues a PWM OFF command and during blanking time periods. By clearing bit **SCFG.DSTCEN**, the DESAT clamping is only activated during blanking time periods.

In order to use the IGBT Monitoring function, bit **SCFG.DSTCEN** shall be cleared.

### 2.4.10.1.11 Activation of the Pulse Suppressor

The pulse suppressor function associated with the TTOFF function can be activated by setting bit **SCFG.PSEN**. When activated, **SRTTOF.RTVAL** shall be programmed with a minimum value (see [Page 118](#)).

### 2.4.10.1.12 Configuration of the Verification Mode Time Out Duration

The duration of the time out in verification mode is selectable via bit **SCFG.TOSEN**.

### 2.4.10.1.13 DESAT Threshold Level Configuration

By writing bit field **SCFG2.DSATL**, it is possible to select the detection level of the **DESAT** comparator (which is also the level for the **DOUT** function).

*Note:* Register **SCFG2** can only be written if bit **SCFG.CFG2** is set.

### 2.4.10.1.14 Configuration of the TTON Delay

The TTON delay can be configured by writing bit field **SCFG2.TTOND**. Programming 0<sub>H</sub> as a delay value disables the TTON for all turn-on sequences. Hard turn-on are performed instead. In case the TTON function is wished, a minimum value for the delay has to be programmed (see [Page 111](#)).

The TTON delay can be calibrated using the TCF feature of the device.

*Note:* Register **SCFG2** can only be written if bit **SCFG.CFG2** is set.

### 2.4.10.1.15 Configuration of DACLP Activation Mode

The **DACLP** activation mode can be programmed by writing bit **SCFG2.ACLPM**. When this bit is cleared, signal **DACLP** is deactivated at every Turn-Off sequence (with the programmed activation time). When it is set, **DACLP** is deactivated **only** in case of an Emergency Turn-Off sequence.

*Note:* Register **SCFG2** can only be written if bit **SCFG.CFG2** is set.

## Functional Description

### 2.4.10.1.16 OVLO3 Operation Mode

The activation mode of the OVLO3 function can be selected by programming bit **SCFG2.OVLO3D**. When this bit is cleared, an Event Class B is generated in case on a OVLO3 event ( $V_{EE2}$  above a given threshold). When this bit is set, no Event Class B is generated in case of an OVLO3 event, but an Event Class C: the OPM mode is not affected, the output stage is not turned off and signal NFLTB is not activated. Nevertheless, bit **SER.OVLO3ER** is set (and mirrored to **PER.OVLO3ER**).

*Note:* Register **SCFG2** can only be written if bit **SCFG.CFG2** is set.

### 2.4.10.1.17 Configuration of the TTOFF Delays

The TTOFF delays for Regular and Safe Turn-Off sequences can be programmed separately by writing registers **SRTTOF** or **SSTTOF**. The delay for Regular Turn-Off can also be configured using the Timing Calibration Feature.

Programming 0<sub>H</sub> as a delay value disables the TTOFF for the concerned Turn-Off Sequence. Hard turn-off are performed instead. In case the TTOFF function is wished, a minimum value for the delay has to be programmed (see [Page 118](#) and [Page 119](#)).

When safe two level turn-off is used (non zero delay) in normal operating mode (OPM4), the programmed safe turn-off delay value shall be higher than the programmed regular two level turn off delay.

### 2.4.10.1.18 Configuration of the Safe TTOFF Plateau Level

The plateau level for safe two level turn off sequences can be programmed with bit field **SSTTOF.GPS**. The plateau level value for safe turn-off sequences shall be lower than the one selected for regular turn-off sequences.

### 2.4.10.1.19 Configuration of the DESAT Blanking Time

The blanking time for the DESAT protection can be configured by writing bit field **SDESAT.DSATBT**. In case this function is used, a minimum value for the delay has to be programmed (see [Page 116](#)).

*Note:* The programmed OCP blanking time shall be smaller than the programmed DESAT blanking time.

### 2.4.10.1.20 Configuration of the OCP Blanking Time

The blanking time for the OCP protection can be configured by writing bit field **SOCP.OCBPT**. Programming 0<sub>H</sub> deactivates the blanking time feature. The programmed blanking time shall not exceed a maximum value (see [Page 117](#)).

*Note:* The programmed OCP blanking time shall be smaller than the programmed DESAT blanking time.

## Functional Description

### 2.4.10.1.21 Configuration of **DACL** Activation Time

The **DACL** activation time after hard commutation can be programmed by writing bit field **SACLT.AT**. In case value 0<sub>H</sub> is programmed, the device delivers at **DACL** a constant High level. In case an activation time is required, a minimum value for the delay has to be programmed (see [Page 122](#)). In case value FF<sub>H</sub> is programmed, the device delivers a constant Low level at **DACL**.

### 2.4.10.2 Dynamic Configuration

The TTOFF plateau level in regular turn-off can be modified during runtime by writing bit field **PCTRL2.GPOF**. The value of this bit field is periodically transferred to the secondary side. The last valid received value by the primary side is available at bit field **PSTAT.GPOFS**. The value currently used by the secondary chip is available at bit field **SCTRL.GPOFS**.

The TTOFF plateau for safe turn-off can only be configured statically with bit field **SSTTOF.GPS**.

This dynamic configuration of the plateau level allows to compensate for temperature variations of the I-V characteristic of the IGBT. In overcurrent conditions, the maximum current flowing through the IGBT when the plateau is reached can be limited more accurately.

Similarly, The WTO and the TTON plateau level can be configured by writing bit field **PCTRL.GPON**.

The plateau value stored in the device at the beginning of the corresponding switching sequence is latched and active until the next switching sequence.

### 2.4.10.3 Delay Calibration

In order to compensate for timing errors due to part-to-part variations, a dedicated Timing Calibration Feature (TCF) has been implemented. The TCF works in such a way that the PWM input signal is used to start and stop a counter clocked by the Start-Stop Oscillator of the Output Stage. As a result, the following delays and timing can be configured that way:

- TTOFF delay for Regular Turn-Off.
- TTON delay.

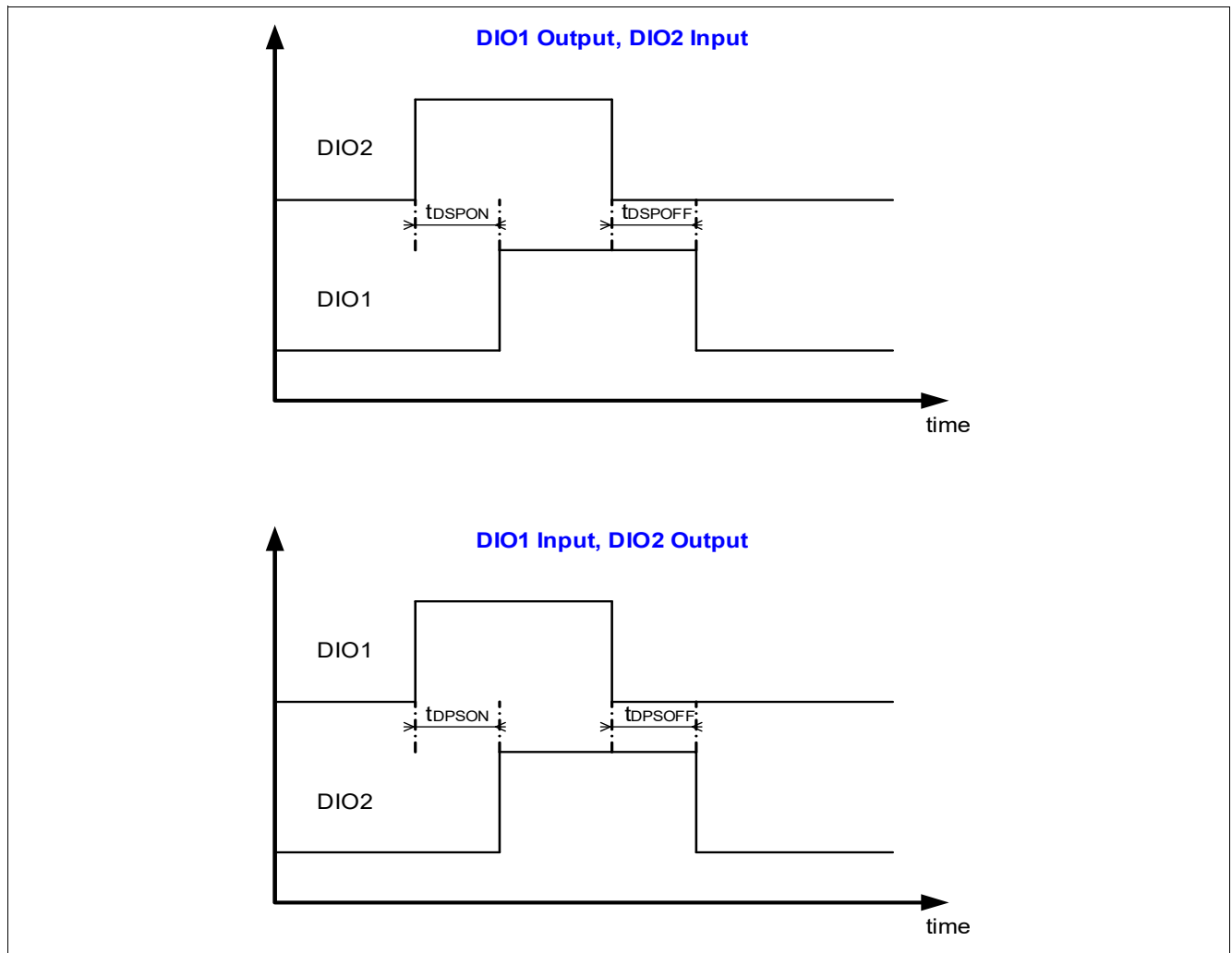
The TCF allows to compensate for part to part variations of the frequency of the Start-Stop oscillator. This results in better accuracy for application critical timing. Device specific variations, e.g. temperature related, are not compensated though.

The TCF can be activated or deactivated in Configuration Mode by writing bit field **SSCR.VFS2**. The device shall then be set in OPM6 and the PWM signal applied. Details about the TCF operation are given in [Chapter 3.5.9](#).

## Functional Description

### 2.4.11 Low Latency Digital Channel

The low latency digital channel aims at providing an alternative to discrete galvanic isolators. Digital signals can be transmitted through pins **DIO1** and **DIO2**. The direction of the channel is given by bit field **PCFG2.DIO1** and **SCFG2.DIO2**. The functionality of the channel is shown **Figure 18**.



**Figure 18 Low Latency Digital Channel**

The voltage level at pin **DIO1** can be read at bit **PPIN.DIO1L**. The voltage level at pin **DIO2** can be read at bit **SSTAT2.DIO2L**.

The input stages of signals **DIO1** and **DIO2** include each a Debouncing Filter. The input signals are that way filtered from glitches and noise (mini-filter of two consecutive OSC2 cycles).

### 3 Protection and Diagnostics

This section can describes the safety relevant functions implemented in the 1EDI2002AS.

#### 3.1 Supervision Overview

The 1EDI2002AS driver provides extended supervision functions, in order to achieve ASIL requirements on system level. **Table 16** gives an overview of the implemented functions.

**Table 16 Safety Related Functions**

Protection Feature	Description	Category	Comments
DESAT	Monitoring of the collector-emitter voltage of the IGBT in ON state.	A	See <a href="#">Chapter 3.2.1</a>
OCP	Monitoring of the current on the IGBT's auxiliary emitter path.	A	See <a href="#">Chapter 3.2.2</a>
External Enable	Fast deactivation via an external Enable signal on the primary.	A	See <a href="#">Chapter 3.2.3</a>
Output Stage Monitoring	Monitoring of <b>TON</b> and <b>TOFF</b> signals.	A	See <a href="#">Chapter 3.2.4</a>
Power Supply Monitoring	Under Voltage Lock-Out function on $V_{CC1}$ , $V_{CC2}$ and $V_{EE2}$ ; Over Voltage Lock-Out on $V_{EE2}$ and $V_{CC2}$ .	B	See <a href="#">Chapter 3.3.1</a>
Internal Supervision	Monitoring of the key internal functions of the chip.	B	See <a href="#">Chapter 3.3.2</a>
STP	Shoot Through Protection.	C	See <a href="#">Chapter 3.4.1</a>
Gate Monitoring	Monitoring of the <b>GATE</b> voltage during a switching sequence.	C	See <a href="#">Chapter 3.4.2</a>
Temperature Monitoring	Over temperature warning for the driver.	C	See <a href="#">Chapter 3.4.3</a>
SPI Error Detection	SPI Error Detection.	C	See <a href="#">Chapter 3.4.4</a>
Active Short Circuit Support	$V_{CC2}$ not valid error notification	C	See <a href="#">Chapter 3.4.5</a>
IGBT State Monitoring	The current state of the IGBT is given by signal <b>DOUT</b> .	C	See <a href="#">Chapter 3.4.6</a>
WTO	Weak Turn-On Functionality	D	See <a href="#">Chapter 3.5.2</a>
<b>DESAT</b> Supervision	Supervision of the DESAT function during application life time.	D	See <a href="#">Chapter 3.5.3</a> , <a href="#">Chapter 3.5.4</a> and <a href="#">Chapter 3.5.5</a>
<b>OCP</b> Supervision	Supervision of the OCP function during application life time.	C & D	See <a href="#">Chapter 3.5.6</a> , <a href="#">Chapter 3.5.7</a> and <a href="#">Chapter 3.2.2</a>

**Protection and Diagnostics**

**Table 16 Safety Related Functions** (cont'd)

Protection Feature	Description	Category	Comments
Power Supply Monitoring Supervision	Supervision of the OVLO / UVLO function during application life time.	D	See <a href="#">Chapter 3.5.8</a>
Internal Clock Supervision	Plausibility check of the frequency of the internal oscillator.	D	See <a href="#">Chapter 3.5.9</a>
DIO Supervision	Supervision of the DIO channel	D	See <a href="#">Chapter 3.5.10</a>
TTOFF	Two Level Turn-Off	E	See <a href="#">Chapter 2.4.6</a>
SPI Communication	SPI Communication (using register <a href="#">PRW</a> ).	E	See <a href="#">Chapter 4.1</a>
Overvoltage robustness	Robustness against transient overvoltage on power supply.	E	See <a href="#">Chapter 5.2</a>

From the conceptual point of view, the protection functions can be clustered into five main categories.

- Category A corresponds to the functions where the device “decides on its own”, after the detection of an Event Class A, to change the state of the output stage and to disable itself. A dedicated action from the user is needed to reactivate the device (fast reactivation).
- Category B corresponds to the functions where the device “decides on its own”, after the detection of an Event Class B, to change the state of the output stage and to disable itself. A complete reinitialization from the user is needed to reactivate the device (slow reactivation).
- Category C corresponds to the functions that only issue a notification in case an error is detected.
- Category D are intrusive supervision functions, aimed at being started when the application is not running.
- Category E corresponds to implemented functions or capabilities supported by the device whose use can enhance the overall safety coverage of the application.



## 3.2 Protection Functions: Category A

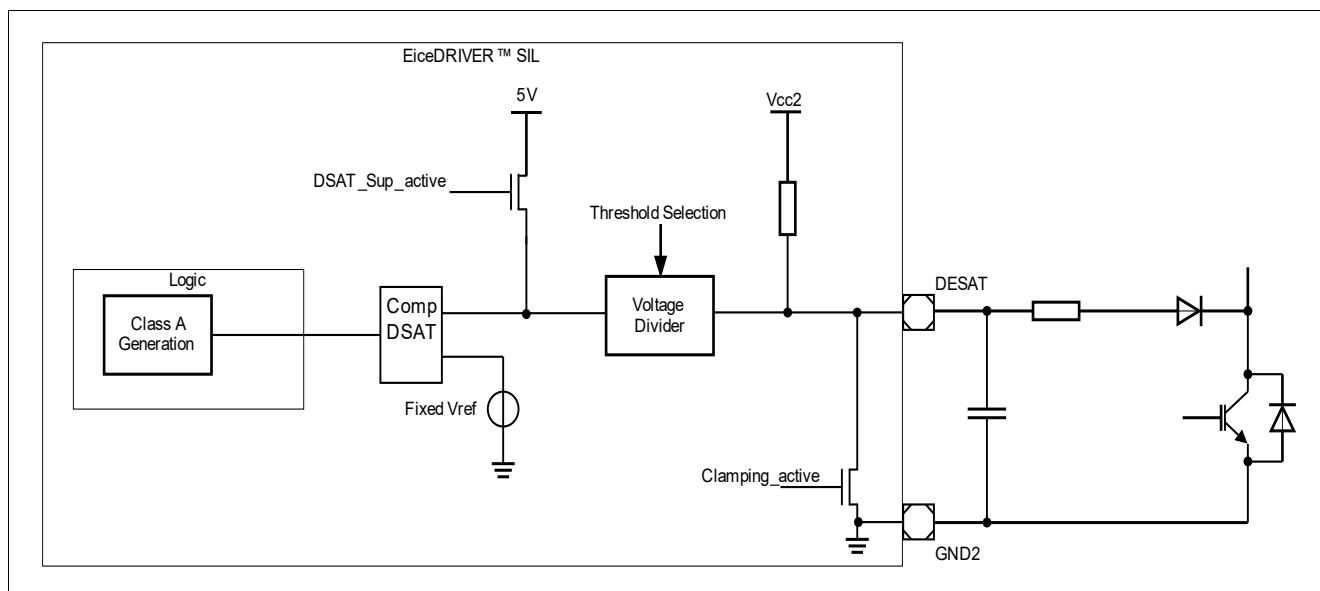
### 3.2.1 Desaturation Protection

The integrated desaturation (DESAT) functionality is summarized in [Table 17](#):

**Table 17 DESAT Protection Overview**

Parameter	Short Description
Function	Monitoring of the $V_{CE}$ voltage of the IGBT.
Periodicity	Continuous while device issues a PWM ON command.
Action in case of failure event	<ol style="list-style-type: none"> <li>Emergency (Safe) Turn-off Sequence.</li> <li>Error Flag <b>SER.DESATER</b> is set.</li> <li>Assertion of signal <b>NFLTA</b>.</li> </ol>
Programmability	Yes (blanking time and detection threshold).
In-System Testability	Yes (see also <a href="#">Chapter 3.5.3</a> and <a href="#">Chapter 3.5.4</a> ).

The DESAT function aims at protecting the IGBT in case of short circuit. The voltage drop  $V_{CE}$  over the IGBT is monitored via the **DESAT** pin while the device issues a PWM ON command. The voltage at pin **DESAT** is externally filtered by an external RC filter, and decoupled by an external diode (see [Figure 19](#)). The DESAT voltage is compared to an internal reference voltage. The result of this comparison is available by reading bit **SSTAT2.DSATC**.



**Figure 19 DESAT Function: Diagram of Principle**

At the beginning of a turn-on sequence, the voltage at pin **DESAT** is forced to Low level for the duration the blanking time defined by register **SDESAT**. Once the blanking time has elapsed, the voltage at pin **DESAT** is released and is compared to an internal reference voltage. Depending on the value of the decoupling capacitance, an additional “analog” blanking time will be added corresponding to the charging of the capacitance through the internal pull-up resistance ([Figure 20](#)).

## Protection and Diagnostics

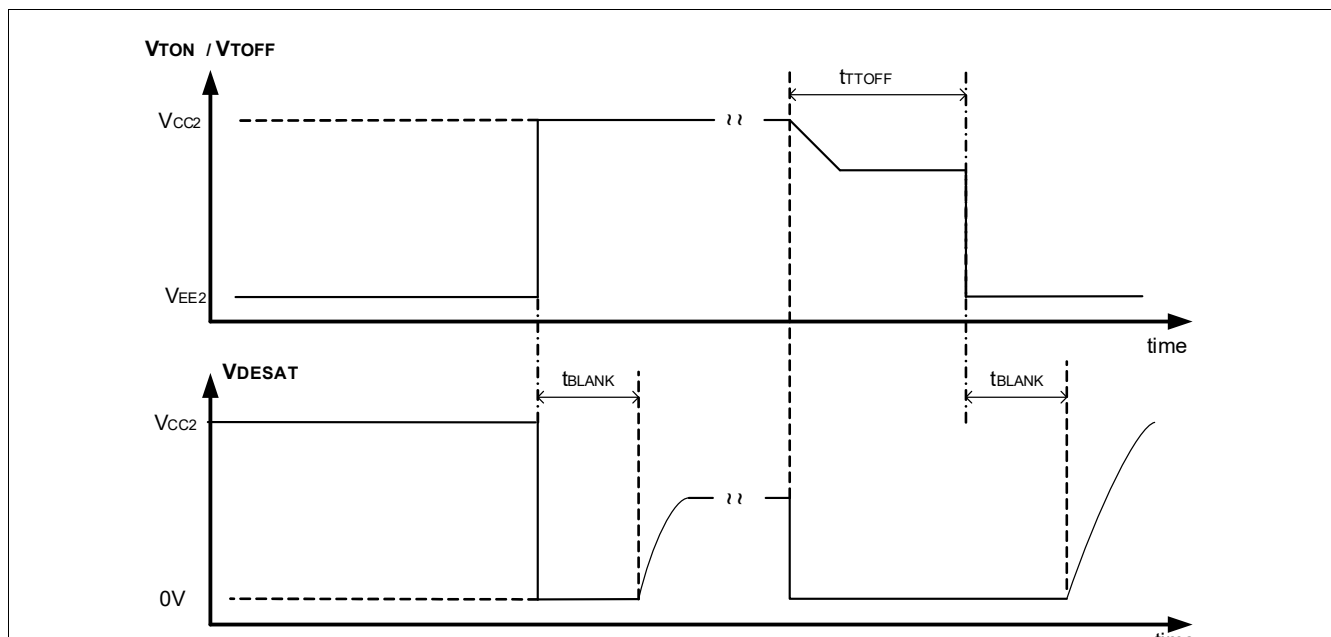
In case the measured voltage is higher than the selected internal threshold, an Emergency (Safe) Turn-Off sequence is initiated, bit **SER.DESATER** is set and a fault notification is issued on pin **NFLTA** (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)).

The DESAT function is not active while the output stage is in PWM OFF state.

The blanking time needs to be chosen carefully, since the DESAT protection may be *de facto* inhibited if the PWM ON-time is too short compared to the chosen blanking time.

The detection threshold can be selected by configuring bit field **SCFG2.DSATL**.

At turn-off, the DESAT signal is pulled down for the duration of the TTOFF plateau time, and extended by the blanking time once the hard turn off sequence is initiated.



**Figure 20 DESAT Operation**

**Note:** . In case the **DESAT** pin is open, the pull-up resistance ensures that a DESAT event is generated at the next PWM turn-on command.

### DESAT Clamping during turn-off

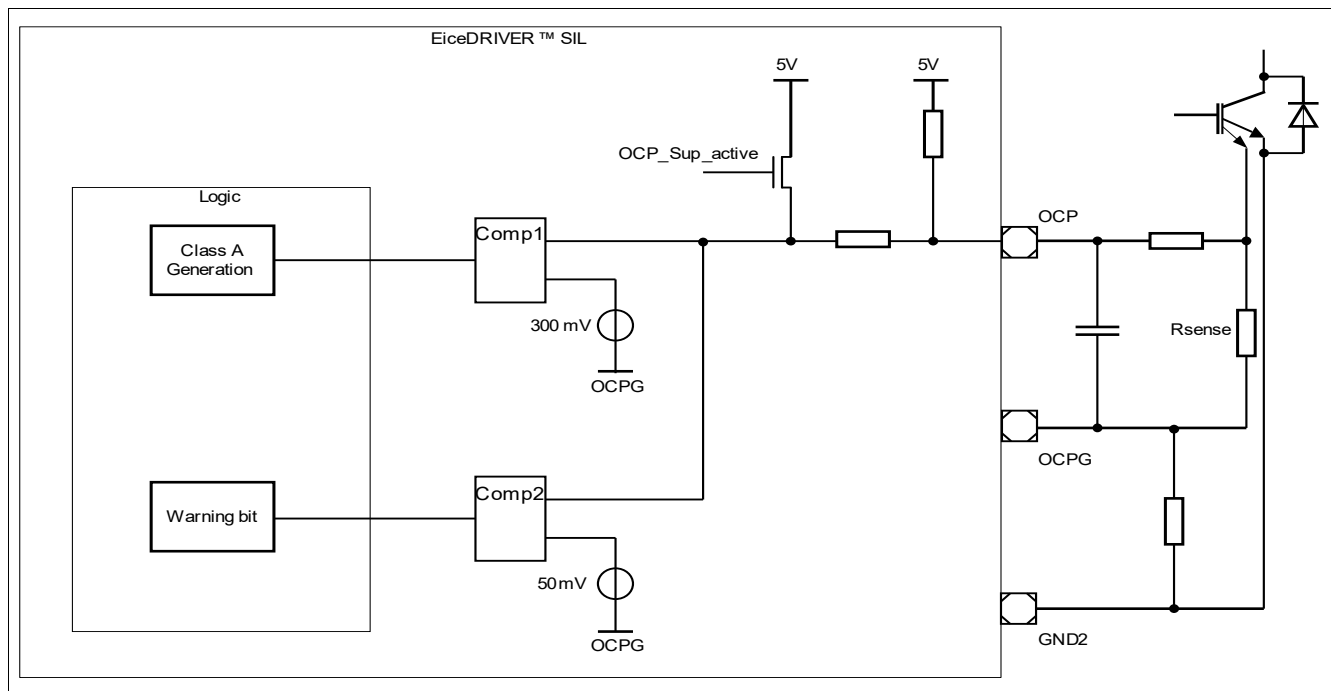
The internal pull-up resistance may lead to the unwanted charging of the DC-link capacitance via the DESAT pin. In order to overcome this, the DESAT function needs to be activated by clearing bit **SCFG.DSTCEN**. When this bit is set, pin **DESAT** is internally clamped to GND2 when a PWM off command is issued by the device.



## Protection and Diagnostics

At the beginning of a turn-on sequence, the internal evaluation of the voltage at pin **OC** is inhibited for the duration the blanking time defined by register **SOCP**. Once the blanking time has elapsed, the voltage at pin **OC** is compared to an internal reference voltage.

In case the measured voltage at pin **OC** is higher than the internal threshold  $V_{OC_{PD1}}$ , an Emergency (Safe) Turn-off sequence is initiated, bit **SER.OCPE** is set and a fault notification is issued on pin **NFLTA** (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case the measured voltage at pin **OC** is higher than the internal threshold  $V_{OC_{PD2}}$ , the sticky bit **SSTAT.OCPCD** is set. The allows to verify during application run time the signal integrity of the sense path. The OCP function is not active while the output stage is in PWM OFF state.



**Figure 22 OCP Function: Principle of Operation**

*Note: Both DESAT and OCP protection mechanisms can be used simultaneously.*

*Note: In case the **OC** pin is open, the pull-up resistance ensures that an OCP event is generated.*

## Protection and Diagnostics

### 3.2.3 External Enable

The External Enable functionality is summarized in [Table 19](#):

**Table 19 External Enable Function Overview**

Parameter	Short Description
Function	External Enable.
Periodicity	Invalid signal on <b>EN/FEN</b> pin.
Action in case of failure event	<ol style="list-style-type: none"><li>1. Emergency (Regular) Turn-off Sequence.</li><li>2. Error Flag <b>PER.ENER</b> is set.</li><li>3. Assertion of signal <b>NFLTA</b>.</li></ol>
Programmability	No.
In-System Testability	Yes.

The functionality of the signal at pin **EN/FEN** is given in [Chapter 2.4.8](#). In case of a Valid-to-Invalid signal transition, an error is detected. In this case, an Emergency (Regular) turn-off sequence is initiated, bit **PER.ENER** is set and a fault notification is issued on pin **NFLTA** (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). The current validity state of the signal at pin **EN/FEN** can be read on bit **PSTAT2.ENVAL**. This function can be tested by generating an invalid signal on pin **EN/FEN** and verifying that the actions done by the device correspond to the expected behavior.

### 3.2.4 Output Stage Monitoring

The Output Stage Monitoring functionality is summarized in **Table 20**:

**Table 20 Output Stage Monitoring Overview**

Parameter	Short Description
Function	Monitoring of signals <b>TON</b> and <b>TOFF</b> .
Periodicity	Continuous.
Action in case of failure event	<ol style="list-style-type: none"> <li>1. Tristate Output Stage (bit <b>SSTAT.HZ</b> set)</li> <li>2. Bit <b>SCTRL.OSTC</b> and error Flag <b>SER.OSTER</b> are set.</li> <li>3. Assertion of signal <b>NFLTA</b>.</li> </ol>
Programmability	Yes (can be disabled).
In-System Testability	Yes.

Signals **TON** and **TOFF** are normally connected to an external booster (**Figure 28**). In case the inputs of the booster can not be driven (e.g. short circuit), the resulting high currents may lead to the destruction of the 1EDI2002AS and / or of the booster. This failure case is avoided thanks to the Output Stage Monitoring function.

When levels at **TON** and **TOFF** differ from the expected levels, the output stage is tristated and bit **SSTAT.HZ** is set. A transition of bit **SSTAT.HZ** from 0<sub>B</sub> to 1<sub>B</sub> generates an Event Class A: bit **SCTRL.OSTC** and error flag **SER.OSTER** are set, signal **NFLTA** is asserted (see **Chapter 2.4.7**).

The monitoring is continuous, but is inhibited for the inhibition time  $t_{OSM}$  after commutation. At turn-on, time  $t_{OSM}$  is counted from the beginning of the turn-on sequence. At turn-off, time  $t_{OSM}$  is counted from the moment where the hard switching action takes place (after the TTOFF plateau). Signal **TON** is compared against  $V_{OSMON}$ . Signal **TOFF** is compared against  $V_{OSMOF}$ .

*Note:* Bit **SCTRL.OSTC** is cleared either by setting bit **PCTRL.CLRS** or by a falling edge of signal **OSD**.

In OPM5 and OPM6, Output Stage Monitoring for **TON** is disabled.

Output Stage Monitoring is disabled when the device is already in tristate (for example, when pin **OSD** is at High Level). The Output Stage returns from tristate to normal conditions when bit **SSTAT.HZ** is cleared. Clearing bit **SSTAT.HZ** reactivates the OSM (after the duration of the blanking time).

*Note:* The OSM can be permanently disabled by setting bit **SCFG.OSMD**, for both **TON** and **TOFF**.

The OSM can be tested on system level by (for example) pulling the IGBT gate signal high while the device issues a PWM Low command. This can be done for example in combination with the ASC function of Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage. It can then be verified that the reaction of the device corresponds to the expected behavior.

### 3.3 Protection Functions: Category B

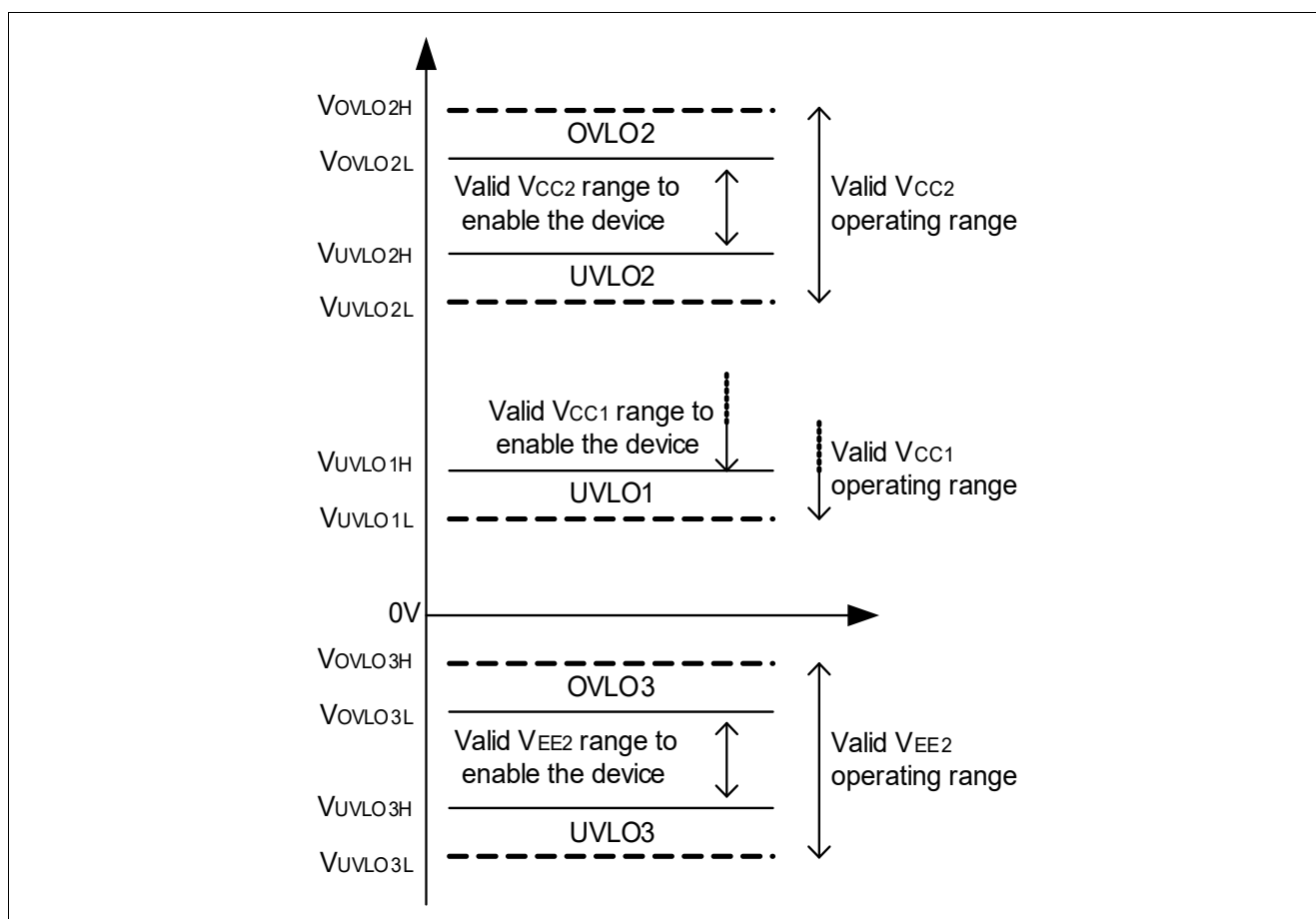
#### 3.3.1 Power Supply Voltage Monitoring

The Power Supply Voltage Monitoring functionality is summarized in [Table 21](#):

**Table 21 Power Supply Voltage Monitoring Overview**

Parameter	Short Description
Function	Monitoring of $V_{CC1}$ , $V_{CC2}$ , $V_{EE2}$ .
Periodicity	Continuous.
Action in case of failure event	<ol style="list-style-type: none"> <li>Emergency (Regular) Turn-off Sequence.</li> <li>Error Flag <b>PER.RST1</b> (UVLO1) or <b>SER.UVLO2ER</b> or <b>OVLO2ER</b> or <b>UVLO3ER</b> or <b>OVLO3ER</b> is set.</li> <li>Assertion of signal <b>NRST/RDY</b> (UVLO1 only) or <b>NFLTb</b>.</li> </ol>
Programmability	Yes (OVLO3 only).
In-System Testability	Yes (see <a href="#">Chapter 3.5.8</a> ).

In order to ensure a correct switching of the IGBT, the device supports an undervoltage lockout (UVLO) function for  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{EE2}$ , and an overvoltage lockout (OVLO) function for  $V_{CC2}$  and  $V_{EE2}$  ([Figure 23](#)).



**Figure 23 Power Supply Supervision Function**

## Protection and Diagnostics

The  $V_{CC1}$  voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage  $V_{CC1}$  of the primary chip drops below  $V_{UVLO1L}$ , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated and signal **NRST/RDY** goes low. In case  $V_{CC1}$  reaches afterwards a level higher than  $V_{UVLO1H}$ , then the error condition is removed and signal **NRST/RDY** is deasserted. Besides, bit **PER.RST1** is set.

The  $V_{CC2}$  voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage  $V_{CC2}$  of the secondary chip drops below  $V_{UVLO2L}$ , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.UVLO2ER** is set and signal **NFLT** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case  $V_{CC2}$  reaches afterwards a level higher than  $V_{UVLO2H}$ , then the error condition is removed and the device can be reenabled.

The  $V_{CC2}$  voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage  $V_{CC2}$  of the secondary chip goes above  $V_{OVLO2H}$ , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.OVLO2ER** is set and signal **NFLT** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case  $V_{CC2}$  reaches afterwards a level below  $V_{OVLO2L}$ , then the error condition is removed and the device can be reenabled.

The  $V_{EE2}$  voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage  $V_{EE2}$  of the secondary chip drops below  $V_{UVLO3L}$ , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.UVLO3ER** is set and signal **NFLT** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case  $V_{EE2}$  reaches afterwards a level higher than  $V_{UVLO3H}$ , then the error condition is removed and the device can be reenabled.

The  $V_{EE2}$  voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage  $V_{EE2}$  of the secondary chip goes above  $V_{OVLO3H}$ , an error is detected. In this case, if bit **SCFG2.OVLO3D** is set, an emergency (Regular) turn-off sequence is initiated, bit **SER.OVLO3ER** is set and signal **NFLT** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case  $V_{EE2}$  reaches afterwards a level below  $V_{OVLO3L}$ , then the error condition is removed and the device can be reenabled. In case an error is detected while bit **SCFG2.OVLO3D** is cleared, no emergency turn-off sequence is initiated, and **NFLT** is not activated. However, bit is **SER.OVLO3ER** set.

The current status of the error detection of OVLO2, UVLO3 and OVLO3 mechanism is available by reading bit **SSTAT2.UVLO2M**, **OVLO2M**, **UVLO3M** or **OVLO3M** respectively.

*Note:* In case  $V_{CC2}$  goes below the voltage  $V_{RST2}$ , the secondary chip is kept in reset state.

### 3.3.2 Internal Supervision

The Internal Supervision functionality is summarized in [Table 22](#):

**Table 22 System Supervision Overview**

Parameter	Short Description
Function	Monitoring of the key internal functions of the chip.
Periodicity	Continuous.
Action in case of failure event	See below
Programmability	No.
In-System Testability	No.

The primary and secondary chips are equipped with internal verification mechanisms ensuring that the key functions of the device are operating correctly. The internal blocks which are supervised are listed below:



## Protection and Diagnostics

- Lifesign watchdog: mutual verification of the response of both chips (both primary and secondary).
- Oscillators (both primary and secondary, including open / short detection on signals **IREF1** and **IREF2**).
- Memory error (both primary and secondary).

### 3.3.2.1 Lifesign watchdog

The primary and the secondary chips monitor each other by the mean of a lifesign signal. The periodicity of the lifesign is typically  $t_{LS}$ . Each chip expects a lifesign from its counterpart within a given time window. In case two consecutive lifesign errors are detected by a chip, an Event Class B is generated. Depending on which side has detected the error, either bit **PER.CER1** or **SER.CER2** is set.

*Note: Bits **PER.CER1** and **SER.CER2** indicate a loss of communication event. The current status of the internal communication is indicated by bit **PSTAT.SRDY**.*

### 3.3.2.2 Oscillator Monitoring

The main oscillators on the primary and on the secondary side are monitored continuously. Two distinct mechanisms are used for this purpose:

- Lifesign Watchdog allows to detect significant deviations from the nominal frequency (both primary and secondary, see above).
- Open / short detection on pin **IREF1**.
- Open detection on pin **IREF2**.

In case a failure is detected on pin **IREF1**, the primary chip is kept in reset state for the duration of the failure and signal **NRST/RDY** is asserted. This leads to the detection of a lifesign error by the secondary chip, generating thus an Event Class B.

In case a failure is detected on pin **IREF2**, an Emergency (regular) Turn-Off sequence is initiated. The secondary chip is kept in reset state for the duration of the failure. This leads to the detection of a lifesign error by the primary chip, generating thus an Event Class B.

### 3.3.2.3 Memory Supervision

The configuration parameters of the device, stored in the registers, are protected with a parity bit protection mechanism. Both primary and secondary chips are protected (refer to **Chapter 4**).

In case a failure is detected on the primary chip, it is kept in reset state, and both signal **NRST/RDY** and **NFLTb** are asserted. The secondary side initiates an Emergency (Regular) Turn-Off sequence.

In case a memory failure is detected by the secondary chip, an Emergency (Regular) Turn-Off sequence is initiated. The secondary chip is kept in reset state for the duration of the failure. This leads to the detection of a lifesign error by the primary chip, generating thus an Event Class B.

### 3.4 Protection Functions: Category C

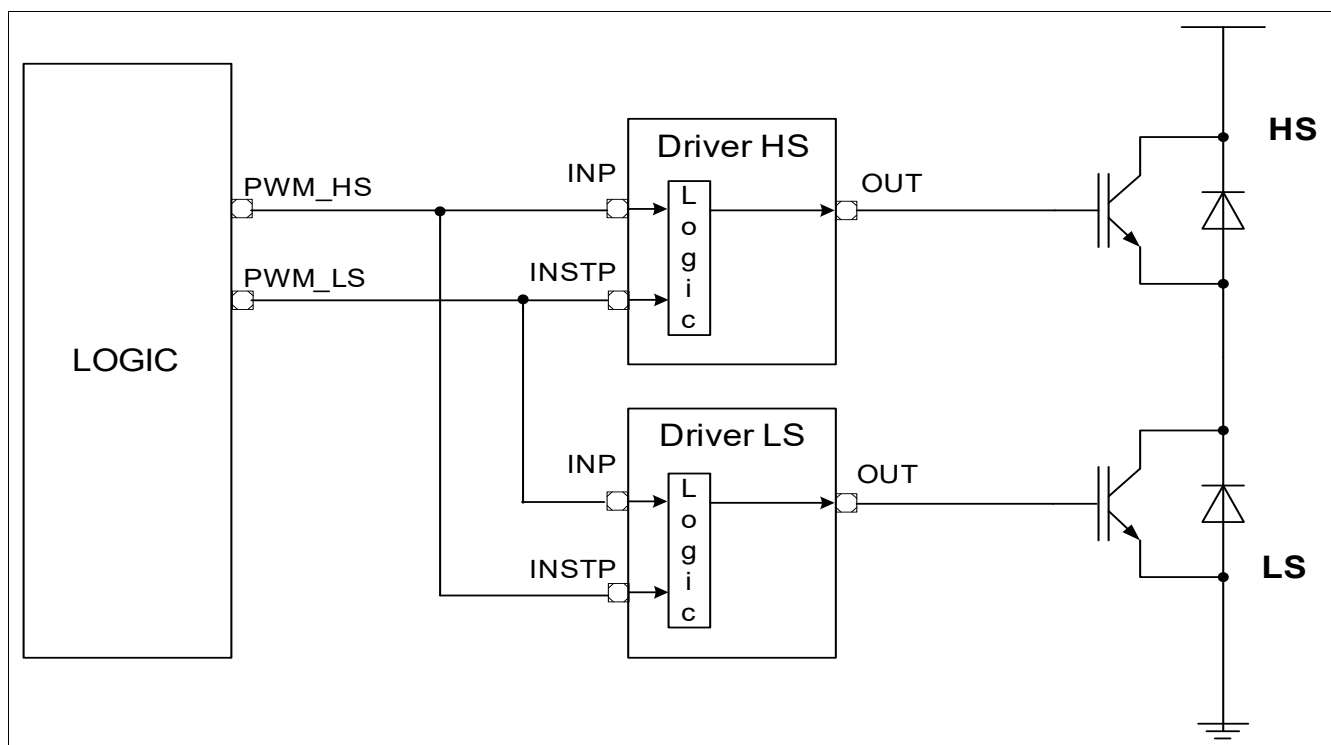
#### 3.4.1 Shoot Through Protection function

The Shoot Through Protection (STP) functionality is summarized in [Table 23](#):

**Table 23 STP Overview**

Parameter	Short Description
Function	Prevents both High-Side and Low-Side Switches to be activated simultaneously.
Periodicity	Continuous.
Action in case of failure event	1. The signal at pin <b>INP</b> is inhibited. 2. Error Flag <b>PER.STPER</b> is set.
Programmability	Yes (dead time).
In-System Testability	Yes.

With the implemented STP function, a low-side (resp. high-side) device is able to monitor the status of its high-side (resp. low-side) counterpart. The input pin **INSTP** provides an input for the PWM signal of the driver's counterpart ([Figure 24](#)).



**Figure 24 Shoot Through Protection: Principle of Operation**

In case one of the driver is in ON state, the driver's counterpart PWM input is inhibited, preventing it to turn-on (See [Chapter 2.4.3](#)). A minimum dead time is defined by hardware. This dead time is programmable via bit field **PCFG2.STPDEL**. Conceptually, the STP aims at providing an additional “line of defense” for the system in case erroneous PWM commands are issued by the primary logic. In normal operation, dead time management shall be performed at the microcontroller level.

## Protection and Diagnostics

In case a PWM ON command is received on pin **INP** during the inhibition time, a failure event is detected. In this case, the high level at pin **INP** is ignored and bit **PER.STPER** is set.

*Note:* Internal filter ensures that **STPER** is not set for glitches smaller than approximately 50ns.

The STP can be tested by applying non valid **INSTP** and **INP** and by checking bit **PSTAT2.STP**.  
The STP can not be disabled. However, setting pin **INSTP** to  $V_{GND1}$  deactivates de facto the function.

### 3.4.2 Gate Monitoring

The Gate Monitoring functionality is summarized in **Table 24**:

**Table 24 Gate Monitoring Overview**

Parameter	Short Description
Function	Monitors the waveform at pin <b>GATE</b> .
Periodicity	Timeout detection at every PWM command transition. Exact timing measurement on request.
Action in case of failure event	Flag <b>PER.GER</b> is set.
Programmability	No
In-System Testability	Yes

The goal of this function is to allow a plausibility check on the IGBT gate voltage signal waveform during a switching sequence, for example in order to track degradations of the IGBT gate resistances.

The Gate Monitoring consists in two functions: Gate Timeout and Gate Timing Capture.

#### Gate Timeout

The Gate Timeout mechanism is active for both turn-on and turn-off sequence. At the beginning of a turn-on sequence, an internal 8-bit timer (in the clock domain OSC2) is cleared and starts counting up. When the gate voltage reaches  $V_{GATE2}$ , the timer stops. In case the timer overflows, flag **PER.GER** is set.

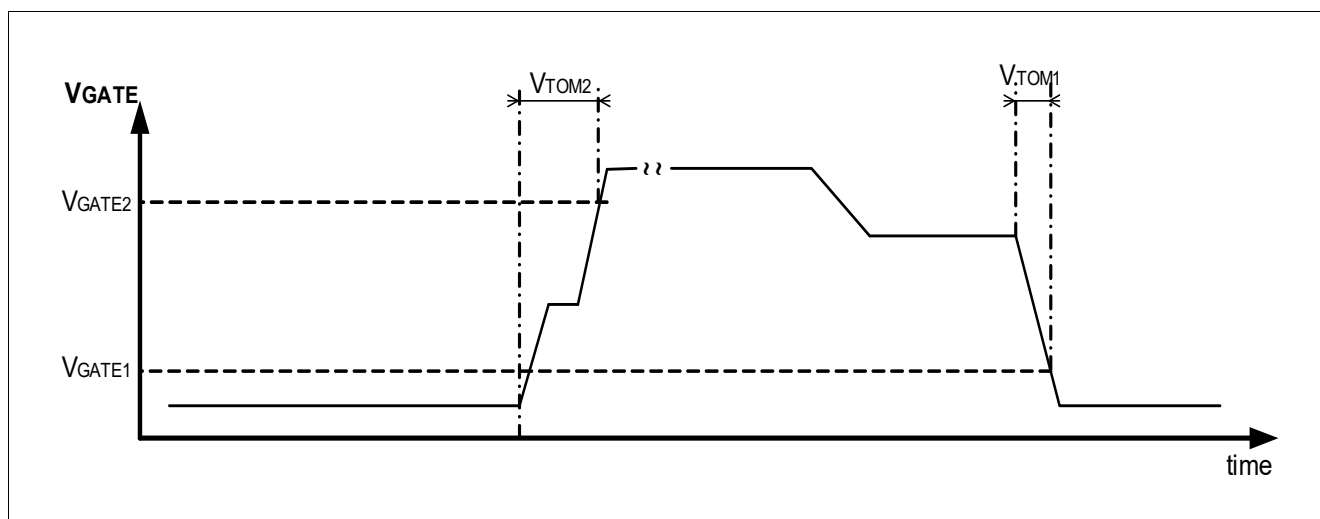
A similar mechanism is initiated at every turn-off sequence (regular or safe). When a **hard** transition occurs, an internal timer is cleared starts counting up. When the gate voltage reaches the value  $V_{GATE1}$ , the timer stops. In case the timer overflows, flag **PER.GER** is set.

The Gate Timeout mechanism is always active, except in OPM5 and OPM6. In OPM5 and OPM6, the Gate Timeout mechanism is disabled during turn-on sequences. It works however normally for turn-off sequences

#### Gate Timing Capture

This function is armed when an SPI command sets bit **PCTRL.GTCT**. This sets both bits **SGM1.GTCT1** and **SGM2.GTCT2** which indicates that the function is armed. At the next turn-on, respectively turn-off, sequence, a timing measurement is performed. At the beginning of a turn-on sequence, bit field **SGM2.VTOM2** is cleared and the device starts incrementing an internal counter (in the clock domain of SSOSC2). When signal **GATE** reaches voltage  $V_{GATE2}$ , the value of the timer is stored in bit field **SGM2.VTOM2** and bit **SGM2.GTCT2** is cleared. In case the timer overflows, value  $FF_H$  is stored.

Similarly, at the **hard** transition of a turn-off sequence, bit field **SGM1.VTOM1** is cleared and the device starts incrementing an internal counter (in the clock domain of SSOSC2). When signal **GATE** reaches voltage  $V_{GATE1}$ , the value of the timer is stored in bit field **SGM1.VTOM1** and bit **SGM1.GTCT1** is cleared. In case the timer overflows, value  $FF_H$  is stored.



**Figure 25 Gate Monitoring Function: Timing Definition**

The Gate Monitoring can be tested on system level by (for example) pulling the IGBT gate signal high while the device issues a PWM Low command. This can be done for example in combination with the ASC function of Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage. It can then be verified that the reaction of the device corresponds to the expected behavior.

### 3.4.3 Temperature Monitoring

The Temperature Monitoring functionality is summarized in [Table 25](#):

**Table 25 Temperature Monitoring Overview**

Parameter	Short Description
Function	Warning in case of over-temperature.
Periodicity	Continuous.
Action in case of failure event	Flag <b>PER.OTER</b> is set.
Programmability	No
In-System Testability	No

The device is equipped with an internal temperature sensor. In case the value measured by the internal sensor temperature exceeds a given threshold, bit **PER.OTER** is set.

### 3.4.4 SPI Error Detection

The SPI Error Detection mechanisms are summarized in [Table 26](#):

**Table 26 SPI Error Detection Overview**

Parameter	Short Description
Function	Non valid SPI command detection and notification.
Periodicity	Continuous.

## Protection and Diagnostics

**Table 26 SPI Error Detection Overview** (cont'd)

Parameter	Short Description
Action in case of failure event	Flag <b>PER.SPIER</b> is set.
Programmability	Yes (parity can be disabled).
In-System Testability	Yes.

For more details, see [Chapter 2.4.4.4](#).

The SPI Error Detection Mechanism can be tested by inserting on purpose a dedicated error and by verifying that the device's reaction is conform to specification.

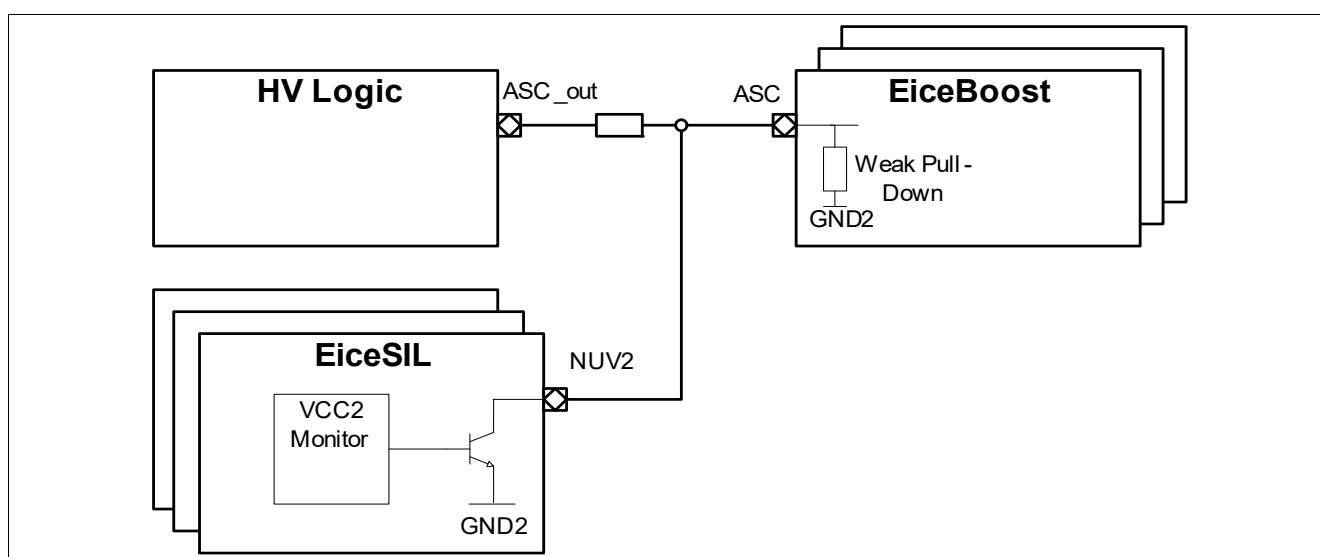
### 3.4.5 Active Short Circuit Support

The Active Short Circuit Support Function is summarized in [Table 27](#):

**Table 27 Active Short Circuit Support Overview**

Parameter	Short Description
Function	Notification in case $V_{CC2}$ is below the UVLO2 threshold or internal digital supply not valid.
Periodicity	Continuous.
Action in case of failure event	Signal <b>NUV2</b> activated.
Programmability	No.
In-System Testability	Yes.

This feature is aimed at being used in combination with a booster device supporting a direct turn-on input (pin ASC, see [Figure 26](#)). Any time the voltage  $V_{CC2}$  goes below threshold  $V_{UVLO2L}$ , or the internal digital voltage supply is not valid, the open drain pin **NUV2** drives a low level for the duration of the event.



**Figure 26 ASC Strategy Support**

## Protection and Diagnostics

The **NUV2** pin functionality can be tested on system level by creating the conditions of its activation and verifying that the reaction of the device corresponds to the expected behavior.

### 3.4.6 IGBT State Monitoring

The IGBT State Monitoring mechanism is summarized in **Table 28**:

**Table 28 IGBT State Monitoring Overview**

Parameter	Short Description
Function	Provides the result of the DESAT comparison logic to pin <b>DOUT</b> .
Periodicity	Continuous.
Action in case of failure event	None.
Programmability	Yes (function can be disabled).
In-System Testability	Yes.

At every PWM command signal transition, once the DESAT blanking time is elapsed, the voltage measured at pin **DESAT** is compared with the internal threshold and the result is forwarded to pin **DOUT**. That way, the primary logic can compare the IGBT state (ON / OFF) with the issues PWM command. The current voltage on pin **DOUT** is accessible via SPI by reading bit **PPIN.DOUTL**. Pin DOUT can be activated or deactivated (tristate) via bit **PCFG2.DOEN1**. Besides, bit **SCFG2.ISMEN** need to be set as well.

In order to be functional, the DESAT clamping shall be disabled (bit **SCFG.DSTCEN** cleared).

### **3.5 Protection Functions: Category D**

#### **3.5.1 Operation in Verification Mode and Weak Active Mode**

Verification Mode and Weak Active Mode are used to start intrusive test functions on device and system level, in order to verify during life time safety relevant functions. The following functions are supported in Verification and Weak Active Mode:

- Weak Turn-On
- DESAT Supervision Level 1
- DESAT Supervision Level 2
- DESAT Supervision Level 3
- OCP Supervision Level 1
- OCP Supervision Level 3
- UVLOx and OVLOx Supervision Level 1
- Internal Clock Supervision
- DIO Supervision
- Timing Calibration Feature

Intrusive test functions can only be started once a correct sequence of SPI commands has been received after reset. The implementation of the device ensures that no intrusive function can be started when the device is normally active.

A time-out function ensures that the device quits OPM5 or OPM6 to OPM1 after a hardware defined time.

The verification functions are triggered by setting the corresponding bit fields in registers **PSCR** or **SSCR** in OPM2. The settings are then activated in OPM5. Only one verification function should be activated at the time.

In OPM5 and OPM6, Gate Monitoring for High level and Output Stage Monitoring on pin **TON** are disabled

*Note:* In OPM5 and OPM6 mode, it is recommended to have bit field **SSTOF.STVAL** programmed to 0<sub>H</sub>.

#### **3.5.2 Weak Turn On**

The Weak-Turn On (WTO) corresponds to the operation when Mode OPM6 is active.

The purpose of the Weak Turn-On functionality is to perform a “probe” test of the IGBT, by switching it on with a reduced gate voltage, in order to limit the current through it in case of overcurrent conditions. This allows to avoid high currents when the system has no memory of the previous state.

In Mode OPM6, when the driver initiates a turn-on sequence after the reception of a PWM command, the ON voltage at signal **TON** is defined by bit field **SCTRL.GPONS**. **Figure 27** shows an idealized weak turn-on sequence.

The device allows for external booster voltage compensation at the IGBT gate. When bit **SCFG2.VBEC** is cleared, the voltage at TON at the plateau corresponds to the programmed value. When bit **SCFG2.VBEC** is set, an additional  $V_{BE}$  (base emitter junction voltage of an internal pn diode) is subtracted to the programmed voltage at TON in order to compensate for the  $V_{BE}$  of an external booster.

*Note:* When using WTO, it is recommended to have the selected TTOFF (if active) plateau at a smaller voltage than the WTO voltage.

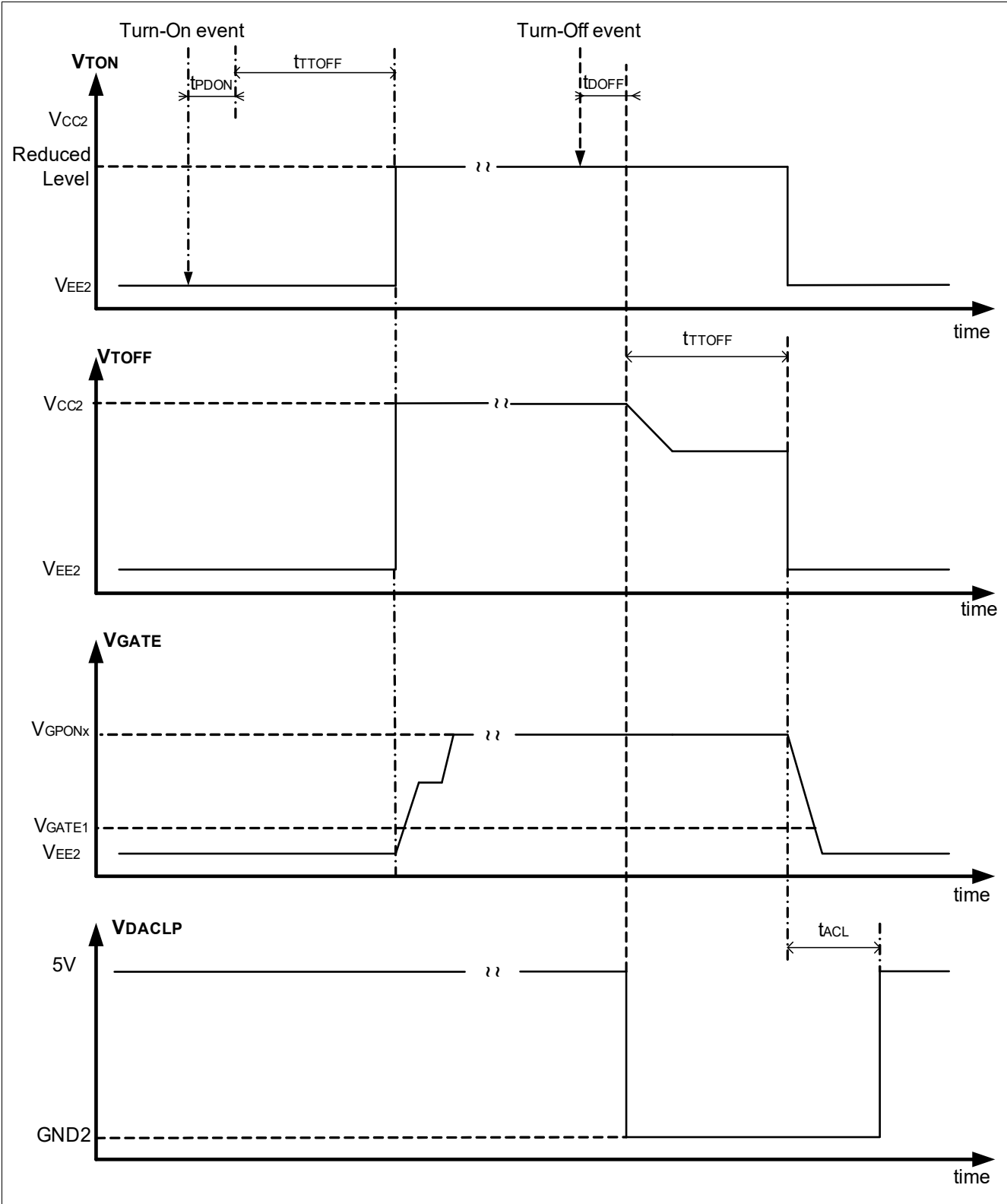


Figure 27 Idealized Weak Turn-On Sequence

3.5.3 DESAT Supervision Level 1

The DESAT Supervision Level 1 functionality is summarized in [Table 29](#):



## Protection and Diagnostics

**Table 29 DESAT Supervision Level 1 Overview**

Parameter	Short Description
Function	Supervision of the DESAT functionality.
Periodicity	On request.
Action in case of failure event	N.a.
Programmability	No
In-System Testability	No

The purpose of the DESAT Supervision Level 1 function is to verify that the DESAT feature is operational over the whole life time of the application. Since the DESAT supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). This mechanism aims at generating artificially a DESAT error, verifying that it is recognized by the device and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where the signal input of the comparator is internally pulled up above the threshold voltage (see [Figure 19](#)). The DESAT function works normally otherwise. When the device enters OPM6 and turns on, after the blanking time has elapsed, a DESAT error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is issued at the output stage (weak turn-on).

### 3.5.4 DESAT Supervision Level 2

The DESAT Supervision Level 2 functionality is summarized in [Table 30](#):

**Table 30 DESAT Supervision Level 2 Overview**

Parameter	Short Description
Function	Supervision of the DESAT functionality.
Periodicity	On request.
Action in case of failure event	N.a.
Programmability	No
In-System Testability	No

The purpose of the DESAT Supervision Level 2 function is to verify that the DESAT feature is operational over the whole life time of the application. Since the DESAT supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). This mechanism aims at generating artificially a DESAT error, verifying that it is recognized by the device and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where, as soon as the device is in OPM6 and a PWM turn-on command is received, no action is executed on the output stage. However, the DESAT logic works normally. It means that after the blanking time has elapsed, the voltage on pin DESAT should exceed the DESAT threshold level, leading to a DESAT error, with the corresponding actions being triggered by the driver.

The **INP** signal is not issued at the output stage.

## Protection and Diagnostics

### 3.5.5 DESAT Supervision Level 3

The DESAT Supervision Level 3 functionality is summarized in [Table 31](#):

**Table 31 DESAT Supervision Level 3 Overview**

Parameter	Short Description
Function	Supervision of the DESAT functionality.
Periodicity	On request.
Action in case of failure event	N.a.
Programmability	No
In-System Testability	No

The purpose of the DESAT Supervision Level 3 function is to verify that the DESAT feature is operational over the whole life time of the application. Since the DESAT supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). This mechanism aims at generating artificially a DESAT error, verifying that it is recognized by the device and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where the signal input of the comparator is internally pulled up above the threshold voltage (see [Figure 19](#)). When the device enters OPM6, independently from the PWM signal, a DESAT error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is not issued at the output stage.

*Note:* When using DESAT supervision Level 3, bit field **SSTTOF.STVAL** must be programmed to 0<sub>H</sub>

### 3.5.6 OCP Supervision Level 1

The OCP Supervision functionality is summarized in [Table 32](#):

**Table 32 OCP Supervision Level 1 Overview**

Parameter	Short Description
Function	Supervision of the OCP functionality.
Periodicity	On Request.
Action in case of failure event	N.a.
Programmability	No
In-System Testability	No

The purpose of the OCP Supervision Level 1 function is to verify that the OCP feature is operational over the whole life time of the application. Since the OCP supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). The main goal of this mechanism is to generate artificially an OCP error, to verify that it is recognized by the driver and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where here the signal input of both comparators is internally pulled up above their respective threshold voltages (see [Figure 22](#)). The OCP function works normally otherwise. When the device enters OPM6 and turns on, after the blanking time has elapsed, an OCP error is generated, with the corresponding actions being triggered by the device.

## Protection and Diagnostics

The **INP** signal is issued at the output stage (weak turn-on).

### 3.5.7 OCP Supervision Level 3

The OCP Supervision functionality is summarized in **Table 33**:

**Table 33 OCP Supervision Level 3 Overview**

Parameter	Short Description
Function	Supervision of the OCP functionality.
Periodicity	On Request.
Action in case of failure event	N.a.
Programmability	No
In-System Testability	No

The purpose of the OCP Supervision Level 3 function is to verify that the OCP feature is operational over the whole life time of the application. Since the OCP supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). The main goal of this mechanism is to generate artificially an OCP error, to verify that it is recognized by the driver and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where here the signal input of both comparators is internally pulled up above their respective threshold voltages (see **Figure 22**). When the device enters OPM6, independently from the PWM command, an OCP error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is not issued at the output stage.

*Note:* When using OCP supervision Level 3, bit field **SSTOF.STVAL** must be programmed to 0<sub>H</sub>

### 3.5.8 Power Supply Monitoring Supervision

The Power Supply Monitoring Supervision monitoring functionality is summarized in **Table 34**:

**Table 34 Power Supply Monitoring Supervision Overview**

Parameter	Short Description
Function	Supervision of the Power Supply Monitoring Mechanisms.
Periodicity	On Request.
Action in case of event	N.a.
Programmability	No
In-System Testability	No

The purpose of this supervision function is to verify that the Power Supply Monitoring functions (UVLO2, OVLO2, UVLO3, OVLO3) are operational over the whole life time of the application. Since this supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 (e.g. after power-up during the initialization phase). The main goal of this mechanism is to generate artificially a power supply monitoring

## **Protection and Diagnostics**

error, in order to verify that it is recognized by the driver and that an error notification is correctly issued to the primary logic.

When this function is triggered, the supervision mechanism of the power supply addressed by the command is activated. The internal threshold of the comparator delivers a “dummy” error, with the corresponding actions being triggered by the driver.

The supervision of UVLO1 is not supported by the device.

## Protection and Diagnostics

### 3.5.9 Internal Clock Supervision

The Primary Clock Supervision functionality is summarized in [Table 35](#):

**Table 35 Primary Clock Supervision Overview**

Parameter	Short Description
Function	Supervision of the frequency of OSC1 and SSOSC2.
Periodicity	On Request.
Action in case of event	N.a.
Programmability	No
In-System Testability	No

The clock supervision function consists on the primary clock supervision and the TCF feature.

#### Primary Clock Supervision

The purpose of this supervision function is to verify the frequency deviation of the primary clock. This function works in such a way that the PWM input signal is used to start and stop a counter clocked by OSC1. The function is activated when the device is in OPM5 or OPM6. The counter is incremented for the duration of the High level at pin **INP**. At a High-to-Low transition at pin INP, the counter is stopped, and its content is transferred to bit field **PCS.CS1**. A plausibility check can therefore be made by the logic. In case of a long **INP** pulse, the counter does not overflow but stays at the maximum value until cleared. **PCS.CS1** is cleared by setting bit **PCTRL.CLRP**.

The **INP** signal is not issued at the output stage.

*Note: OSC2 is indirectly monitored by the Life Sign mechanism.*

#### Timing Calibration Feature

The purpose of this supervision function is to measure the frequency of oscillator SSOC2. The PWM input signal is used to start and stop a counter clocked by SSOSC2. The function is activated when the device is in OPM6 (only). The counter is incremented for the duration of the High level at pin **INP**. At a High-to-Low transition at pin INP, the counter is stopped, and its content is transferred to bit field **SCS.CS2**. A plausibility check can therefore be made by the logic. In case of a long **INP** pulse, the counter does not overflow but stays at the maximum value until cleared. **SCS.CS2** is cleared by a reset event only.

The **INP** signal is not issued at the output stage.

### 3.5.10 DIO Supervision

The IGBT State Monitoring mechanisms summarized in [Table 28](#):

**Table 36 DIO Supervision Overview**

Parameter	Short Description
Function	Supervision of the Digital Channel.
Periodicity	On Request.
Action in case of failure event	None.

---

**Protection and Diagnostics**

**Table 36 DIO Supervision Overview** (cont'd)

Parameter	Short Description
Programmability	No.
In-System Testability	No.

The purpose of this supervision function is to verify the digital channel functionality. Pin **DIO1** shall be configured as an output. The following is valid for OPM5 and OPM6. This function works on such a way that the signal at pin **INP** is forwarded internally to pin **DIO1**, allowing the detection of short circuits on this signal.

The **INP** signal is in this case not forwarded to the secondary chip.

## Register Description

### 4 Register Description

This chapter describes the internal registers of the device. [Table 37](#) provides an overview of the implemented registers. The abbreviations shown in [Table 38](#) are used in the whole section.

**Table 37 Register Overview**

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
<b>Register Description, Primary Register Description</b>				
<b>PID</b>	Primary ID Register	00 <sub>H</sub>	n.a.	xxxx <sub>H</sub>
<b>PSTAT</b>	Primary Status Register	01 <sub>H</sub>	n.a.	087D <sub>H</sub>
<b>PSTAT2</b>	Primary Second Status Register	02 <sub>H</sub>	n.a.	0010 <sub>H</sub>
<b>PER</b>	Primary Error Register	03 <sub>H</sub>	n.a.	1C00 <sub>H</sub>
<b>PCFG</b>	Primary Configuration Register	04 <sub>H</sub>	n.a.	0004 <sub>H</sub>
<b>PCFG2</b>	Primary Second Configuration Register	05 <sub>H</sub>	n.a.	0045 <sub>H</sub>
<b>PCTRL</b>	Primary Control Register	06 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>PCTRL2</b>	Primary Second Control Register	07 <sub>H</sub>	n.a.	003D <sub>H</sub>
<b>PSCR</b>	Primary Supervision Function Control Register	08 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>PRW</b>	Primary Read/Write Register	09 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>PPIN</b>	Primary Pin Status Register	0A <sub>H</sub>	n.a.	xxxx <sub>H</sub>
<b>PCS</b>	Primary Clock Supervision Register	0B <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>Register Description, Secondary Registers Description</b>				
<b>SID</b>	Secondary ID Register	10 <sub>H</sub>	n.a.	xxxx <sub>H</sub>
<b>SSTAT</b>	Secondary Status Register	11 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>SSTAT2</b>	Secondary Second Status Register	12 <sub>H</sub>	n.a.	xxxx <sub>H</sub>
<b>SER</b>	Secondary Error Register	13 <sub>H</sub>	n.a.	8011 <sub>H</sub>
<b>SCFG</b>	Secondary Configuration Register	14 <sub>H</sub>	n.a.	0190 <sub>H</sub>
<b>SCFG2</b>	Secondary Second Configuration Register	15 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>SCTRL</b>	Secondary Control Register	16 <sub>H</sub>	n.a.	00F1 <sub>H</sub>
<b>SSCR</b>	Secondary Supervision Function Control Register	17 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>SDESAT</b>	Secondary DESAT Blanking Time Register	18 <sub>H</sub>	n.a.	2000 <sub>H</sub>
<b>SOCBP</b>	Secondary OCP Blanking Time Register	19 <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>SRTTOF</b>	Secondary Regular TTOFF Configuration Register	1A <sub>H</sub>	n.a.	0001 <sub>H</sub>
<b>SSTTOF</b>	Secondary Safe TTOFF Configuration Register	1B <sub>H</sub>	n.a.	2000 <sub>H</sub>
<b>SGM1</b>	Secondary First Gate Monitoring Register	1C <sub>H</sub>	n.a.	FF01 <sub>H</sub>
<b>SGM2</b>	Secondary Second Gate Monitoring Register	1D <sub>H</sub>	n.a.	FF01 <sub>H</sub>

## Register Description

**Table 37 Register Overview** (cont'd)

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
<b>SACLT</b>	Secondary Active Clamping Configuration Register	1E <sub>H</sub>	n.a.	2600 <sub>H</sub>
<b>SCS</b>	Secondary Clock Supervision Register	1F <sub>H</sub>	n.a.	0001 <sub>H</sub>

The registers are addressed wordwise.

**Table 38 Bit Access Terminology**

Mode	Symbol	Description
<b>Basic Access Types</b>		
read/write	rw	This bit or bit field can be written or read.
read	r	This bit or bit field is read only.
write	w	This bit or bit field is write only (read as 0 <sub>H</sub> ).
read/write hardware affected	rwh	As rw, but bit or bit field can also be modified by hardware.
read hardware affected	rh	As r, but bit or bit field can also be modified by hardware.
sticky	s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten they can be switched again into their reset state only by a reset operation. Software and internal logic (except reset-like functions) cannot switch this type of bit into its reset state by writing directly the register. The sticky attribute can be combined to other functions (e.g. ‘rh’).
Reserved / not implemented	0	Bit fields named ‘0’ indicate not implemented functions. They have the following behavior: <ul style="list-style-type: none"> <li>• Reading these bit fields returns 0<sub>H</sub>.</li> <li>• Writing these bit fields has no effect.</li> </ul> These bit fields are reserved. When writing, software should always set such bit fields to 0 <sub>H</sub> in order to preserve compatibility with future products.
Reserved / not defined	Res	Certain bit fields or bit combinations in a bit field can be marked as ‘Reserved’, indicating that the behavior of the device is undefined for that combination of bits. Setting the register to such an undefined value may lead to unpredictable results. When writing, software must always set such bit fields to legal values.



## 4.1 Primary Register Description

This register contains the identification number of the primary chip version.

PID	Offset	WakeUp Value	Reset Value
Primary ID Register	00 <sub>H</sub>	n.a.	xxxx <sub>H</sub>

Bit field diagram for Primary ID Register:

- Bits 15-8: PVERS (8 bits)
- Bits 7-4: PVERS (4 bits)
- Bit 3: 0 (1 bit)
- Bit 2: LMI (1 bit)
- Bit 1: P (1 bit)

Field	Bits	Type	Description
<b>PVERS</b>	15:4	r	<b>Primary Chip Identification</b> This bit field defines the version of the primary chip. This bit field is hard-wired: 4A3 <sub>H</sub> : AD step
<b>0</b>	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Status Register

This register contains information on the status of the device.

PSTAT Primary Status Register				Offset 01 <sub>H</sub>	Wakeup Value n.a.	Reset Value 087D <sub>H</sub>
15	12	11	10	9	8	
0				ERR	0	GPONS
	r	rh	r		rh	
7	6	5	2	1	0	
ACT	SRDY	GPOFS		LMI	P	
rh	rh	rh		rh	rh	

Field	Bits	Type	Description
0	15:12	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
ERR	11	rh	<b>Error Status</b> This bit is the OR combination of all bits of register <a href="#">PER</a> . 0 <sub>B</sub> <b>noError</b> , No error is detected. 1 <sub>B</sub> <b>error</b> , An error is detected.
0	10	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
GPONS	9:8	rh	<b>Gate Turn-On Plateau Level Configuration Status</b> This bit field indicates the latest turn-on plateau level configuration request (WTO, TTON) received by the primary side via the SPI interface. Coding is identical to bit field <a href="#">PCTRL.GPON</a> .
ACT	7	rh	<b>Active State Status</b> This bit indicates if the device is in Active State (OPM4). 0 <sub>B</sub> <b>notActive</b> , The device is not in Active State. 1 <sub>B</sub> <b>active</b> , The device is in Active State.
SRDY	6	rh	<b>Secondary Ready Status</b> This bit indicates if the secondary chip is ready for operation. 0 <sub>B</sub> <b>notReady</b> , Secondary chip is not ready. 1 <sub>B</sub> <b>ready</b> , Secondary chip is ready.
GPOFS	5:2	rh	<b>Gate Turn-Off Plateau Level Configuration Status (regular turn-off)</b> This bit field indicates the latest turn-off plateau level configuration request (regular TTOFF) received by the primary side via the SPI interface. Coding is identical to bit field <a href="#">PCTRL2.GPOF</a> .

## Register Description

Field	Bits	Type	Description
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Second Status Register

This register contains information on the status of the device.

PSTAT2 Primary Second Status Register				Offset 02 <sub>H</sub>	Wakeup Value n.a.	Reset Value 0010 <sub>H</sub>	
15	12	11	10	9	8		
0				OSTC	STP	OT	HZ
r				rh	rh	rh	rh
7	5	4	3	2	1	0	
OPM		FLTB	FLTA	ENVAL	LMI	P	
rh		rhs	rhs	rh	rh	rh	

Field	Bits	Type	Description
0	15:12	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
OSTC	11	rh	<b>Output Stage Tristate Control</b> This bit is set in case an OSM event.  <i>Note:</i> This bit is a mirror of bit <b>SCTRL.OSTC</b>
STP	10	rh	<b>Shoot Through Protection Status</b> This bit is set in case the shoot through protection inhibition time (i.e. would inhibit a PWM rising edge). 0 <sub>B</sub> <b>inhibitionNotActive</b> , STP inhibition is not active. 1 <sub>B</sub> <b>inhibitionActive</b> , STP inhibition is active.
OT	9	rh	<b>Over Temperature Status</b> This bit is set in case an overtemperature condition is detected.  <i>Note:</i> This bit is a mirror of bit <b>SSTAT.OT</b>  0 <sub>B</sub> <b>noOverTemperature</b> , No over Temperature detected. 1 <sub>B</sub> <b>overTemperatureActive</b> , over Temperature was detected.
HZ	8	rh	<b>Tristate Output Stage Status</b> This bit is set in case the output stage is in tristate.  <i>Note:</i> This bit is a mirror of bit <b>SSTAT.HZ</b>  0 <sub>B</sub> <b>normal</b> , The output stage is in normal operation. 1 <sub>B</sub> <b>tristate</b> , The output stage is tristated.

## Register Description

Field	Bits	Type	Description
<b>OPM</b>	7:5	rh	<p><b>Operating Mode</b> This bit field indicates which operating mode is active.</p> <p><i>Note:</i> This bit field is a mirror of bit field <b>SSTAT.OPM</b></p> <p>000<sub>B</sub> <b>opm0</b>, Mode OPM0 is active .  001<sub>B</sub> <b>opm1</b>, Mode OPM1 is active .  010<sub>B</sub> <b>opm2</b>, Mode OPM2 is active.  011<sub>B</sub> <b>opm3</b>, Mode OPM3 is active.  100<sub>B</sub> <b>opm4</b>, Mode OPM4 is active.  101<sub>B</sub> <b>opm5</b>, Mode OPM5 is active.  110<sub>B</sub> <b>opm6</b>, Mode OPM6 is active.  111<sub>B</sub> , Reserved.</p>
<b>FLTB</b>	4	rhs	<p><b>NFLTB Driver Request</b> This bit indicates what output state is driven by the device at pin <b>NFLTB</b>. This bit is sticky.  0<sub>B</sub> <b>tristate</b>, <b>NFLTB</b> is in tristate.  1<sub>B</sub> <b>lowLevel</b>, A Low Level is issued at <b>NFLTB</b>.</p>
<b>FLTA</b>	3	rhs	<p><b>NFLTA Driver Request</b> This bit indicates what output state is driven by the device at pin <b>NFLTA</b>. This bit is sticky.  0<sub>B</sub> <b>tristate</b>, <b>NFLTA</b> is in tristate.  1<sub>B</sub> <b>lowLevel</b>, A Low Level issued at <b>NFLTA</b>.</p>
<b>ENVAL</b>	2	rh	<p><b>EN/FEN Valid Status</b> This bit indicates if the signal received on pin <b>EN/FEN</b> is valid.  0<sub>B</sub> <b>notValid</b>, A non-valid signal is detected.  1<sub>B</sub> <b>valid</b>, A valid signal is detected.</p>
<b>LMI</b>	1	rh	<p><b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device.  0<sub>B</sub> , Previous Message was processed correctly.  1<sub>B</sub> , Previous Message was discarded.</p>
<b>P</b>	0	rh	<p><b>Parity Bit</b> Odd Parity Bit.</p>

## Register Description

### Primary Error Register

This register provides information on the error status of the device.

PER Primary Error Register				Offset 03 <sub>H</sub>	Wakeup Value n.a.	Reset Value 1C00 <sub>H</sub>	
15	13	12	11	10	9	8	
	0	RSTE1	RST1	ENER	STPER	SPIER	
	r	rhs	rhs	rhs	rhs	rhs	
7	6	5	4	3	2	1	0
VMTO	GER	OVLO3ER	OTER	OSTER	CER1	LMI	P
rh	rh	rh	rh	rh	rhs	rh	rh

Field	Bits	Type	Description
0	15:13	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
RSTE1	12	rhs	<b>Primary External Hard Reset Flag</b> This bit indicates if a reset event has been detected on the primary chip due to the activation of pin <b>NRST/RDY</b> . This bit is sticky. 0 <sub>B</sub> <b>notSet</b> , No external hard reset event has been detected. 1 <sub>B</sub> <b>set</b> , An externally hard reset event has been detected.
RST1	11	rhs	<b>Primary Reset Flag</b> This bit indicates if a reset event has been detected on the primary chip. This bit is sticky. 0 <sub>B</sub> <b>notSet</b> , No reset event has been detected. 1 <sub>B</sub> <b>set</b> , A reset event has been detected.
ENER	10	rhs	<b>EN/FEN Signal Invalid Flag</b> This bit indicates if an invalid-to-valid transition on signal <b>EN/FEN</b> has been detected. This bit is sticky.  <i>Note: This bit can not be cleared while an error condition is active (bit <b>PSTAT2.ENVAL</b> cleared).</i>  0 <sub>B</sub> <b>notSet</b> , No event has been detected. 1 <sub>B</sub> <b>set</b> , An event has been detected.

## Register Description

Field	Bits	Type	Description
<b>STPER</b>	9	rhs	<p><b>Shoot Through Protection Error Flag</b> This bit indicates if a shoot through protection error event has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared while an error condition is active (bit <b>PSTAT2.STP</b> set).</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>SPIER</b>	8	rhs	<p><b>SPI Error Flag</b> This indicates if an SPI error event has been detected. This bit is sticky.</p> <p>0<sub>B</sub> <b>notSet</b>, No error event has been detected. 1<sub>B</sub> <b>set</b>, An error event has been detected.</p>
<b>VMTO</b>	7	rh	<p><b>Verif. Mode Time-Out Flag</b> This bit indicates if a verification mode time-out event has been detected.</p> <p><i>Note:</i> This bit is a mirror of bit <b>SER.VMTO</b>.</p> <p>0<sub>B</sub> <b>notSet</b>, No time-out event has been detected. 1<sub>B</sub> <b>set</b>, A time-out event has been detected.</p>
<b>GER</b>	6	rh	<p><b>GATE Monitoring Error Flag</b> This bit indicates if a GATE monitoring timer overflow occurred during a switching sequence.</p> <p><i>Note:</i> This bit is a mirror of bit <b>SER.GER</b>.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>OVLO3ER</b>	5	rh	<p><b>OVLO3 Error Flag</b> This bit indicates if an Overvoltage Lockout event on V<sub>EE2</sub> has been detected.</p> <p><i>Note:</i> This bit is a mirror of bit <b>SER.OVLO3ER</b>.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>OTER</b>	4	rh	<p><b>Overtemperature Error Flag</b> This bit indicates if an overtemperature condition has been detected.</p> <p><i>Note:</i> This bit is a mirror of bit <b>SER.OTER</b>.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>

## Register Description

Field	Bits	Type	Description
<b>OSTER</b>	3	rh	<p><b>Output Stage Tristate Event Flag</b> This bit indicates if the output stage has been tristated.</p> <p><i>Note:</i> This bit is a mirror of bit <b>SER.OSTER</b>.</p> <p>0<sub>B</sub> <b>notSet</b>, No tristate event has been detected. 1<sub>B</sub> <b>set</b>, A tristate event has been detected.</p>
<b>CER1</b>	2	rhs	<p><b>Communication Error Primary Flag</b> This indicates if a loss of communication event<sup>1)</sup> with the secondary chip has been detected by the primary chip. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared while an error condition is active (bit <b>PSTAT2.SRDY</b> cleared).</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>LMI</b>	1	rh	<p><b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device.</p> <p>0<sub>B</sub> , Previous Message was processed correctly. 1<sub>B</sub> , Previous Message was discarded.</p>
<b>P</b>	0	rh	<p><b>Parity Bit</b> Odd Parity Bit.</p>

1) This bit is not set after a reset event



## Register Description

### Primary Configuration Register

This register is used to select the configuration of the device.

PCFG	Offset	Wakeup Value	Reset Value
Primary Configuration Register	04 <sub>H</sub>	n.a.	0004 <sub>H</sub>

15							8
0							
r							
7	6	5	4	3	2	1	0
0	OSMAEN	OSTAEN	CFG1	PAREN	LMI	P	
r	rw	rw	rwh	rw	rh	rh	

Field	Bits	Type	Description
0	15:6	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
OSMAEN	5	rw	<b>NFLTA Activation on OSM Event Enable Bit</b> This bit enables the activation of signal NFLTA in case of a transition from 0 <sub>B</sub> to 1 <sub>B</sub> of bit <b>PSTAT2.OSTC</b> . 0 <sub>B</sub> <b>disabled</b> , NFLTA activation is disabled. 1 <sub>B</sub> <b>enabled</b> , NFLTA activation is enabled.
OSTAEN	4	rw	<b>NFLTA Activation on Tristate Event Enable Bit</b> This bit enables the activation of signal NFLTA in case of a transition from 0 <sub>B</sub> to 1 <sub>B</sub> of bit <b>PER.OSTER</b> . 0 <sub>B</sub> <b>disabled</b> , NFLTA activation is disabled. 1 <sub>B</sub> <b>enabled</b> , NFLTA activation is enabled.
CFG1	3	rwh	<b>Primary Advanced Configuration Enable Bit</b> This bit enables write accesses to register <b>PCFG2</b> . This bit is automatically cleared when mode OPM2 is left. 0 <sub>B</sub> <b>disabled</b> , Write access to <b>PCFG2</b> are discarded. 1 <sub>B</sub> <b>enabled</b> , Write access to <b>PCFG2</b> are executed normally.
PAREN	2	rw	<b>Parity Enable Bit</b> This bit indicates if the SPI parity error detection is active (reception only). 0 <sub>B</sub> <b>disabled</b> , Parity Check is disabled. 1 <sub>B</sub> <b>enabled</b> , Parity Check is enabled.
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.

---

**Register Description**

Field	Bits	Type	Description
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Second Configuration Register

This register is used to select the configuration of the device. It can only be written if bit **PCFG.CFG1** is set.

PCFG2 Primary Second Configuration Register				Offset 05 <sub>H</sub>	Wakeup Value n.a.	Reset Value 0045 <sub>H</sub>
<div> <div>15</div> <div>10</div> <div>9</div> <div>8</div> </div> <div> <div>0</div> <div>DOEN1</div> <div>DIO1</div> </div>						
r					rw	rw
<div> <div>7</div> <div>6</div> <div>2</div> <div>1</div> <div>0</div> </div> <div> <div>FEN</div> <div>STPDEL</div> <div>LMI</div> <div>P</div> </div>						
rw					rh	rh

Field	Bits	Type	Description
<b>0</b>	15:10	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>DOEN1</b>	9	rw	<b>Primary DOUT Output Enable Bit</b> This bit is used to enable the <b>DOUT</b> signal. 0 <sub>B</sub> <b>disabled</b> , <b>DOUT</b> is disabled (and in tristate). 1 <sub>B</sub> <b>enabled</b> , <b>DOUT</b> is enabled (output).
<b>DIO1</b>	8	rw	<b>Digital Channel Configuration</b> This bit field determines the direction of pin <b>DIO1</b> . 0 <sub>B</sub> <b>output</b> , <b>DIO1</b> is an input. 1 <sub>B</sub> <b>input</b> , <b>DIO1</b> is an output.
<b>FEN</b>	7	rw	<b>EN/FEN Mode Configuration</b> This bit determines the validity mode of a signal at pin <b>EN/FEN</b> . 0 <sub>B</sub> <b>enModeActive</b> , A valid signal is defined as a high level. 1 <sub>B</sub> <b>fenModeActive</b> , A valid signal is defined as a periodic signal.
<b>STPDEL</b>	6:2	rw	<b>Shoot Through Protection Delay Configuration</b> This bit field determines the dead time for the shoot-through protection (in number of OSC1 clock cycles).
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

This register is used to control the device during run-time.

Diagram illustrating the 16-bit register structure. The top part shows a 16-bit bus with bit positions 15 down to 0. Bit 0 is labeled 'r'. The bottom part shows a 7-bit bus with bit positions 7 down to 0. Bit 0 is labeled 'r'. Bits 1-7 are labeled with their respective fields: 1 is 'LMI' (rh), 2-3 are 'GPON' (rw), 4 is 'GTCT' (rwh), 5 is 'CLRP' (rwh), 6 is 'CLRS' (rwh), and 7 is '0' (r).

Field	Bits	Type	Description
0	15:7	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
CLRS	6	rwh	<b>Clear Secondary Request Bit</b> This bit is used to clear the sticky bits on the secondary side. This bit is automatically cleared by hardware. 0 <sub>B</sub> <b>noAction</b> , No action. 1 <sub>B</sub> <b>clear</b> , Clear sticky bits.
CLRP	5	rwh	<b>Clear Primary Request Bit</b> This bit is used to clear the sticky bits on the primary side. This bit is automatically cleared by hardware. 0 <sub>B</sub> <b>noAction</b> , No action. 1 <sub>B</sub> <b>clear</b> , Clear sticky bits and deassert signals <b>NFLTA</b> and <b>NFLTb</b> .
GTCT	4	rwh	<b>Gate Timing Capture Trigger Bit</b> This bit is used to trigger the timing capture mechanism measurements of the Gate Monitoring function. This bit is automatically cleared by hardware. 0 <sub>B</sub> <b>noAction</b> , No action. 1 <sub>B</sub> <b>captureRequest</b> , Request timing captureing.
GPON	3:2	rw	<b>Gate Turn-On Plateau Level Configuration</b> This bit field is used to configure the voltage of the plateau during Weak Turn-On and Two Level Turn-On. 0 <sub>H</sub> <b>gpon0</b> , V <sub>GPON0</sub> selected. 1 <sub>H</sub> <b>gpon1</b> , V <sub>GPON1</sub> selected. 2 <sub>H</sub> <b>gpon2</b> , V <sub>GPON2</sub> selected. 3 <sub>H</sub> <b>gpon3</b> , Reserved (WTO) or Hard Switching (TTON).

## Register Description

Field	Bits	Type	Description
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Second Control Register

This register is used to control the device during run-time.

PCTRL2	Offset	Wakeup Value	Reset Value
Primary Second Control Register	07 <sub>H</sub>	n.a.	003D <sub>H</sub>

15																8
0																
r																

7	6	5					2	1	0
0		GPOF					LMI		P
r		rw					rh		rh

Field	Bits	Type	Description
0	15:6	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
GPOF	5:2	rw	<b>Gate Turn-Off Plateau Level Configuration (regular turn-off)</b> This bit field is used to configure the Two-Level Turn-Off plateau voltage (regular turn-off). 0 <sub>H</sub> <b>gpof0</b> , V <sub>GPOF0</sub> selected. 1 <sub>H</sub> <b>gpof1</b> , V <sub>GPOF1</sub> selected. 2 <sub>H</sub> <b>gpof2</b> , V <sub>GPOF2</sub> selected. 3 <sub>H</sub> <b>gpof3</b> , V <sub>GPOF3</sub> selected. 4 <sub>H</sub> <b>gpof4</b> , V <sub>GPOF4</sub> selected. 5 <sub>H</sub> <b>gpof5</b> , V <sub>GPOF5</sub> selected. 6 <sub>H</sub> <b>gpof6</b> , V <sub>GPOF6</sub> selected. 7 <sub>H</sub> <b>gpof7</b> , V <sub>GPOF7</sub> selected. 8 <sub>H</sub> <b>gpof8</b> , V <sub>GPOF8</sub> selected. 9 <sub>H</sub> <b>gpof9</b> , V <sub>GPOF9</sub> selected. A <sub>H</sub> <b>gpof10</b> , V <sub>GPOF10</sub> selected. B <sub>H</sub> <b>gpof11</b> , V <sub>GPOF11</sub> selected. C <sub>H</sub> <b>gpof12</b> , V <sub>GPOF12</sub> selected. D <sub>H</sub> <b>gpof13</b> , V <sub>GPOF13</sub> selected. E <sub>H</sub> <b>gpof14</b> , V <sub>GPOF14</sub> selected. F <sub>H</sub> <b>gpof15</b> , V <sub>GPOF15</sub> selected.
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Supervision Function Control Register

This register is used to trigger the verification functions on the primary side.

PSCR	Offset	Wakeup Value	Reset Value
Primary Supervision Function Control Register	08 <sub>H</sub>	n.a.	0001 <sub>H</sub>

15								8
0								
r								
7		4	3	2	1	0		
0			VFS1		LMI	P		
r			rwh		rh	rh		

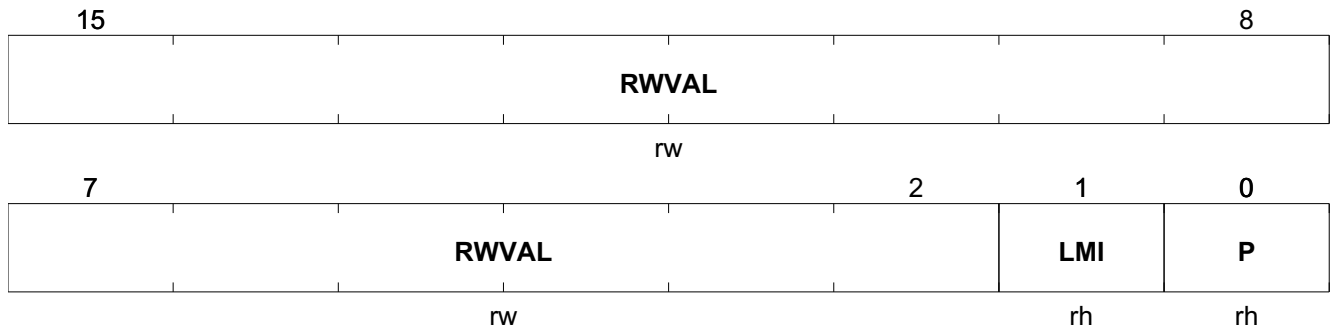
Field	Bits	Type	Description
0	15:4	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
VFS1	3:2	rwh	<b>Primary Verification Function Selection</b> This bit field is used to activate the primary verification functions.  <i>Note:</i> The selection defined by this bit field is only effective when the device enters Mode OPM5. This bit field is automatically cleared when entering OPM1.  00 <sub>B</sub> <b>disabled</b> , No function activated. 01 <sub>B</sub> , Reserved. 10 <sub>B</sub> <b>primaryClockSupervision</b> , Primary Clock Supervision active. 11 <sub>B</sub> <b>dioSupervision</b> , DIO Supervision active.
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Read/Write Register

This register provides a readable and writable address space for data integrity test during runtime. This register is not associated with any hardware functionality.

PRW	Offset	Wakeup Value	Reset Value
Primary Read/Write Register	09 <sub>H</sub>	n.a.	0001 <sub>H</sub>



Field	Bits	Type	Description
<b>RWVAL</b>	15:2	rw	<b>Read/Write value</b> This bit field is “don’t care” for the device.
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.



## Register Description

### Primary Pin Status Register

This register provides status information on the I/Os of the primary chip.

PPIN				Offset	Wakeup Value	Reset Value	
Primary Pin Status Register				0A <sub>H</sub>	n.a.	xxxx <sub>H</sub>	
15				9		8	
0						DIO1L	
r						rh	
7	6	5	4	3	2	1	0
DOUTL	NFLTBL	NFLTAL	ENL	INSTPL	INPL	LMI	P
rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
0	15:9	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
DIO1L	8	rh	<b>Pin DIO1 Level</b> This bit indicates the logical level read on pin <b>DIO1</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.
DOUTL	7	rh	<b>Pin DOUT Level</b> This bit indicates the logical level read on pin <b>DOUT</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.
NFLTBL	6	rh	<b>Pin NFLTBL Level</b> This bit indicates the logical level read on pin <b>NFLTBL</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.
NFLTAL	5	rh	<b>Pin NFLTAL Level</b> This bit indicates the logical level read on pin <b>NFLTAL</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.
ENL	4	rh	<b>Pin EN/FEN Level</b> This bit indicates the logical level read on pin <b>EN/FEN</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.
INSTPL	3	rh	<b>Pin INSTPL Level</b> This bit indicates the logical level read on pin <b>INSTPL</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.

## Register Description

Field	Bits	Type	Description
<b>INPL</b>	2	rh	<b>Pin INP Level</b> This bit indicates the logical level read on pin <b>INP</b> . 0 <sub>B</sub> <b>low</b> , Low-level is detected. 1 <sub>B</sub> <b>high</b> , High-level is detected.
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Primary Clock Supervision Register

This register shows the result of the Primary Clock Supervision function.

PCS	Offset	Wakeup Value	Reset Value
Primary Clock Supervision Register	0B <sub>H</sub>	n.a.	0001 <sub>H</sub>

15								8
CS1								
rh								

7					2	1	0
0						LMI	P
r						rh	rh

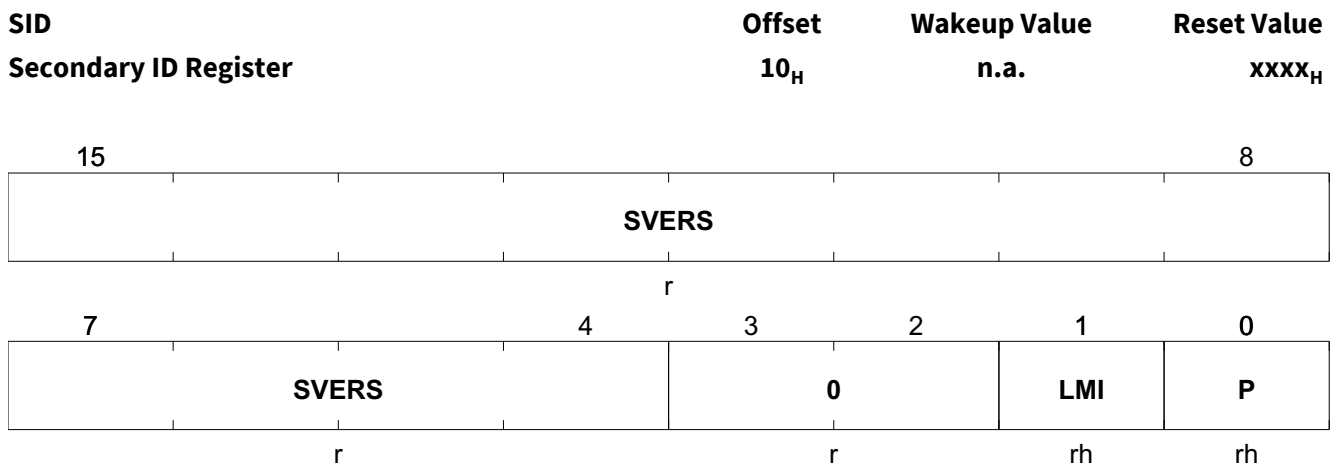
Field	Bits	Type	Description
CS1	15:8	rh	<b>Primary Clock Supervision</b> This bit field is written by hardware by the Primary Clock Supervision function and gives the number of measured OSC1 clock cycles.  <i>Note: This bit field can be cleared by setting bit <b>PCTRL.CLRP</b>.</i>
0	7:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### 4.2 Secondary Registers Description

#### Secondary ID Register

This register contains the identification number of secondary chip version.



Field	Bits	Type	Description
<b>SVERS</b>	15:4	r	<b>Secondary Chip Identification</b> This bit field defines the version of the secondary chip. This bit field is hard-wired: 8B1 <sub>H</sub> : AD Step.
<b>0</b>	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Status Register

This register contains information on the status of the device.

SSTAT Secondary Status Register							
				Offset 11 <sub>H</sub>	Wakeup Value n.a.	Reset Value 0001 <sub>H</sub>	
15	14	13	12	11	10	9	8
VMTOA	G	OT	HZ	OCPCD	DBG	OPM	
rh	rh	rh	rh	rhs	rh	rh	
7	6	5	4	3	2	1	0
OPM	FLTB	FLTA	PWM	0		LMI	P
rh	rh	rh	rh	r		rh	rh

Field	Bits	Type	Description
Res	15:14	rh	<b>Reserved</b> This bit field is reserved.
OT	13	rh	<b>Overtemperature Status</b> This bit indicates if an overtemperature condition is detected. 0 <sub>B</sub> <b>normal</b> , No overtemperature condition is detected. 1 <sub>B</sub> <b>overtempActive</b> , Overtemperature condition is detected.
HZ	12	rh	<b>Output Stage Status</b> This bit indicates the state of the output stage. 0 <sub>B</sub> <b>normal</b> , The output stage is operating normally. 1 <sub>B</sub> <b>tristate</b> , The output stage is tristated.
OCPCD	11	rhs	<b>OCP Current Detection Flag</b> This bit indicates if the voltage at pin <b>OC</b> has been above the internal threshold V <sub>OCPD2</sub> . This bit is sticky. 0 <sub>B</sub> <b>notSet</b> , <b>OC</b> voltage has not been above internal threshold. 1 <sub>B</sub> <b>set</b> , <b>OC</b> voltage has been above internal threshold.
DBG	10	rh	<b>Debug Mode Active Bit</b> This bit indicates if the Debug Mode is active. 0 <sub>B</sub> <b>notSet</b> , Debug Mode is not active. 1 <sub>B</sub> <b>set</b> , Debug Mode is active.
OPM	9:7	rh	<b>Operating Mode</b> This bit field indicates in which operating mode is active. The coding is identical to <b>PSTAT2</b> .

## Register Description

Field	Bits	Type	Description
<b>FLTB</b>	6	rh	<b>Event Class B Error</b> This bit indicates if the conditions leading to an Event Class B are detected. 0 <sub>B</sub> <b>notSet</b> , Event conditions are not met. 1 <sub>B</sub> <b>set</b> , Event conditions are met.
<b>FLTA</b>	5	rh	<b>Event Class A Error</b> This bit indicates if the conditions leading to an Event Class A are detected. 0 <sub>B</sub> <b>notSet</b> , Event conditions are not met. 1 <sub>B</sub> <b>set</b> , Event conditions are met.
<b>PWM</b>	4	rh	<b>PWM Command Status</b> This bit indicates the status of the PWM command received from the primary side. 0 <sub>B</sub> <b>off</b> , PWM OFF command is detected. 1 <sub>B</sub> <b>on</b> , PWM ON command is detected.
<b>0</b>	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Second Status Register

This register contains information on the status of the device.

SSTAT2				Offset	Wakeup Value	Reset Value	
Secondary Second Status Register				12 <sub>H</sub>	n.a.	xxxx <sub>H</sub>	
15	14	13	12	11	10	9	8
DIO2L	DACLPL	GC2	GC1	OVLO3M	UVLO3M	OVLO2M	UVLO2M
rh	rh	rh	rh	rh	rh	rh	rh
7	6	5	4	3	2	1	0
OCPC2	OCPC1	OSDL	DSATC	0		LMI	P
rh	rh	rh	rh	r		rh	rh

Field	Bits	Type	Description
DIO2L	15	rh	<b>DIO2 Level</b> This bit indicates the level read at pin <b>DIO2</b> . 0 <sub>B</sub> <b>low</b> , <b>DIO2</b> level is Low. 1 <sub>B</sub> <b>high</b> , <b>DIO2</b> level is High.
DACLPL	14	rh	<b>DACLPL Level</b> This bit indicates the level read at pin <b>DACLPL</b> . 0 <sub>B</sub> <b>low</b> , <b>DACLPL</b> level is Low. 1 <sub>B</sub> <b>high</b> , <b>DACLPL</b> level is High.
GC2	13	rh	<b>Gate Second Comparator Status</b> This bit shows the output of the second comparator of the Gate Monitoring function. 0 <sub>B</sub> <b>belowVgate2</b> , <b>GATE</b> voltage is below $V_{GATE2}$ . 1 <sub>B</sub> <b>aboveVgate2</b> , <b>GATE</b> voltage is above $V_{GATE2}$ .
GC1	12	rh	<b>Gate First Comparator Status</b> This bit indicates the output of the first comparator of the Gate Monitoring function. 0 <sub>B</sub> <b>belowVgate1</b> , <b>GATE</b> voltage is below $V_{GATE1}$ . 1 <sub>B</sub> <b>aboveVgate1</b> , <b>GATE</b> voltage is above $V_{GATE1}$ .
OVLO3M	11	rh	<b>OVLO3 Comparator Status</b> This bit indicates the result of the OVLO3 monitoring function. 0 <sub>B</sub> <b>noError</b> , No failure condition is detected. 1 <sub>B</sub> <b>error</b> , One failure condition is detected.
UVLO3M	10	rh	<b>UVLO3 Monitoring Result</b> This bit indicates the result of the UVLO3 monitoring function. 0 <sub>B</sub> <b>noError</b> , No failure condition is detected. 1 <sub>B</sub> <b>error</b> , One failure condition is detected.

## Register Description

Field	Bits	Type	Description
<b>OVLO2M</b>	9	rh	<b>OVLO2 Monitoring Result</b> This bit indicates the result of the OVLO2 monitoring function. 0 <sub>B</sub> <b>noError</b> , No failure condition is detected. 1 <sub>B</sub> <b>error</b> , One failure condition is detected.
<b>UVLO2M</b>	8	rh	<b>UVLO2 Monitoring Result</b> This bit indicates the result of the UVLO2 monitoring function. 0 <sub>B</sub> <b>noError</b> , No failure condition is detected. 1 <sub>B</sub> <b>error</b> , One failure condition is detected.
<b>OCPC2</b>	7	rh	<b>OCP Second Comparator Result</b> This bit indicates the (blanked) output of the second comparator of the OCP function. 0 <sub>B</sub> <b>belowThreshold</b> , <b>OCP</b> voltage is below $V_{OCPD2}$ . 1 <sub>B</sub> <b>aboveThreshold</b> , <b>OCP</b> voltage is above $V_{OCPD2}$ .
<b>OCPC1</b>	6	rh	<b>OCP First Comparator Result</b> This bit indicates the (blanked) output of the first comparator of the OCP function. 0 <sub>B</sub> <b>belowThreshold</b> , <b>OCP</b> voltage is below $V_{OCPD1}$ . 1 <sub>B</sub> <b>aboveThreshold</b> , <b>OCP</b> voltage is above $V_{OCPD1}$ .
<b>OSDL</b>	5	rh	<b>OSD Level</b> This bit indicates the level read at pin <b>OSD</b> . 0 <sub>B</sub> <b>low</b> , <b>OSD</b> level is Low. 1 <sub>B</sub> <b>high</b> , <b>OSD</b> level is High.
<b>DSATC</b>	4	rh	<b>DESAT Comparator Result</b> This bit indicates the output of the comparator of the DESAT function. 0 <sub>B</sub> <b>belowThreshold</b> , <b>DESAT</b> voltage is below the $V_{DESAT}$ threshold. 1 <sub>B</sub> <b>aboveThreshold</b> , <b>DESAT</b> voltage is above the $V_{DESAT}$ threshold.
<b>0</b>	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.



## Register Description

### Secondary Error Register

This register provides information on the error status of the device.

SER Secondary Error Register				Offset 13 <sub>H</sub>	Wakeup Value n.a.	Reset Value 8011 <sub>H</sub>	
15	14	13	12	11	10	9	8
RST2	OCPER	DESATER	UVLO2ER	OVLO2ER	UVLO3ER	VMTO	GER
rhs	rhs	rhs	rhs	rhs	rhs	rhs	rhs
7	6	5	4	3	2	1	0
OVLO3ER	OTER	OSTER	CER2	0		LMI	P
rhs	rhs	rhs	rhs	r		rh	rh

Field	Bits	Type	Description
RST2	15	rhs	<b>Hard Reset Secondary Flag</b> This bit indicates if a hard reset event has been detected on the secondary chip (due to a $V_{CC2}$ power-up). This bit is sticky. 0 <sub>B</sub> <b>notSet</b> , No hard reset event has been detected. 1 <sub>B</sub> <b>set</b> , A hard reset event has been detected.
OCPER	14	rhs	<b>OCP Error Flag</b> This bit indicates if an OCP event has been detected. This bit is sticky.  <i>Note: This bit can not be cleared while an error condition is active (bit <a href="#">SSTAT2.OCPC1</a> set).</i>  0 <sub>B</sub> <b>notSet</b> , No event has been detected. 1 <sub>B</sub> <b>set</b> , An event has been detected.
DESATER	13	rhs	<b>DESAT Error Flag</b> This bit indicates if a DESAT event has been detected. This bit is sticky. 0 <sub>B</sub> <b>notSet</b> , No event has been detected. 1 <sub>B</sub> <b>set</b> , An event has been detected.

## Register Description

Field	Bits	Type	Description
UVLO2ER	12	rhs	<p><b>UVLO2 Error Flag</b> This bit indicates if an Undervoltage Lockout event (on <math>V_{CC2}</math>) has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared while an error condition is active (bit <b>SSTAT2.UVLO2M</b> set).</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
OVLO2ER	11	rhs	<p><b>OVLO2 Error Flag</b> This bit indicates if an Overvoltage Lockout event (on <math>V_{CC2}</math>) has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared while an error condition is active (bit <b>SSTAT2.OVLO2M</b> set).</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
UVLO3ER	10	rhs	<p><b>UVLO3 Error Flag</b> This bit indicates if an Undervoltage Lockout event (on <math>V_{EE2}</math>) has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared while an error condition is active (bit <b>SSTAT2.UVLO3M</b> set).</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
VMTO	9	rhs	<p><b>Verif. Mode Time-Out Flag</b> This bit indicates if time-out event in Verification Mode has been detected. This bit is sticky.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
GER	8	rhs	<p><b>Gate Monitoring Error Flag</b> This bit indicates in a Gate Monitoring error event has been detected. This bit is sticky.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>

## Register Description

Field	Bits	Type	Description
<b>OVLO3ER</b>	7	rhs	<p><b>OVLO3 Error Flag</b> This bit indicates if an Overvoltage Lockout event (on <math>V_{EE2}</math>) has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared while an error condition is active (bit <b>SSTAT2.OVLO3M</b> set).</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>OTER</b>	6	rhs	<p><b>Overtemperature Error Flag</b> This bit indicates if an overtemperature event has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared if bit <b>SSTAT.OT</b> is set.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>OSTER</b>	5	rhs	<p><b>Output Stage Tristate Event Flag</b> This bit indicates if an output stage tristate event has been detected. This bit is sticky.</p> <p><i>Note:</i> This bit can not be cleared if bit <b>SSTAT.HZ</b> is set.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>CER2</b>	4	rhs	<p><b>Communication Error Secondary Flag</b> This indicates if a loss of communication event with the primary chip has been detected by the secondary chip. This bit is sticky.</p> <p>0<sub>B</sub> <b>notSet</b>, No event has been detected. 1<sub>B</sub> <b>set</b>, An event has been detected.</p>
<b>0</b>	3:2	r	<p><b>Reserved</b> Read as 0<sub>B</sub>.</p>
<b>LMI</b>	1	rh	<p><b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0<sub>B</sub> , Previous Message was processed correctly. 1<sub>B</sub> , Previous Message was discarded.</p>
<b>P</b>	0	rh	<p><b>Parity Bit</b> Odd Parity Bit.</p>

## Register Description

### Secondary Configuration Register

This register is used to select the configuration of the device.

SCFG				Offset	Wakeup Value	Reset Value	
Secondary Configuration Register				14 <sub>H</sub>	n.a.	0190 <sub>H</sub>	
15				11	10	9	8
0				TOSEN		PSEN	DSTCEN
r				rw		rw	rw
7	6	5	4	3	2	1	0
OSDAD	OSMD	CFG2	VBEC	0		LMI	P
rw	rw	rwh	rw	r	rh		rh

Field	Bits	Type	Description
0	15:11	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
TOSEN	10	rw	<b>Verification Mode Time Out Duration Selection</b> This bit selects the duration of the verification mode time out. 0 <sub>B</sub> <b>regular</b> , Regular time-out value (typ. 15 ms). 1 <sub>B</sub> <b>slow</b> , Slow time-out value (typ. 60 ms).
PSEN	9	rw	<b>Pulse Suppressor Enable Bit</b> This bit enables the internal pulse suppressor. 0 <sub>B</sub> <b>disabled</b> , Pulse suppressor is disabled. 1 <sub>B</sub> <b>enabled</b> , Pulse suppressor is enabled.
DSTCEN	8	rw	<b>DESAT Clamping Enable Bit</b> This bit enables the internal clamping (to GND2) of the DESAT pin during PWM OFF commands. 0 <sub>B</sub> <b>disabled</b> , DESAT clamping is disabled. 1 <sub>B</sub> <b>enabled</b> , DESAT clamping is enabled.
OSDAD	7	rw	<b>OSD Event Class A Disable Bit</b> This bit disables the generation of an Event Class A in case of an OSD pin Tristate event. 0 <sub>B</sub> <b>enabled</b> , Event Class A is enabled. 1 <sub>B</sub> <b>disabled</b> , Event Class A is disabled.
OSMD	6	rw	<b>Output Stage Monitoring Disable Bit</b> This bit disables the internal Output Stage Monitoring mechanism. 0 <sub>B</sub> <b>enabled</b> , OSM is working normally. 1 <sub>B</sub> <b>disabled</b> , OSM is disabled.

## Register Description

Field	Bits	Type	Description
<b>CFG2</b>	5	rwh	<b>Advanced Secondary Configuration Enable Bit</b> This bit field enables write accesses to register <b>SCFG2</b> . This bit is cleared when leaving Mode OPM2. 0 <sub>B</sub> <b>disabled</b> , Write access to <b>SCFG2</b> are discarded. 1 <sub>B</sub> <b>enabled</b> , Write access to <b>SCFG2</b> are executed normally.
<b>VBEC</b>	4	rw	<b>V<sub>BE</sub> Compensation</b> This bit enables the V <sub>BE</sub> compensation of the TTOFF, TTON and WTO plateau levels. 0 <sub>B</sub> <b>disabled</b> , V <sub>BE</sub> Compensation disabled. 1 <sub>B</sub> <b>enabled</b> , V <sub>BE</sub> Compensation enabled.
<b>0</b>	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Second Configuration Register

This register is used to select the configuration of the device. It can only be written if bit **SCFG.CFG2** is set.

SCFG2				Offset	Wakeup Value	Reset Value	
Secondary Second Configuration Register				15 <sub>H</sub>	n.a.	0001 <sub>H</sub>	
15	14	13	12	11	10	9	8
CT2DIO		ISMEN	OVLO3D	ACLPM	DIO2	TTOND	
rw		rw	rw	rw	rw	rw	
7	6	5	4	3	2	1	0
TTOND		DSATL		0		LMI	P
rw		rw		r		rh	rh

Field	Bits	Type	Description
Res	15:14	rw	<b>Reserved</b> This bit field is reserved. It should be written with 0 <sub>H</sub> .
ISMEN	13	rw	<b>IGBT State Monitoring Function Enable Bit</b> This bit enables the IGBT State Monitoring Function on the secondary side. 0 <sub>B</sub> <b>disabled</b> , Functionality disabled. 1 <sub>B</sub> <b>enabled</b> , Functionality enabled.
OVLO3D	12	rw	<b>OVLO3 Mode Configuration</b> This bit configures the operation of the OVLO3 function. 0 <sub>B</sub> <b>classBEvent</b> , OVLO3 generation of class B event selected. 1 <sub>B</sub> <b>classCEvent</b> , OVLO3 generation of class C event selected.
ACLPM	11	rw	<b>Active Clamping Mode</b> This bit determines the mode of operation of pin <b>DACL</b> . 0 <sub>B</sub> <b>bothActive</b> , <b>DACL</b> is active for Regular and Safe Turn-Off sequences. 1 <sub>B</sub> <b>safeActive</b> , <b>DACL</b> is active only in case of a Safe Turn-Off sequence.
DIO2	10	rw	<b>Digital Channel Configuration</b> This bit field determines the direction of pin <b>DIO2</b> . 0 <sub>B</sub> <b>input</b> , <b>DIO2</b> is an input. 1 <sub>B</sub> <b>output</b> , <b>DIO2</b> is an output.

## Register Description

Field	Bits	Type	Description
<b>TTOND</b>	9:6	rw	<b>TTON Delay Configuration</b> This bit field defines the TTON delay (in SSOSC2 clock cycles). Writing 00 <sub>H</sub> to this field deactivates the TTON function. If used, a minimal value of at least A <sub>H</sub> has to be programmed.
<b>DSATL</b>	5:4	rw	<b>DESAT Threshold Level Selection</b> This bit field configures the threshold level of the DESAT function. 00 <sub>B</sub> <b>vdesat0</b> , Threshold $V_{DESAT0}$ selected. 01 <sub>B</sub> <b>vdesat1</b> , Threshold $V_{DESAT1}$ selected. 10 <sub>B</sub> <b>vdesat2</b> , Threshold $V_{DESAT2}$ selected. 11 <sub>B</sub> <b>vdesat3</b> , Threshold $V_{DESAT3}$ selected.
<b>0</b>	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Control Register

This register is used to control the device during run-time.

SCTRL	Offset	Wakeup Value	Reset Value			
Secondary Control Register	16 <sub>H</sub>	n.a.	00F1 <sub>H</sub>			
15	13	12	11	10	9	8
0		OSTC	CLRS	0	GPONS	
r		rhs	rh	rh	rh	
7	4	3	2	1	0	
GPOFS			0		LMI	P
rh			r	rh		rh

Field	Bits	Type	Description
0	15:13	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
OSTC	12	rhs	<b>Output Stage Tristate Control</b> This bit is used by the hardware to control the state of the output stage. This bit is set in case of an OSM event. It is cleared by either a falling edge on pin <b>OSD</b> or when bit <b>PCTRL.CLRS</b> is set.
CLRS	11	rh	<b>Clear Secondary Request Bit</b> This bit is set by writing <b>PCTRL.CLRS</b> .
0	10	rh	<b>Reserved</b> Read as 0 <sub>B</sub> .
GPONS	9:8	rh	<b>Gate Turn-On Plateau Level Configuration</b> This bit field indicates the current configuration of the plateau level for WTO and TTON. Coding is identical to <b>PCTRL.GPON</b> .  <i>Note: This bit field is a mirror of <b>PSTAT.GPONS</b>.</i>
GPOFS	7:4	rh	<b>Gate Turn-Off Plateau Level Configuration (regular turn-off)</b> This bit field indicates the current configuration of the TTOFF plateau level (for regular turn-off). Coding is identical to <b>PCTRL2.GPOF</b> .  <i>Note: This bit field is a mirror of <b>PSTAT.GPOFS</b>.</i>
0	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .



## Register Description

Field	Bits	Type	Description
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Supervision Function Control Register

This register is used to trigger the verification functions on the secondary side.

SSCR	Offset	Wakeup Value	Reset Value
Secondary Supervision Function Control Register	17 <sub>H</sub>	n.a.	0001 <sub>H</sub>

15								8
0								
r								
7			4	3	2	1	0	
VFS2				0		LMI	P	
rwh				r		rh	rh	

Field	Bits	Type	Description
0	15:8	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
VFS2	7:4	rwh	<b>Secondary Verification Function Selection</b> This bit field is used to activate the secondary verification function. All other bit combinations are reserved.  <i>Note: The selection defined by this bit field is only effective when the device enters Mode OPM5. This bit field is automatically cleared when entering OPM1.</i>  0 <sub>H</sub> <b>disabled</b> , No function activated. 1 <sub>H</sub> <b>desatLevel1</b> , DESAT Supervision Level 1 active. 2 <sub>H</sub> <b>desatLevel2</b> , DESAT Supervision Level 2 active. 3 <sub>H</sub> <b>ocpLevel1</b> , OCP Supervision Level 1 active. 4 <sub>H</sub> <b>uvlo2Enabled</b> , UVLO2 Supervision active. 5 <sub>H</sub> <b>ovlo2Enabled</b> , OVLO2 Supervision active. 6 <sub>H</sub> <b>uvlo3Enabled</b> , UVLO3 Supervision active. 7 <sub>H</sub> <b>ovlo3Enabled</b> , OVLO3 Supervision active. 8 <sub>H</sub> <b>tcf</b> , TCF function active. 9 <sub>H</sub> <b>desatLevel3</b> , DESAT Supervision Level 3 active. A <sub>H</sub> <b>ocpLevel3</b> , OCP Supervision Level 3 active.
0	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.

---

**Register Description**

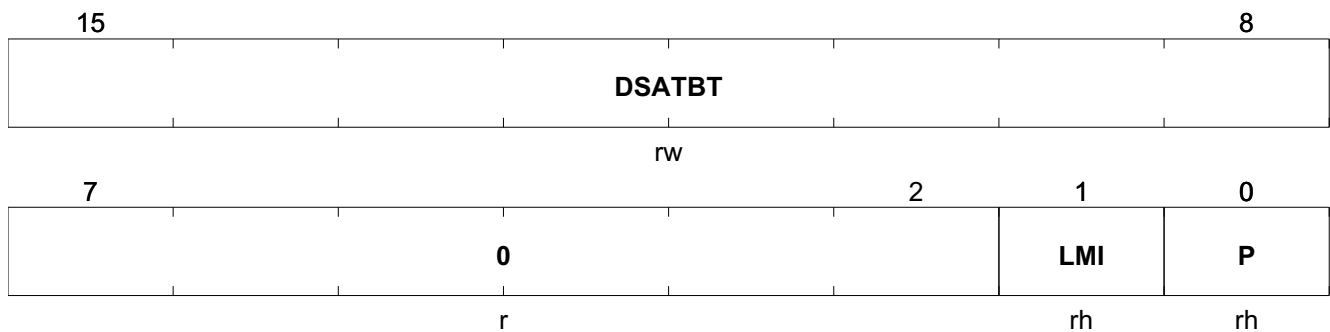
Field	Bits	Type	Description
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary DESAT Blanking Time Register

This register configures the blanking time of the DESAT function.

SDESAT	Offset	Wakeup Value	Reset Value
Secondary DESAT Blanking Time Register	18 <sub>H</sub>	n.a.	2000 <sub>H</sub>



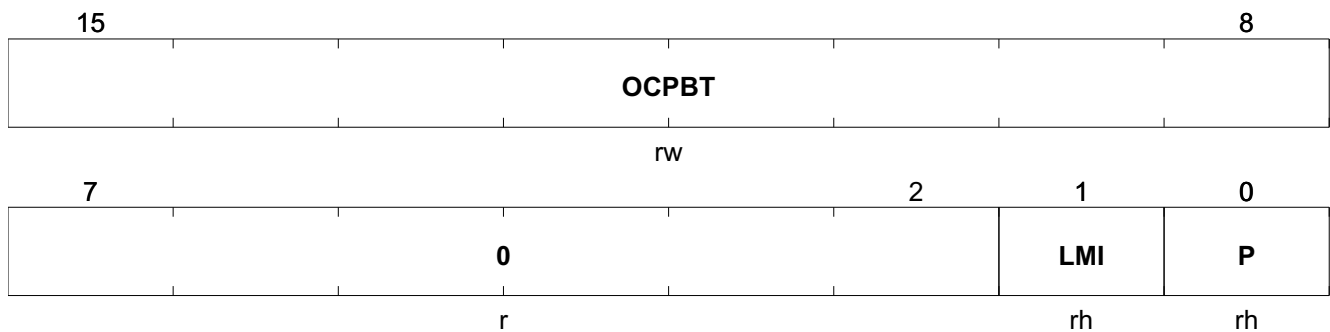
Field	Bits	Type	Description
DSATBT	15:8	rw	<b>DESAT Blanking Time Value.</b> This bit field defines the blanking time of the DESAT function (in OSC2 clock cycles). If the DESAT function is used, a value of at least A <sub>H</sub> shall be programmed.
0	7:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary OCP Blanking Time Register

This register configures the blanking time of the OCP function.

SOCP	Offset	Wakeup Value	Reset Value
Secondary OCP Blanking Time Register	19 <sub>H</sub>	n.a.	0001 <sub>H</sub>



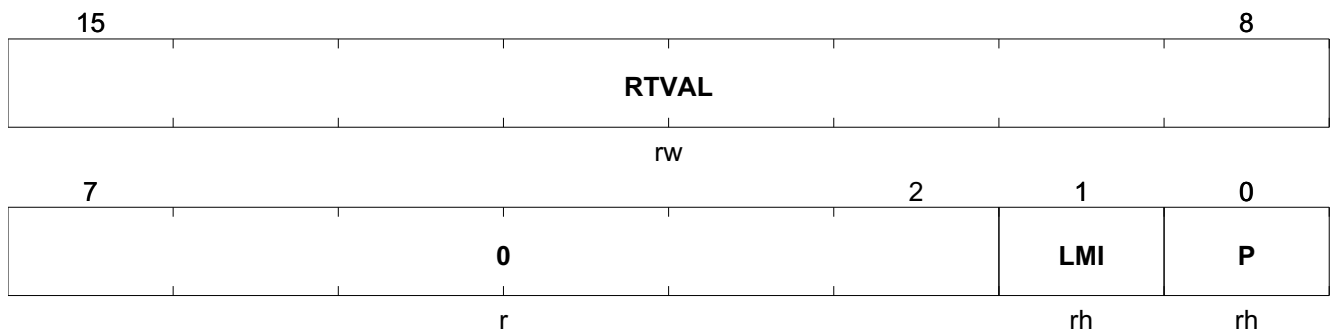
Field	Bits	Type	Description
OCPBT	15:8	rw	<b>OCP Blanking Time Value.</b> This bit field defines the blanking time of the OCP function (in OSC2 clock cycles). Writing 0 <sub>H</sub> to this field deactivates the digital blanking time generation. This field shall not be programmed with values above 2F <sub>H</sub> .
0	7:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Regular TTOFF Configuration Register

This register shows the configuration of the TTOFF function for regular turn-off.

SRTTOF	Offset	Wakeup Value	Reset Value
Secondary Regular TTOFF Configuration Register	1A <sub>H</sub>	n.a.	0001 <sub>H</sub>



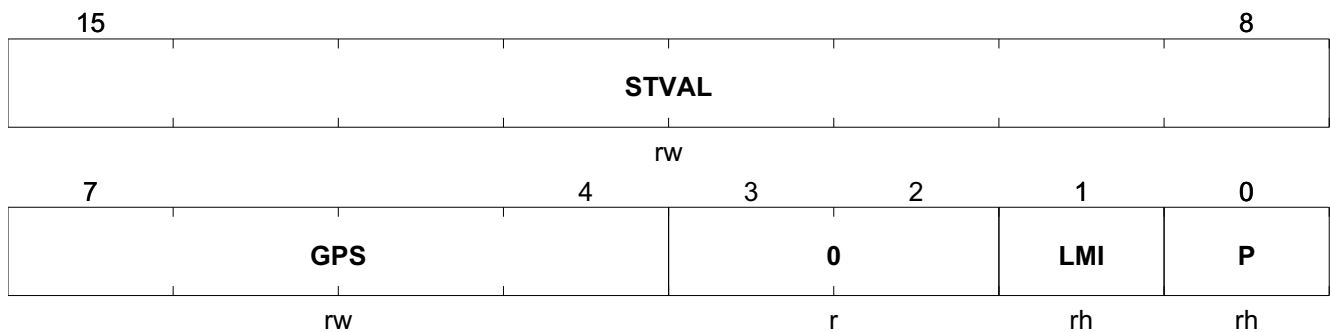
Field	Bits	Type	Description
RTVAL	15:8	rw	<b>TTOFF Delay Value (regular turn-off).</b> This bit field defines the TTOFF delay for a regular turn-off (in SSOSC2 clock cycles). Writing 00 <sub>H</sub> to this field deactivates the TTOFF function for regular turn-off. If used, a minimal value of at least 2 <sub>H</sub> has to be programmed.
0	7:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Safe TTOFF Configuration Register

This register shows the configuration of the TTOFF function for safe turn-off.

SSTOF	Offset	Wakeup Value	Reset Value
Secondary Safe TTOFF Configuration Register	1B <sub>H</sub>	n.a.	2000 <sub>H</sub>



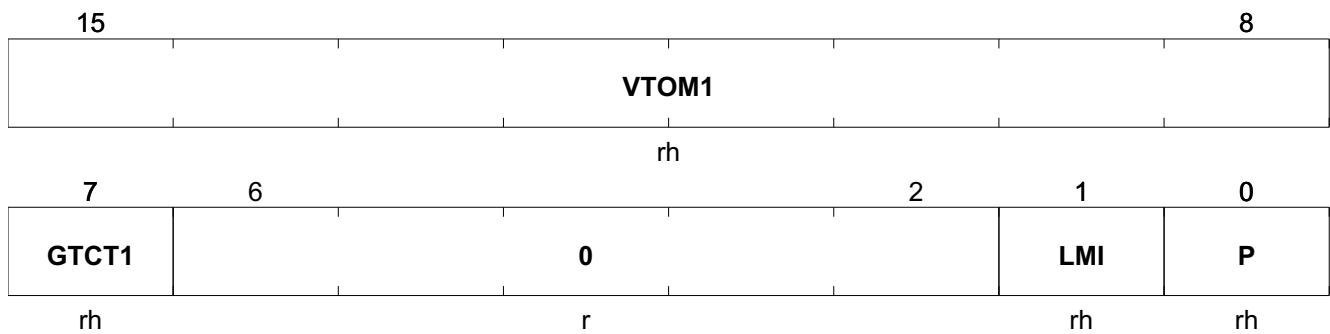
Field	Bits	Type	Description
STVAL	15:8	rw	<b>TTOFF Delay Value (safe turn-off).</b> This bit field defines the TTOFF delay for a safe turn-off (in OSC2 clock cycles). Writing 00 <sub>H</sub> to this field deactivates the TTOFF function for regular turn-off. if used, a minimal value of at least A <sub>H</sub> has to be programmed.  <i>Note:</i>  1. In OPM5 and OPM6, it is recommended to have this bit field programmed to 0 <sub>H</sub> . 2. In OPM4, when safe two level turn off is used, bit field <b>STVAL</b> shall be programmed with a higher value than field <b>SRTTOF.RTVAL</b> .
GPS	7:4	rw	<b>TTOFF Plateau voltage (safe turn-off)</b> This bit field defines the TTOFF plateau voltage for safe turn-off sequences. Coding is identical to <b>PCTRL2.GPOF</b> .
0	3:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary First Gate Monitoring Register

This register captures the value of the counter monitoring during the switching sequence.

SGM1	Offset	Wakeup Value	Reset Value
Secondary First Gate Monitoring Register	1C <sub>H</sub>	n.a.	FF01 <sub>H</sub>



Field	Bits	Type	Description
VTOM1	15:8	rh	<b>Turn-Off Counter Value</b> This bit field is used to capture the timing of signal <b>GATE</b> during turn-off sequences. It is cleared at the beginning of the timing measurement.
GTCT1	7	rh	<b>Gate Timing Capture Trigger 1</b> This bit indicates the state of the timing capture mechanism. When it is set, the mechanism is armed. This bit is cleared at the end of the timing measurement.  <i>Note: In case a new request occurs while the mechanism is already armed, then this bit is cleared and the mechanism disarmed.</i>
0	6:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

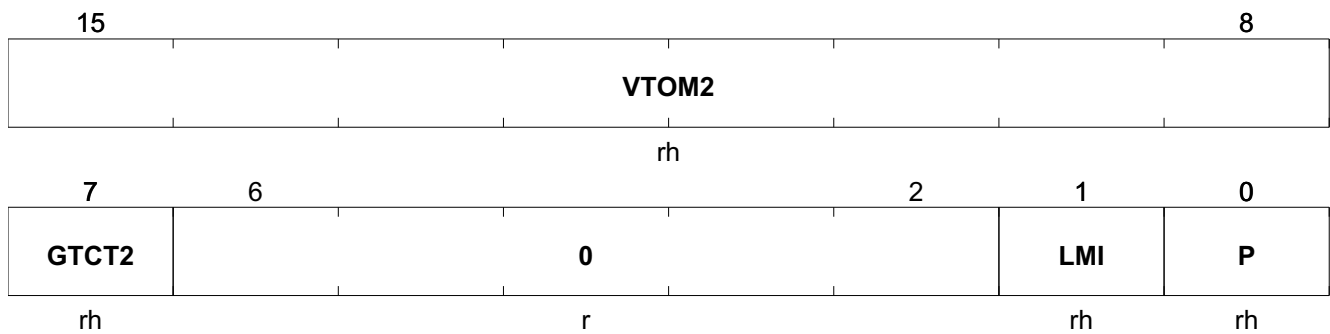


## Register Description

### Secondary Second Gate Monitoring Register

This register captures the value of the counter monitoring during the switching sequence.

SGM2	Offset	Wakeup Value	Reset Value
Secondary Second Gate Monitoring Register	1D <sub>H</sub>	n.a.	FF01 <sub>H</sub>



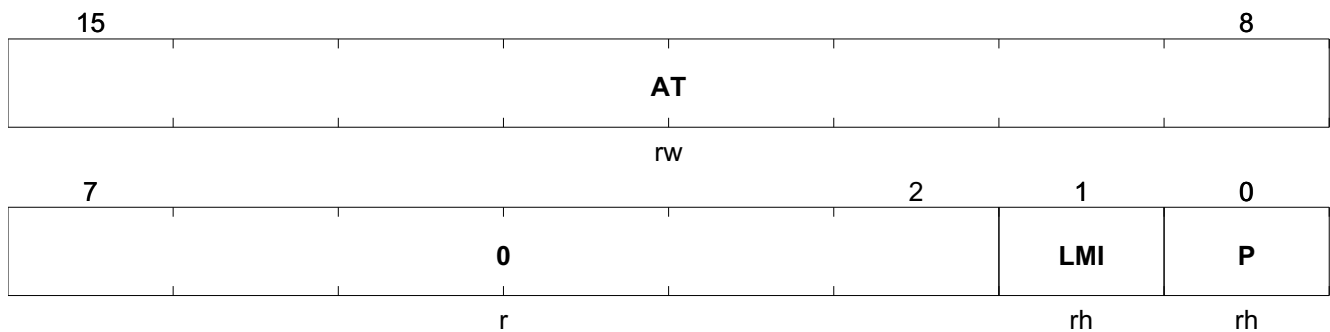
Field	Bits	Type	Description
VTOM2	15:8	rh	<b>Turn-On Counter Value</b> This bit field is used to capture the timing of signal <b>GATE</b> during turn-on sequences. It is cleared at the beginning of the timing measurement.
GTCT2	7	rh	<b>Gate Timing Capture Trigger 2</b> This bit indicates the state of the timing capture mechanism. When it is set, the mechanism is armed. This bit is cleared at the end of the timing measurement.  <i>Note: In case a new request occurs while the mechanism is already armed, then this bit is cleared and the mechanism disarmed.</i>
0	6:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary **DACLP** Activation Configuration Register

This register defines the activation time of signal **DACLP**.

SACLT	Offset	Wakeup Value	Reset Value
Secondary Active Clamping Configuration Register	1E <sub>H</sub>	n.a.	2600 <sub>H</sub>



Field	Bits	Type	Description
<b>AT</b>	15:8	rw	<b>Activation time</b> This bit field defines the activation time for signal <b>DACLP</b> (In SSOSC2 clock cycles). 01 <sub>H</sub> ...09 <sub>H</sub> : Reserved. 0A <sub>H</sub> ...FE <sub>H</sub> : <b>DACLP</b> activation time. 00 <sub>H</sub> <b>high</b> , The signal <b>DACLP</b> is constant high. FF <sub>H</sub> <b>low</b> , The signal <b>DACLP</b> is constant low.
<b>0</b>	7:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
<b>LMI</b>	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
<b>P</b>	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### Secondary Clock Supervision Register

This register is for internal purpose only.

SCS	Offset	Wakeup Value	Reset Value
Secondary Clock Supervision Register	1F <sub>H</sub>	n.a.	0001 <sub>H</sub>

15								8
CS2								
rh								

7					2	1	0
0						LMI	P
r						rh	rh

Field	Bits	Type	Description
CS2	15:8	rh	<b>Secondary Clock Supervision</b> This bit field is written by hardware by the TCF function and gives the number of measured Start Stop Oscillator clock cycles.
0	7:2	r	<b>Reserved</b> Read as 0 <sub>B</sub> .
LMI	1	rh	<b>Last Message Invalid Notification</b> This bit indicates if the last received SPI Message was correctly processed by the device. 0 <sub>B</sub> , Previous Message was processed correctly. 1 <sub>B</sub> , Previous Message was discarded.
P	0	rh	<b>Parity Bit</b> Odd Parity Bit.

## Register Description

### 4.3 Read / Write Address Ranges

**Table 39** summarizes which register is accessible with a READ command for a given operating mode.

**Table 39 Read Access Validity**

	OPM1	OPM2	OPM3	OPM4	OPM5	OPM6
<b>PID</b>	X	X	X	X	X	X
<b>PSTAT</b>	X	X	X	X	X	X
<b>PSTAT2</b>	X	X	X	X	X	X
<b>PER</b>	X	X	X	X	X	X
<b>PCFG</b>	X	X	X	X	X	X
<b>PCFG2</b>	X	X	X	X	X	X
<b>PCTRL</b>	X	X	X	X	X	X
<b>PCTRL2</b>	X	X	X	X	X	X
<b>PSCR</b>	X	X	X	X	X	X
<b>PRW</b>	X	X	X	X	X	X
<b>PPIN</b>	X	X	X	X	X	X
<b>PCS</b>	X	X	X	X	X	X
<b>SID</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SSTAT</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SSTAT2</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SER</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SCFG</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SCFG2</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SCTRL</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SSCR</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SDESAT</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SOC</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SRTTOF</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SSTTOF</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SGM1</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SGM2</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SACLT</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>
<b>SCS</b>	X	X	X	X <sup>1)</sup>	X	X <sup>1)</sup>

1) Increased latency time

## Register Description

**Table 40** summarizes which register is accessible with a WRITEL command for a given operating mode.

**Table 40 Write Access Validity**

	OPM1	OPM2	OPM3	OPM4	OPM5	OPM6
<b>PID</b>						
<b>PSTAT</b>						
<b>PSTAT2</b>						
<b>PER</b>						
<b>PCFG</b>		X				
<b>PCFG2</b> <sup>1)</sup>		X				
<b>PCTRL</b>	X	X	X	X	X	X
<b>PCTRL2</b>	X	X	X	X	X	X
<b>PSCR</b>		X				
<b>PRW</b>	X	X	X	X	X	X
<b>PPIN</b>						
<b>PCS</b>						
<b>SID</b>						
<b>SSTAT</b>						
<b>SSTAT2</b>						
<b>SER</b>						
<b>SCFG</b>		X				
<b>SCFG2</b> <sup>2)</sup>		X				
<b>SCTRL</b>						
<b>SSCR</b>		X				
<b>SDESAT</b>		X				
<b>SOCP</b>		X				
<b>SRTTOF</b>		X				
<b>SSTTOF</b>		X				
<b>SGM1</b>						
<b>SGM2</b>						
<b>SACLT</b>		X				
<b>SCS</b>						

1) Write access only allowed if **PCFG.CFG1** is set

2) Write access only allowed if **SCFG.CFG2** is set

**Specification**

## 5 Specification

### 5.1 Typical Application Circuit

**Table 41 Component Values**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Decoupling Capacitance (Between VEE2 and GND2)	$C_d$	2 x 0.5	11	-	$\mu\text{F}$	10 $\mu\text{F}$ capacitance next to the power supply source (e.g. flyback converter). 1 $\mu\text{F}$ close to the device. It is strongly recommended to have at least two capacitances close to the device (e.g. 2 x 500 nF).
Decoupling Capacitance (Between VCC2 and GND2)	$C_d$	-	11	-	$\mu\text{F}$	10 $\mu\text{F}$ capacitance next to the power supply source (e.g. flyback converter). 1 $\mu\text{F}$ close to the device.
Decoupling Capacitance (Between VCC1 and GND1)	$C_d$	-	11	-	$\mu\text{F}$	10 $\mu\text{F}$ capacitance next to the power supply source (e.g. flyback converter). 1 $\mu\text{F}$ close to the device.
Series Resistance	$R_{s1}$	0	1	-	$\text{k}\Omega$	
Pull-up Resistance	$R_{pu1}$	-	10	-	$\text{k}\Omega$	
Filter Resistance	$R_1$	-	1	-	$\text{k}\Omega$	
Filter Capacitance	$C_1$	-	47	-	$\text{pF}$	
Reference Resistance	$R_{ref1}$	-	26.7 <sup>1)</sup>	-	$\text{k}\Omega$	high accuracy, as close as possible to the device
Reference Capacitance	$C_{ref1}$	-	100	-	$\text{pF}$	As close as possible to the device.
Pull-up Resistance	$R_{pu2}$	-	10	-	$\text{k}\Omega$	
Reference Resistance	$R_{ref2}$	-	23.7	-	$\text{k}\Omega$	high accuracy, as close as possible to the device
Reference Capacitance	$C_{ref2}$	-	100	-	$\text{pF}$	As close as possible to the device.
<b>DESAT</b> filter Resistance	$R_{desat}$	1	3	-	$\text{k}\Omega$	Depends on required response time.
<b>DESAT</b> filter Capacitance	$C_{desat}$	-	n/a	-	$\text{nF}$	Depends on required response time.
<b>DESAT</b> Diode	$D_{desat}$	-	n/a	-	-	HV diode.
<b>OSD</b> Filter Resistance	$R_{osd}$	-	1	-	$\text{k}\Omega$	
<b>OSD</b> Filter Capacitance	$C_{osd}$	-	47	-	$\text{pF}$	

**Specification**

**Table 41 Component Values** (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Sense Resistance	$R_{\text{sense}}$	-	n/a	-	$\Omega$	Depends on IGBT specification.
<b>OCF</b> filter Resistance	$R_{\text{ocp}}$	-	n/a	-	$\Omega$	Depends on required response time.
<b>OCF</b> filter Capacitance	$C_{\text{ocp}}$	-	n/a	-	nF	Depends on required response time.
<b>OCPG</b> resistance	$R_{\text{ocpg}}$	0	-	100	$\Omega$	
<b>DACL</b> filter Resistance	$R_{\text{dclp}}$	-	1	-	k $\Omega$	
<b>DACL</b> filter Capacitance	$C_{\text{dclp}}$	-	470	-	pF	
<b>NUV2</b> Filter Resistance	$R_2$	-	n/a	-	$\Omega$	Depends on required response time.
<b>NUV2</b> Filter Capacitance	$C_2$	-	-	100	pF	
Active Clamping Resistance	$R_{\text{acl1}}$	-	n/a	-	$\Omega$	Depends on application requirements
Active Clamping Resistance	$R_{\text{acl2}}$	-	n/a	-	k $\Omega$	Depends on application requirements
Active Clamping Capacitance	$C_{\text{ac1i}}$	-	n/a	-	nF	Depends on application requirements
TVS Diode	$D_{\text{tvsac1}}, D_{\text{tvsac2}}$	-	n/a	-	-	Depends on application requirements
Active Clamping Diode	$D_{\text{acl}}$	-	n/a	-	-	Depends on application requirements
ACLI Clamping Diode	$D_{\text{acl2}}$	-	n/a	-	-	Depends on application requirements
<b>VREG</b> Capacitance	$C_{\text{vreg}}$		1		$\mu\text{F}$	As close as possible to the device.
<b>GATE</b> Resistance	$R_{\text{gon}}$	0.5	-	-	$\Omega$	
<b>GATE</b> Resistance	$R_{\text{goff}}$	0.5	-	-	$\Omega$	
<b>GATE</b> Clamping Diode	$D_{\text{gcl1}}$	-	n/a	-	-	<sup>2)</sup>
<b>GATE</b> Clamping Diode	$D_{\text{gcl2}}$	-	n/a	-	-	E.g. Schottky Diode. <sup>2)</sup>
<b>GATE</b> Series Resistance	$R_{\text{gate}}$	0	10	-	$\Omega$	Optional component.
VEE2 Clamping Diode	$D_{\text{gcl3}}$	-	n/a	-	-	E.g. Schottky Diode. <sup>2)</sup>

1) 26.1 k $\Omega$ m can also be used

2) Characteristics of this components are application specific.

Specification

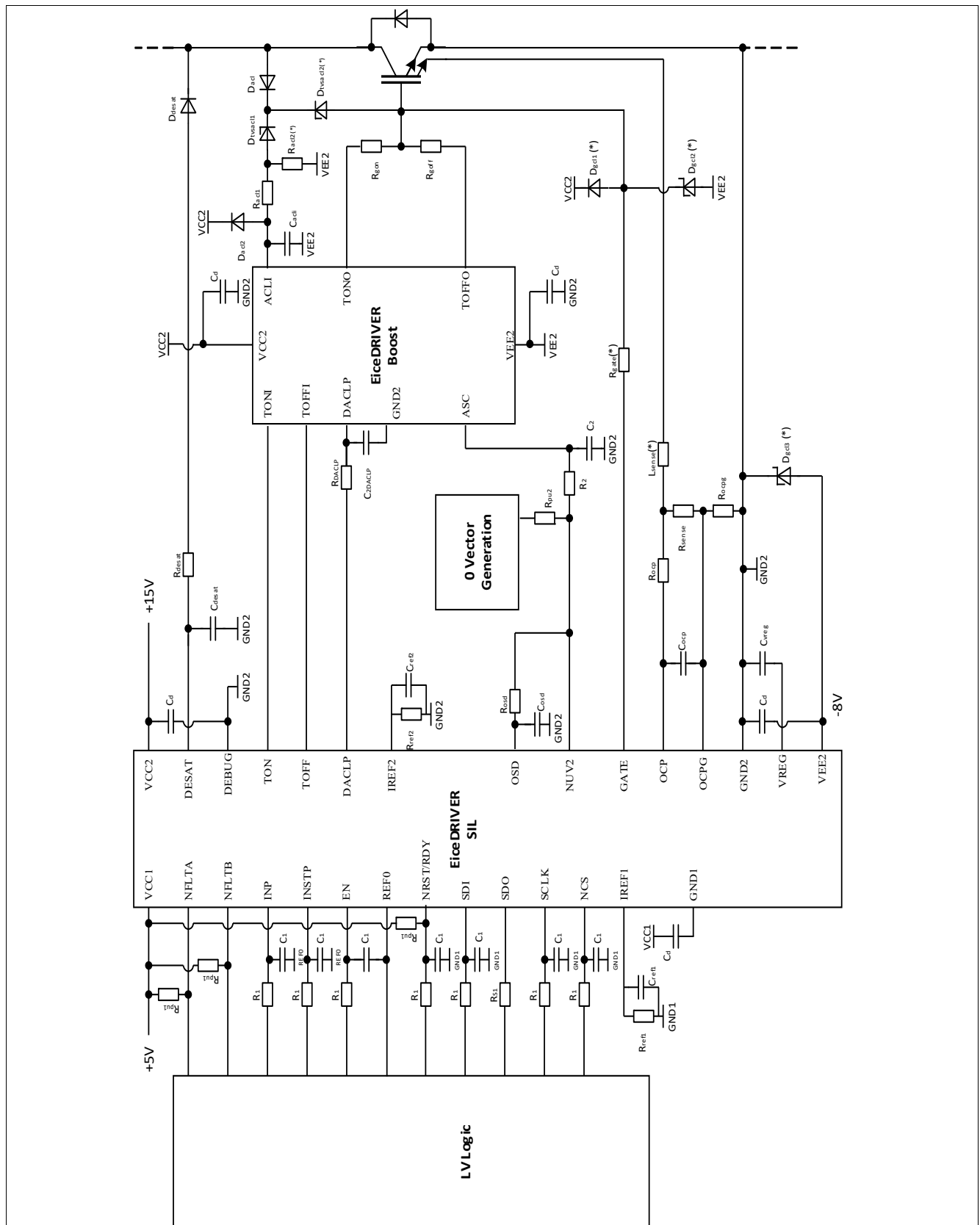


Figure 28 Typical Application Example

Note: Components marked with (\*) are optional.



## Specification

### 5.2 Absolute Maximum Ratings

Stress above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 42 Absolute Maximum Ratings<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Junction temperature	$T_{JUNC}$	-40	-	150	°C	
Storage temperature	$T_{STO}$	-55	-	150	°C	
Positive power supply (primary)	$V_{CC1}$	-0.3	-	6.0	V	Referenced to <b>GND1</b>
Positive power supply (secondary)	$V_{CC2}$	-0.3	-	28	V	Referenced to <b>GND2</b>
Negative power supply	$V_{EE2}$	-13	-	0.3	V	Referenced to <b>GND2</b>
Power supply voltage difference (secondary) $V_{CC2}-V_{EE2}$	$V_{DS2}$	-	-	40	V	
Voltage on any I/O pin on primary side except <b>INP</b> , <b>INSTP</b> , <b>EN/FEN</b>	$V_{IN1}$	-0.3	-	6.0	V	Referenced to <b>GND1</b>
Voltage on <b>INP</b> , <b>INSTP</b> , <b>EN/FEN</b> pins	$V_{INR1}$	-0.3	-	6.0	V	Referenced to <b>REF0</b>
Voltage difference between <b>REF0</b> and <b>GND1</b>	$V_{DG1}$	-5	-	5	V	
Voltage difference between <b>OC PG</b> and <b>GND2</b>	$V_{OCPG2}$	-0.3	-	0.3	V	
Output current on push-pull I/O on primary side	$I_{OUTPP1}$	-	-	20	mA	
Output current on push-pull I/O on secondary side	$I_{OUTPP2}$	-	-	5	mA	
Output current on open drain I/O on primary side	$I_{OUTOD1}$	-	-	20	mA	
Output current on pin <b>OSD</b> , <b>NUV2</b>	$I_{OUTOD2}$	-	-	5	mA	
Voltage on 5 V pin on secondary side.	$V_{IN52}$	-0.3	-	6.5	V	Referenced to <b>GND2</b>
Voltage on 15 V pin on secondary side.	$V_{IN152}$	$V_{EE2}-0.3$	-	$V_{CC2}+0.3$	V	Referenced to <b>GND2</b> , except <b>DESAT</b>
Voltage on <b>DESAT</b> pin.	$V_{INDESAT}$	-0.3	-	20	V	Referenced to <b>GND2</b>
ESD Immunity	$V_{ESD}$	-	-	2	kV	HBM <sup>2)</sup>
		-	-	750	V	CDM <sup>3)</sup> , pins 1, 18, 19, 36
		-	-	500	V	CDM <sup>3)</sup> , all other pins
MSL Level	MSL	n.a.	3	n.a.		

1) Not subject to production test. Absolute maximum Ratings are verified by design / characterization.

2) According to EIA/JESD22-A114-B.

## Specification

3) According to JESD22-C101-C.

### 5.3 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the 1EDI2002AS. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

**Table 43 Operating Conditions**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Ambient temperature	$T_{amb}$	-40	-	125	°C	
Positive power supply (primary)	$V_{CC1}$	4.65	5.0	5.5	V	Referenced to <b>GND1</b> <sup>1)</sup>
Positive power supply (secondary)	$V_{CC2}$	13.0	15.0	18.0	V	Referenced to <b>GND2</b> <sup>2)</sup>
Negative power supply	$V_{EE2}$	-10.0	-8.0	-5.0	V	Referenced to <b>GND2</b> <sup>3)</sup>
PWM switching frequency	$f_{sw}$	-	-	30	kHz	<sup>4)</sup>
Common Mode Transient Immunity	$dV_{ISO}/dt$	-50	-	50	kV/μs	At 500 V <sup>5)</sup>

1) Deterministic and correct operation of the device is ensured down to  $V_{UVLO1L}$ .

2) Deterministic and correct operation of the device is ensured down to  $V_{UVLO2L}$  and up to 28 V.

3) Deterministic and correct operation of the device is ensured up to 0.3 V.

4) Maximum junction temperature of the device must not be exceeded.

5) Not subject to production test. This parameter is verified by design / characterization.

### 5.4 Thermal Characteristics

The indicated thermal parameters apply to the full operating range, unless otherwise specified.

**Table 44 Thermal Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal Resistance Junction to Ambient	$R_{THJA}$	-	60	-	K/W	$T_{amb}=25^{\circ}\text{C}$ <sup>1)</sup>
Thermal Resistance Junction to Case (bottom)	$R_{THJCB}$	-	-	41	K/W	$T_{amb}=25^{\circ}\text{C}$ <sup>1)</sup> ,

1) Not subject to production test. This parameter is verified by design / characterization.

## Specification

### 5.5 Electrical Characteristics

The indicated electrical parameters apply to the full operating range, unless otherwise specified.

#### 5.5.1 Power Supply

**Table 45 Power Supplies Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UVLO1 Threshold High	$V_{UVLO1H}$	4.20	4.45	4.65	V	Referenced to <b>GND1</b>
UVLO1 Threshold Low	$V_{UVLO1L}$	4.15	4.40	4.60	V	Referenced to <b>GND1</b>
UVLO1 Hysteresis	$V_{UVLO1HYS}$	40	70	100	mV	
UVLO2 Threshold High	$V_{UVLO2H}$	11.5	12.5	13.0	V	Referenced to <b>GND2</b>
UVLO2 Threshold Low	$V_{UVLO2L}$	11.0	11.7	12.5	V	Referenced to <b>GND2</b>
UVLO2 Hysteresis	$V_{UVLO2H}$	500	850	-	mV	
OVLO2 Threshold High	$V_{OVLO2H}$	18.5	19.14	20	V	Referenced to <b>GND2</b>
OVLO2 Threshold Low	$V_{OVLO2L}$	18.5	19.10	20	V	Referenced to <b>GND2</b>
UVLO3 Threshold High	$V_{UVLO3H}$	-12.0	-10.99	-10.0	V	Referenced to <b>GND2</b>
UVLO3 Threshold Low	$V_{UVLO3L}$	-12.0	-11.02	-10.0	V	Referenced to <b>GND2</b>
OVLO3 Threshold High	$V_{OVLO3H}$	-5.0	-3.99	-3.0	V	Referenced to <b>GND2</b>
OVLO3 Threshold Low	$V_{OVLO3L}$	-5.0	-4.02	-3.0	V	Referenced to <b>GND2</b>
$V_{CC2}$ Reset Level	$V_{RST2}$	7.9	8.3	8.8	V	Referenced to <b>GND2</b>
Quiescent Current Input Chip	$I_{Q1}$	-	8.0	10.0	mA	$V_{CC1}=5.5V$ , all I/Os inactive, OPM0
Quiescent Current Output Chip (VCC2)	$I_{QVCC2}$	-	11.4	14.0	mA	$V_{CC2}=18V$ , $V_{EE2}=-10V$ , all I/Os inactive, OPM0
Quiescent Current Output Chip (VEE2)	$I_{QVEE2}$	-4.6	-1.1	-	mA	$V_{CC2}=18V$ , $V_{EE2}=-10V$ , all I/Os inactive, OPM0
VCC1 ramp-up / down slew rate	$ t_{RP1} $	-	-	0.5	V/ms	Absolute value
VCC2 ramp-up / down slew rate	$ t_{RP2} $	-	-	1.5	V/ms	Absolute value
VEE2 ramp-up / down slew rate	$ t_{RP3} $	-	-	0.8	V/ms	Absolute value
Power Dissipation - Primary Chip	$P_{DIS1}$	-	37	-	mW	$T_{AMB}=25^{\circ}C$ , $V_{CC1}=5V$ , all I/Os inactive, OPM0
Power Dissipation - Secondary Chip	$P_{DIS2}$	-	170	-	mW	$T_{AMB}=25^{\circ}C$ , $V_{CC2}=15V$ , $V_{EE21}=-8V$ , all I/Os inactive, OPM0

**Specification**

**5.5.2 Internal Oscillators**

**Table 46 Internal Oscillators**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Primary main oscillator frequency	$f_{clk1}$	14.0	16.6	19.1	MHz	Resistances on pin <b>IREF1</b> nominal
Secondary main oscillator / Start-Stop Oscillator Frequency	$f_{clk2}, f_{clkst2}$	15.0	17.1	19.0	MHz	Resistances on pin <b>IREF2</b> nominal

**Specification**

**5.5.3 Primary I/O Electrical Characteristics**

**Table 47 Electrical Characteristics for Pins: INP, INSTP, EN/FEN**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low Input Voltage	$V_{INPRL1}$	0	-	$0.3 \times V_{CC1}$	V	Referenced to <b>REF0</b>
High Input Voltage	$V_{INPRH1}$	$0.7 \times V_{CC1}$	-	$V_{CC1}$	V	Referenced to <b>REF0</b>
Weak pull down resistance <b>INP</b> , <b>INSTP</b> , <b>EN/FEN</b>	$R_{PDIN1}$	20	-	100	kΩ	To <b>REF0</b>
Input Current	$ I_{INPR1} $	-	-	300	μA	
Input Pulse Suppression	$t_{INPS1}$	-	20	-	ns	<sup>1)</sup>
Time between <b>EN/FEN</b> valid and <b>INP</b> High Level	$t_{INPEN}$	8	-	-	μs	See <b>Chapter 2.4.3</b>
<b>INP</b> High / Low Duration	$t_{INPPD}$	250	-	-	ns	<sup>1)</sup>
<b>INSTP</b> High / Low Duration	$t_{INSTPP}$	250	-	-	ns	<sup>1)</sup>
Duration between <b>EN/FEN</b> valid-to-invalid transition and the next invalid-to-valid transition	$t_{ENINV}$	8	-	-	μs	<sup>1)</sup>

1) Not subject to production test. This parameter is verified by design / characterization.

**Table 48 Electrical Characteristics for Pins: NRST/RDY, SCLK, SDI, NCS, DIO1 (input)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low Input Voltage	$V_{INPH1}$	0	-	$0.3 \times V_{CC1}$	V	Referenced to <b>GND1</b>
High Input Voltage	$V_{INPH1}$	$0.7 \times V_{CC1}$	-	$V_{CC1}$	V	Referenced to <b>GND1</b>
Weak pull up resistance to <b>SCLK</b> , <b>SDI</b> , <b>NCS</b>	$R_{PUSPI1}$	26.5	-	100	kΩ	To <b>VCC1</b> .
Weak pull down resistance on <b>DIO1</b>	$R_{PDDIO1}$	26.5	-	100	kΩ	To <b>GND1</b> ,
Input Current	$ I_{INP1} $	-	-	400	μA	
<b>NRST/RDY</b> Output Voltage in Non-Ready conditions.	$V_{OUTNR}$	-	-	1	V	$V_{CC1}=5\text{ V}, I_{load}=2\text{ mA}$
		-	0.7	1	V	$V_{CC1}=0\text{ V}, I_{load}=500\text{ μA}$
<b>NRST/RDY</b> driven-active time after power supplies are within operating range.	$t_{RST}$	-	15.4	-	μs	<sup>1)</sup>
<b>NRST/RDY</b> minimum activation time.	$t_{RSTAT}$	10	-	-	μs	

1) Not subject to production test. This parameter is verified by design / characterization.

**Specification**

**Table 49 Electrical Characteristics for Pins: SDO, DOUT, DIO1 (output)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low Output Voltage	$V_{OUTPL1}$	-	-	0.5	V	$I_{load} = 5mA$
High Output Voltage	$V_{OUTPH1}$	3.85	-	-	V	$I_{load} = 5mA$

**Table 50 Electrical Characteristics for Pins: NFLTA, NFLTB**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low Output Voltage	$V_{OUTDL1}$	-	-	0.5	V	$I_{SINK} = 5mA$

**Specification**

**5.5.4 Secondary I/O Electrical Characteristics**

**Table 51 Electrical Characteristics for Pins: **TON**, **TOFF** & **GATE****

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>TON</b> & <b>TOFF</b> Output Voltage High	$V_{15OH2}$	$V_{CC2}-1$	-	$V_{CC2}+0.3$	V	Referenced to <b>GND2</b>
<b>TON</b> & <b>TOFF</b> Output Voltage Low	$V_{15OL2}$	$V_{EE2}-0.3$	-	$V_{EE2}+1$	V	Referenced to <b>GND2</b>
<b>TON</b> & <b>TOFF</b> Source / Sink Current	$I_{15O2}$	1	-	-	A	<sup>1)</sup>
<b>GATE</b> Input voltage range	$V_{15GATE}$	$V_{EE2}$	-	$V_{CC2}$	V	Referenced to <b>GND2</b> <sup>1)2)</sup>
<b>GATE</b> Passive Clamping Voltage	$V_{PCLPG}$	-	-	$V_{EE2}+1$	V	Secondary chip not supplied; $I_{CLAMP}=10$ mA.
<b>TON</b> & <b>TOFF</b> Passive Clamping Voltage	$V_{PCLP}$	-	-	$V_{EE2}+2$	V	Secondary chip not supplied; $I_{CLAMP}=10$ mA.
<b>GATE</b> Passive Clamp Current	$I_{PCLPG}$	5	-	-	mA	Secondary chip not supplied; $V_{GATE}=V_{EE2}+2$ V

1) Not subject to production test. This parameter is verified by design / characterization.

2) Pin is robust against negative transient

**Table 52 Electrical Characteristics for Pins: **OSD**, **DEBUG**, **DIO2** (input)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low Input Voltage	$V_{SINL2}$	0	-	1.5	V	Referenced to <b>GND2</b>
High Input Voltage	$V_{SINH2}$	3.5	-	5.5	V	Referenced to <b>GND2</b>
Weak pull down on <b>DIO2</b>	$R_{PDDIO2}$	40	100	175	kΩ	To <b>GND2</b> .
Weak pull down on <b>DEBUG</b>	$R_{PDIN2}$	40	100	175	kΩ	To <b>GND2</b> .
Weak pull down on <b>OSD</b>	$R_{PDOSD2}$	60	100	175	kΩ	To <b>GND2</b>

**Table 53 Electrical Characteristics for Pin: **NUV2****

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Low Output Voltage	$V_{OUTDL2}$	0	-	0.5	V	$I_{SINK}=5$ mA, Referenced to <b>GND2</b>

**Specification**

**Table 54 Electrical Characteristics for Pins: DACLP, DIO2 (output)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output Voltage High	$V_{50H2}$	4.0	-	5.25	V	Referenced to <b>GND2</b> , $I_{LOAD} = 2 \text{ mA}$
Output Voltage Low	$V_{50L2}$	0	-	0.5	V	Referenced to <b>GND2</b> , $I_{LOAD} = 2 \text{ mA}$

**Table 55 Electrical Characteristics for Pin: VREG**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>VREG</b> output voltage range	$V_{REG2}$	4.75	5	5.30	V	Referenced to <b>GND2</b> , $C_{LOAD} = 1 \mu\text{F}$
<b>VREG</b> output DC current	$I_{REG2}$	-	-	525	$\mu\text{A}$	<sup>1)</sup>

1) Not subject to production test. This parameter is verified by design / characterization.



**Specification**

**5.5.5 Switching Characteristics**

**Table 56 Switching Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input to Output Propagation Delay ON	$t_{PDON}$	175	215	255	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$
Input to Output Propagation Delay OFF	$t_{PDOFF}$	175	215	255	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$
Input to Output Propagation Delay Distortion ( $t_{PDOFF}-t_{PDON}$ )	$t_{PDISTO}$	-20	0	40	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$
Input to Output Propagation Delay Distortion Variation for two consecutive pulses	$t_{PDISTOV}$	-	25	-	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$ , $T_{JUNC}=25^{\circ}\text{C}$ <sup>1)</sup>
Rise Time	$t_{RISE}$	-	120	205	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$ , $C_{LOAD} = 10\text{ nF}$ , 10%-90%
		-	30	50	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$ , no Load, 90%-10%
Fall Time	$t_{FALL}$	-	150	235	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$ , $C_{LOAD} = 10\text{ nF}$ , 90%-10%
		-	60	100	ns	$V_{CC1}=5\text{ V}$ , $V_{CC2}=15\text{ V}$ , $V_{EE2}=-8\text{ V}$ , no Load, 90%-10%
TTOFF Plateau level	$V_{GPOF0}$	9.250	9.740	10.250	V	Referenced to <b>GND2</b> , measured at pin <b>TON</b> (shorted with <b>TOFF</b> ) $V_{CC2}=15\text{ V}$ , $T_{JUNC}=25^{\circ}\text{C}$ , no VBE Compensation.
	$V_{GPOF1}$	9.335	9.820	10.335	V	
	...	...	...	...	...	
	$V_{GPOF14}$	10.440	10.95	11.440	V	
	$V_{GPOF15}$	11.1	11.7	12.3	V	
TTOFF Plateau level	$V_{GPOF0}$	8.600	9.08	9.600	V	Referenced to <b>GND2</b> , measured at pin <b>TON</b> (shorted with <b>TOFF</b> ) $V_{CC2}=15\text{ V}$ , $T_{JUNC}=25^{\circ}\text{C}$ , with VBE Compensation.
	$V_{GPOF1}$	8.685	9.16	9.685	V	
	...	...	...	...	...	
	$V_{GPOF14}$	9.790	10.28	10.790	V	
	$V_{GPOF15}$	10.4	11.0	11.6	V	
Variation from configured $V_{TTOFF}$ @ $T_J = -40^{\circ}\text{C}$	$d_{VTm40}$	-	40	-	mV	<sup>1)</sup>
Variation from configured $V_{TTOFF}$ @ $T_J = 150^{\circ}\text{C}$	$d_{VT150}$	-	-80	-	mV	<sup>1)</sup>
TTOFF decrease rate	$t_{SLEW}$	-	9	-	V/ $\mu\text{s}$	

**Specification**

**Table 56 Switching Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
TTOFF delay deviation from nominal value	$t_{DEVTTTOFF}$	-100	0	100	ns	For a target time of 2 $\mu$ s, using the TCF. <sup>1)</sup>
TTOFF (Regular) Plateau Time	$t_{TTOFF}$	2.00	2.22	2.54	$\mu$ s	<b>SRTTOF.RTVAL</b> =26 <sub>H</sub> , assuming no TCF.
Gate Voltage Reference 1	$V_{GATE1}$	-	$V_{EE2}+2$	-	V	Measured at pin <b>GATE</b>
Gate Voltage Reference 2	$V_{GATE2}$	-	$V_{CC2}-3$	-	V	Measured at pin <b>GATE</b>
Output Stage Monitoring ( <b>TON</b> )	$V_{OSMON}$	-	$V_{CC2}-3$	-	V	
Output Stage Monitoring ( <b>TOFF</b> )	$V_{OSMOF}$	-	$V_{EE2}+2$	-	V	
Active Clamping Activation Time	$t_{ACL}$	2.00	2.22	2.54	$\mu$ s	Default value of bit field <b>SACLT.AT</b> .
WTO & TTON Plateau Level	$V_{GPON0}$	8.65	9.25	9.95	V	Referenced to <b>GND2</b> , measured at pin <b>TON</b> (shorted with <b>TOFF</b> ) $V_{CC2}=15$ V, $T_{JUNC}=25^{\circ}$ C, no VBE Compensation.
	$V_{GPON1}$	9.85	10.5	11.25	V	
	$V_{GPON2}$	10.75	11.4	12.1	V	
WTO & TTON Plateau Level	$V_{GPON0}$	9.15	9.9	10.75	V	Referenced to <b>GND2</b> , measured at pin <b>TON</b> (shorted with <b>TOFF</b> ) $V_{CC2}=15$ V, $T_{JUNC}=25^{\circ}$ C, with VBE Compensation.
	$V_{GPON1}$	10.4	11.0	11.6	V	
	$V_{GPON2}$	11.1	11.6	12.2	V	
TTON Delay	$t_{TTON}$	0.78	0.88	1.00	$\mu$ s	<b>SCFG2.TTOND</b> =F <sub>H</sub> , assuming no TCF.

1) Not subject to production test. Parameters are verified by design / characterization.

Specification

## 5.5.6 Desaturation Protection

Table 57 **DESAT** characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>DESAT</b> Input voltage range	$V_{15DESAT}$	0	-	$V_{CC2}$	V	Referenced to <b>GND2</b> <sup>1) 2)</sup>
<b>DESAT</b> Reference Level	$V_{DESAT0}$	8.4	9	9.4	V	$V_{CC2} = 15\text{ V}$ , $V_{EE2} = -8\text{ V}$
	$V_{DESAT1}$	9.25	10	10.45	V	
	$V_{DESAT2}$	7.4	8	8.4	V	
	$V_{DESAT3}$	6.5	7	7.5	V	
<b>DESAT</b> Pull-up Resistance	$R_{PUDSAT2}$	19.5	30	50	k $\Omega$	to <b>VCC2</b>
<b>DESAT</b> Low Voltage	$V_{DESATL}$	-	200	-	mV	Referenced to <b>GND2</b> , Desat clamping enabled, $I_{sink} = 5\text{ mA}$ .
<b>DESAT</b> blanking time deviation from programmed value	$d_{tDESATBL}$	-20	-	+20	%	After transition of the PWM command, assuming a 1 $\mu\text{s}$ programmed blanking time

1) Pin is robust against negative transient

2) Not subject to production test. This parameter is verified by design / characterization.

## 5.5.7 Overcurrent Protection

Table 58 **OCP** characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OC error detection threshold	$V_{OCPD1}$	270	300	330	mV	Referenced to <b>OCPG</b>
OC current warning detection threshold	$V_{OCPD2}$	35	50	70	mV	Referenced to <b>OCPG</b>
<b>OCP</b> blanking time deviation from programmed value	$d_{tOCPBL}$	-20	-	+20	%	After transition of the PWM command, assuming a 1 $\mu\text{s}$ programmed blanking time <sup>1)</sup>
<b>OCP</b> Pull-up Resistance	$R_{PUOCP2}$	40	100	175	k $\Omega$	to internal 5 V reference.

1) Not subject to production test. Parameters are verified by design / characterization.

## Specification

### 5.5.8 Low Latency Digital Channel

**Table 59 Digital channel characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input to output propagation time ON (secondary to primary)	$t_{DSPON}$	-	2.0	4.5	μs	PCFG2.DIO1=1 <sub>B</sub> , SCFG2.DIO2=0 <sub>B</sub>
Input to output Propagation time OFF (secondary to primary)	$t_{DSPOFF}$	-	2.0	4.5	μs	
Input to output propagation time ON (primary to secondary)	$t_{DPSON}$	-	2.0	4.5	μs	PCFG2.DIO1=0 <sub>B</sub> , SCFG2.DIO2=1 <sub>B</sub>
Input to output Propagation time OFF (primary to secondary)	$t_{DPSOFF}$	-	2.0	4.5	μs	

### 5.5.9 DOUT

**Table 60 Data Out characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
DESAT comparator output transition to DOUT transition.	$t_{SPDOUT}$	-	2.0	4.5	μs	

### 5.5.10 Over temperature Warning

**Table 61 Over temperature Warning Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Threshold Junction Temperature	$T_{j\_ovt}$	140	-	-	°C	1)

1) Not subject to back-end test

**Specification**

**5.5.11 Error Detection Timing**

**Table 62 Error Detection Timing**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Dead Time for Shoot Through Protection	$t_{\text{DEAD}}$	840	-	1200	ns	Default value of bit field <b>PCFG2.STPDEL</b>
Class A event detection to <b>NFLTA</b> activation	$t_{\text{AFLTA}}$	-	2	4.5	μs	
Class A event detection to turn off sequence activation	$t_{\text{OFFCLA}}$	-	-	400	ns	$V_{\text{TOFF}} = V_{\text{CC2}} - 1 \text{ V}$
DESAT event detection to turn off sequence activation	$t_{\text{OFFDESAT2}}$	-	-	430	ns	$V_{\text{TOFF}} = V_{\text{CC2}} - 1 \text{ V}$ , after blanking time elapsed
OCP event occurrence to turn off sequence activation	$t_{\text{OFFOCP2}}$	-	110	130	ns	$V_{\text{TOFF}} = V_{\text{CC2}} - 1 \text{ V}$ , after blanking time elapsed
Class B event detection to <b>NFLTB</b> activation	$t_{\text{BFLTB}}$	-	2	4.5	μs	
Class B event detection to turn off sequence activation	$t_{\text{OFFCLB2}}$	-	-	400	ns	$V_{\text{TOFF}} = V_{\text{CC2}} - 1 \text{ V}^{1)}$
Verification Mode time out	$t_{\text{VMTO}}$	-	15	-	ms	After a transition from OPM2 to OPM5, <b>SCFG.TOSEN</b> = 0 <sub>B</sub>
		-	60	-	ms	After a transition from OPM2 to OPM5, <b>SCFG.TOSEN</b> = 1 <sub>B</sub>
Gate Monitoring time out	$t_{\text{GMTO}}$	-	15.0	-	μs	<sup>1)</sup>
Life sign error detection time	$t_{\text{LS}}$	-	5	-	μs	After error condition detected by logic.
Output stage monitor inhibit time.	$t_{\text{OSM}}$	-	4	-	μs	After hard transition <sup>1)</sup> .
<b>EN/FEN</b> half-pulse acceptance window	$t_{\text{FENW}}$	1.20		3.00	μs	<b>PCFG2.FEN</b> =1 <sub>B</sub> , $f_{\text{OSC1}}$ =16.6 MHz <sup>1)</sup>

<sup>1)</sup> Verified by design / characterization. Not tested in production.

**Specification**

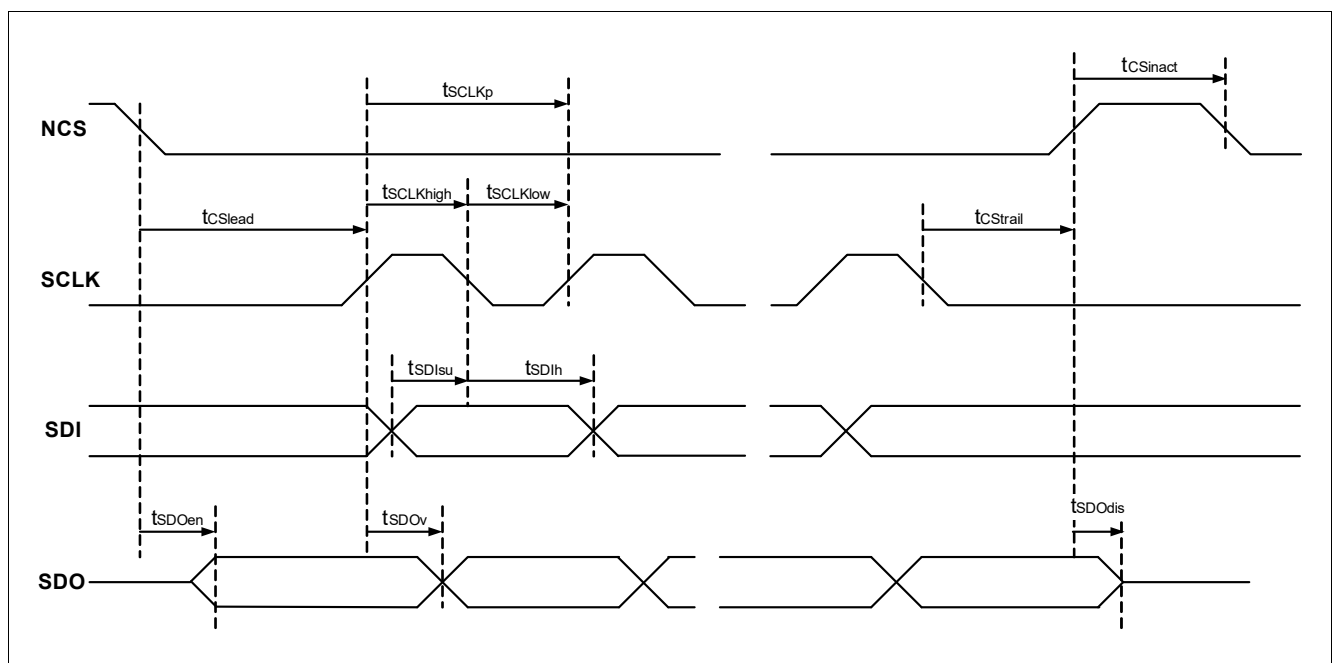
**5.5.12 SPI Interface**

**Table 63 SPI Interface Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
SPI frame size	$N_{\text{bit}}$	N.a.	$N \cdot 16$	N.a.	bit	N is the daisy chain length
Baud rate	$f_{\text{SCLK}}$	0.1	-	2.0	MHz	Standard SPI configuration, <sup>1)</sup>
		0.1	-	1.8	MHz	Daisy chain configuration, <sup>1)</sup>
<b>SCLK</b> duty cycle	$D_{\text{SCLK}}$	45	-	55	%	2)
<b>SDI</b> set-up time	$t_{\text{SDIsu}}$	65	-	-	ns	2)
<b>SDI</b> hold time	$t_{\text{SDIh}}$	100	-	-	ns	2)
<b>NCS</b> lead time	$t_{\text{CSlead}}$	1	-	-	μs	2)
<b>NCS</b> trail time	$t_{\text{CStrail}}$	1	-	-	μs	2)
<b>NCS</b> inactive time	$t_{\text{CSinact}}$	10	-	-	μs	2)
<b>SDO</b> enable time	$t_{\text{SDOen}}$	-	-	500	ns	$C_{\text{load}} = 20 \text{ pF}^{2)}$
<b>SDO</b> disable time	$t_{\text{SDOdis}}$	-	-	1	μs	$C_{\text{load}} = 20 \text{ pF}^{2)}$
<b>SDO</b> valid time	$t_{\text{SDOv}}$	10	-	185	ns	$C_{\text{load}} = 20 \text{ pF}^{2)}$

1) Low Limit verified by design / characterization. Not tested in production.

2) Verified by design / characterization. Not tested in production.



**Figure 29 SPI Interface Timing**

**Specification**

**5.5.13 Insulation Characteristics**

**Table 64 Insulation Characteristics in compliance with DIN V VDE 0884 - 10 : 2006-12, expired on December 31st, 2019**

Description	Symbol	Characteristic	Unit
Installation classification per EN60664-1, Table 1: rated main voltage less than 150 V <sub>rms</sub> rated main voltage less than 300 V <sub>rms</sub> rated main voltage less than 600 V <sub>rms</sub>		I - IV I - III I - II	
Climatic Classification		40 / 125 / 21	
Pollution Degree (EN 60664-1)		2	
Minimum External Clearance	CLR	8.12	mm
Minimum External Creepage	CPG	8.24	mm
Minimum Comparative Tracking Index	CTI	400	
Maximum Repetitive Insulation Voltage	V <sub>IORM</sub>	1420	V <sub>PEAK</sub>
Highest Allowable Overvoltage	V <sub>IOTM</sub>	6000	V <sub>PEAK</sub>
Maximum Surge Insulation Voltage	V <sub>IOSM</sub>	4615	V <sub>PEAK</sub>
Surge Insulation Test Voltage V <sub>IOSM,test</sub> = V <sub>IOSM</sub> * 1.3	V <sub>IOSM,test</sub>	6000	V <sub>PEAK</sub>
Input to output test voltage, method b <sup>1)</sup> V <sub>pd(m)</sub> = V <sub>IORM</sub> * 1.875, 100% production test with t <sub>m</sub> = 1 sec, partial discharge charge < 5 pC	V <sub>pd(m)</sub>	2663	V <sub>PEAK</sub>
	V <sub>ini(b)</sub>	6000	V <sub>PEAK</sub>
Input to output test voltage, method a <sup>1)</sup> V <sub>pd(m)</sub> = V <sub>IORM</sub> * 1.6, 100% sample test with t <sub>m</sub> = 60 sec, partial discharge charge < 5 pC	V <sub>pd(m)</sub>	2272	V <sub>PEAK</sub>
	V <sub>ini(a)</sub>	6000	V <sub>PEAK</sub>
Insulation resistance at T <sub>s</sub> = 150°C, V <sub>IO</sub> = 500 V	R <sub>IO</sub>	> 10 <sup>9</sup>	Ω
Insulation resistance at 100°C ≤ T <sub>amb</sub> ≤ 125°C, V <sub>IO</sub> = 500 V	R <sub>IO</sub>	> 10 <sup>12</sup>	Ω

1) Refer to VDE 0884 - 10 for a detailed description of Method a and b partial discharge

**Table 65 Isolation Characteristics referring to UL 1577**

Description	Symbol	Characteristic	Unit
Insulation Test Voltage / 1 min	V <sub>ISO</sub>	3750	V <sub>rms</sub>
Insulation Test Voltage / 1 sec	V <sub>ISO</sub>	4500	V <sub>rms</sub>

## 6 Package Information

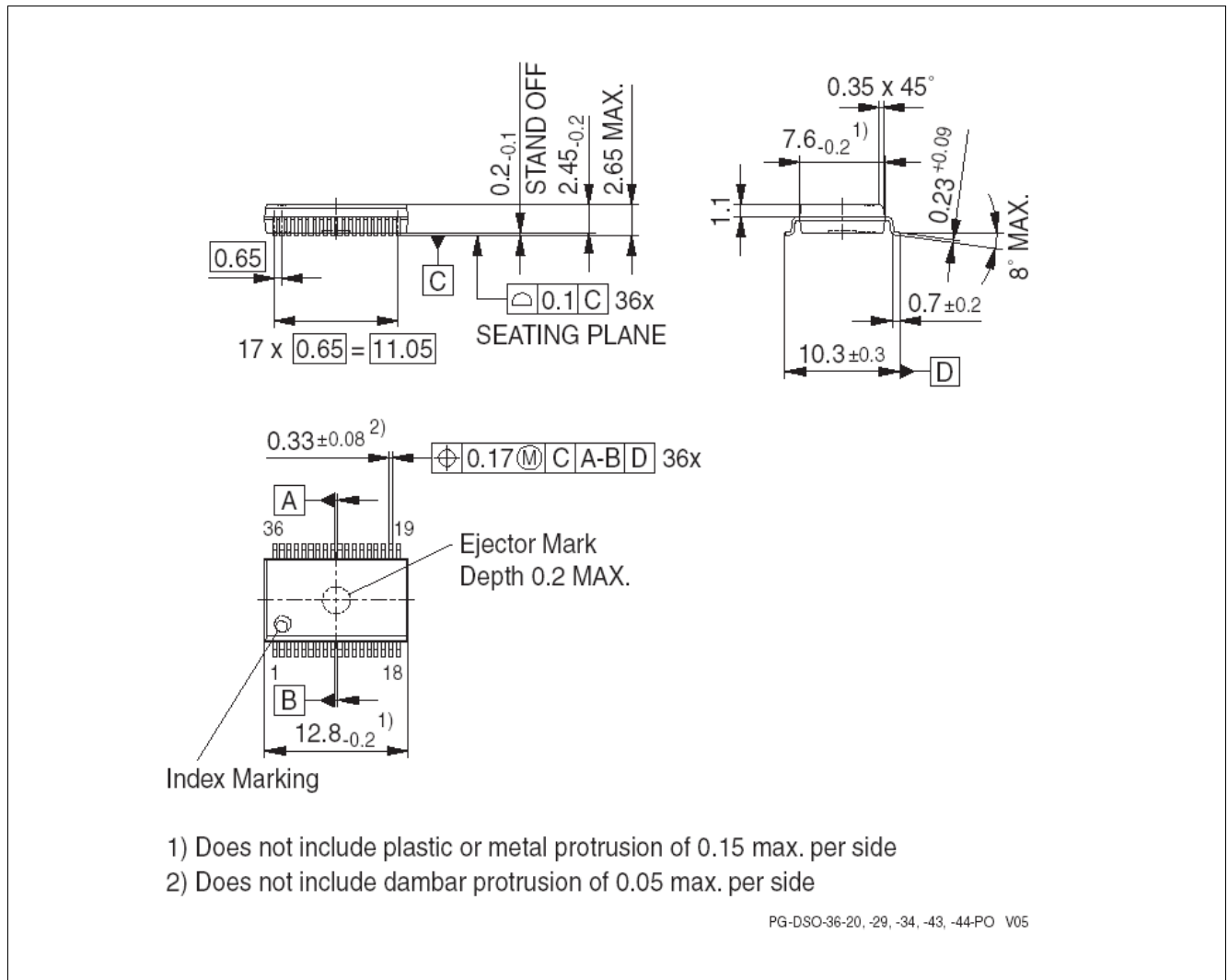


Figure 30 Package Dimensions

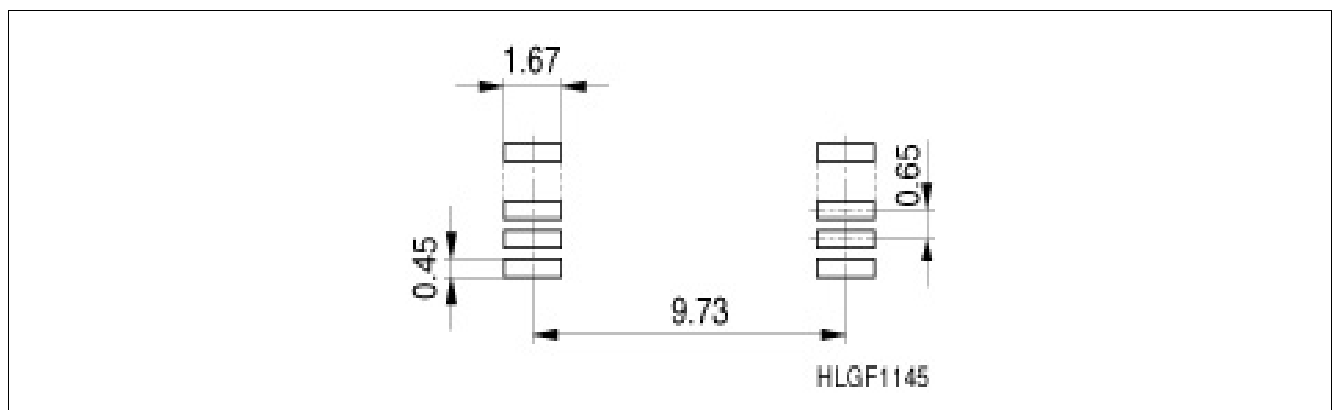


Figure 31 Recommended Footprint



## Revision History

### 7 Revision History

Page or Item	Subjects (major changes since previous revision)
<b>Rev. 3.3, 2022-01-10</b>	
<b>Page 100</b>	SVERS chip ID in SID register changed to 8B1 <sub>H</sub> in <b>Chapter 4.2</b>
<b>Page 33</b>	Added note: “Events class A and class B can occur quasi simulatnously....
<b>Rev 3.2, 2021-11-15</b>	
<b>Page 143</b>	Added info that DIN V VDE 0884-10:2006 -12 expired on December 31st, 2019 VIO SM updated to reflect actual rated value instead of test voltage Added specification for isolation resistance and partial discharge
<b>Page 129</b>	Typo fixed in ESD immunity rating - corner pins are 1, 18, 19, 36
<b>Page 1,</b> <b>Page 2</b>	Update Frontcover: Change Applications to “Potential applications” added Special paragraph “Product Validation”, moved automotive qualification to this paragraph. Changed Trademark Info at the backcover.
	Added new PRO-SIL on frontpage without trademark
	Target applications renamed potential applications
All	Updated layout of the document(New start page, editorial changes, chapter numbering changed, new Variable sheet)
<b>Page 139</b>	moved DESAT Input Voltage Range to DESAT characteristics <b>Table 57</b>
<b>Page 135</b>	combined Table 5-11 & Table 5-12 to <b>Table 51</b>
<b>Page 79</b>	Updated <b>Chapter 4</b> with constant names for better readability,
<b>Page 145</b>	Revision History moved to <b>Chapter 7</b>
<b>Page 36</b>	Removed misleading and confusing example in <b>Chapter 2.4.5.6</b>

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2021-01-10**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2022 Infineon Technologies AG.**

**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference  
Z8F80223577**

#### IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[1EDI2002AS](#) [1EDI2002ASXUMA2](#)