EiceDRIVER™ 1EDBx275F

Single-channel isolated gate-driver ICs in 150 mil DSO package

Description

EiceDRIVER™ 1EDBx275F is a family of single-channel isolated gate-driver ICs, designed to drive Si, SiC and GaN power switches.

1EDBx275F is available in an 8-pin DSO package with 4 mm input-to-output creepage distance; it provides isolation by means of on-chip coreless transformer (CT) technology.

With tight timing specifications, 1EDBx275F is designed for fast-switching medium-to-high power systems. Excellent common-mode rejection, low part-to-part skew, fast signal propagation and small package size make 1EDBx275F a superior alternative to high-side driving solutions using optocouplers or pulse transformers.

Features

- Single-channel isolated gate-driver
- 45 ns input-to-output propagation delay with excellent accuracy (+4/-4 ns)
- Separate low impedance source and sink outputs
- Fast clamping of parasitics-induced output overshoots under UVLO conditions
- Fast start-up times and fast recovery after supply glitches
- Optimized UVLO levels (4 V, 8 V, 13 V) for Si, SiC and GaN transistors
- High common mode transient immunity (CMTI > 300 V/ns)
- Available in 8-pin 150mil DSO package
- Qualified for industrial grade applications

Isolation and safety certificates

- UL1577 with V_{ISO} = 3000 V_{RMS} (certification pending)

Potential Applications

- Server, telecom and industrial Switch-Mode Power Supplies (SMPS)
- EV power modules, motor drives and power tools
- Solar power inverters and Uninterruptable Power Supplies (UPS)

Table 1 EiceDRIVER™ 1EDBx275F Portfolio

Part number	Peak source / sink current	UVLO ON / OFF	Isolation certification	Package
1EDB7275F	5.4 A / 9.8 A (for V_{DDO} = 15V)	4.2 V / 3.9 V	UL1577 (V_{ISO} = 3000 V_{RMS})	PG-DSO-8
1EDB8275F		8.0 V / 7.0 V		
1EDB9275F		13.7 V / 12.9 V		

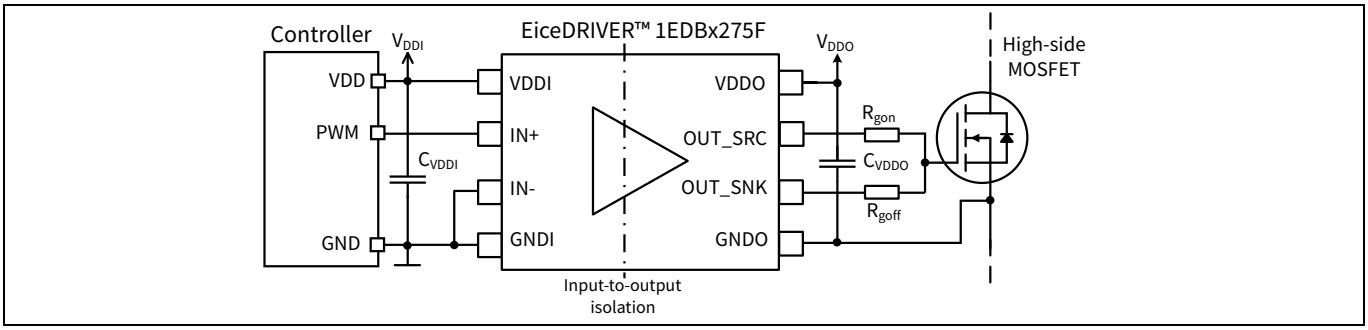

Figure 1 Typical application

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1 Pin configuration and description

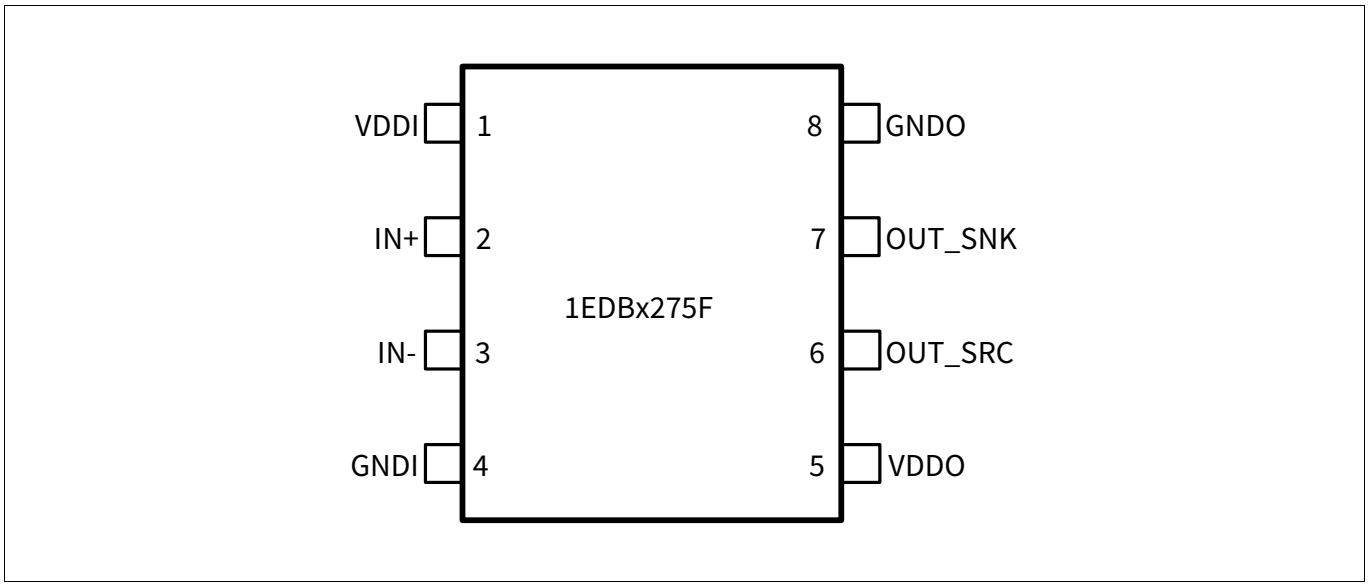


Figure 2 Pin configuration (top side view)

Table 2 Pin description

Pin	Symbol	Description
1	VDDI	Input-side supply voltage (3 V to 15 V)
2	IN+	Non-inverting driver input (active high); if IN+ is low or left open, OUT_SNK is low
3	IN-	Inverting driver input (active low); if IN- is high or left open, OUT_SNK is low
4	GNDI	Input-side ground reference
5	VDDO	Output-side supply voltage (up to 20 V)
6	OUT_SRC	Driver output source, low-impedance switch to VDDO
7	OUT_SNK	Driver output sink, low-impedance switch to GNDO
8	GNDO	Output-side ground reference

For package drawing details see **Chapter 8 Package outline dimensions**.

2 Functional description

2.1 Block diagram

A simplified functional block diagram for the EiceDRIVER™ 1EDBx275F is given in **Figure 3**.

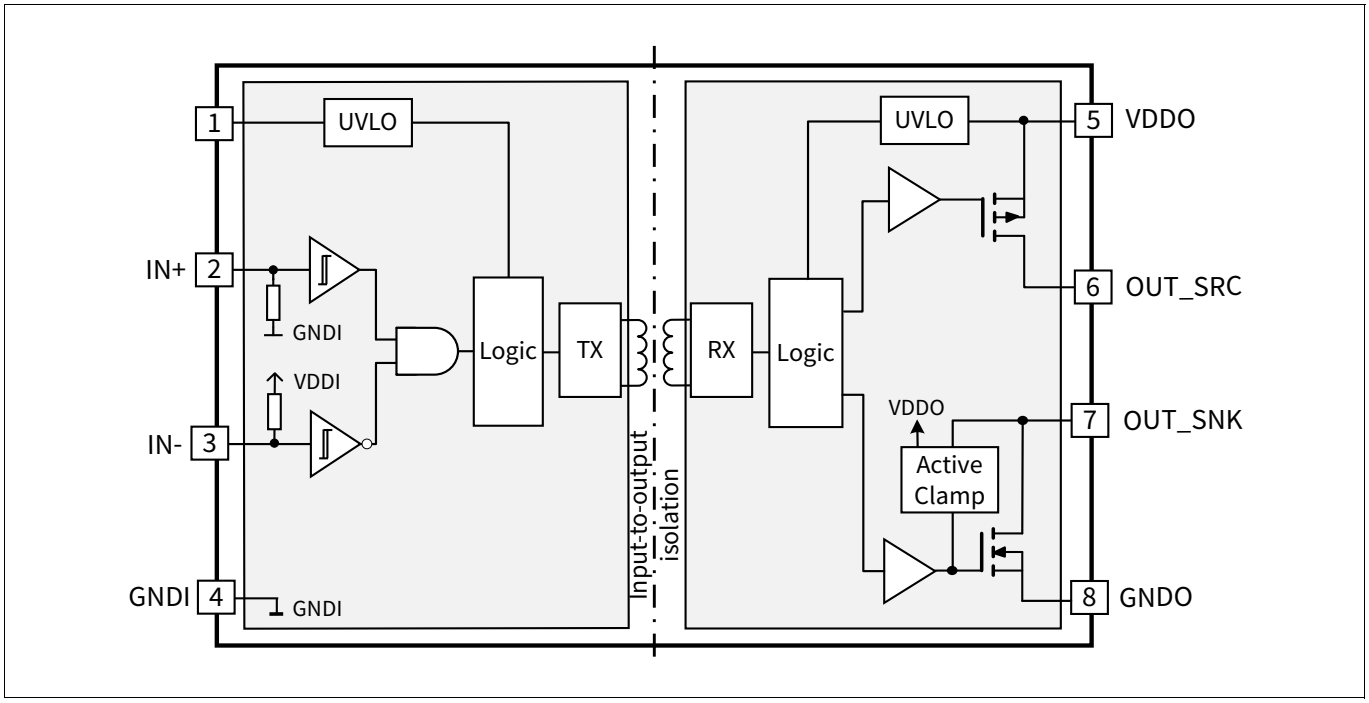


Figure 3 Block diagram

2.2 Power supply and Undervoltage Lockout (UVLO)

Due to the isolation between input and output side, two power domains with independent power management are required. Undervoltage Lockout (UVLO) functions for both input and output supplies ensure a defined startup and robust functionality under all operating conditions.

2.2.1 Input supply voltage

The input die is powered via VDDI and supports a wide supply voltage range from 3 V to 15 V. A ceramic bypass capacitor must be placed between VDDI and GNDI in close proximity to the device; a minimum capacitance of 100 nF is recommended.

Power consumption to some extent depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the coreless transformer. Due to the chosen robust encoding scheme the average repetition rate of these pulses and thus the average supply current depends on the switching frequency, f_{sw}. However, for $f_{sw} < 500$ kHz this effect is very small.

The Undervoltage Lockout function for the input supply VDDI ensures that, as long as VDDI is below UVLO (e.g. in startup), no data is transferred to the output side and the gate driver output is held low (Safety Lock-down at startup). When VDDI exceeds the UVLO level, the PWM input signal is transferred to the output side. If the output side is ready (not in UVLO condition), the output reacts according to the logic input.

2.2.2 Output supply voltage

The output die is powered via VDDO (up to 20 V). A ceramic bypass capacitor must be placed between VDDO and GNDO in close proximity to the device. A minimum capacitance of 20 x C_{iss} (MOSFET input capacitance) is recommended to ensure an acceptable ripple (5% of VDDO) on the supply pin.

The minimum supply voltage is set by the Undervoltage Lockout (UVLO) function. The gate-driver output can be switched only, if the output supply voltage (VDDO) exceeds the output-side UVLO. Thus it can be guaranteed that the switch transistor is not operated, if the driving voltage is too low to achieve a complete and fast transition to the "on" state. Low driving voltage in fact could cause the power MOSFET to enter its saturation (ohmic) region with potentially destructive power dissipation; the output UVLO ensures that the switch transistor always stays within its Safe Operating Area (SOA). Versions with 4 V, 8 V, 13 V UVLO thresholds for the output supply are currently available; **Table 3** shows the recommended UVLO levels for different Infineon power switch families.

Table 3 Recommended 1EDBx275F UVLO levels for typical use-cases

Switch family	Switch part number example	Recommended 1EDBx275F
Logic level OptiMOS™	BSC010N04LS6, BSZ070N08LS5, ..	1EDB7275F (4 V UVLO)
Normal level OptiMOS™	BSC040N10NS5, BSZ084N08NS5, ..	1EDB8275F (8 V UVLO)
CoolMOS™	IPP60R099C7, IPB60R600P6, ..	1EDB8275F (8 V UVLO)
650 V CoolSiC™	IMZA65R027M1H, IMW65R107M1H, ..	1EDB9275F (13 V UVLO)
600 V CoolGaN™	IGOT60R070D1, IGLD60R070D1, ..	1EDB7275F (4V UVLO)

2.2.3 Input stage

The logic driver output state is equal to the non-inverted or inverted input signal state at pins IN+ or IN-, respectively. The non-inverting input IN+ is internally pulled down to a logic low voltage and the inverting input is internally pulled up to a logic high voltage. This prevents any switching-on during power-up or in other situations with insufficient supply voltage.

The input is compatible with LV-TTL levels and provide a hysteresis of typically 0.9 V. This hysteresis is independent of the supply voltage V_{DDI}.

Table 4 shows the IN+, IN- driver logic in case of sufficiently high supply voltage. Otherwise the outputs of the driver are determined by the Undervoltage Lockout (UVLO) and Output Active Clamping functionalities as shown in **Table 5**.

Table 4 Logic table in case of sufficient bias power

Inputs		Supplies	Outputs	Note
IN+	IN-	V_{DDI}, V_{DDO}	OUT	
H	L	>$UVLO_{VDDx,on}$ (active)	H	–
x	H		L	The output is disabled via IN- (active low)
L	x		L	The output is disabled via IN+ (active high)

2.3 Driver output

The rail-to-rail output stage realized with complementary MOS transistors is able to provide a typical 5.4 A sourcing and 9.8 A sinking peak current for a 15 V supply. The low on-resistance coming together with high driving current is particularly beneficial for fast switching of very large MOSFETs. With a R_{on} of 0.95 Ω for the sourcing pMOS and 0.48 Ω for the sinking nMOS transistor the driver can in most applications be considered as a nearly ideal switch. The p-channel sourcing transistor enables real rail-to-rail behavior without suffering from the voltage drop unavoidably associated with nMOS source follower stages.

In case of floating inputs or insufficient supply voltage not exceeding the UVLO thresholds, the driver output is actively clamped to the "low" level (GNDO).

2.4 Output active clamping

The Undervoltage Lockout (UVLO) ensures no driver operation for supplies below the UVLO thresholds. However, this is not sufficient to guarantee that the output of the driver is kept low. Transient-induced current on the MOSFETs side may pull-up the output node of the driver and the gate voltage causing an unwanted turn-on of the switch; this is particularly critical in systems using bootstrapping since, during start-up, the supply of the high-side channel is delayed, while the low-side MOSFETs is already switching. In resonant topologies (as LLC), the half-bridge switching node may be pulled up after the turn-off of the low-side switch. When this is turned on again, the dv/dt induced increase of the high-side gate voltage cannot be clamped by the drivers $R_{DSON,sink}$ if the the boostrap supply is not yet available.

With a fast active clamping circuit in the output stage, EiceDRIVER™ 1EDBx275F ensures safe operation in all UVLO situations. This structure allows fast reaction and effective clamping of the output pins (OUT). The exact reaction time depends on the output supply (V_{DDO}) and on the output voltage levels; however, already for very low supply levels (~1 V), the active clamping is able to react in some tens of ns.

Undervoltage Lockout together with the Output Active Clamping ensure that the output is actively held low in case of unsufficient output-side supply voltage.

Table 5 Logic table in case of insufficient supply voltages

Inputs	Supplies		Output
INx	**V_{DDI}**	**V_{DDO}**	**OUT**
x	> $UVLO_{VDDI,on}$	1.2 V < V_{DDO} < $UVLO_{VDDO,on}$	L

2.5 CT communication and input to output data transmission

A coreless transformer (CT) based communication module is used for PWM signal transfer between input and output. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog timeout at the receiver side enables recovery from communication fails and ensures safe system shutdown in failure cases.

3 Electrical characteristics and parameters

The absolute maximum ratings are listed in **Table 6**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 6 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	-0.3	–	17	V	–
Output supply voltage	V_{DDO}	-0.3	–	22	V	–
Voltage at pins IN+, IN-	V_{IN}	-0.3	–	17	V	–
		-5	–	–	V	transient for 50 ns [1]
Voltage at pin OUT_SRC	V_{OUT_SRC}	V_{DDO}-24	–	V_{DDO}+0.3	V	OUT = low, DC
		V_{DDO}-24	–	V_{DDO}+2	V	OUT = low, transient for 200 ns [1]
Voltage at pin OUT_SNK	V_{OUT_SNK}	-0.3	–	24	V	OUT = high, DC
		-2	–	24	V	OUT = high, transient for 200 ns [1]
Reverse current peak at pin OUT_SRC	I_{SRC_rev}	-5	–	–	A_{pk}	transient for 500 ns [2]
Reverse current peak at pin OUT_SNK	I_{SNK_rev}	–	–	5	A_{pk}	transient for 500 ns [2]
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150	°C	–
Soldering temperature	T_{SOL}	–	–	260	°C	reflow / wave soldering [2]
ESD capability	V_{ESD_CDM}	–	–	0.5	kV	Charged Device Model (CDM) [3]
	V_{ESD_HBM}	–	–	2	kV	Human Body Model (HBM) [4]

1) parameter verified by design, not tested in production
2) according to JESD22A111
3) according to ANSI/ ESDA/JEDEC JS-002
4) according to ANSI/ ESDA/JEDEC JS-001 (discharging 100 pF capacitor through 1.5 kΩ resistor)

3.2 Thermal characteristics

Table 7 Thermal characteristics at T_A= 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient [1]	R_{thJA25}	–	117	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	54	–	K/W	
Thermal resistance junction-board [3]	R_{thJB25}	–	37	–	K/W	
Characterization parameter junction-top [4]	Ψ_{thJT25}	–	9	–	K/W	
Characterization parameter junction-board [4]	Ψ_{thJB25}	–	36	–	K/W	

1) obtained by simulating a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a
2) obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88
3) obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8
4) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7)

3.3 Operating range

Table 8 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	3.0	–	15	V	Min. defined by UVLO
Output supply voltage	V_{DDO}	4.5	–	20	V	for 1EDB7275F
		8.5	–	20	V	for 1EDB8275F
		14.3	–	20	V	for 1EDB9275F
Logic input voltage at pins IN+, IN-	V_{IN}	-0.3	–	15	V	–
Junction temperature	T_J	-40	–	150	°C	[1]
Ambient temperature	T_A	-40	–	125	°C	–

1) continuous operation above 125°C may reduce lifetime

3.4 Electrical characteristics

Unless otherwise noted the electrical characteristics are given for V_{DDI} = 3.3 V, V_{DDO} = 12 V (V_{DDO} = 18 V for 1EDB9275F) and no load.

Typical values are given at T_J = 25°C. Min. and max. values are the lower and upper limits valid within the full operating temperature range.

Table 9 Power supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
I_{VDDI} quiescent current	I_{VDDIq}	–	0.85	1	mA	no switching
I_{VDDO} quiescent current	I_{VDDOq}	–	0.65	0.85	mA	OUT = low, no switching, V_{DDO} = 12 V
		–	0.73	1.0	mA	OUT = low, no switching, V_{DDO} = 18 V
		-	0.84	1.0	mA	OUT = high, no switching, V_{DDO} = 12 V
		–	0.97	1.1	mA	OUT = high, no switching, V_{DDO} = 18 V

Table 10 Undervoltage Lockout V_{DDI}

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold V_{DDI}	$UVLO_{VDDI,on}$	2.7	2.85	3.0	V	–
Undervoltage Lockout (UVLO) turn-off threshold V_{DDI}	$UVLO_{VDDI,off}$	–	2.65	–	V	–
UVLO threshold hysteresis V_{DDI}	$UVLO_{VDDI, hys}$	0.15	0.2	0.25	V	–

Table 11 Undervoltage Lockout V_{DDO} for 1EDB7275F (4 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	4.0	4.2	4.4	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	3.9	–	V	–
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.2	0.3	0.4	V	–

Table 12 Undervoltage Lockout VDDO for 1EDB8275F (8 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	7.6	8.0	8.4	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	7.0	–	V	–
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.7	1	1.3	V	–

Table 13 Undervoltage Lockout VDDO for 1EDB9275F (13 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	13.0	13.7	14.2	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	12.9	–	V	–
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.4	0.8	1.2	V	–

Table 14 Logic inputs IN+, IN-

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.2	2.5	V	–
Input voltage threshold for transition HL	V_{INL}	1	1.3	1.6	V	–
Input voltage threshold hysteresis	V_{IN_hys}	–	0.9	–	V	–
High-level input leakage current at pin IN+	$I_{IN+,H}$	–	40	70	µA	IN+ tied to VDDI
Low-level input leakage current at pin IN-	$I_{IN-,L}$	-55	-40	–	µA	IN- tied to GNDI
Input pull-down resistor	$R_{IN,PD}$	–	75	–	kΩ	–
Input pull-up resistor	$R_{IN,PU}$	–	75	–	kΩ	–

Table 15 Static output characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High-level (sourcing) output resistance	R_{on_SRC}	0.52	0.95	1.70	Ω	I_{SNK} = 50 mA
Peak sourcing output current [1]	I_{SRC_pk}	–	5.2	–	A	V_{DDO} = 12 V, V_{OUT} = 0 V; see **Figure 23**, **Figure 24**
		–	5.6	–	A	V_{DDO} = 18 V, V_{OUT} = 0 V; see **Figure 23**, **Figure 24**
Low-level (sinking) output resistance	R_{on_SNK}	0.31	0.48	0.88	Ω	I_{SRC} = 50 mA
Peak sinking output current [1]	I_{SNK_pk}	–	-9.2	–	A	V_{DDO} = 12 V, V_{OUT} = 12 V; see **Figure 23**, **Figure 24**
		–	-10.2	–	A	V_{DDO} = 18 V, V_{OUT} = 18 V; see **Figure 23**, **Figure 24**

1) parameter not subject to production test - verified by design / characterization

Table 16 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
IN+ /IN- to output propagation delay	t_{PDon}, t_{PDoff}	41	45	49	ns	see **Figure 4**
Part-to-part skew	$\Delta t_{PDon,p-p}$	–	–	2	ns	[1]
	$\Delta t_{PDoff,p-p}$	–	–	2	ns	[1]
Pulse width distortion $\lvert t_{PDoff} - t_{PDon} \rvert$ [2]	t_{PWD}	–	–	2	ns	see **Figure 5**
Rise time [3]	t_{rise}	–	6.5	12	ns	V_{DDO} = 12 V, C_{LOAD} = 1.8 nF, see **Figure 6**
		–	8.3	16	ns	V_{DDO} = 18 V, C_{LOAD} = 1.8 nF, see **Figure 6**
Fall time [3]	t_{fall}	–	4.5	8	ns	V_{DDO} = 12 V, C_{LOAD} = 1.8 nF, see **Figure 6**
		–	5	9	ns	V_{DDO} = 18 V, C_{LOAD} = 1.8 nF, see **Figure 6**
Minimum input pulse width that changes output state	t_{PW}	15	19	23	ns	see **Figure 7**
Input-side start-up time [3]	$t_{START,VDDI}$	–	3	–	µs	see **Figure 8**
Input-side deactivation time [3]	$t_{STOP,VDDI}$	–	300	–	ns	see **Figure 8**
Output-side start-up time [3]	$t_{START,VDDO}$	–	5	–	µs	see **Figure 9**

Table 16 Dynamic characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output-side deactivation time [3]	$t_{STOP,VDDO}$	–	125	–	ns	see **Figure 9**
Activation time of output clamping in UVLO condition [3]	$t_{CLAMP,OUT}$	–	20	–	ns	see **Figure 10**

1) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
2) The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
3) parameter not subject to production test - verified by design / characterization

Table 17 Common Mode Transient Immunity (CMTI)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Static Common Mode Transient Immunity [1] [2]	$\lvert CM_{Static,H} \rvert$	300	–	–	V/ns	V_{CM} = 1500 V; IN- tied to GNDI, IN+ tied to V_{DDI} (logic high inputs)
	$\lvert CM_{Static,L} \rvert$	300	–	–	V/ns	V_{CM} = 1500 V; IN- tied to GNDI, IN+ tied to GNDI (logic low inputs)
Dynamic Common Mode Transient Immunity [1] [3]	$\lvert CM_{Dynamic} \rvert$	300	–	–	V/ns	V_{CM} = 1500 V; IN- tied to GNDI, dynamic IN+ (10 MHz square wave)

1) minimum slew rate of a common mode voltage that is able to cause a wrong output signal
2) verified by characterization according to VDE0884-11 standard definitions and test-methods
3) verified by characterization with ground reference for the common mode pulse generator connected to the coupler output-side ground to reflect real applications requirements

3.5 Isolation specifications

Table 18 Input-to-output isolation specifications

	Parameter	Symbol	Value	Unit	Note or Test Condition
Package characteristics	Nominal input-to-output clearance [1]	CLR	4.0	mm	Shortest distance in air between any input pin and any output pin
	Nominal input-to-output creepage [1]	CRP	4.0	mm	Shortest distance over package surface between any input pin and any output pin
	Comparative tracking index	CTI	> 400	V	According to DIN EN 60112 (VDE 0303-11)
	Material group	–	II	–	According to IEC 60112
	Overvoltage category	–	I -IV	–	Rated mains voltage ≤ 150 V_{RMS}
		–	I -III	–	Rated mains voltage ≤ 300 V_{RMS}
		–	I -II	–	Rated mains voltage ≤ 600 V_{RMS}
UL1577 specification [2]	Input-to-output isolation voltage	V_{ISO}	3000	V_{RMS}	$V_{TEST} = V_{ISO}$ for t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ for t = 1 s (100% productive tests)

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed-circuit-board level

2) safety certification pending

4 Timing diagrams

Figure 4 illustrates the input-to-output propagation delays as observed at the capacitively loaded output.

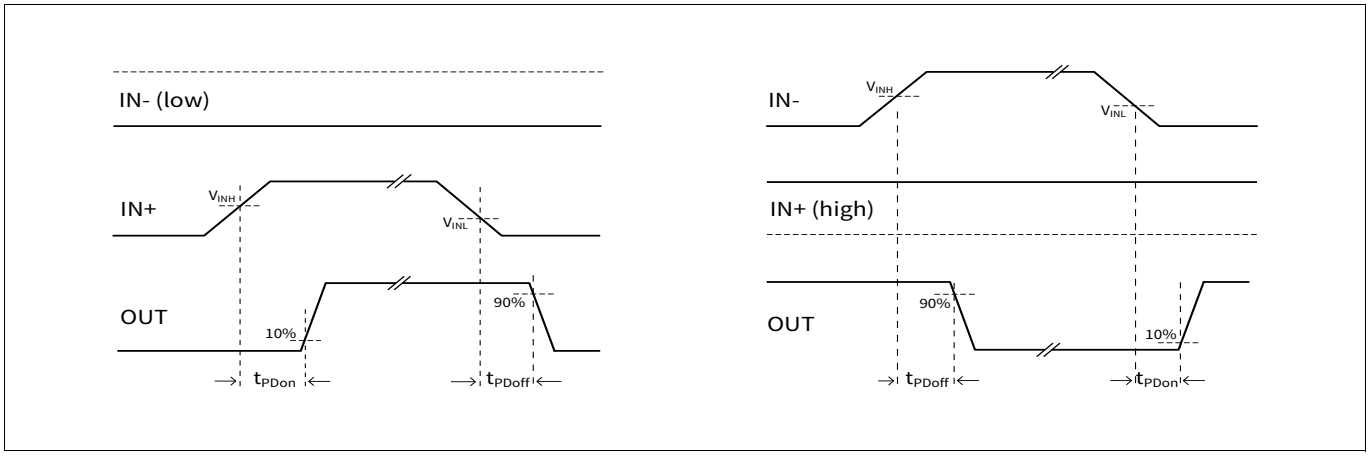


Figure 4 Input-to-output propagation delays (inverting and non-inverting case)

Figure 6 illustrates the pulse width distortion. It depicts the duty cycle distortion of the signal observed at the driver output due to the mismatch between on and off propagation delay.

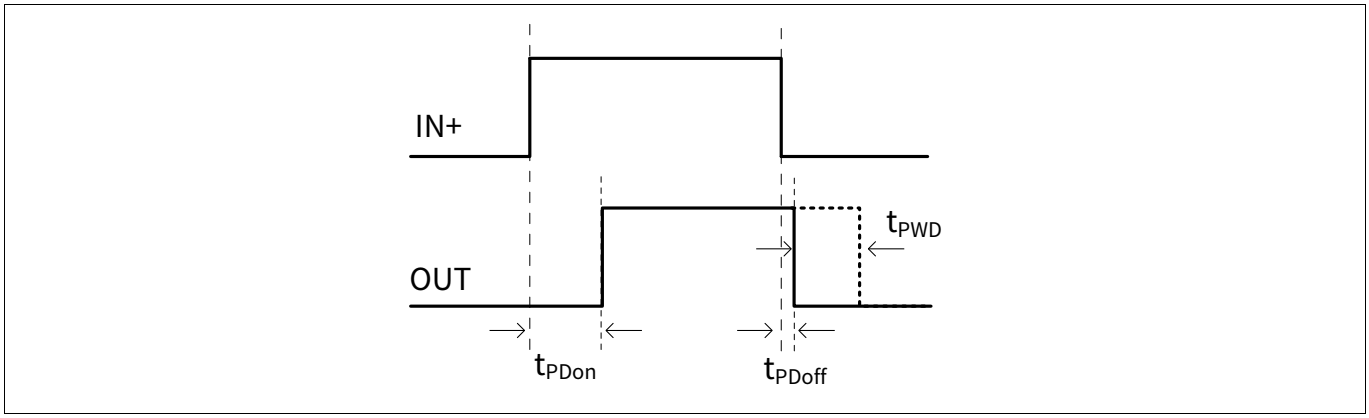


Figure 5 Pulse width distortion (unloaded output)

Figure 6 illustrates the rise and fall time as observed at the capacitively loaded output.

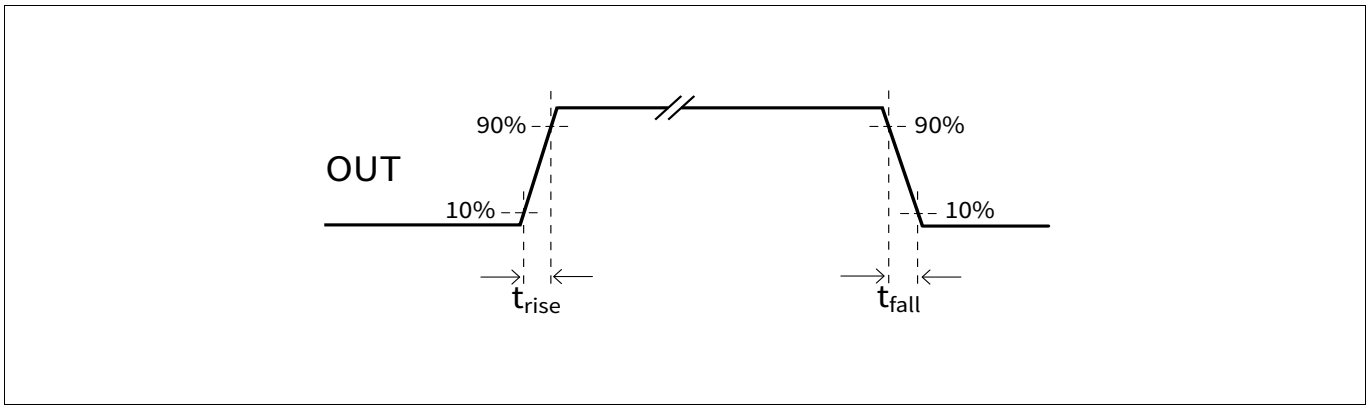


Figure 6 Rise and fall times

Timing diagrams

Figure 7 illustrates the behavior of the deglitch filter that suppresses input pulses with duration shorter than t_{PWmin}.

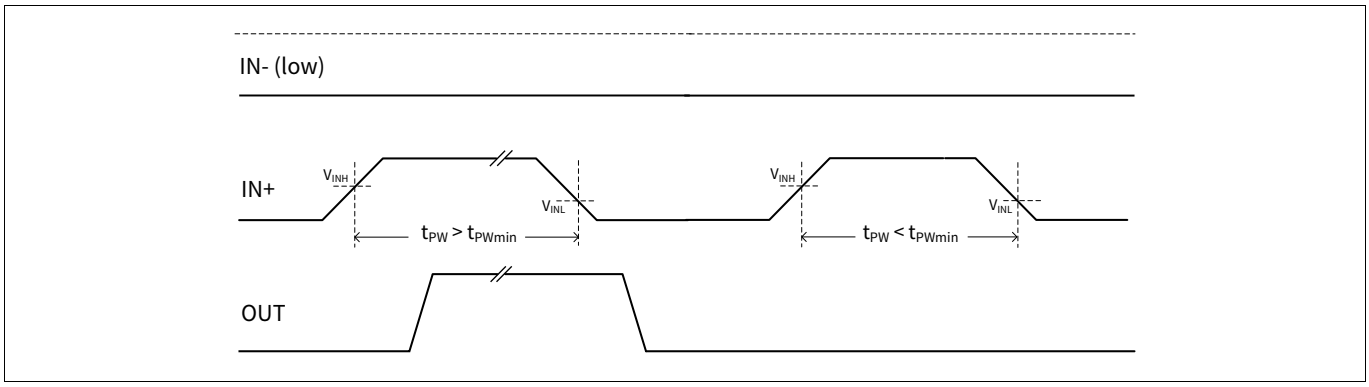


Figure 7 Minimum pulse that changes the output state

Figure 8 illustrates the input supply UVLO behavior. It depicts the reaction time to UVLO events when V_{DDI} crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

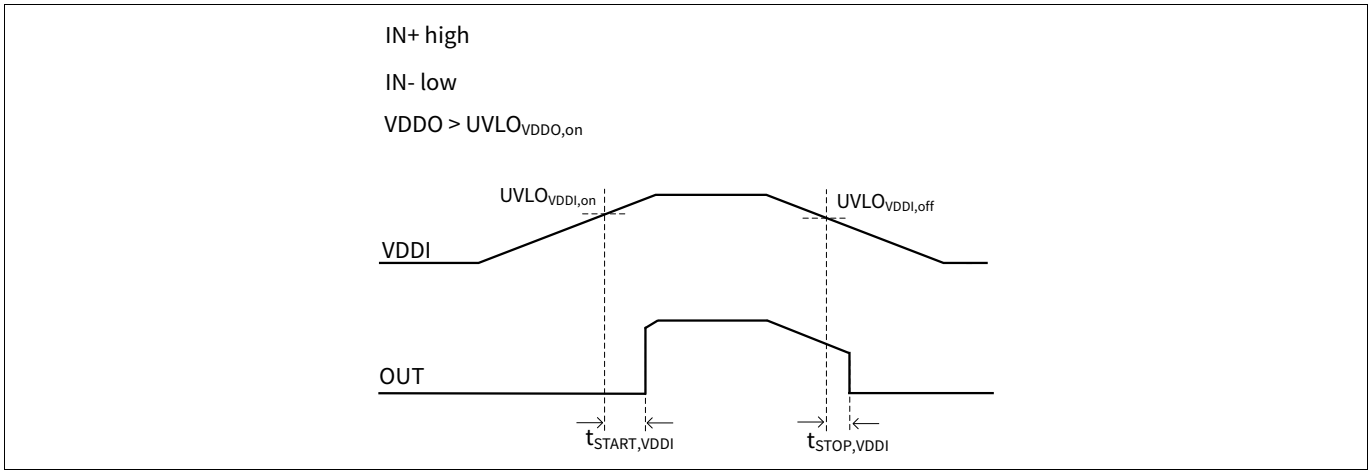


Figure 8 V_{DDI} UVLO behavior, start-up and deactivation time (unloaded output)

Figure 9 illustrates the output supply UVLO behavior. It depicts the reaction time to UVLO events when V_{DDO} crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

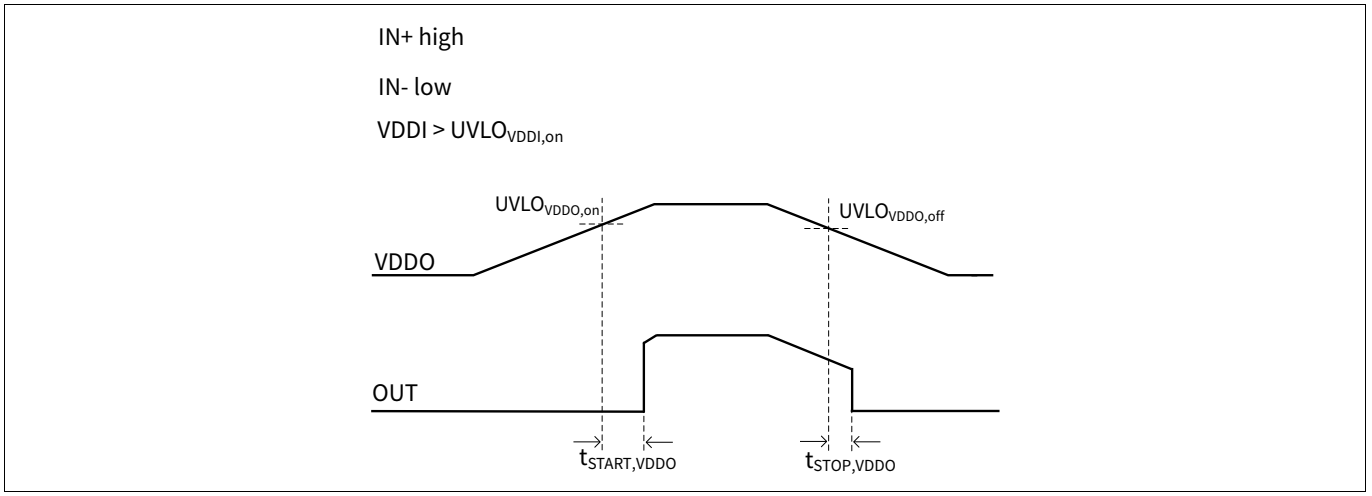


Figure 9 V_{DDO} UVLO behavior, start-up and deactivation time (unloaded output)

Timing diagrams

Figure 10 illustrates $t_{CLAMP,OUT}$, the time required to clamp potential output induced overshoots in UVLO condition ($V_{DDO} < UVLO_{VDDO,on}$).

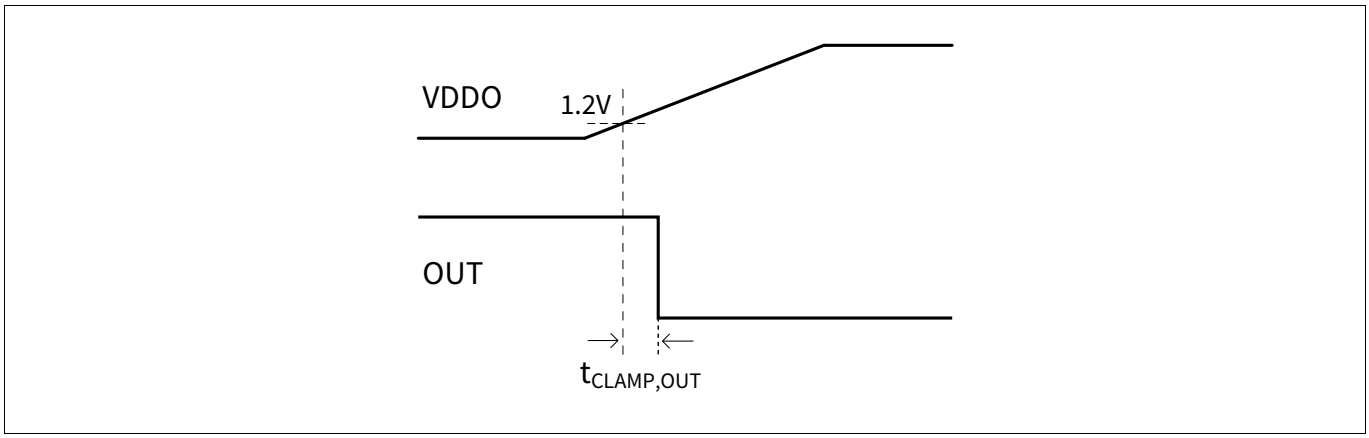


Figure 10 Activation time of output clamping in UVLO conditions (unloaded output)

5 Layout recommendation

For any fast-switching power system the PCB layout is crucial to achieve optimum performance. Among the many existing rules, recommendations, guidelines, tips and tricks, the ones of highest importance are listed as follow.

- Use low-ESR decoupling capacitances ($C_{VDDI,}$ C_{VDDO}) and place them as close as possible to the driver to support high peak currents during switching and to ensure stable supply voltages for the driver. The use of PCB planes at ground potential is also recommended to further reduce the inductance to ground.
- Minimize the gate loop inductance by placing the driver as close as possible to the driven transistor and by ensuring that the gate traces are always placed on top of a PCB plane at ground (GNDO) potential. Minimizing the power loop inductance is the key measure to limit voltage overshoots and enable fast switching.
- In case of boostrapping, minimize the boostrap loop inductance to ensure reliable operation and fast bootstrap charge. The boostrap capacitor is, in fact, charged every cycle through the bootstrap diode and the turned-on low-side transistor and the loop is subject to potential high peak charging currents. When this is not possible, use a split bootstrap capacitor with one part placed in some distance of the driver to avoid induced noise; if big enough, this acts as a stable supply for the high-side driver decoupling capacitance (placed close to the driver).
- Pay attention to keep any source of noise (like half-bridge high-current switching traces) away from the driver to avoid any coupling capacitance.
- According to the application requirements, pay attention to keep the needed input-to-output clearance and creepage on PCB level. To fully benefits from the isolation capabilities of the driver, any trace or plane below the device must be strictly avoided.
- Connect the driver ground pin to proper PCB planes to reduce the junction-to-board resistance and support the spread of heat outside the driver

A layout recommendation for EiceDRIVER™ 1EDBx275F is given in **Figure 11**.

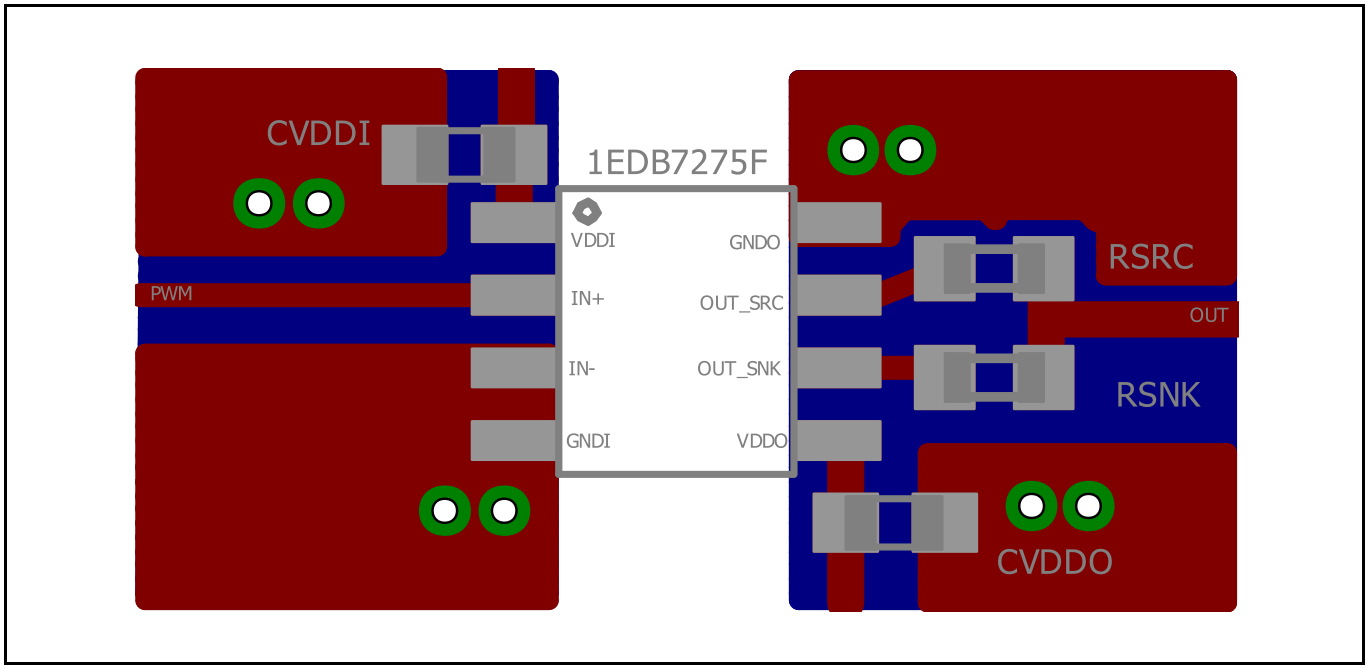


Figure 11 Layout recommendation

6 Application notes

Due to the input-to-output isolation, EiceDRIVER™ 1EDBx275F is best suited for use as high-side driver. In particular, the combination with **EiceDRIVER™ 1EDNx550B** (single-channel gate driver with true differential inputs), is best suited for half-bridge driving due to perfect matching in timing performances and output capability.

By making use of the drivers inverting and non-inverting inputs, shoot-through protection can be implemented as depicted in **Figure 12**; any undesired overlap of low-side and high-side PWM signals is not propagated at the transistors input.

This solution is preferable compared to dual-channel gate drivers in case of high-power or high-frequency designs; here minimizing the gate loop may become a critical requirement that can be more easily fulfilled by using single-channel solutions.

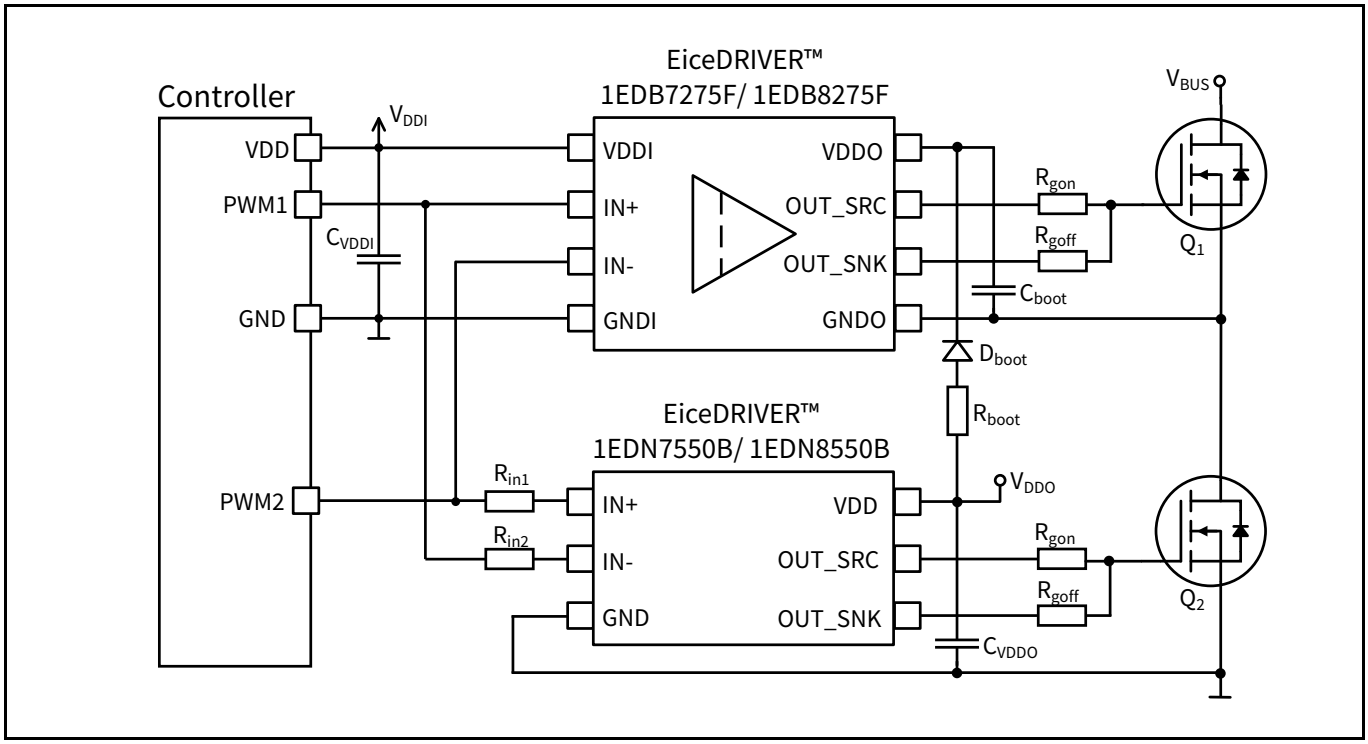


Figure 12 Typical application circuit for half-bridge driving

The high CMTI of 300 V/ns, in conjunction with the ability to drive 4-pin Kelvin source transistors, makes the combination 1EDBx275F, 1EDNx550B ideal to drive GaN and SiC power switches.

6.1 Driving 600 V CoolGaN™

Figure 13 depicts a 1EDB7275F typical use case driving Infineon´s 600V GaN power switches (CoolGaN™). The example shows a soft-switching topology; here , due to acceptable switching speed, unipolar driving is possible without risk of false triggering of the devices due to switching induced overshoots.

Details of component dimensioning can be found in the **EiceDRIVER™ 1EDi-GaN** product family datasheet.

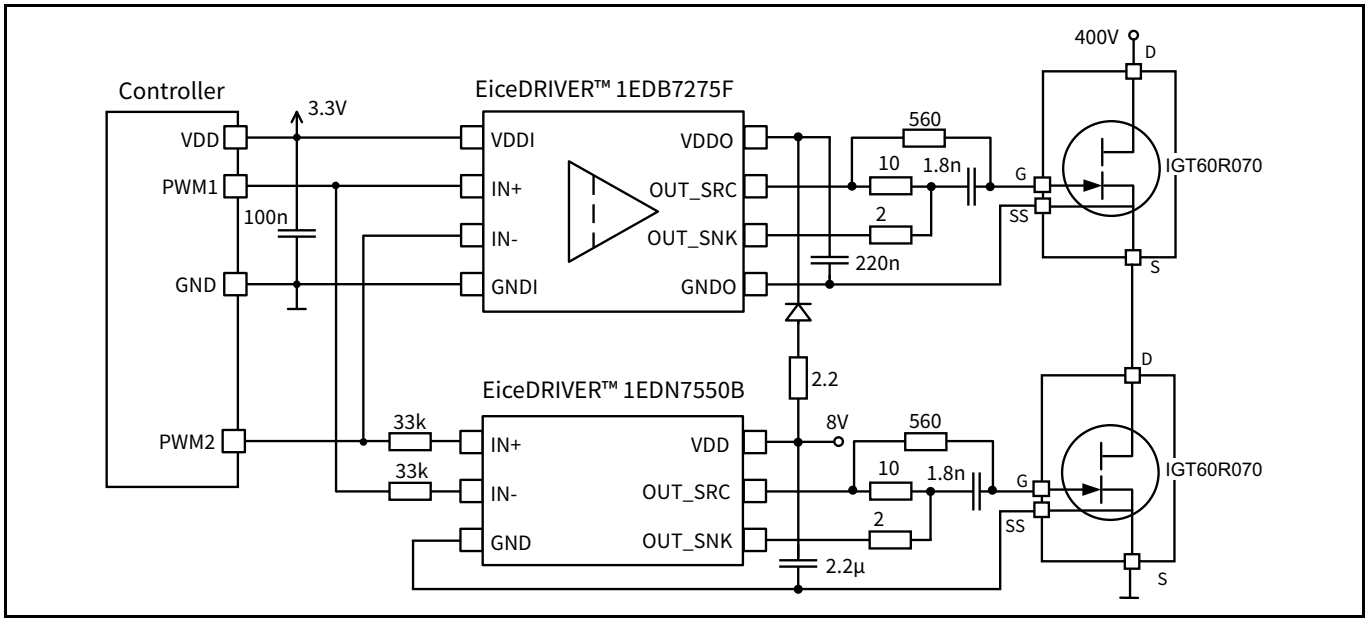


Figure 13 Typical application circuit for 600 V CoolGaN™ driving

6.2 Driving 650 V CoolSiC™

Figure 14 depicts a typical use case for 600V Infineon´s SiC power switches (CoolSiC™) in a so-called "totem-pole" PFC. It consists of a 48mΩ SiC half-bridge controlled by two 1EDB9275F EiceDRIVER™; the diode functions indicated in the power path are usually realized with low-RDSON MOSFETs operating as synchronous rectifiers. 3.3 kW of power can be handled at very high efficiency (above 99%).

Considering a typical 18 V gate-to-source voltage driving, EiceDRIVER™ 1EDB9275F offers an output UVLO level fitting for 650 V CoolSiC™. With a typical $UVLO_{VDDO,off}$ of 12.9 V, 1EDB9275F ensures that even in an unsupplied case the transistor (e.g. IMZA65R048M1H in a 3.3kW totem-pole PFC) stays within the Safe Operating Area (SOA) with acceptable power dissipation.

In **Figure 14** a Schottky diode at the CoolSiC™ gate is recommended to clamp switching induced undershoots on the gate terminal which may cause a potential drift in the gate threshold voltage $V_{gs,th}$ over lifetime.

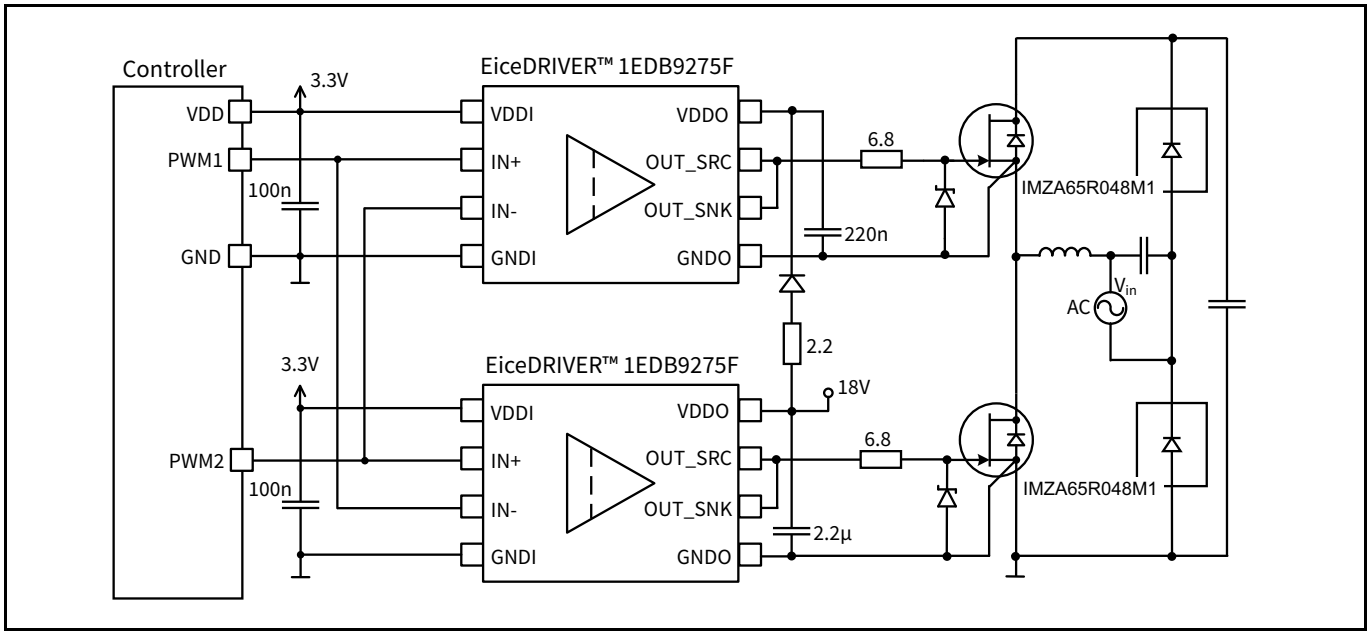


Figure 14 Typical application circuit for 650 V CoolSiC™ driving

7 Typical characteristics

V_{DDI} = 3.3 V, V_{DDO} = 12 V, T_A = 25°C, f_{sw}= 1MHz, no load unless otherwise noted.

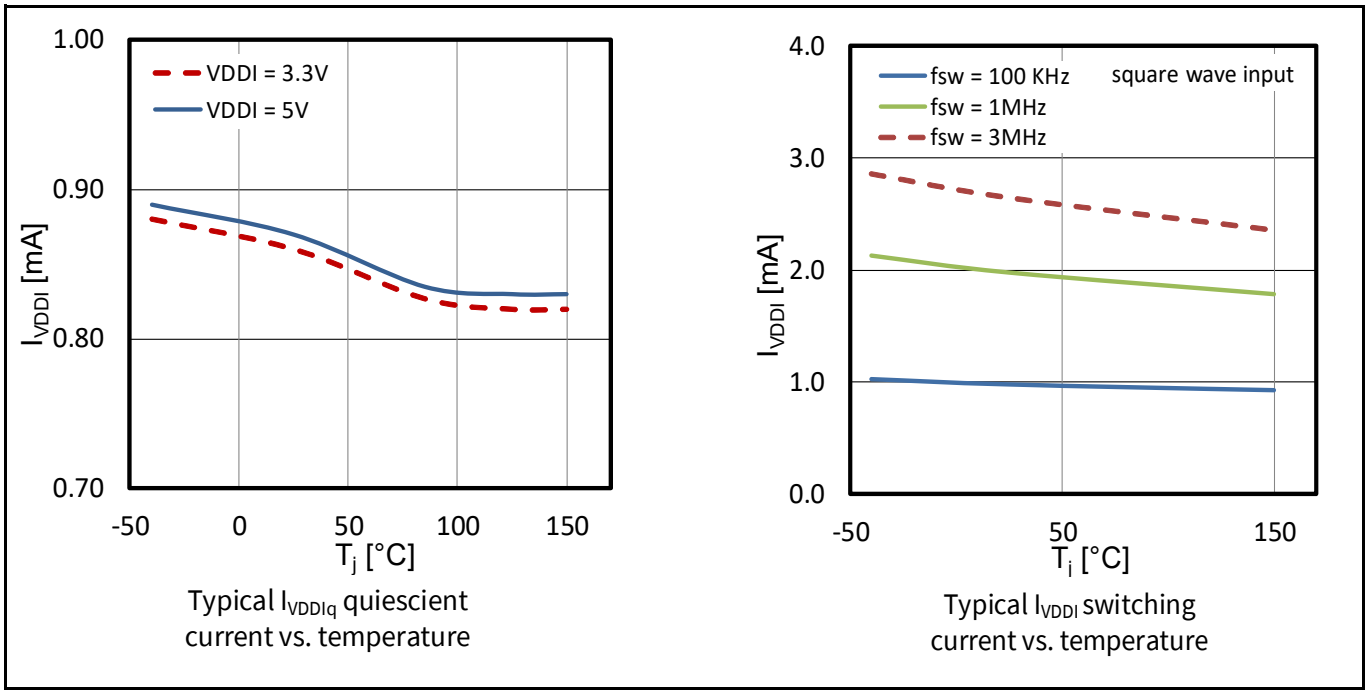


Figure 15 Input-side supply current I_{VDDIq} (quiescent and switching current)

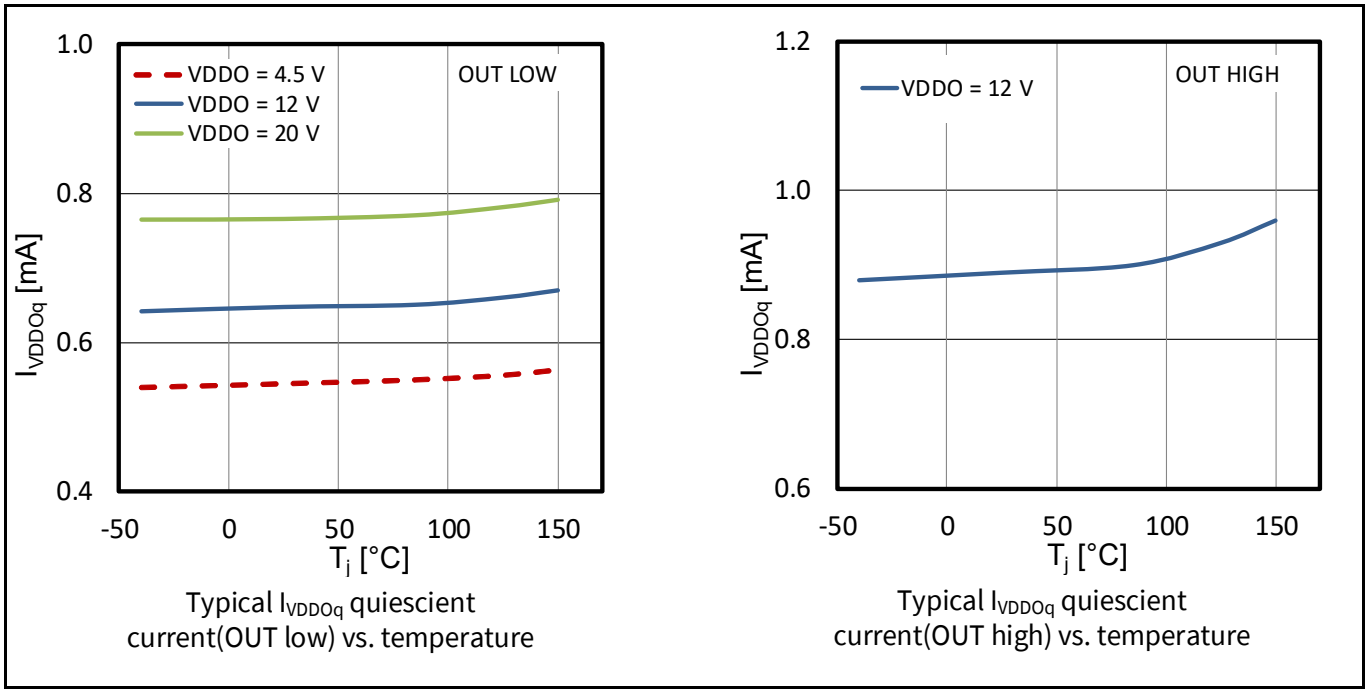
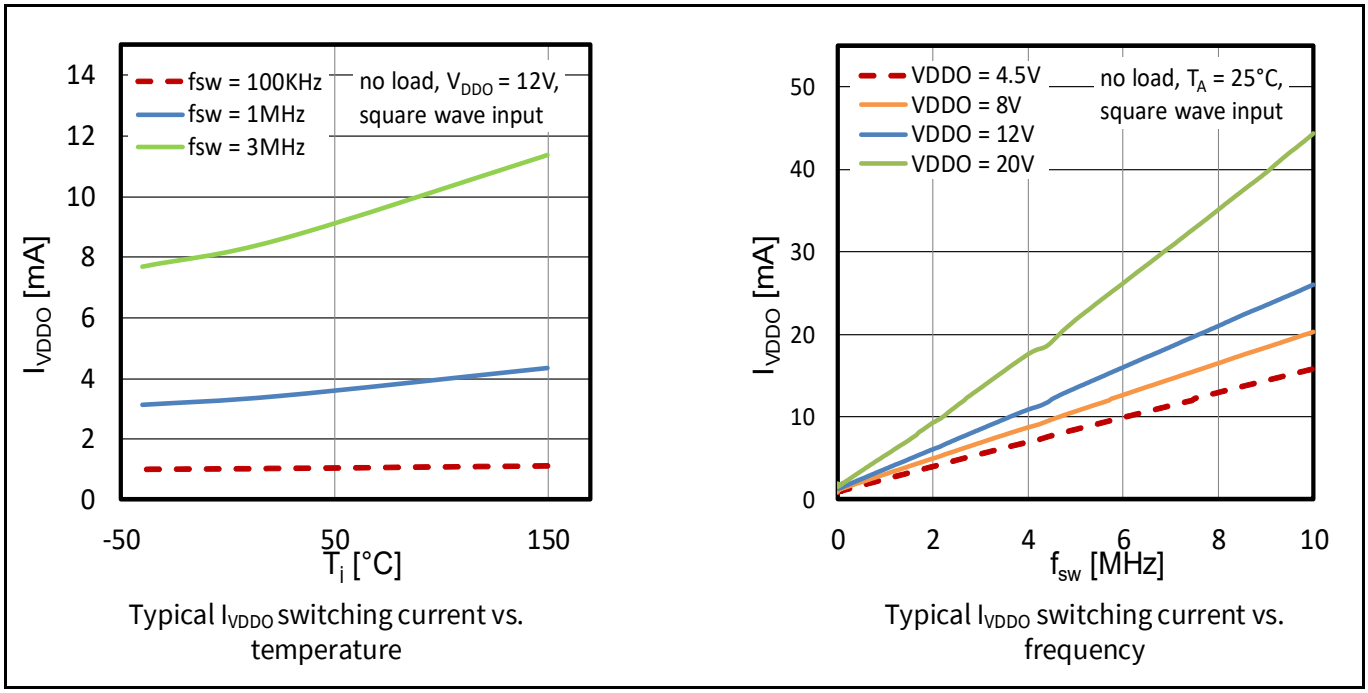


Figure 16 Output-side supply current I_{VDDOq} (quiescent current)

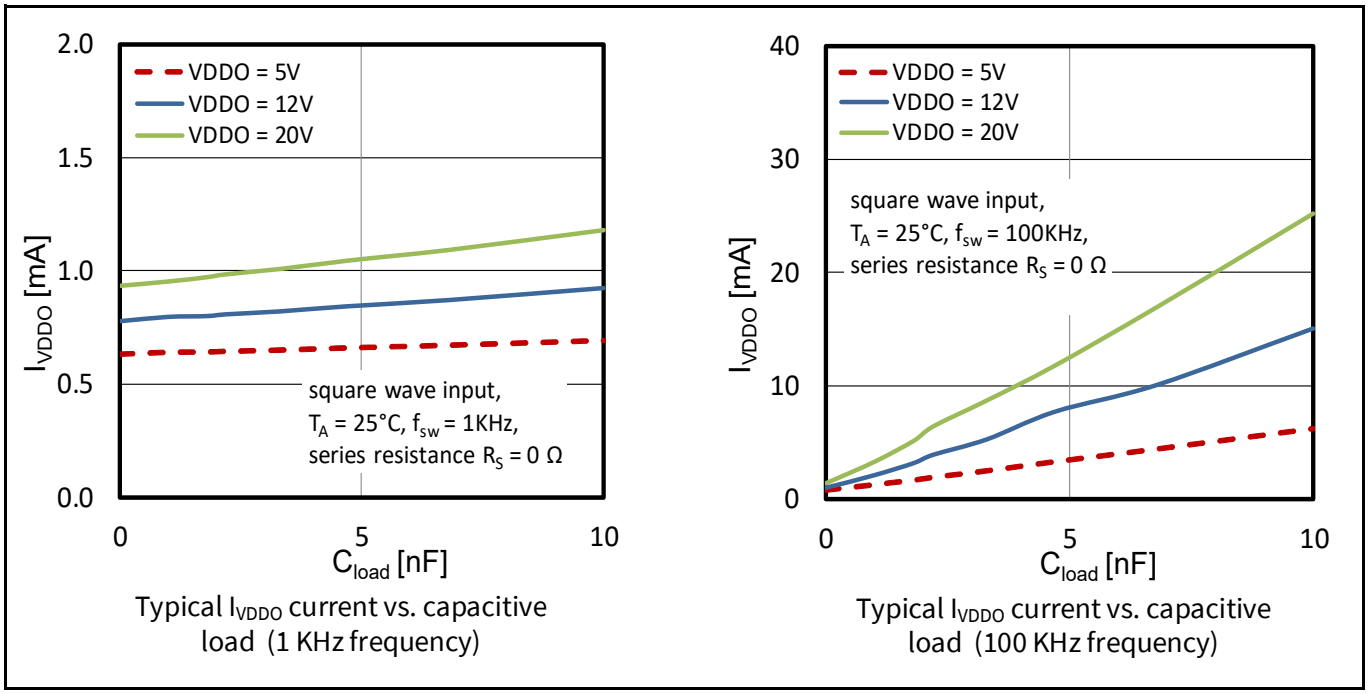
Typical characteristics



Typical I_{VDDO} switching current vs. temperature

Typical I_{VDDO} switching current vs. frequency

Figure 17 Output-side supply current I_{VDDO} (switching current without load)

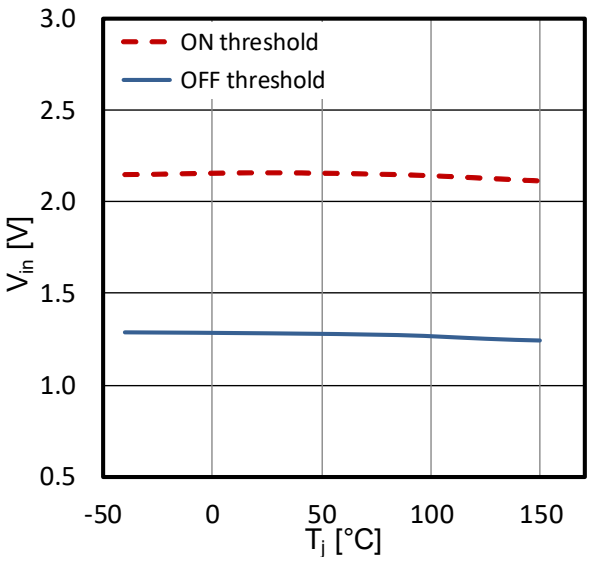


Typical I_{VDDO} current vs. capacitive load (1 KHz frequency)

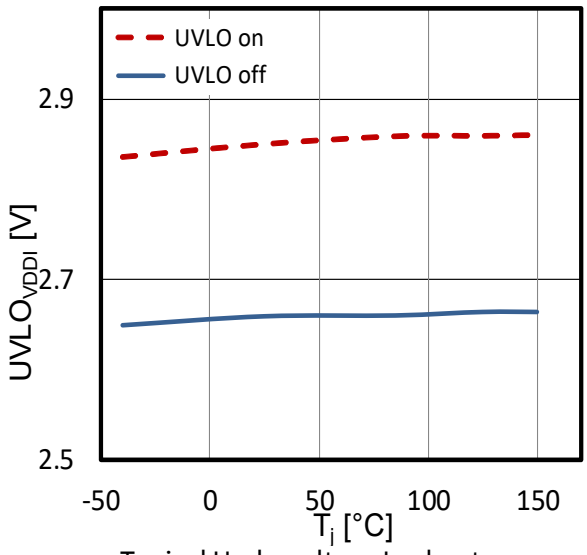
Typical I_{VDDO} current vs. capacitive load (100 KHz frequency)

Figure 18 Output-side supply current I_{VDDO} (switching current with load)

Typical characteristics

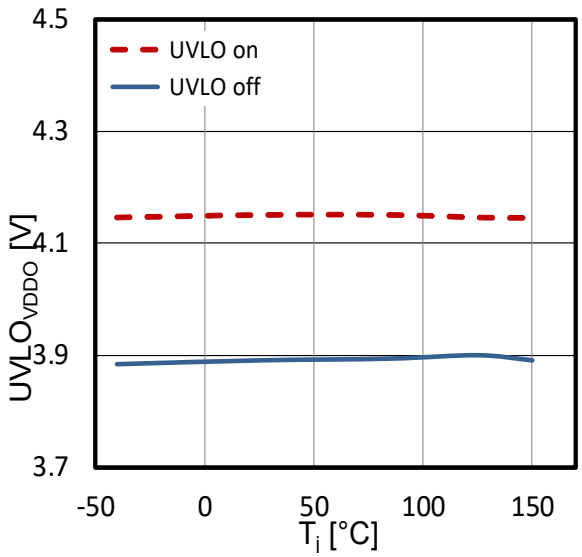


Typical input voltage thresholds vs. temperature

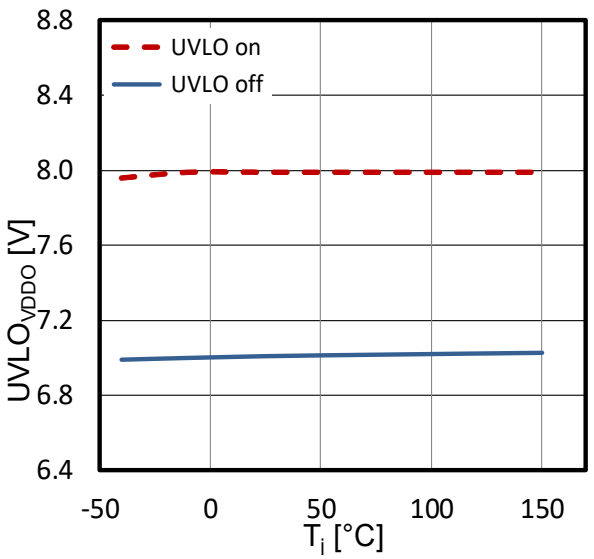


Typical Undervoltage Lockout thresholds VDDI vs. temperature

Figure 19 Logic input thresholds and V_{DDI} UVLO thresholds



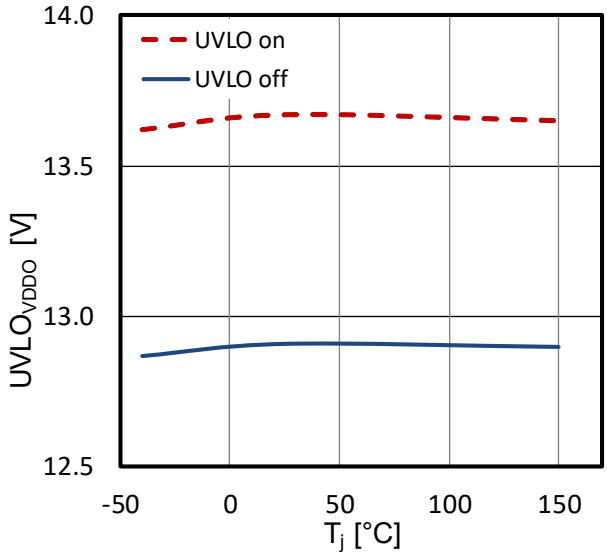
Typical Under Voltage Lockout VDDO thresholds vs. temperature (4 V version)



Typical Under Voltage Lockout VDDO thresholds vs. temperature (8 V version)

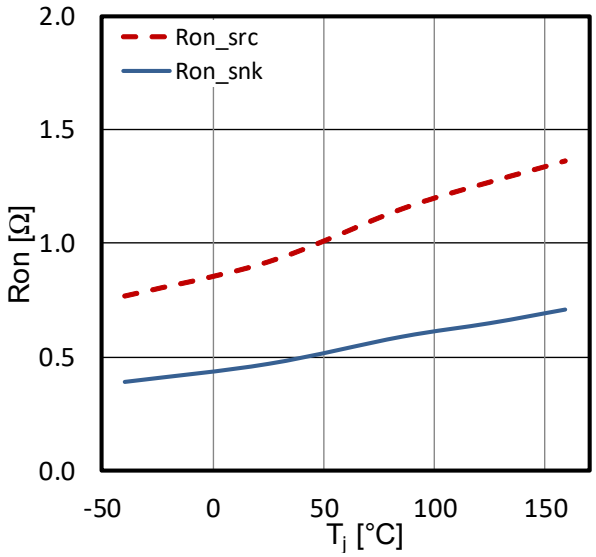
Figure 20 V_{DDO} UVLO thresholds (4 V, 8 V options)

Typical characteristics

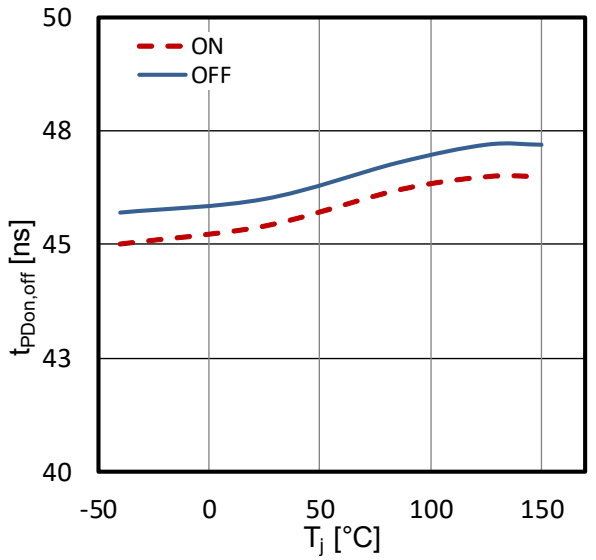


Typical Under Voltage Lockout VDDO thresholds vs. temperature (13 V version)

Figure 21 V_{DDO} UVLO thresholds (13 V options)



Typical output resistance vs. temperature



Typical propagation delay vs. temperature

Figure 22 Output resistance and propagation delay

Typical characteristics

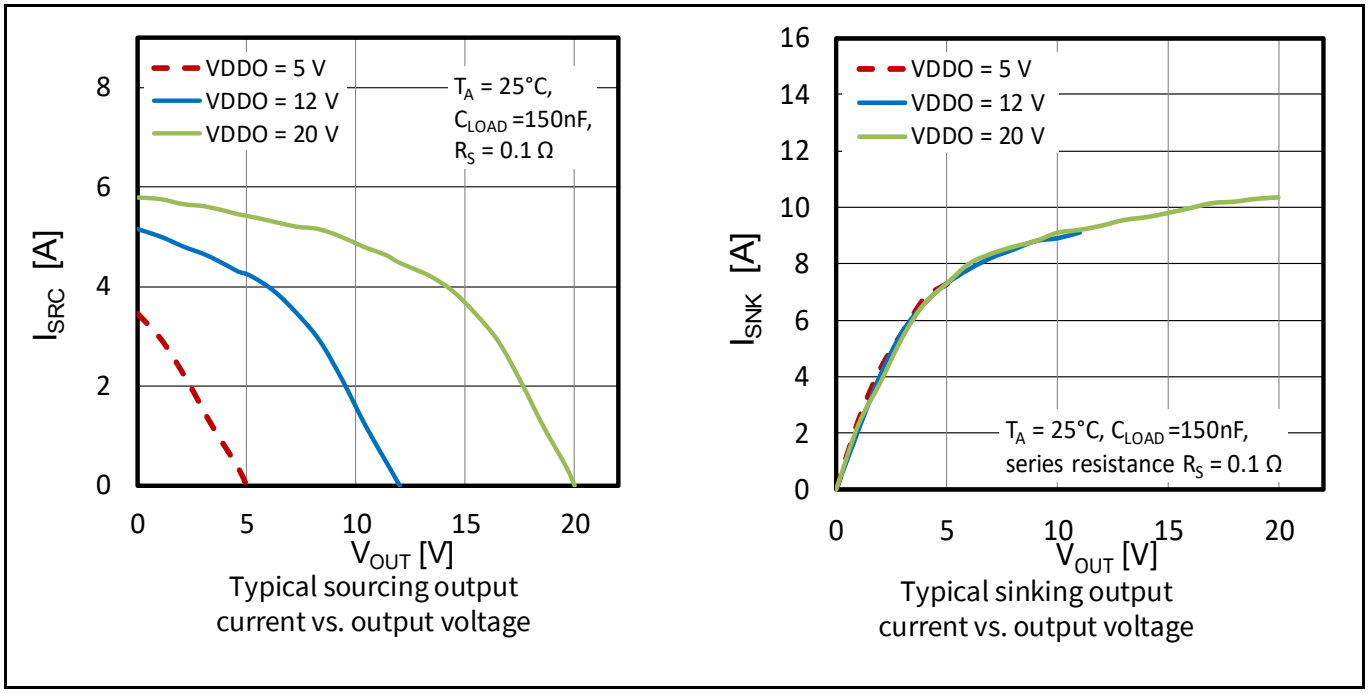


Figure 23 Source and sink current with output voltage

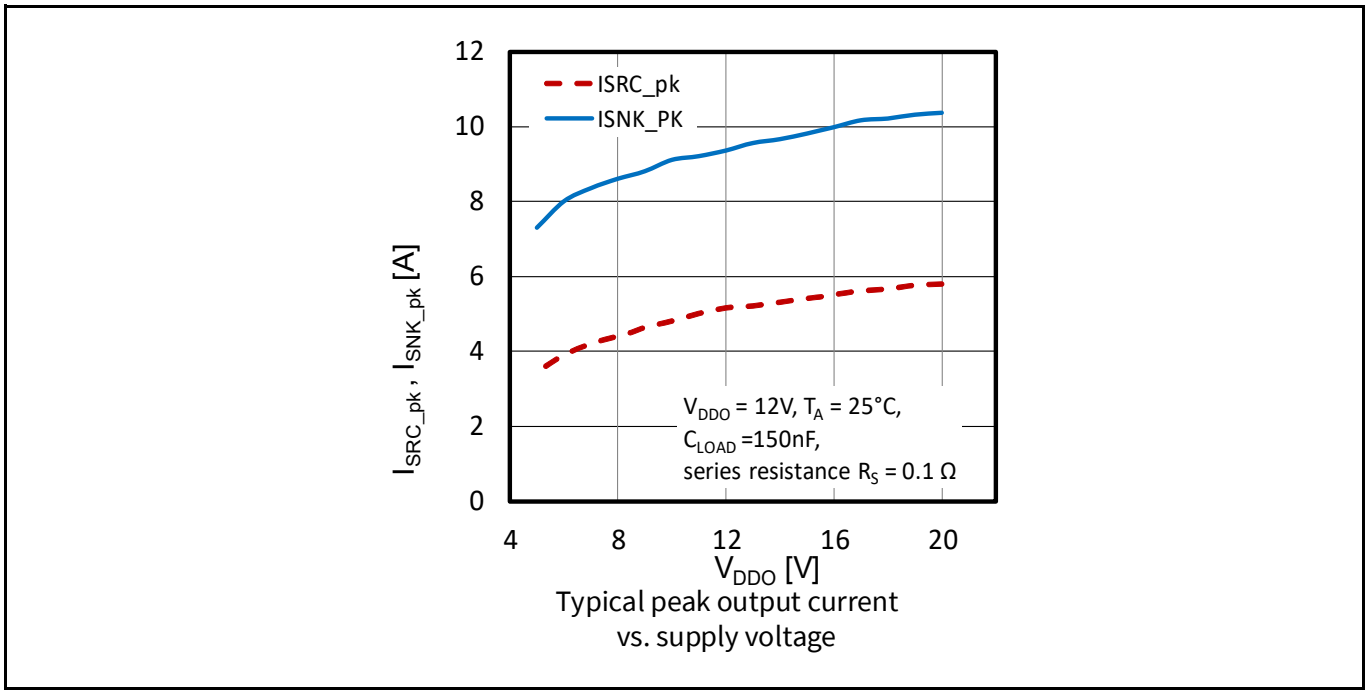


Figure 24 Peak source and sink current with supply voltage

Typical characteristics

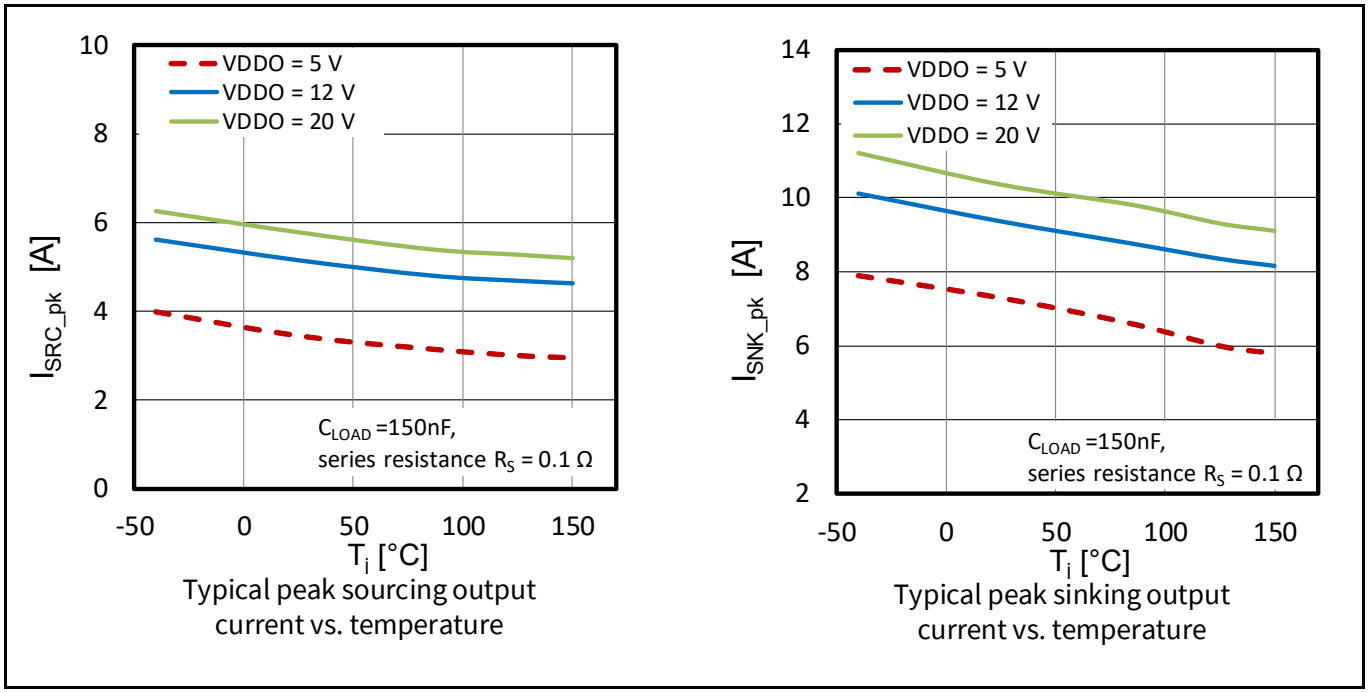


Figure 25 Peak source and sink current with temperature

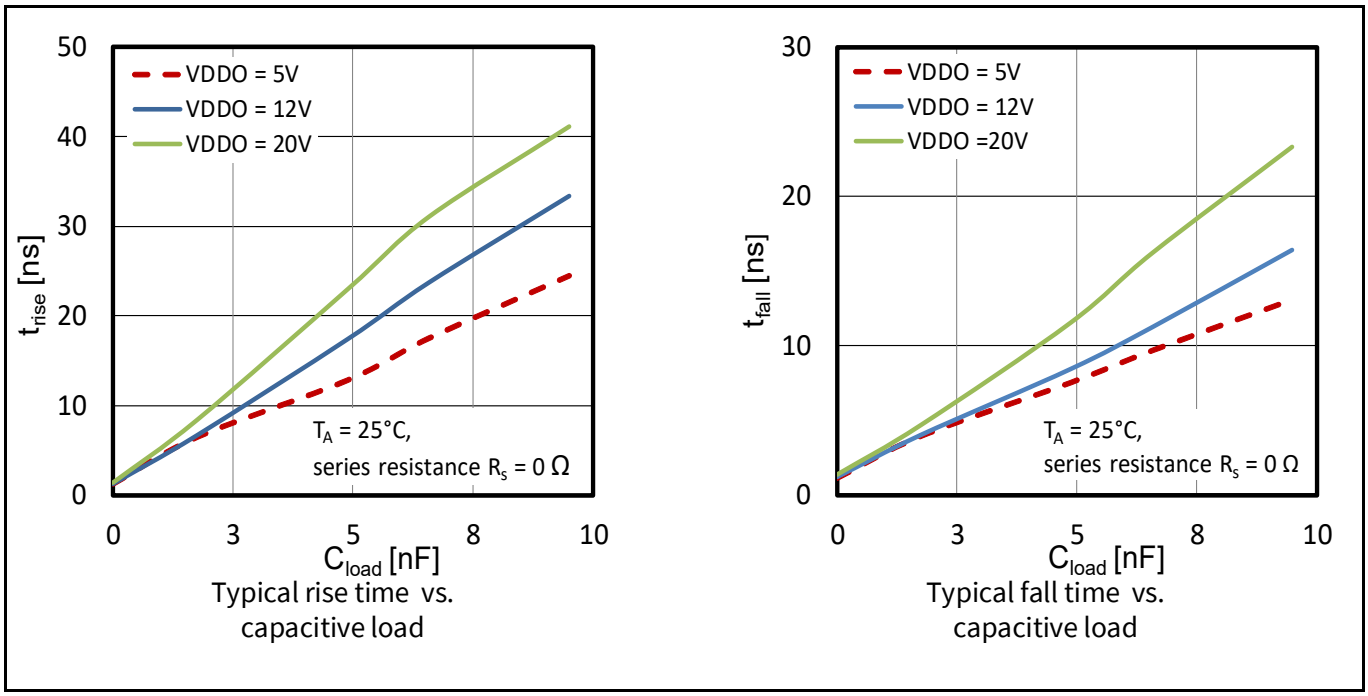
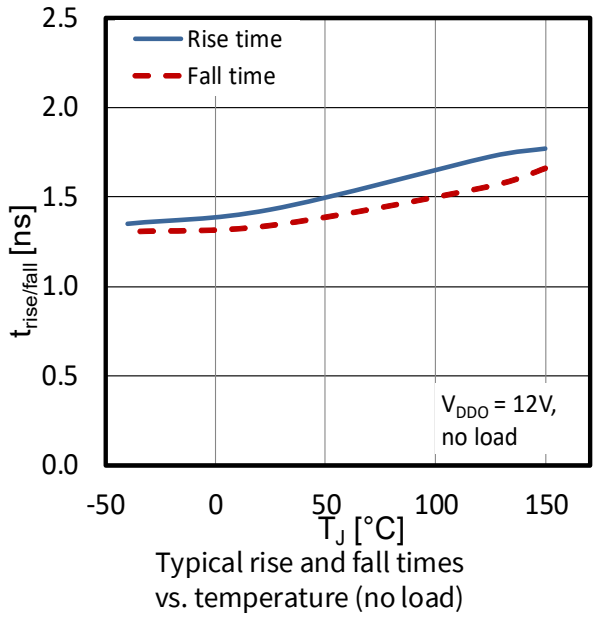


Figure 26 Rise and fall times with capacitive load

Typical characteristics



Typical rise and fall times
vs. temperature (no load)

Figure 27 Rise and fall times with temperature

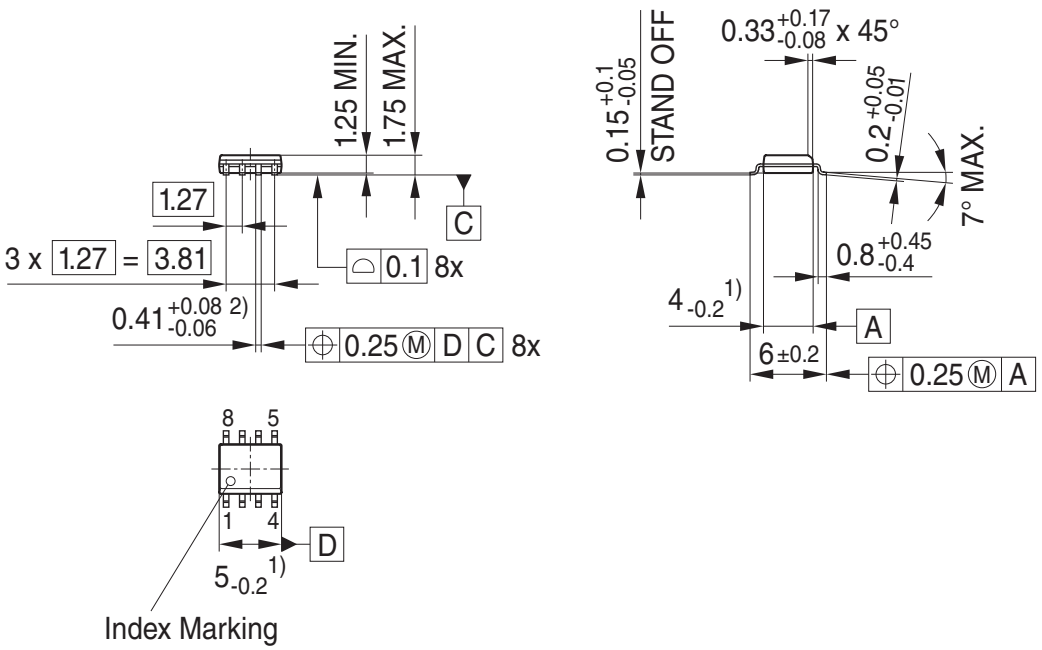
8 Package outline dimensions

8.1 Device numbers and markings

Table 19 Device numbers and markings

Part number	Orderable part number (OPN)	Device marking
1EDB7275F	1EDB7275FXUMA1	1B7275A
1EDB8275F	1EDB8275FXUMA1	1B8275A
1EDB9275F	1EDB9275FXUMA1	1B9275A

8.2 Package PG-DSO-8



1) Does not include plastic or metal protrusion
2) Does not include dambar protrusion of 0.127 max. in excess of the lead width dimension

PG-DSO-8-41, -42, -51, -53, -58-PO V06

Figure 28 PG-DSO-8 outline[1)]

1) Dimensions in mm

Package outline dimensions

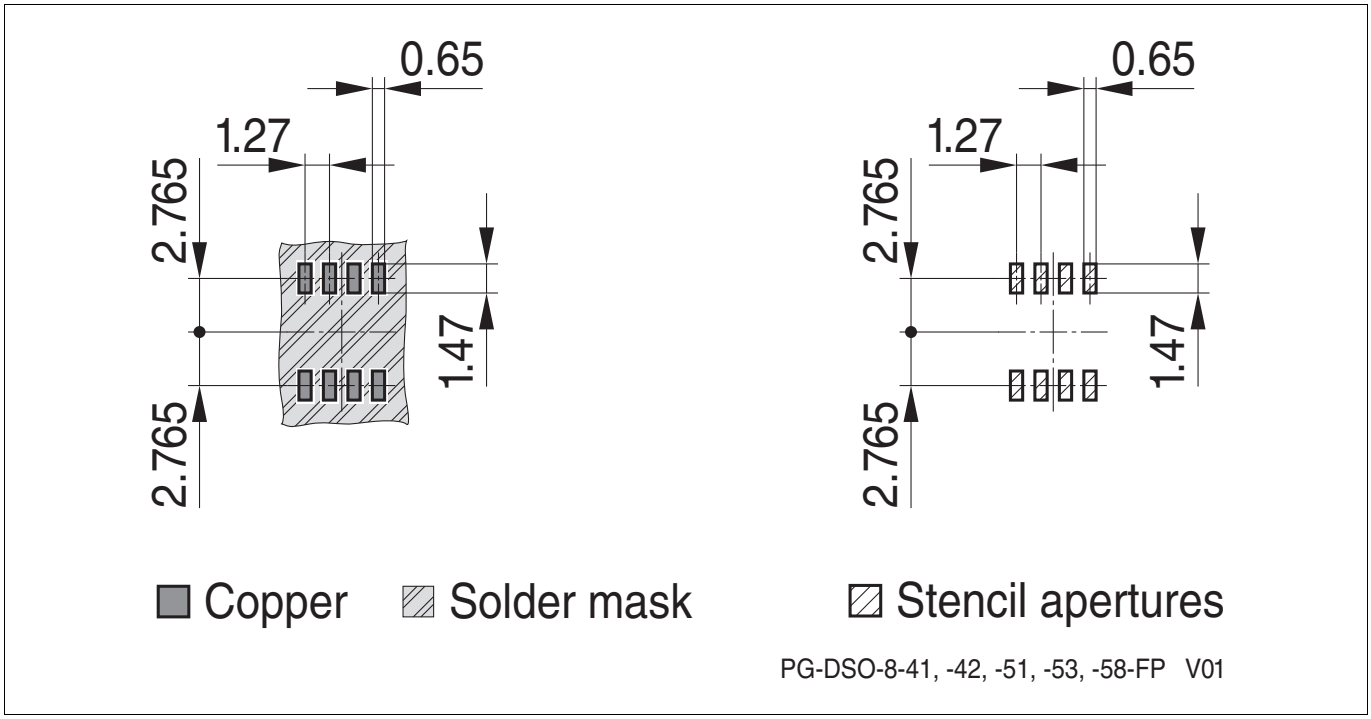


Figure 29 PG-DSO-8 footprint

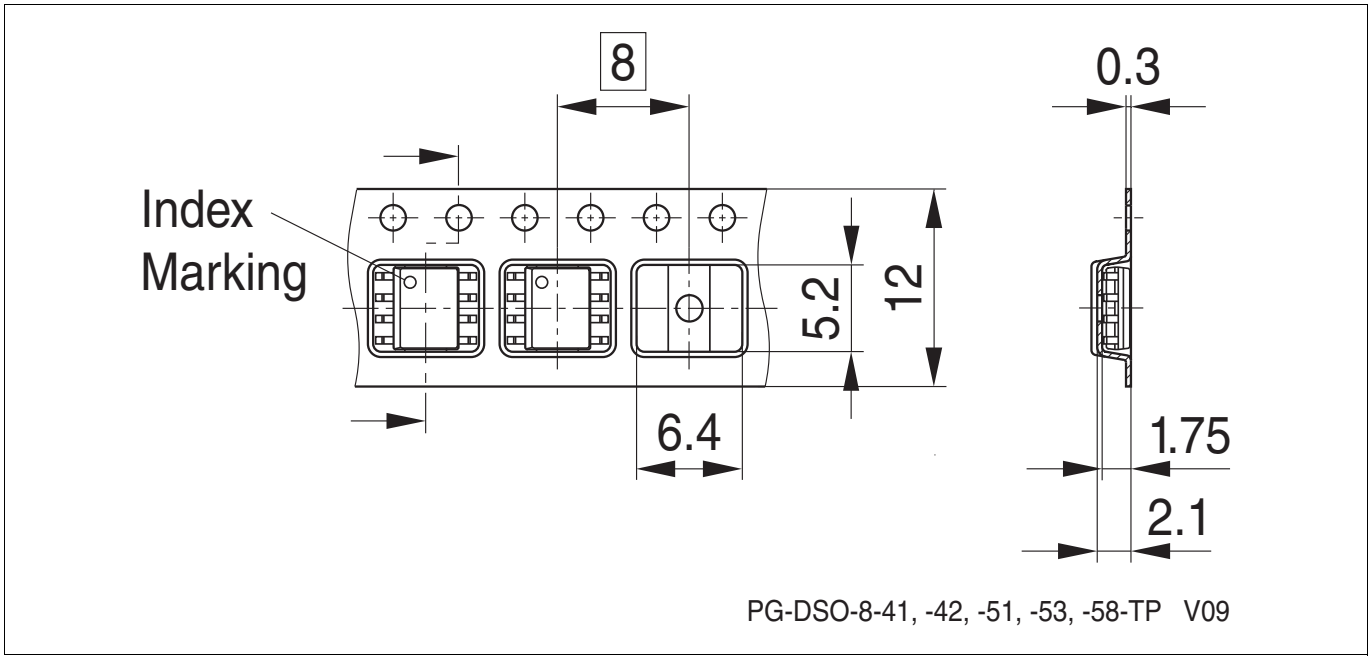


Figure 30 PG-DSO-8 packaging

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

Revision history

Page or Item	Subjects (major changes since previous revision)
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	Final datasheet created

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