EZ-USB™ FX5

USB 5 Gbps peripheral controller

Overview

EZ-USB™ FX5 is a family of USB 5 Gbps peripheral controllers targeting the next-generation USB applications in camera, video, imaging, and data acquisition markets. FX5 consists of dual Arm® Cortex®-M4 and M0+ core CPUs, 512 KB flash, 128 KB SRAM, 128 KB ROM, seven Serial Communication Blocks (SCBs), cryptography accelerator, and high bandwidth data subsystem providing DMA data transfers between LVDS/LVCMOS and USB ports at speeds up to 5 Gbps. An additional 1 MB SRAM is included in the high bandwidth data subsystem to provide buffering for USB data. FX5 also supports USB Type-C plug orientation detection and flip-mux function without the need for external logic.

Features

- USB 3.2 Gen 1 (5 Gbps) device port
  - Integrated 5 Gbps, and 480 Mbps PHYs
  - USB Type-C plug orientation detection and correction
  - Up to 30 USB endpoints, 15 IN and 15 OUT; each end point is configured as bulk, isochronous, or interrupt type
- Dual-core CPU subsystem
  - 150 MHz Arm® Cortex®-M4F (CM4) CPU with single-cycle multiply, floating point (FP), and memory protection unit (MPU)
  - 100 MHz Arm® Cortex®-M0+ (CM0+) CPU with single-cycle multiply and memory protection unit (MPU)
- Memory subsystem
  - 512 KB built-in application flash, read-while-write (RWW) support
  - 128 KB SRAM with power and data retention control
  - 128 KB ROM for device initialization, flash write, security, eFuse programming
  - 1 MB SRAM for LVDS/LVCMOS to USB data buffer
  - 1024 bits one-time programmable (OTP) eFuse array
- Dual-port General Programmable Interface (GPIF III)
  - LVDS/subLVDS multi-lane serial-data bus receiver mode
    - Each port consists of eight data lanes, one control lane, one clock lane, and seven LVCMOS control signals
    - Two ports can be combined into one link of sixteen data lanes
    - Maximum data rate: 1.25 Gbps per lane DDR RX only, 625 Mbps per lane SDR RX only
  - LVCMOS parallel-data bus transceiver mode
    - Each port consists of sixteen data, one clock, and ten control signals
    - Two ports can be combined into one 32-bit wide data bus
    - Maximum 160 MHz DDR or SDR mode for receiver (RX), 100 MHz SDR mode for transmitter (TX), and 80 MHz DDR TX
- Peripheral IO subsystem – total of 48 shared IOs
  - Quad SPI (QSPI) configurable as single, dual, quad, dual-quad, and octal interfaces
  - Seven Serial Communication Blocks (SCBs) configurable as I2C, UART, or SPI
  - Two-channel configurable audio interfaces
    - I2S master or slave, RX or TX
    - Pulse-density modulation (PDM) to pulse-code modulation (PCM) converter for microphone
  - One USB Full Speed (FS) device for virtual communication (COM) function
  - Seven TCPWMs (timers/counters/pulse width modulators)
  - One CAN FD
  - GPIOs: each peripheral IO can be configured as GPIO

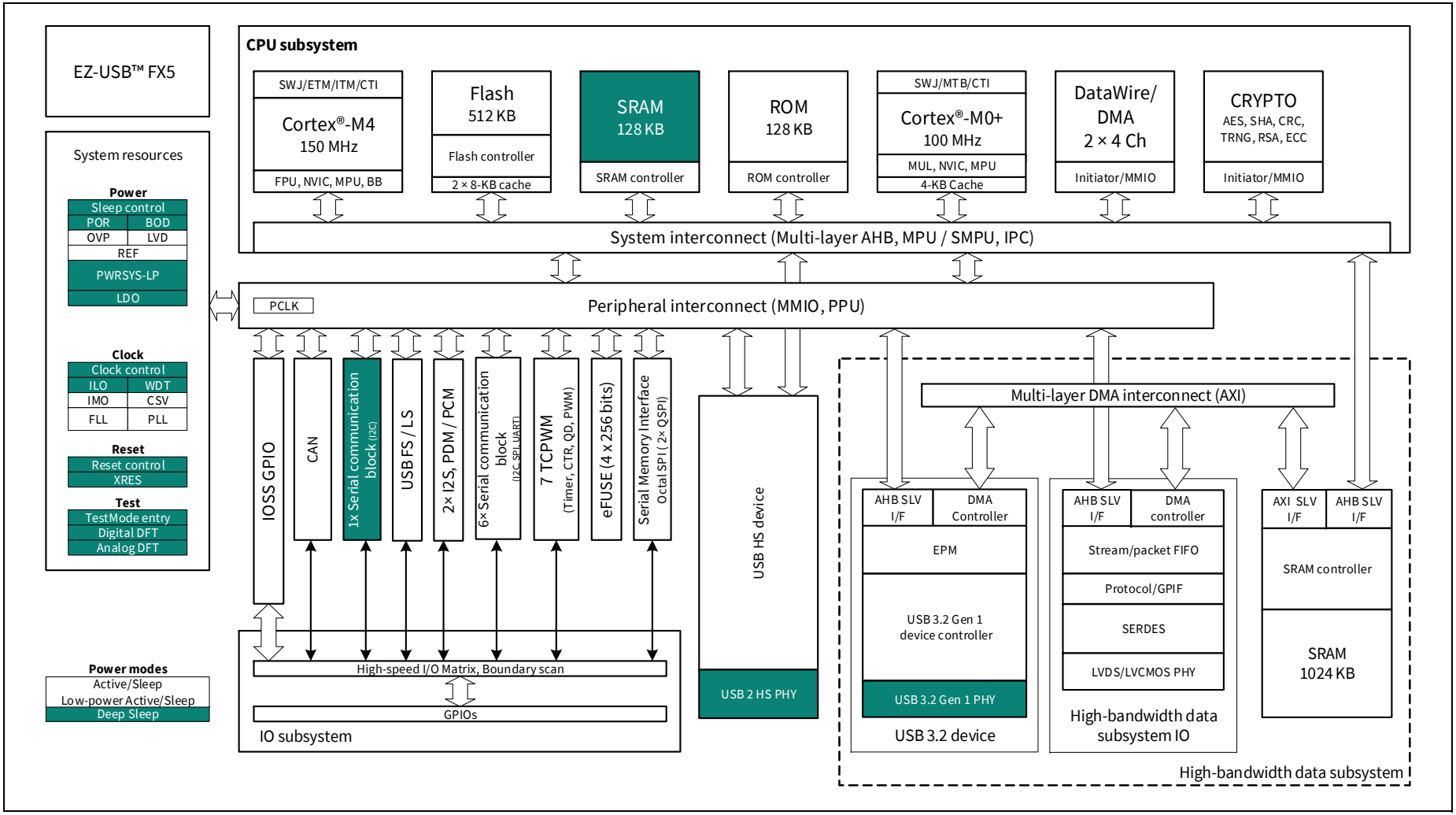
Applications

- Ultra low-power (ULP) with fine-grained power management
  - 1.7 V to 3.6 V operation
  - Deep Sleep mode with SRAM retention
- Flexible clocking options
  - 8 MHz internal main oscillator (IMO) with ±2% accuracy
  - Low-power (LP) 32 kHz internal low-speed oscillator (ILO)
  - 24 MHz external crystal oscillator
  - Phase-locked loop (PLL) for multiplying clock frequency
  - Frequency-locked loop (FLL) for multiplying IMO frequency
  - Integer and fractional peripheral clock dividers
- Security
  - ROM-based root of trust via uninterrupted “Secure Boot”
  - Stepwise authentication of execution images
  - Secured execution of code in the execute-only mode for protected routines
  - All debug and test ingress paths can be disabled
  - Eight protection contexts
  - Cryptography accelerator
    - Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
    - True Random Number Generation (TRNG) function
- Package information
  - 169-ball, 10 × 10 × 1.2 mm, 13 × 13 ball array, 0.75 mm pitch FBGA
- Development tools
  - ModusToolbox™ software enables cross-platform code development with a robust suite of tools and software libraries.
  - Firmware samples including USB3 Vision (U3V) standard, UVC, UAC, HID, CDC, and vendor-specific classes
  - **Infineon developer community** enables connection with fellow EZ-USB™ developers around the world, 24 hours a day, and 7 days a week.

Applications

- Machine vision / industrial cameras
- HDMI/SDI high-bandwidth frame grabbers
- 3D scanners
- Video conference cameras
- Document scanners
- Streaming spectrum analyzer
- Medical Imaging cameras
- High-bandwidth instruments

Block diagram



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1 EZ-USB™ FX5 resources

Table 1 FX5 resources

Resources	Description
Overview	FX5 portfolio, FX5 roadmap
Product selectors	**FX5**
Application notes (AN)	Application notes cover a broad range of topics, from basic to advanced level, and include the following: • FX5 hardware design guidelines • Getting started with FX5 • Developing UVC + UAC based video capture solution using FX5
Code examples	Code examples demonstrate product features and usage, and are also available on GitHub repositories.
FX5 programming specification	FX5 programming specification provides the information necessary to program the FX5 memory.
Development tools	ModusToolbox™ software enables cross-platform code development with a robust suite of tools and software libraries.
Development kits and solution demos	• KIT_FX5_FMC_001: The kit shall use the FX5 controller to stream up to 4K 30fps video from an external camera module seamlessly to USB Host using off-the-shelf FPGA add-on board and camera modules • FX5 CAD libraries provide footprint and schematic symbol support for common tools • BSDL files and IBIS models are also available
Infineon developer community	**Infineon developer community** enables connection with fellow EZ-USB™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated Infineon Community.

2 Functional description

The following sections provide an overview of the features, capabilities, and operation of each functional block identified in the **Block diagram**. For more information, see the following documentation:

- **Board support package (BSP) documentation**

BSPs are available on **GitHub**. They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example here. This search link finds all currently available BSPs on the Infineon **GitHub** site.

- **Peripheral driver library (PDL) Application Programming Interface (API) reference manual**

The PDL integrates device header files and peripheral drivers into a single package and supports all FX5 product lines. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the **PDL API Reference**. Example applications that use the FX5 PDL download it automatically from the GitHub repository.

- **Architecture reference manual**

The architecture reference manual provides a detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

- **Register reference manual**

The register reference manual provides a complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox™ and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

2.1 USB interface

2.1.1 USB 5 Gbps peripheral[1]

FX5 supports the following features:

- Configurable to operate in USB 3.2 Gen 1x1 (5 Gbps)
- Up to 30 endpoints (EPs), 15 IN, 15 OUT; each function endpoint (EP) can be configured as bulk, isochronous, or interrupt type
- Supports simultaneous transactions across multiple IN EPs
- Supports all USB low-power states
- Supports USB precision time measurement (PTM)
- Supports USB bus-powered and self-powered mode
- Detect USB-C connector orientation using CC lines. External Rd resistors are required on CC lines

Note
1. USB certification and compliance are pending.

2.1.2 USB 2.0 high-speed device

The USB HS device will be compliant to USB 2.0 specifications.

The following features are supported in FX5's USB 2.0 HS interface:

- FX5 is pre-programmed with a USB bootloader which allows firmware download over USB 2.0 HS interface. The bootloader will support boot mode selection using PMODE GPIO.
- USB 2.0 HS interface supports firmware download to an external flash using SPI/QSPI interface as well

2.1.3 Compliance to USB 2.0 DC resistance ECN

The ECN updates the USB 2.0 specification to account for DC resistance (DCR) on the D+ and D– data paths between the USB transceiver device and the connector. This increased resistance could be due to multiple crossbar switches and/or passive components such as common-mode chokes. The ECN updates affect the following high-speed parameters: VHSOH transmit voltage, VHSDSC disconnect level, and VHSSQ squelch level.

2.1.3.1 Allowable transmit output voltage (VHSOH)

The ECN expands the allowable TX output voltage from 400 mV ± 10% to 360 mV to 625 mV. FX5 supports the default transmit voltage of 400 mV and a programmable nominal range of 370 mV to 520 mV.

2.1.3.2 Disconnect envelope detector threshold voltage (VHSDSC)

The ECN changes the disconnect envelope detector threshold range from 525 mV to 625 mV to a much wider range. The design guide shows a minimum threshold range of 550 mV to 640 mV to a maximum of ~820 mV to ~950 mV. FX 20 supports programmable threshold levels that cover the original 525 mV to 625 mV range up to the maximum range of ~820 mV to ~950 mV.

2.1.3.3 Squelch threshold voltage (VHSSQ)

The ECN changes the squelch threshold from 100 mV to 150 mV to a lowered range depending on the DCR. FX5 supports the original threshold range of 100 mV to 150 mV and can be programmed to a lowered threshold range of 85 mV to 135 mV.

FX5 also supports multiple programmable options for pre-emphasis which can be used to compensate for increased DCR and other components that cause channel degradation.

2.1.4 Renumeration

FX5 has a soft configuration, where one chip can take on the identities of multiple distinct USB devices. When first plugged into USB, FX5 enumerates automatically with the vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and reconnect. FX5 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called "ReNumeration", happens instantly when the device is plugged in.

2.1.5 Precision time measurement (PTM)

When multiple devices are connected to the same host, it is necessary for them to have a common sense of time based on the host specified timestamp to avoid deviations due to different propagation delays. The precision time measurement (PTM) provides a mechanism for the device to estimate the link and hub propagation delays to compensate for this deviation. For more details, see the architecture reference manual.

2.2 High-bandwidth data subsystem

The high-bandwidth data subsystem provides DMA data transfers between LVDS / LVCMOS IO subsystem and the USB 3.2 Gen 1 device at speeds up to 5 Gbps. A 1-MB SRAM is included in the high bandwidth data subsystem to provide buffering for data. The data is transferred over an AXI3 interconnect. This subsystem interfaces to the System Interconnect for data transfer to other low-bandwidth peripherals and the memory-mapped IO (MMIO) Interconnect.

The high-bandwidth data subsystem IOs can be configured as LVDS or LVCMOS interfaces.

It has two links and each link can be configured independently to support the LVDS interface or LVCMOS parallel interface.

2.2.1 LVDS interface

The LVDS interface supports only RX and can be configured to support one of the following modes:

- Two links with 1, 2, 4, or 8 data lanes, 1 control lane, 1 clock lane or one wide link with up to 16 data lanes, 1 control lane, and 2 clock lanes. The same clock has to be fed to both clock lanes.
- The gearing ratios: 1:1, 2:1, 4:1, and 8:1 are supported on each configuration of the link. Gearing ratio indicates the number of bits transferred, per data lane, per clock on the interface.
- The LVDS interface supports a clock from 74.25 MHz to 625 MHz
- The LVDS interface supports a maximum data rate of 1.25 Gbps, so at 625 MHz, only gear ratios of 1:1 and 1:2 can be used
- Each LVDS link has seven LVCMOS control signals of which 3 are input only and other 4 are input/output control signals

Note: For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can work in the entire 1.8 V or 3.3 V range depending on the desired CTRL signal logic level.

The LVDS subsystem has a programmable protocol layer with the following features:

- Supports two independent links
- Combines data from both links

Each independent link supports the following:

- Deserialize data
- Data on the same link can be routed to different sockets and therefore on different endpoints or streams (in the case of Bulk Stream enabled endpoints). This is supported subject to the limitation on the number of sockets (16 per port for narrow link and 32 in case of wide link).
- Supports GPIF III-based programmable state machine (256 states). For more details, see the architecture reference manual.
- GPIF III state machine has access to all the control signals (LVCMOS control signal and control signals on LVDS control lane) of the link. For more details on control signals, see the architecture reference manual.
- Generate configurable test patterns (for example, color bar) that can be used to test streaming of data from FX5 to PC without using any external video source

The LVDS-RX has the following low-power mode entry and exits:

- L0: Active state in which all configured data lanes, one control lane, and clock lanes are active. It should be noted that one clock lane is used for links with up to 8 data lanes and two clock lanes for the wide link (with 16 data lanes). In this state, FPGA is actively transmitting clock, control, and data lanes and FX5 is receiving them. In this active state, when FPGA has no valid data to send, FPGA can send IDLE control bytes and data lanes can carry any data. The data on data lanes will be discarded by the LVDS port when the control lane has an IDLE control byte.
- L1: A low power state in which FX5 LVDS receivers on data lanes are powered down (clock and control lanes continue to be active in L1)

- L2: Not defined
- L3: A low-power state in which FX5 LVDS receivers on all (data, control, and clock) lanes are powered down

2.2.1.1 Link initialization

- On power-up, FX5 CPU does the programming of all registers, including the LVDS-RX block
- After FX5 is powered up, firmware enables and configures its LVDS-RX block and is ready to receive training data
- When FX5 is ready to receive training data, it asserts a link-ready (LINK_RDY) indication to LVDS transmitter device (LVDS-TX) such as FPGA via I2C, SPI, or control signals indicating LVDS-TX should transmit the clock and training sequence for 50 µs (PHY_TS_TIME) before sending data within PHY_TS_TIME, PLL and DLL locks
- FX5 CPU waits for LINKx_TRAINING_DONE interrupt bit(s) to confirm that LVDS-TX is ready for operation. Note both bits need to be set for wide link configuration.
- LVDS-TX may send out a clock and training sequence as soon as LVDS-TX powers up even before LINK_RDY

2.2.1.2 Port - 0/Port - 1 link training

- LVDS-TX must send a training sequence to FX5's LVDS-RX for PLL lock, lane, and link alignment. After FX5's LVDS-RX block is enabled or exit from LVDS lower-power modes, LVDS-TX must send the link training sequence on all the lanes of the link before sending data. The control lane is used to identify the training sequence, from other types of data transmitted on the data lanes.
- The training sequence must be sent by LVDS-TX as a repeated 8-bit training pattern (TS_Pattern). The 8-bit training pattern is programmable on the LVDS-RX side (within FX5).
- LVDS-TX must send the training sequence for a minimum training time (TS_Time) of around 50 µs from Link-ready
- After trained, the link does not need to be trained until the clock is stopped by LVDS-TX or the next low-power mode exit or LVDS-RX re-enable. LVDX-RX does not provide acknowledgment to indicate training completion back to LVDS-TX.
- For links on port 0 or port 1 up to 8 data lanes wide, after sending the training sequence for TS-time, LVDS-TX can start transmitting frame data or data packet immediately after sending the training sequence. LVDS-RX PLL-lock and lane-alignment are achieved within TS_Time.
- There is no bit-error-rate on LVDS links. LVDS link is susceptible to abnormal EMI

2.2.1.3 Wide-link training

For a wide-link that spans both ports, port 0 and port 1, for the purposes of link-alignment, LVDS-TX is required to send a block of 64 bytes as described below.

- On wide-link spanning port 0 and port 1, the LVDS-TX is required to send a link training block after sending the PHY training sequence
- The link training block is used to align the data lanes on Port 0 and Port 1
- The link training control byte, TRBLK (0x71), identifies that the link training block is present on data lanes for wide-link configuration
- Non-wide-link configurations do not require a link training sequence

The link training block consists of a 4-byte (P3, P2, P1, P0) sequence on each of the data lanes L15 through L0 and the control lane having TRBLK (0x71) as shown in **Table 2**.

Table 2 Wide-link training block

Data lane	Control lane TRBLK (0x71)			
L0	P0	P1	P2	P3
L1	P0	P1	P2	P3
L2	P0	P1	P2	P3
L3	P0	P1	P2	P3
L4	P0	P1	P2	P3
L5	P0	P1	P2	P3
L6	P0	P1	P2	P3
L7	P0	P1	P2	P3
L8	P0	P1	P2	P3
L9	P0	P1	P2	P3
L10	P0	P1	P2	P3
L11	P0	P1	P2	P3
L12	P0	P1	P2	P3
L13	P0	P1	P2	P3
L14	P0	P1	P2	P3
L15	P0	P1	P2	P3

2.2.2 LVCMOS parallel interface

The LVCMOS parallel interface supports two links each with RX and TX interface. Each link contains sixteen LVCMOS IOs and seven control signals. The maximum data rate on each LVCMOS IO is:

- 160 MHz for SDR and DDR in RX mode
- 100 MHz SDR only in TX mode
- 80 MHz DDR in TX mode

The following lists the maximum frequency that the seven control signals can operate:

- **LVDS mode:** Input or Output mode at a maximum of 5 MHz
- **LVCMOS SDR at 160 MHz:** A maximum of four out of seven control signals can operate up to a maximum of 80 MHz input/output toggle rate
- **LVCMOS SDR at 100 MHz:** All seven control pins can operate up to a maximum of 50 MHz
- **LVCMOS DDR at 160 MHz:** A maximum of four out of seven control pins can operate up to a maximum of 80 MHz
- **LVCMOS mode:** P0CTL7/8/9 and P1CTL7/8/9 control signals are restricted to be used only in the Input mode

2.2.3 GPIF III interface

The GPIF III is a programmable state machine that enables a flexible interface that may function as a master or slave in industry-standard or proprietary interfaces. Only parallel interfaces are implemented with GPIF III.

The following are the GPIF III features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit, 16-bit, 24-bit, and 32-bit parallel data bus
- Supports two independent instances of GPIF III state machines, each connected to a link, or a single GPIF III state machine (first instance) connected to a wide link

The GPIF III state transitions are based on control input signals. The control output signals are driven as a result of the GPIF III state transitions. For more details, see the architecture reference manual.

2.2.4 High-bandwidth direct memory access (HB-DMA)

The DMA controller includes the following features:

- Supports multiple simultaneous streams
- Supports maximum throughput of 5 Gbps
- DMA is configurable by the CPU. Once configured, the DMA operates automatically and transfers the video stream from the LVDS/LVCMOS interface to the USB 3.2 device without CPU intervention.
- Adds headers and footers with every data packet (payload) without CPU intervention

2.2.5 Internal pattern generator

In this mode, only DMA layer and link layer logic are validated. For PHY validation, there is a separate PHY loopback mode. Here cross connections between port0 and port1 are done at link layer interface signals.

Purpose of this loopback is to provide a mechanism for software to validate general peripheral interface finite state machine (GPIF FSM) programming for various protocols, on customer board, without applying stimulus on IO pins.

The control signals and data to be driven on to the link interface is controlled by loopback program stored in HBWSS SRAM. Format and fields of loopback programming stored in HBWSS SRAM is captured in **Table 3**.

- Each instruction of loopback program is of 128-bits
- Loopback program shall be stored in HBWSS SRAM, using socket/descriptor/buffer mechanism
- CPU populates SRAM with required loopback program
- CPU programs any relevant configuration registers, GPIF FSMs and triggers loopback testing
- Thread 1 or Thread 3 shall execute loopback program. Hence in loopback mode thread 1 and 3 cannot be used by GPIF FSM.

There are different combinations of link-layer loopback:

- Port-0 under test
  - CPU shall setup Thread 3/Socket 31 as consumer socket and associate loopback program to this socket
  - GPIF-1 FSM will be setup to read loopback program and apply loopback stimulus to port-0 link-layer interface
  - GPIF-0 FSM will be setup to work on loopback stimulus and push data to producer socket/descriptor/buffer
- Port-1 under test
  - CPU shall setup Thread 1/Socket 15 as consumer socket and associate loopback program to this socket
  - GPIF-0 FSM will be setup to read loopback program and apply loopback stimulus to port-1 link-layer interface
  - GPIF-1 FSM will be setup to work on loopback stimulus and push data to producer socket/descriptor/buffer
- Wide port under test – not supported

Table 3 Loopback fields

Field	Width	Bit position	Comments
VLD	1	0	Indicates that loopback program entry in HBWSS SRAM is valid.
START	1	1	Indicates start of loopback program. This should be the first line of loopback program. When this is set, only DATA_MODE field is valid.
END	1	2	Last entry of loopback program
Reserved	1	3	Reserved
DATA_MODE	4	7:4	This field is valid only when START field is set. This indicates the interface mode of this loopback program. 3'b000 – LVDS mode 3'b010 – LVCMOS SDR mode 3'b011 – LVCMOS DDR mode 3'b100 – Enhanced LVCMOS SDR mode 3'b101 – Enhanced LVCMOS DDR mode
REPEAT_CNT	12	19:8	Decides for how many interface clock cycles, the control and data read from current instruction has to be repeated.
DATA_SRC	2	21:20	This field is relevant only when REPEAT_CNT is greater than '1'. 2'b00 – repeat data of current instruction for REPEAT_CNT times 2'b01 – increment least significant byte (LSB) 8-bits of data read from current instruction, every cycle by 1 and apply on interface in next cycle. Repeat this for REPEAT_CNT cycles. Here same 8-bits of data is applied on all valid data bus width.
Reserved	10	31:22	Reserved
CTRL_BYTE	8	39:32	Control byte to be applied on link-layer interface. Valid only for LVDS or enhanced LVCMOS mode.
Reserved	4	43:40	Reserved
CTRL	20	63:44	Control signals to be applied on link-layer interface. Out of 20-bits, LSB 10-bits are for port-0 and MSB 10-bits are for port-1. In case of widelink, all 20-bits are meant for port-0 only.
Data	64	127:64	Maximum 64-bits of data can be stored in a single instruction, which is sufficient for a narrow port. In case of widelink, 128-bits of data is needed, hence same 64-bit data is repeated 2x and applied on link-layer data interface. If bus width is < 64-bits, then only LSB 'bus width' bits of 64-bit are used and rest of data bits are ignored. If DATA_SRC is set to 2'd0, then data read from current instruction is applied to interface for REPEAT_CNT times. If DATA_SRC is set to 2'd1, then LSB 8-bits of data read from current instruction is incremented by INC_STEP(=1) and applied to interface. Same 8-bit data is copied on to all bits of valid bus width.

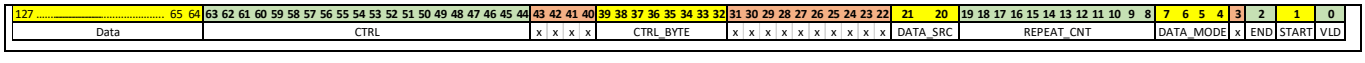


Figure 1 Loopback data packet

2.3 CPU and memory subsystem

The CPU subsystem has the following major components:

- 150 MHz Cortex®-M4 core
- 100 MHz Cortex®-M0+ core
- 512 KB flash memory
- 128 KB SRAM
- 128 KB ROM
- DMA
- Cryptography accelerator

Following are the multiple bus masters in FX5 (see **Block diagram**):

- CPUs
- DMA controllers
- QSPI
- USB
- Cryptography accelerator

Generally, all the memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm® AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

2.3.1 CPUs

There are two Arm® Cortex® CPUs:

- The Cortex®-M4 (CM4) has a single-cycle multiply, a floating point unit (FPU), and a memory protection unit (MPU). It can run up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.
  CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the **Arm®v7-M Architecture Reference Manual**).
- The Cortex®-M0+ (CM0+) has a single-cycle multiply and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Therefore, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

CM0+ is the secondary CPU; it is used to implement system calls and device-level safety and protection features. CM0+ provides a secured, uninterruptible boot function. This helps ensure that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Arm®v6-M Thumb instruction set (defined in the **Arm®v6-M Architecture Reference Manual**).

The CPUs have the following power draw, at VDDD = 3.3 V:

Table 4 Active current slope at VDDD = 3.3 V, using the internal LDO regulator

System power consumption	
CPU	**LP mode**
Cortex®-M0+	28 µA/MHz
Cortex®-M4	40 µA/MHz

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm®.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. FX5 has a debug access port (DAP) that acts as the interface for device programming and debugging. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers the following debug and trace features:

- CM4 supports
  - Six hardware breakpoints and four watchpoints
  - 4-bit embedded trace macrocell (ETM)
  - Serial wire viewer (SWV)
  - Printf()-style debugging through the single wire output (SWO) pin
- CM0+ supports
  - Four hardware breakpoints and two watchpoints
  - A micro trace buffer (MTB) with 4-KB dedicated RAM

Additionally, FX5 has an embedded cross trigger for synchronized debugging and tracing of both CPUs.

2.3.2 Interrupts

FX5 has 168 system and peripheral interrupt sources, and supports interrupts and system exceptions on both CPUs. CM4 has 168 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has eight interrupts IRQ[7:0] with configurable mapping of one or more interrupt sources to any of the IRQ[7:0]. CM0+ also supports eight internal (software-only) interrupts.

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). Up to four system interrupts can be mapped to each of the CPUs’ non-maskable interrupts (NMI). Up to 39 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. See the architecture reference manual for more details.

2.3.3 Inter-processor communication (IPC)

In addition to the Arm® SEV and WFE instructions, a hardware IPC block is included. It includes 16 IPC channels and 16 IPC interrupt structures. The IPC channels can be used to implement data communication between the processors. Each IPC channel also implements a locking scheme which can be used to manage shared resources. The IPC interrupts let one processor interrupt the other, signaling an event. This is used to trigger events such as notify and the release of the corresponding IPC channels. Some IPC channels and other resources are reserved, as shown in **Table 5**.

Table 5 Distribution of IPC channels and other resources

Resource available	Resources consumed
IPC channels, 16 available	Eight reserved
IPC channels, 16 available	Eight reserved
Other interrupts	One reserved
CM0+ NMI	Reserved
Other resources: clock dividers, DMA channels, and so on	One CM0+ interrupt MUX

2.3.4 Direct memory access (DMA) controllers

FX5 has three DMA controllers, which support CPU-independent access to memory and peripherals. Two of them have 29 channels each and the third has four channels. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors is limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. See the Reference manual for more details.

2.3.5 Cryptography accelerator

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The cryptography subsystem supports the following:

- Encryption/Decryption functions
  - Data Encryption Standard (DES)
  - Triple DES (3DES)
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
  - Elliptic Curve Cryptography (ECC)
  - RSA cryptography functions
- Hashing functions
  - Secure Hash Algorithm (SHA)
  - SHA-1
  - SHA-224/-256/-384/-512
- Message authentication functions (MAC)
  - Hashed message authentication code (HMAC)
  - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random Number Generators
  - Pseudo Random Number Generator (PRNG)
  - True Random Number Generator (TRNG)

2.3.6 Protection units

This product line has multiple types of protection units to control erroneous or unauthorized access to memory and Peripheral registers. CM4 and CM0+ have Arm® MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement protection for memory resources that are shared among multiple bus masters. The peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space. Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secured/non-secured, and protection context. The protection units are configured at boot to control access privileges and rights for bus masters and peripherals. Up to eight protection contexts (boot is in protection context 0) allow access privileges for memory and system resources to be set by the boot process per protection context by bus master and code privilege level. Multiple protection contexts are available.

2.3.7 Memory

FX5 contains flash, SRAM, ROM, and eFuse memory blocks.

2.3.7.1 Flash

There is up to 512 KB of internal application flash. There are also two 32-KB flash sectors:

- Auxiliary flash (AUXflash): used for EEPROM emulation
- Supervisory flash (Sflash): Data stored in Sflash includes device trim values, **Flash boot** code, and encryption keys. After the device transitions into the “Secure” lifecycle stage, Sflash can no longer be changed.

The flash has 128-bit-wide accesses to reduce power. Write operations can be performed at the row level. A row is 512 bytes. The flash controller has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

2.3.7.2 SRAM

Up to 128 KB of SRAM is provided. The SRAM bank provides control over power modes to manage power consumption. Power control and retention granularity are configurable in four 32-KB regions. For normal operation, the SRAM regions can be enabled or disabled to save power. For Deep Sleep mode, the regions can also be configured to retain data.

2.3.7.3 ROM

The 128 KB ROM, also referred to as the supervisory ROM (SROM), provides code (**ROM boot**) for several system functions. The ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU or the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

2.3.7.4 eFuse

A one-time-programmable (OTP) eFuse array consists of 1024 bits, of which 648 bits are reserved for system use such as die ID, device ID, initial trim settings, device life cycle, and security settings. The remaining bits are available for storing key information, hash values, unique IDs, or similar custom content.

Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of ‘0’ to ‘1’. To program an eFuse, VDDD must be at 2.5 V ±5%, at 14 mA.

Because blowing an eFuse is an irreversible process, programming is recommended only in mass production under controlled factory conditions. For more information, see FX5 programming specifications.

2.3.8 Boot code

Two blocks of code, ROM boot, and flash boot are preprogrammed into the device and work together to provide device startup and configuration, basic security features, lifecycle stage management, and other system functions.

2.3.8.1 ROM boot

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Integrity checks of flash boot code
- Device trim setting (calibration)
- Setting the device protection units (DPU)
- Setting device access restrictions for the “Secure” lifecycle states ROM cannot be changed and acts as the root of trust in a secured system

2.3.8.2 Flash boot

The flash boot is firmware stored in SFlash that ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

Flash boot:

- Is validated by ROM boot
- Runs after ROM boot and before the user application
- Enables system calls
- Configures the DAP
- Launches the user application

If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state.

2.3.9 Memory map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the Arm®-defined regions shown in **Table 6**. Note that code can be executed from the code and external RAM regions.

Table 6 Address map for CM4 and CM0+

Address range	Name	Use
0x0000 0000 to 0x1FFF FFFF	Code	Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0.
0x2000 0000 to 0x3FFF FFFF	Reserved	Reserved
0x4000 0000 to 0x5FFF FFFF	Peripheral	All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in FX5.
0x6000 0000 to 0x9FFF FFFF	External RAM	Quad SPI, (see the **Quad SPI/serial memory interface (SMIF)** section). Code can be executed from this region.
0xA000 0000 to 0xDFFF FFFF	External Device	Not used
0xE000 0000 to 0xE00F FFFF	Private Peripheral Bus	Provides access to peripheral registers within the CPU core
0xE010 0A000 to 0xFFFF FFFF	Device	Device-specific system registers

The device memory map shown in **Table 7** applies to both CPUs. That is, the CPUs share access to all FX5 memory and peripheral registers.

Table 7 Internal memory address map for CM4 and CM0+

Address range	Memory type	Size
0x0000 0000 to 0x0001 FFFF	ROM	128 KB
0x0800 0000 to 0x0801 FFFF	SRAM	128 KB
0x1000 0000 to 0x1007 FFFF	Internal application flash	Up to 512 KB
0x1400 0000 to 0x1400 7FFF	Auxiliary flash, can be used for EEPROM Emulation	32 KB
0x1600 0000 to 0x1600 7FFF	SFlash	32 KB
0x1C00 0000 to 0x1C0F FFFF	High bandwidth DMA buffer SRAM	Up to 1 MB

Note that FX5 SRAM is located in the Arm® Code region for both CPUs (see **Table 6**). There is no physical memory located in the CPUs' Arm® SRAM regions. Only the data that is placed in the DMA Buffer SRAM can be transferred across the USB 3.2 interface. This region can be used for data and volatile code segments as well.

2.4 System resources

2.4.1 Power system

The power system assures that voltage levels are as required for each respective mode and will either delay mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between the power supply voltage drops below-specified levels (for example, below 1.7 V) and the reset occurs. There are no voltage sequencing requirements.

The VDDD supply (1.7 V to 3.6 V) powers a low-dropout regulator (LDO). The system low-power (LP) operates the core operating voltage (VCCD) at 1.1 V and offers high-performance with no restrictions on device configuration.

2.4.2 Power modes

FX5 can operate in four systems and three CPU power modes. These modes are intended to minimize the average power consumption in an application[2].

FX5 supports the following power modes, in order of decreasing power consumption:

- System low-power (LP) – All peripherals and CPU power mode are available at maximum speed
- CPU Active – CPU is executing code in system LP
- CPU Sleep – CPU code execution is halted in system LP
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode:
  - USB3 operation at 5 Gbps or 10 Gbps
  - USB3 low-power modes (U1, U2)
  - High-bandwidth data subsystem IOs port in LVCMOS SDR or DDR mode
  - High-bandwidth data subsystem IOs port in LVDS 625 Mbps or 1.25 Gbps mode (**Note:** For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can be at either 1.8 V or 3.3 V depending on the desired CTRL signal logic level.)

The I/O power supplies VDDIOP0, VDDIOP1, VDDIO_P0CTRL, and VDDIO_P1CTRL can be turned OFF when the corresponding interface is not in use. These supplies cannot be turned OFF at any time if the GPIF III interface is used in the application.

- Other Low-power modes (see **Table 8**):
  - Suspend mode with USB 3.0 mode
  - Deep Sleep mode
  - Core power-down mode

The CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). The system LP and Deep Sleep modes are additional low-power modes supported by the FX5.

Note
2. The power consumption depends on how the FX5 IOs are utilized in the application.

Table 8 Entry and exit methods for low-power modes

Low-power mode	Characteristics	Methods of entry	Methods of exit
Suspend mode with USB 3.2 PHY enabled	• The power consumption in this mode does not exceed 1.8 mW • USB 3.2 PHY is enabled and is in U3 mode (one of the Suspend modes defined by the USB 3.2 specification). This one block alone is operational with its internal clock, while all other clocks are shut down. • All I/Os maintain their previous state • The power supply for the wakeup source and core power must be retained. All other power domains can be turned ON/OFF individually. • CPU shall be in Deep Sleep mode • The states of the configuration registers, buffer memory, and all internal RAM are maintained • All transactions must be completed before FX5 enters Suspend mode (the state of outstanding transactions is not preserved) • The firmware resumes operation from where it was suspended (except when woken up by an XRES assertion) because the program counter does not reset	Firmware executing on the Arm® core can put FX5 into Suspend mode. For example, on a USB suspend condition, the firmware may decide to put FX5 into Suspend mode.	• Resume condition on SSRX± • D+ transitioning to LOW or HIGH • D– transitioning to LOW or HIGH • Detection of VBUS • GPIO or I2C activity • GPIF III interface assertion of any LVCMOS CTL pins • Assertion of XRES pins

Table 8 Entry and exit methods for low-power modes *(continued)*

Low-power mode	Characteristics	Methods of entry	Methods of exit
Deep Sleep mode	• The power consumption in this mode does not exceed 120 µW • All configuration register settings and program/data RAM contents are preserved • All blocks are powered OFF including the USB PHY • GPIO pins maintain their configuration • Crystal oscillator is turned OFF • Internal PLL is turned OFF • USB transceiver is turned OFF • Arm® core is in the Deep Sleep state. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM. • Power supply for the wakeup source and core power must be retained. All other power domains can be turned ON/OFF individually.	Firmware executing on Arm® core configures the appropriate register	GPIO or I2C activity • GPIF III interface assertion of LVCMOS I/Os • Assertion of XRES pins
Core power-down mode	• The power consumption in this mode does not exceed 15 µW • Core power is turned OFF along with all other power supplies to FX5 • All buffer memory, configuration registers and the program RAM do not maintain their state. After exiting this mode, the firmware will be reloaded • In this mode, all other power domains can be turned ON/OFF individually	Turn off all power domains	Reapply power supplies and assertion of XRES pins

2.4.3 Booting options

FX5 can load boot images from various sources, selected by the configuration of the PMODE pin. Following are the FX5 boot options:

- Boot from USB
- Boot from internal application flash

Table 9 FX5 booting options

PMODE_P13.0	Boot from
LOW	Internal application flash
HIGH	USB

2.4.4 Clock system

The clock system as shown in **Figure 2**, consists of the following features:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- External 24-MHz crystal oscillator (ECO)
- External clock input
- Two phase-locked loops (PLLs)
- One frequency-locked loop (FLL)

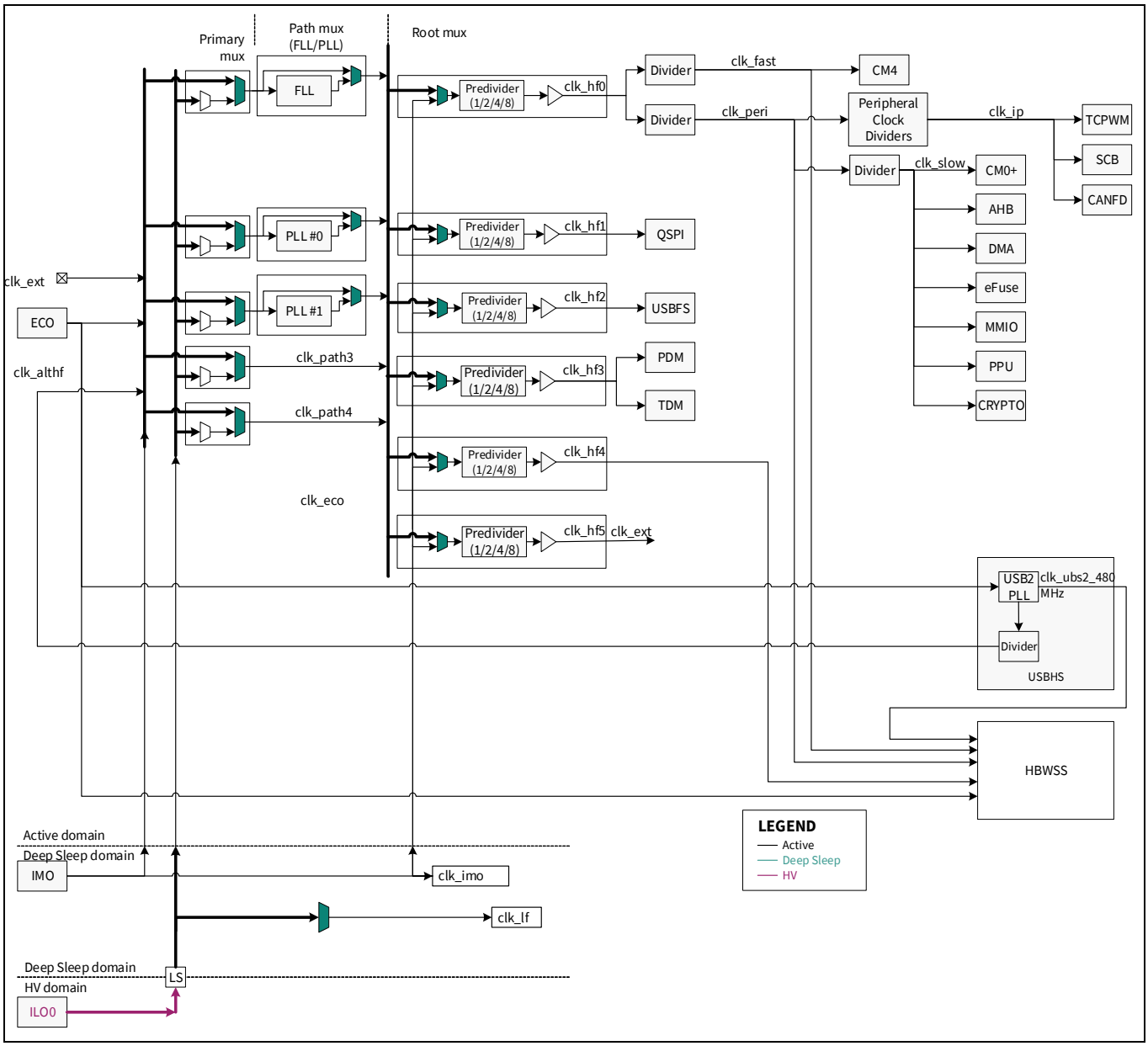


Figure 2 Clocking diagram

2.4.5 Internal main oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed at the factory to achieve the specified accuracy. The IMO frequency is 8 MHz and the tolerance is ±2%.

2.4.6 Internal low-speed oscillator (ILO)

The ILO is a very low-power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

2.5 System-level ESD

All pins of FX5 support ±2.0-kV human body model (HBM) based on JESD22-A114 Specification.

IEC protection has to be provided at the system level.

2.5.1 External crystal oscillators (ECO)

When an external crystal is used, the start-up time for the clock output from the crystal driver circuit is determined by the following:

- External crystal oscillator's intrinsic characteristics
- Internal settings of the crystal driver
- Load capacitance on the XIP and XOP pins

Figure 3 shows the crystal model components, the load capacitors, the XIP and XOP pins of FX5, and the crystal driver circuit. The model consists of the following parameters:

- Crystal motional capacitance (Cs)
- Crystal motional inductance (Ls)
- Crystal equivalent series resistance (ESR)
- Crystal shunt capacitance (C0)
- Load capacitors CL1 and CL2

See **Clock system** for the crystal values and the crystal datasheet for the load capacitor values. The ECO requires balanced external load capacitors.

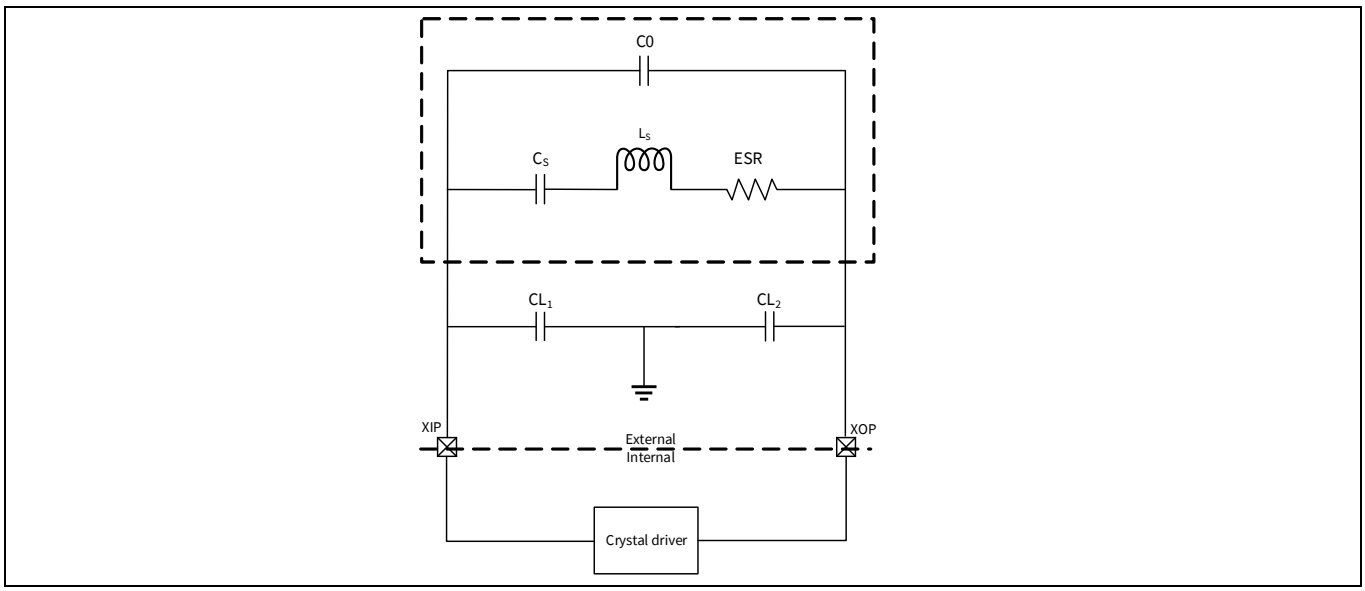


Figure 3 Oscillator circuits

2.5.2 Clock dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are following clock dividers:

- Eight 8-bit clock dividers
- Eight 16-bit integer clock dividers
- Two 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

2.5.3 Trigger routing

FX5 contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers”, which connect a specific source to a destination. The user can enable or disable the route.

2.5.4 Reset

FX5 can be reset from a variety of sources:

- POR to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up
- BOD reset to monitor the digital voltage supply VDDD and generate a reset if VDDD falls below the minimum required logic operating voltage
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active LOW and has a weak internal pull up of 85 kΩ. An optional 4.7 kΩ pull up resistor can be connected to VDDD as shown in **Figure 4**.

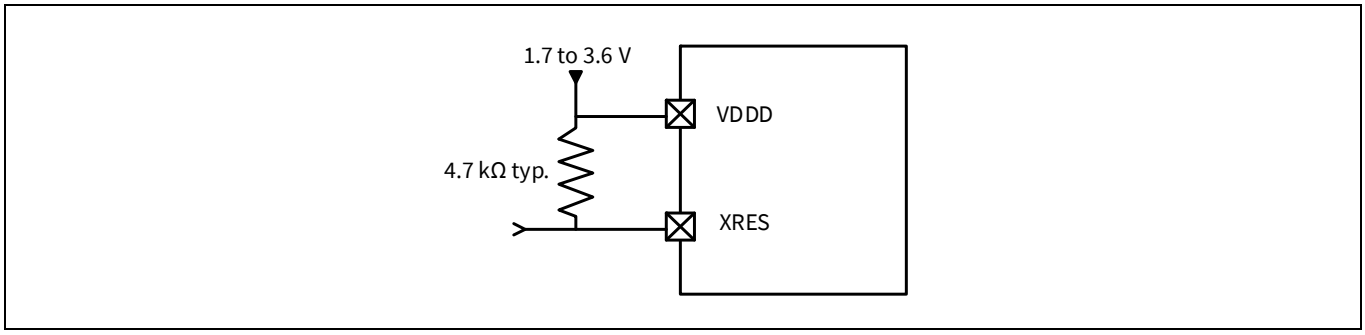


Figure 4 XRES connection diagram

- Software-initiated reset to reset the device on demand using the firmware
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code

The reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows the software to determine the cause of the reset. RAM contents are not retained across the reset event.

2.6 Fixed-function digital

2.6.1 Timer/Counter/Pulse-width Modulator (TCPWM)

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse-width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes
- Clock prescaling (division by 1, 2, 4,... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with the rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device, there are 7 × 32-bit TCPWMs.

2.6.2 Serial Communication Block (SCB)

FX5 has seven SCBs (see **Table 14**).

- **I^2C mode:** The SCB can implement a full multi-master and slave interface (it is capable of multi-master arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI2C, which creates a mailbox address range and effectively reduces I2C communication to reading from and writing to an array in memory. The SCB supports a 256-byte FIFO for receiving and transmitting.
  The I2C peripheral is compatible with I2C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the **I2C-bus specification and user manual (UM10204)**.The I2C bus I/O is implemented with GPIO in open-drain modes.
- **UART mode:** This is a full-featured UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO 7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. The common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.
- **SPI mode:** The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (which essentially adds a start pulse that is used to synchronize SPI codecs), and National Microwire (a half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with a 25-MHz clock.

2.6.3 USB full-speed device interface

This product line incorporates a full-speed USB device interface. The device can have up to eight endpoints. A 512-byte SRAM buffer is provided and DMA is supported.

Note that if the USB-FS pins are not used, connect VDDUSB to ground and leave the USBDP and USBDM pins unconnected.

2.6.4 Quad SPI/serial memory interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, quad, dual-quad, and octal SPI configurations and supports up to four external memory devices. It supports two modes of operation:

- MMIO, a command mode interface that provides data access via registers and FIFOs
- Execute-in-place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers

In XIP mode, the external memory is mapped into the FX5 internal address space, enabling code execution directly from the external memory. To improve the performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secured storage and access of code and data in the external memory.

2.7 GPIO

FX5 has 48 GPIOs including the pins used for low-speed peripheral interface, which implement the following:

- Eight drive modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
  - In strong drive mode, there are four selectable drive strengths for IOL and IOH current drive
- Input threshold select (CMOS or LVTTL)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized into logical entities called ports, which are up to eight pins wide. Data output and pin state register store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled, and each port has an interrupt request (IRQ) associated with it.

The ports 10.0 and 10.1 pins are capable of overvoltage tolerant (OVT) operation, where the input voltage may be higher than VDDD. The OVT pins are commonly used with I2C to allow powering the chip OFF while maintaining a physical connection to an operating I2C bus without affecting its functionality.

The GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see **Electrical specifications**.

2.8 Special-function peripherals

2.8.1 Audio subsystem

This subsystem consists of the following hardware blocks:

- Two Inter-IC Sound (I2S) interfaces
- Two PDM to PCM decoder channels

Each of the I2S interfaces implements two independent hardware FIFO buffers – TX and RX, which can operate in master or slave mode. The following features are supported:

- Multiple data formats – I2S, left-justified, time division multiplexed (TDM) mode A, and TDM mode B
- Programmable channel/word lengths – 8/16/18/20/24/32 bits
- Internal/external clock operation up to 192 ksps
- Interrupt mask events – trigger, not empty, full, overflow, underflow, and watchdog
- Configurable FIFO trigger level with DMA support

The I2S interface is commonly used to connect with audio codecs, simple DACs, and digital microphones.

The PDM-to-PCM decoder implements a single hardware RX FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length – 16/18/20/24 bits
- Programmable gain amplifier (PGA) for volume control from –12 dB to +10.5 dB in 1.5-dB steps
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksps
- Programmable high-pass filter gain
- Interrupt mask events – not empty, overflow, trigger, and underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM Data line.

3 Pinouts

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	P0CP	P0CN	V33	P1D0P	P1D1P	P1D2P	P1D3P	P1CLKP	P1D4P	P1D5P	P1D6P	P1D7P	P1CP	A
B	P0D7P	P0D7N	VSS	P1D0N	P1D1N	P1D2N	P1D3N	P1CLKN	P1D4N	P1D5N	P1D6N	P1D7N	P1CN	B
C	P0D6P	P0D6N	VDDIO_P0	VSS	VDDIO_P1	VSS	VDDIO_P1_CTRL	VSS	VDDIO_P1	VSS	VDDIO_QSPI	VSS	P6.4 SPICS3	C
D	P0D5P	P0D5N	VSS	P0CTL6	P1CTL0	P1CTL1	P1CTL2	P1CTL3	P1CTL4	P1CTL5	P1CTL6	P6.3 SPICS2	P6.2 SPICS1	D
E	P0D4P	P0D4N	VDDIO_P0_CTRL	P0CTL5	P7.2 SPIDAT2	P7.3 SPIDAT3	P7.4 SPIDAT4	P7.5 SPIDAT5	P7.6 SPIDAT6	P7.7 SPIDAT7	P6.0 SPICLK	P6.1 SPICS0	P8.7 P1SCL	E
F	P0CLKP	P0CLKN	VSS	P0CTL4	P7.0 SPIDAT0	P7.1 SPIDAT1	VDDIO	VSS	VDDD	P4.4 GPIO2	P13.0 PMODE	P13.1 GPIO4	P8.6 P1SDA	F
G	P0D3P	P0D3N	VDDIO_P0	P0CTL3	P4.0 VBUSDETECTn	P4.1 PDMCLK	VCCD	VSS	VCCD	P4.2 PDMDAT	P4.3 GPIO1	P10.1 I2CSDA	P0.1 P0SCL	G
H	P0D2P	P0D2N	VSS	P0CTL2	P8.0 UART-RX	P8.1 UART-TX	P8.2 UART-RTS	VSS	P8.3 UART-CTS	P8.4 CANRX	P8.5 CANTX	P10.0 I2CSCL	P0.0 P0SDA	H
J	P0D1P	P0D1N	V33	P0CTL1	P9.0 I2SSCKOUT	P9.1 I2SSCKIN	P9.2 I2STXWS	P9.3 I2STXMCLK	P9.4 I2SSDI	P9.5 I2SSDO	P9.6 I2SRXWS	P9.7 I2SRXMCLK	P1.1 CC2	J
K	P0D0P	P0D0N	VSS	P0CTL0	RESREF	XRES	P11.0 TDOSWO	P11.1 TDI	P11.2 TMS SWDIO	P11.3 TCLK SWDCLK	P11.4 SWDRST	P11.5 GPIO5	P1.0 CC1	K
L	VSS	VSS	USB3V18	VSS	USB3V18	VSS	USB3V18	VSS	VSS	V33	VDDD	VSS	VDDIO	L
M	USBFSDN	USB3V18	USB3RX1P	USB3V18	USB3TX1P	USB3V18	USB3TX2P	USB3V18	USB3RX2P	VDDD	USBHSDN	VDDIO_XTAL	P5.1 XTALOUT	M
N	USBFSDP	VSS	USB3RX1N	VSS	USB3TX1N	VSS	USB3TX2N	VSS	USB3RX2N	VSS	USBHSDP	VSS	P5.0 XTALIN	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

- LVDS pin with boundary scan
- LVDS pin without boundary scan
- USB pin
- GPIO pin with boundary scan
- GPIO pin without boundary scan
- Power
- Ground

Figure 5 Preliminary ball map (top view)

3.1 Pin definitions

Table 10 High-bandwidth data interface

Pin#	Category	Signal name			Type of signal	Signal description	Associated supply
		LVCMOS mode		LVDS mode			
		SDR mode (RX / TX)	DDR mode (RX only)				
A1	LVDS interface Port 0[3]	P0CLK[4]	P0CTL8[4]	P0CP[4]	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
A2		P0CTL9	P0CTL9	P0CN	LVDS / LVCMOS		VDDIO_P0
B1		P0D15	P0D15	P0D7P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
B2		P0D7	P0D7	P0D7N	LVDS / LVCMOS		VDDIO_P0
C1		P0D14	P0D14	P0D6P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
C2		P0D6	P0D6	P0D6N	LVDS / LVCMOS		VDDIO_P0
D1		P0D13	P0D13	P0D5P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
D2		P0D5	P0D5	P0D5N	LVDS / LVCMOS		VDDIO_P0
E1		P0D12	P0D12	P0D4P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
E2		P0D4	P0D4	P0D4N	LVDS / LVCMOS		VDDIO_P0
F1		P0D9[4]	P0CLK[4]	P0CLKP[4]	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
F2		P0CTL7	P0CTL7	P0CLKN	LVDS / LVCMOS		VDDIO_P0
G1		P0D11	P0D11	P0D3P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
G2		P0D3	P0D3	P0D3N	LVDS / LVCMOS		VDDIO_P0
H1		P0D10	P0D10	P0D2P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
H2		P0D2	P0D2	P0D2N	LVDS / LVCMOS		VDDIO_P0
J1		P0CTL8[4]	P0D9[4]	P0D1P[4]	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
J2		P0D1	P0D1	P0D1N	LVDS / LVCMOS		VDDIO_P0
K1		P0D8	P0D8	P0D0P	LVDS / LVCMOS	Port 0 signal	VDDIO_P0
K2		P0D0	P0D0	P0D0N	LVDS / LVCMOS		VDDIO_P0
D4		P0CTL6	P0CTL6	P0CTL6	LVCMOS	Port 0 control signal 6	VDDIO_P0_CTRL
E4		P0CTL5	P0CTL5	P0CTL5	LVCMOS	Port 0 control signal 5	VDDIO_P0_CTRL
F4		P0CTL4	P0CTL4	P0CTL4	LVCMOS	Port 0 control signal 4	VDDIO_P0_CTRL
G4		P0CTL3	P0CTL3	P0CTL3	LVCMOS	Port 0 control signal 3	VDDIO_P0_CTRL
H4		P0CTL2	P0CTL2	P0CTL2	LVCMOS	Port 0 control signal 2	VDDIO_P0_CTRL
J4		P0CTL1	P0CTL1	P0CTL1	LVCMOS	Port 0 control signal 1	VDDIO_P0_CTRL
K4		P0CTL0	P0CTL0	P0CTL0	LVCMOS	Port 0 control signal 0	VDDIO_P0_CTRL

Notes
3. For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can work in the entire 1.8 V–3.3 V range depending on the desired CTRL signal logic level.
4. Cannot be used as GPIO.

Table 10 High-bandwidth data interface *(continued)*

Pin#	Category	Signal name			Type of signal	Signal description	Associated supply
		LVCMOS mode		LVDS mode			
		SDR mode (RX / TX)	DDR mode (RX only)				
A12	LVDS interface Port 1[3]	P1D15	P1D15	P1D7P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B12		P1D7	P1D7	P1D7N	LVDS / LVCMOS		VDDIO_P1
A11		P1D14	P1D14	P1D6P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B11		P1D6	P1D6	P1D6N	LVDS / LVCMOS		VDDIO_P1
A10		P1D13	P1D13	P1D5P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B10		P1D5	P1D5	P1D5N	LVDS / LVCMOS		VDDIO_P1
A9		P1D12	P1D12	P1D4P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B9		P1D4	P1D4	P1D4N	LVDS / LVCMOS		VDDIO_P1
A8		P1D9[4]	P1CLK[4]	P1CLKP[4]	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B8		P1CTL7	P1CTL7	P1CLKN	LVDS / LVCMOS		VDDIO_P1
A7		P1D11	P1D11	P1D3P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B7		P1D3	P1D3	P1D3N	LVDS / LVCMOS		VDDIO_P1
A6		P1D10	P1D10	P1D2P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B6		P1D2	P1D2	P1D2N	LVDS / LVCMOS		VDDIO_P1
A5		P1CLK[4]	P1D9[4]	P1D1P[4]	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B5		P1D1	P1D1	P1D1N	LVDS / LVCMOS		VDDIO_P1
A4		P1D8	P1D8	P1D0P	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B4		P1D0	P1D0	P1D0N	LVDS / LVCMOS		VDDIO_P1
A13		P1CTL8	P1CTL8	P1CP	LVDS / LVCMOS	Port 1 - signal	VDDIO_P1
B13		P1CTL9	P1CTL9	P1CN	LVDS / LVCMOS		VDDIO_P1
D11		P1CTL6	P1CTL6	P1CTL6	LVCMOS	Port 1 control signal 6	VDDIO_P1_CTRL
D10		P1CTL5	P1CTL5	P1CTL5	LVCMOS	Port 1 control signal 5	VDDIO_P1_CTRL
D9		P1CTL4	P1CTL4	P1CTL4	LVCMOS	Port 1 control signal 4	VDDIO_P1_CTRL
D8		P1CTL3	P1CTL3	P1CTL3	LVCMOS	Port 1 control signal 3	VDDIO_P1_CTRL
D7		P1CTL2	P1CTL2	P1CTL2	LVCMOS	Port 1 control signal 2	VDDIO_P1_CTRL
D6		P1CTL1	P1CTL1	P1CTL1	LVCMOS	Port 1 control signal 1	VDDIO_P1_CTRL
D5		P1CTL0	P1CTL0	P1CTL0	LVCMOS	Port 1 control signal 0	VDDIO_P1_CTRL

Notes
3. For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can work in the entire 1.8 V–3.3 V range depending on the desired CTRL signal logic level.
4. Cannot be used as GPIO.

Table 11 USB and clock signals

Pin#	Category	Signal name	Type of signal	Signal description	Associated supply
N3	USB SS+HS	USB3RX1N	USBSS	USB SS RX pair - Lane 1	USB3V18
M3		USB3RX1P	USBSS		USB3V18
N5		USB3TX1N	USBSS	USB SS TX pair - Lane 1	USB3V18
M5		USB3TX1P	USBSS		USB3V18
N7		USB3TX2N	USBSS	USB SS TX pair - Lane 2	USB3V18
M7		USB3TX2P	USBSS		USB3V18
N9		USB3RX2N	USBSS	USB SS RX pair - Lane 2	USB3V18
M9		USB3RX2P	USBSS		USB3V18
N11		USBHSDP	USBHS	USB HS pair	V33
M11		USBHSDN	USBHS		V33
K5		RESREF	RESREF	Connect 6.04 kΩ ± 1% resistor pull down to GND	VDDIO
N13	Clock	XTALIN	XTAL	Crystal IN/OSC IN	VDDIOXTAL
M13		XTALOUT	XTAL	Crystal OUT/OSC IN	VDDIOXTAL
K6		XRES	Reset	–	VDDD

Table 12 Peripheral and other signals

Pin#	Category	Signal name		Type of signal	Signal description	Associated supply
		Function after reset	Alternate functions			
E11	SPI/QSPI/ Octal SPI	P6.0	SPICLK (SMIF) UART-RX1 (SCB6) I2C-SCL1 (SCB6) SPICLK (SCB3)	GPIO	–	VDDIOQSPI
E12		P6.1	SPICS0 (SMIF) UART-TX1 (SCB6) I2C-SDA1 (SCB6) SPICS0 (SCB3)	GPIO	–	VDDIOQSPI
D13		P6.2	SPICS1 (SMIF) SPI-MOSI (SCB3)	GPIO	–	VDDIOQSPI
D12		P6.3	SPICS2 (SMIF) SPI-MISO (SCB3)	GPIO	–	VDDIOQSPI
C13		P6.4	SPICS3 (SMIF)	GPIO	–	VDDIOQSPI

Table 12 Peripheral and other signals *(continued)*

Pin#	Category	Signal name		Type of signal	Signal description	Associated supply
		Function after reset	Alternate functions			
F5	SPI/QSPI/ Octal SPI	P7.0	SPIDAT0 (SMIF) UART-RX1 (SCB0) I2C-SCL (SCB0) SPICLK (SCB2)	GPIO	–	VDDIOQSPI
F6		P7.1	SPIDAT1 (SMIF) UART-TX1 (SCB0) I2C-SDA (SCB0) SPICS0 (SCB2)	GPIO	–	VDDIOQSPI
E5		P7.2	SPIDAT2 (SMIF) UART-CTS0 (SCB0) SPI-MOSI (SCB2)	GPIO	–	VDDIOQSPI
E6		P7.3	SPIDAT3 (SMIF) UART-CTS0 (SCB3) UART-RTS0 (SCB0) SPI-MISO (SCB2)	GPIO	–	VDDIOQSPI
E7		P7.4	SPIDAT4 (SMIF) UART-CTS0 (SCB2)	GPIO	–	VDDIOQSPI
E8		P7.5	SPIDAT5 (SMIF)	GPIO	–	VDDIOQSPI
E9		P7.6	SPIDAT6 (SMIF) UART-RX1 (SCB1) I2C-SDA1 (SCB1)	GPIO	–	VDDIOQSPI
E10		P7.7	SPIDAT7 (SMIF) UART-TX1 (SCB1) I2C-SCL1 (SCB1)	GPIO	–	VDDIOQSPI
H5	UART	P8.0	UART-RX0 (SCB1) I2C-SDA0 (SCB1) SPI-MISO (SCB1) PDM1-CLK0 I2S1-SCKOUT TCPWM0_P	GPIO	–	VDDIO
H6		P8.1	UART-TX0 (SCB1) I2C-SCL0 (SCB1) SPICLK (SCB1) PDM1-DATA0 I2S1-SCKIN TCPWM0_N	GPIO	–	VDDIO
H7		P8.2	UART-RTS0 (SCB1) SPI-MOSI (SCB1) PDM1-CLK1 I2S1-TXWS TCPWM1_P	GPIO	–	VDDIO
H9		P8.3	UART-CTS0 (SCB1) SPICS0 (SCB1) PDM1-DATA1 I2S1-TXMCLK TCPWM1_N	GPIO	–	VDDIO

Table 12 Peripheral and other signals *(continued)*

Pin#	Category	Signal name		Type of signal	Signal description	Associated supply
		Function after reset	Alternate functions			
J5	I2S master/ slave, PDM	P9.0	I2S0-SCKOUT PDM2-CLK0 TCPWM4_P UART-RX0 (SCB6) I2C-SCL0 (SCB6) SPICLK (SCB6)	GPIO	–	VDDIO
J6		P9.1	I2S0-SCKIN PDM2-DATA0 TCPWM4_N UART-TX0 (SCB6) I2C-SDA0 (SCB6) SPI-MOSI (SCB6)	GPIO	–	VDDIO
J7		P9.2	I2S0-TXWS PDM2-CLK1 TCPWM5_P UART-RTS0 (SCB6) SPI-MISO (SCB6)	GPIO	–	VDDIO
J8		P9.3	I2S0-TXMCLK PDM2-DATA1 TCPWM5_N UART-CTS0 (SCB6) SPICS0 (SCB6)	GPIO	–	VDDIO
J9		P9.4	I2S0-SDI TCPWM6_P SPICS1 (SCB6)	GPIO	–	VDDIO
J10		P9.5	I2S0-SDO TCPWM6_N UART-RTS0 (SCB2) SPICS2 (SCB6) CAN2-RX	GPIO	–	VDDIO
J11		P9.6	I2S0-RXWS TCPWM7_P UART-RX0 (SCB2) I2C-SDA1 (SCB2) SPICS3 (SCB6) CAN2-TX	GPIO	–	VDDIO
J12		P9.7	I2S0-RXMCLK TCPWM7_N UART-TX0 (SCB2) I2C-SCL1 (SCB2)	GPIO	–	VDDIO
G6		P4.1	PDM0-CLK0 UART-RX1 I2C-SDA1 (SCB3)	GPIO	–	VDDIO
G10		P4.2	PDM0-DAT0 UART-TX1 I2C-SCL1 (SCB3)	GPIO	–	VDDIO

Table 12 Peripheral and other signals *(continued)*

Pin#	Category	Signal name		Type of signal	Signal description	Associated supply
		Function after reset	Alternate functions			
G11	User GPIOs	P4.3	GPIO1 UART-RX0 I2C-SCL0 (SCB5) SPICLK (SCB5)	GPIO	–	VDDIO
F10		P4.4	GPIO2 UART-TX0 I2C-SDA0 (SCB5) SPI-CS0 (SCB5) CAN1-RX	GPIO	–	VDDIO
F11		P13.0	PMODE UART-RTS0 (SCB5) SPI-MOSI (SCB5) CAN1-TX	GPIO	–	VDDIO
F12		P13.1	GPIO4 UART-CTS0 (SCB5) SPI-MISO (SCB5)	GPIO	–	VDDIO
K12		P11.5	GPIO5 UART-TX1 (SCB5) I2C-SDA1 (SCB5) CAN3-TX	GPIO	–	VDDIO
H12	I2C	P10.0	I2C-SCL0 (SCB0) UART-RX0 (SCB0)	OVT GPIO	I2C clock (SCL)	VDDIO
G12		P10.1	I2C-SDA0 (SCB0) UART-TX0 (SCB0)	OVT GPIO	I2C data (SDA)	VDDIO
G13		P0.1	P0SCL (SCB2) UART-TX0 (SCB2)	GPIO	I2C clock (SCL)	VDDIO
H13		P0.0	P0SDA (SCB2) UART-RX0 (SCB2)	GPIO	I2C data (SDA)	VDDIO
E13		P8.7	P1SCL (SCB3) UART-TX0 (SCB3)	GPIO	I2C clock (SCL)	VDDIO
F13		P8.6	P1SDA (SCB3) UART-RX0 (SCB3)	GPIO	I2C data (SDA)	VDDIO

Table 12 Peripheral and other signals *(continued)*

Pin#	Category	Signal name		Type of signal	Signal description	Associated supply
		Function after reset	Alternate functions			
K11	SWD/JTAG	P11.4	SWDRST UART-RX1 (SCB5) I2C-SCL1 (SCB5) CAN3-RX	GPIO	–	VDDIO
K10		P11.3	TCLKSWDCLK PDM3-DATA1 UART-CTS1 (SCB4) SPI-MISO (SCB4)	GPIO	–	VDDIO
K9		P11.2	TMSSWDIO PDM3-CLK1 UART-RTS1 (SCB4) SPI-MOSI (SCB4)	GPIO	–	VDDIO
K8		P11.1	TDI PDM3-DATA0 UART-RX1 (SCB4) I2C-SDA1 (SCB4) SPICS0 (SCB4)	GPIO	–	VDDIO
K7		P11.0	TDOSWO PDM3-CLK0 UART-TX1 (SCB4) I2C-SCL1 (SCB4) SPICLK (SCB4)	GPIO	–	VDDIO
H10	CAN FD	P8.4	CAN0-RX TCPWM2_P I2S1-SDO PDM0-CLK1 UART-RX0 (SCB4) I2C-SCL0 (SCB4) SPICLK (SCB4)	GPIO	–	VDDIO
H11		P8.5	CAN0-TX TCPWM2_N I2S1-SDI PDM0-DATA1 UART-TX0 (SCB4) I2C-SDA0 (SCB4) SPICS0 (SCB4)	GPIO	–	VDDIO
K13	USB Ctrl	P1.0	CC1[5]	GPIO	USB CC pair	VDDIO
J13		P1.1	CC2[5]	GPIO		VDDIO
G5		P4.0	VBUSDETECTn UART-RTS0 (SCB3)	GPIO	–	VDDIO
N1	USBFS	USBFSDP	USBFSDP	USBFS	USB FS pair	V33
M1		USBFSDN	USBFSDN	USBFS		V33

Note
5. For proper USB-C operation with the external Rd resistor, the VDDD supply should be powered simultaneously with or before the V33 supply. If the VDDD supply stays unpowered after the V33 supply for more than 1 ms, then the Rd resistor may not be detected properly.

Table 13 Power

Pin#	Category	Signal name	Type of signal	Signal description	Associated supply
E3	Power	VDDIO_P0_CTRL[6]	Power	PHY/LVCMOS supply for Port 0 control signals	VDDIOP0
C3		VDDIO_P0[6]	Power	PHY/LVCMOS supply for Port 0	VDDIOP0
G3		VDDIO_P0[6]	Power		VDDIOP0
C7		VDDIO_P1_CTRL[6]	Power	PHY/LVCMOS supply for Port 1 control signals	VDDIOP1
C9		VDDIO_P1[6]	Power	PHY/LVCMOS supply for Port 1	VDDIOP1
C5		VDDIO_P1[6]	Power		VDDIOP1
M8		USB3V18	Power	–	USB3V18
M4		USB3V18	Power	–	USB3V18
M6		USB3V18	Power	–	USB3V18
M2		USB3V18	Power	–	USB3V18
L5		USB3V18	Power	–	VDDD
L3		USB3V18	Power	–	VDDD
L7		USB3V18	Power	–	USB3V18
L10		V33	Power	3.3 V supply (LVDS and USB HS)	V33
A3		V33	Power		V33
J3		V33	Power		V33
L11	Core power supply	VDDD	Power	SRSS VDDD	VDDD
M10		VDDD	Power		VDDD
F9		VDDD	Power		VDDD
G7		VCCD	Power	SRSS VCCD, capacitor 4.7 µF ±20% must be connected to this pin. VCCD is generated inside the IC and it is a power output pin, only capacitor to be connected at the pin externally.	VCCD
G9		VCCD	Power		VCCD
M12	VDDIO-XTAL	VDDIOXTAL	Power	Dedicated VDDIO for XTAL	VDDIOXTAL
C11	VDDIO-QSPI	VDDIOQSPI	Power	–	VDDIOQSPI
L13	VDDIO	VDDIO	Power	–	VDDIO
F7		VDDIO	Power	–	VDDIO

Note
6. For LVDS operation, VDDIOP0 and VDDIOP1 must be kept at 3.3 V. VDDIOP0_CTRL and VDDIOP1_CTRL can be at either 1.8 V or 3.3 V depending on the desired CTRL signal logic level.

Table 13 Power *(continued)*

Pin#	Category	Signal name	Type of signal	Signal description	Associated supply
L12	VSS	VSS	Ground	–	–
F8		VSS	Ground	–	–
H8		VSS	Ground	–	–
L1		VSS	Ground	–	–
L2		VSS	Ground	–	–
L9		VSS	Ground	–	–
L8		VSS	Ground	–	–
G8		VSS	Ground	–	–
D3		VSS	Ground	–	–
F3		VSS	Ground	–	–
H3		VSS	Ground	–	–
K3		VSS	Ground	–	–
C10		VSS	Ground	–	–
C6		VSS	Ground	–	–
C8		VSS	Ground	–	–
B3		VSS	Ground	–	–
C4		VSS	Ground	–	–
N10		VSS	Ground	–	–
L4		VSS	Ground	–	–
N8		VSS	Ground	–	–
N6		VSS	Ground	–	–
N4		VSS	Ground	–	–
N2		VSS	Ground	–	–
L6		VSS	Ground	–	–
N12		VSS	Ground	–	–
C12		VSS	Ground	–	–

Note
6. For LVDS operation, VDDIOP0 and VDDIOP1 must be kept at 3.3 V. VDDIOP0_CTRL and VDDIOP1_CTRL can be at either 1.8 V or 3.3 V depending on the desired CTRL signal logic level.

Each port pin has multiple alternate functions. These are defined in **Table 14** to **Table 19**. A consolidated view is also provided in **Table 20**. The columns ACT #x and DS #y denote active (System LP) and Deep Sleep mode signals respectively.

The notation for a signal is of the form IPName[x].signal_name[u]:y.

IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there is more than one signal for a particular signal name, y = Designates copies of the signal name.

For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. The signal copies are provided to allow flexibility in routing and to maximize the use of on-chip resources.

Table 14 SCB port and pin details

SCB#	Function	Signal	Port number	Pin number
SCB0	UART	RX	P7.0	F5
			P10.0	H12
		TX	P7.1	F6
			P10.1	G12
		CTS	P7.2	E5
		RTS	P7.3	E6
	I2C	SCL	P7.0	F5
			P10.0	H12
		SDA	P7.1	F6
			P10.1	G12
SCB1	UART	RX	P7.6	E9
			P8.0	H5
		TX	P7.7	E10
			P8.1	H6
		CTS	P8.3	H9
		RTS	P8.2	H7
	I2C	SCL	P7.7	E10
			P8.1	H6
		SDA	P7.6	E9
			P8.0	H5
	SPI	CS	P8.3	H9
		CLK	P8.1	H6
		MISO	P8.0	H5
		MOSI	P8.2	H7

Table 14 SCB port and pin details *(continued)*

SCB#	Function	Signal	Port number	Pin number
SCB2	UART	RX	P0.0	H13
			P9.6	J11
		TX	P0.1	G13
			P9.7	J12
		CTS	P7.4	E7
		RTS	P9.5	J10
	I2C	SCL	P0.1	G13
			P9.7	J12
		SDA	P0.0	H13
			P9.6	J11
	SPI	CS	P7.1	F6
		CLK	P7.0	F5
		MISO	P7.3	E6
		MOSI	P7.2	E5
SCB3	UART	RX	P8.6	F13
			P4.1	G6
		TX	P8.7	E13
			P4.2	G10
		CTS	P7.3	E6
		RTS	P4.0	G5
	I2C	SDA	P8.6	F13
			P4.1	G6
		SCL	P8.7	E13
			P4.2	G10
	SPI	CS	P6.1	E12
		CLK	P6.0	E11
		MISO	P6.3	D12
		MOSI	P6.2	D13

Table 14 SCB port and pin details *(continued)*

SCB#	Function	Signal	Port number	Pin number
SCB4	UART	RX	P11.1	K8
			P8.4	H10
		TX	P11.0	K7
			P8.5	H11
		CTS	P11.3	K10
		RTS	P11.2	K9
	I2C	SDA	P11.1	K8
			P8.5	H11
		SCL	P11.0	K7
			P8.4	H10
	SPI	CS	P11.1	K8
			P8.5	H11
		CLK	P11.0	K7
			P8.4	H10
		MISO	P11.3	K10
		MOSI	P11.2	K9
SCB5	UART	RX	P11.4	K11
			P4.3	G11
		TX	P11.5	K12
			P4.4	F10
		CTS	P13.1	F12
		RTS	P13.0	F11
	I2C	SDA	P11.5	K12
			P4.4	F10
		SCL	P11.4	K11
			P4.3	G11
	SPI	CS	P4.4	F10
		CLK	P4.3	G11
		MISO	P13.1	F12
		MOSI	P13.0	F11

Table 14 SCB port and pin details *(continued)*

SCB#	Function	Signal	Port number	Pin number
SCB6	UART	RX	P9.0	J5
			P6.0	E11
		TX	P9.1	J6
			P6.1	E12
		CTS	P9.3	J8
		RTS	P9.2	J7
	I2C	SDA	P9.1	J6
			P6.1	E12
		SCL	P9.0	J5
			P6.0	E11
	SPI	CS0	P9.3	J8
		CS1	P9.4	J9
		CS2	P9.5	J10
		CS3	P9.6	J11
		CLK	P9.0	J5
		MISO	P9.2	J7
		MOSI	P9.1	J6

Table 15 TCPWM port and pin details

Signal	Port number	Pin number
T0_p	P8.0	H5
T0_n	P8.1	H6
T1_p	P8.2	H7
T1_n	P8.3	H9
T2_p	P8.4	H10
T2_n	P8.5	H11
T4_p	P9.0	J5
T4_n	P9.1	J6
T5_p	P9.2	J7
T5_n	P9.3	J8
T6_p	P9.4	J9
T6_n	P9.5	J10
T7_p	P9.6	J11
T7_n	P9.7	J12

Table 16 I2S port and pin details

Type	Signal	Port number	Pin number
I2S0	SCKOUT	P9.0	J5
	TXWS	P9.2	J7
	TXMCLK	P9.3	J8
	SDO	P9.5	J10
	SCKIN	P9.1	J6
	RXWS	P9.6	J11
	RXMCLK	P9.7	J12
	SDI	P9.4	J9
I2S1	SCKOUT	P8.0	H5
	TXWS	P8.2	H7
	TXMCLK	P8.3	H9
	SDO	P8.5	H11
	SCKIN	P8.1	H6
	SDI	P8.4	H10

Table 17 PDM

Type	Signal	Port no.	Pin no.
PDM0	CLK0	P4.1	G6
	DATA0	P4.2	G10
	CLK1	P8.4	H10
	DATA1	P8.5	H11
PDM1	CLK0	P8.0	H5
	DATA0	P8.1	H6
	CLK1	P8.2	H7
	DATA1	P8.3	H9
PDM2	CLK0	P9.0	J5
	DATA0	P9.1	J6
	CLK1	P9.2	J7
	DATA1	P9.3	J8
PDM3	CLK0	P11.0	K7
	DATA0	P11.1	K8
	CLK1	P11.2	K9
	DATA1	P11.3	K10

Table 18 SMIF

Signal	Port number	Pin number
CLK	P6.0	E11
CS0	P6.1	E12
CS1	P6.2	D13
CS2	P6.3	D12
CS3	P6.4	C13
DATA0	P7.0	F5
DATA1	P7.1	F6
DATA2	P7.2	E5
DATA3	P7.3	E6
DATA4	P7.4	E7
DATA5	P7.5	E8
DATA6	P7.6	E9
DATA7	P7.7	E10

Table 19 CAN

Type	Signal	Port no.	Pin no.
CAN0	TX	P8.5	H11
	RX	P8.4	H10
CAN1	TX	P13.0	F11
	RX	P4.4	F10
CAN2	TX	P9.6	J11
	RX	P9.5	J10
CAN3	TX	P11.4	K11
	RX	P11.3	K10

Table 20 Multiple alternate functions

Port/ Pin	Active								Deep Sleep	
	ACT #0	DS #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #10	DS #4	DS #5
P0.0	–	–	–	–	scb[2].uart_rx:0	scb[2].i2c_sda:0	–	–	lvds2usb32ss.lnk1_l3_entry_gpio_i:3	–
P0.1	–	–	–	–	scb[2].uart_tx:0	scb[2].i2c_scl:0	–	–	–	–
P4.0	–	–	–	–	scb[3].uart_rts:0	–	–	–	–	–
P4.1	–	–	–	pdm[0].pdm_clk[0]:0	scb[3].uart_rx:1	scb[3].i2c_sda:1	–	–	–	–
P4.2	–	–	–	pdm[0].pdm_data[0]:0	scb[3].uart_tx:1	scb[3].i2c_scl:1	–	–	–	–
P4.3	–	–	–	–	scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_clk	–	–	–
P4.4	–	–	–	–	scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_select0	canfd[0].ttcan_rx:1	lvds2usb32ss.lnk0_l3_entry_gpio_i:3	–
P5.0	–	–	–	–	–	–	–	–	–	–
P5.1	–	–	–	–	–	–	–	–	–	–
P6.0	–	–	–	smif.spi_clk	scb[6].uart_rx:1	scb[6].i2c_scl:1	scb[3].spi_clk	–	–	–
P6.1	–	–	–	smif.spi_select0	scb[6].uart_tx:1	scb[6].i2c_sda:1	scb[3].spi_select0	–	–	–
P6.2	–	–	–	smif.spi_select1	–	–	scb[3].spi_mosi	–	–	–
P6.3	–	–	–	smif.spi_select2	–	–	scb[3].spi_miso	–	–	–
P6.4	–	–	–	smif.spi_select3	–	–	–	–	–	–
P7.0	–	scb[0].i2c_scl:1	–	smif.spi_data0	scb[0].uart_rx:1	–	scb[2].spi_clk	–	–	–
P7.1	–	scb[0].i2c_sda:1	–	smif.spi_data1	scb[0].uart_tx:1	–	scb[2].spi_select0	–	–	–
P7.2	–	–	–	smif.spi_data2	scb[0].uart_cts:0	–	scb[2].spi_mosi	–	–	–
P7.3	–	–	–	smif.spi_data3	scb[3].uart_cts:0	scb[0].uart_rts:0	scb[2].spi_miso	–	–	–
P7.4	–	–	–	smif.spi_data4	scb[2].uart_cts:0	–	–	–	–	–
P7.5	–	–	–	smif.spi_data5	–	–	–	–	–	–
P7.6	–	–	–	smif.spi_data6	scb[1].uart_rx:1	scb[1].i2c_sda:1	–	–	–	–
P7.7	–	–	–	smif.spi_data7	scb[1].uart_tx:1	scb[1].i2c_scl:1	–	–	–	–
P8.0	tcpwm[0].line[0]	–	tdm.tdm_tx_sck:1	pdm[0].pdm_clk[0]:1	scb[1].uart_rx:0	scb[1].i2c_sda:0	scb[1].spi_miso:0	–	–	–
P8.1	tcpwm[0].line_compl[0]	–	tdm.tdm_rx_sck:1	pdm[0].pdm_data[0]:1	scb[1].uart_tx:0	scb[1].i2c_scl:0	scb[1].spi_clk:0	–	–	–
P8.2	tcpwm[0].line[1]	–	tdm.tdm_tx_fsync:1	pdm[0].pdm_clk[1]:1	scb[1].uart_rts:0	–	scb[1].spi_mosi:0	–	lvds2usb32ss.lnk0_l3_entry_gpio_i:2	–
P8.3	tcpwm[0].line_compl[1]	–	tdm.tdm_tx_mck:1	pdm[0].pdm_data[1]:1	scb[1].uart_cts:0	–	scb[1].spi_select0:0	–	lvds2usb32ss.lnk1_l3_entry_gpio_i:2	–
P8.4	tcpwm[0].line[2]	–	tdm.tdm_rx_sd:1	pdm[0].pdm_clk[1]:0	scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_clk:0	canfd[0].ttcan_rx:0	–	–

Table 20 Multiple alternate functions *(continued)*

Port/ Pin	Active								Deep Sleep	
	ACT #0	DS #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #10	DS #4	DS #5
P8.5	tcpwm[0].line_compl[2]	–	tdm.tdm_tx_sd:1	pdm[0].pdm_data[1]:0	scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_select0:0	canfd[0].ttcan_tx:0	–	–
P8.6	–	–	–	–	scb[3].uart_rx:0	scb[3].i2c_sda:0	–	–	–	–
P8.7	–	–	–	–	scb[3].uart_tx:0	scb[3].i2c_scl:0	–	–	–	–
P9.0	tcpwm[0].line[4]	–	tdm.tdm_tx_sck:0	pdm[0].pdm_clk[0]:2	scb[6].uart_rx:0	scb[6].i2c_scl:0	scb[6].spi_clk:0	–	lvds2usb32ss.lnk0_l3_entry_gpio_i:1	–
P9.1	tcpwm[0].line_compl[4]	–	tdm.tdm_rx_sck:0	pdm[0].pdm_data[0]:2	scb[6].uart_tx:0	scb[6].i2c_sda:0	scb[6].spi_mosi:0	–	lvds2usb32ss.lnk1_l3_entry_gpio_i:1	–
P9.2	tcpwm[0].line[5]	–	tdm.tdm_tx_fsync:0	pdm[0].pdm_clk[1]:2	scb[6].uart_rts:0	–	scb[6].spi_miso:0	–	–	–
P9.3	tcpwm[0].line_compl[5]	–	tdm.tdm_tx_mck:0	pdm[0].pdm_data[1]:2	scb[6].uart_cts:0	–	scb[6].spi_select0:0	–	–	–
P9.4	tcpwm[0].line[6]	–	tdm.tdm_rx_sd:0	–	–	–	scb[6].spi_select1:0	–	–	–
P9.5	tcpwm[0].line_compl[6]	–	tdm.tdm_tx_sd:0	–	scb[2].uart_rts:0	–	scb[6].spi_select2:0	canfd[0].ttcan_rx:2	–	–
P9.6	tcpwm[0].line[7]	–	tdm.tdm_rx_fsync:0	–	scb[2].uart_rx:1	scb[2].i2c_sda:1	scb[6].spi_select3:0	canfd[0].ttcan_tx:2	–	–
P9.7	tcpwm[0].line_compl[7]	–	tdm.tdm_rx_mck:0	–	scb[2].uart_tx:1	scb[2].i2c_scl:1	–	–	–	–
P10.0	–	scb[0].i2c_scl:0	–	–	scb[0].uart_rx:0	–	–	–	–	–
P10.1	–	scb[0].i2c_sda:0	–	–	scb[0].uart_tx:0	–	–	–	–	–
P11.0	–		–	pdm[0].pdm_clk[0]:3	scb[4].uart_tx:1	scb[4].i2c_scl:1	scb[4].spi_clk:1	–	lvds2usb32ss.lnk0_l3_entry_gpio_i:0	cpuss.swj_swo_tdo
P11.1	–	–	–	pdm[0].pdm_data[0]:3	scb[4].uart_rx:1	scb[4].i2c_sda:1	scb[4].spi_select0:1	–	lvds2usb32ss.lnk1_l3_entry_gpio_i:0	cpuss.swj_swdoe_tdi
P11.2	–	–	–	pdm[0].pdm_clk[1]:3	scb[4].uart_rts:1	–	scb[4].spi_mosi:1	–	–	cpuss.swj_swdio_tms
P11.3	–	–	–	pdm[0].pdm_data[1]:3	scb[4].uart_cts:1	–	scb[4].spi_miso:1	–	–	cpuss.swj_swclk_tclk
P11.4	–	–	–	–	scb[5].uart_rx:1	scb[5].i2c_scl:1	–	canfd[0].ttcan_rx:3	–	cpuss.swj_trstn
P11.5	–	–	–	–	scb[5].uart_tx:1	scb[5].i2c_sda:1	–	canfd[0].ttcan_tx:3	–	–
P13.0	–	–	–	–	scb[5].uart_rts:0	–	scb[5].spi_mosi	canfd[0].ttcan_tx:1	–	–
P13.1	–	–	–	–	scb[5].uart_cts:0	–	scb[5].spi_miso	–	–	–

4 Power supply consideration

Figure 6 shows the power system requirements for power pins for all supported packages.

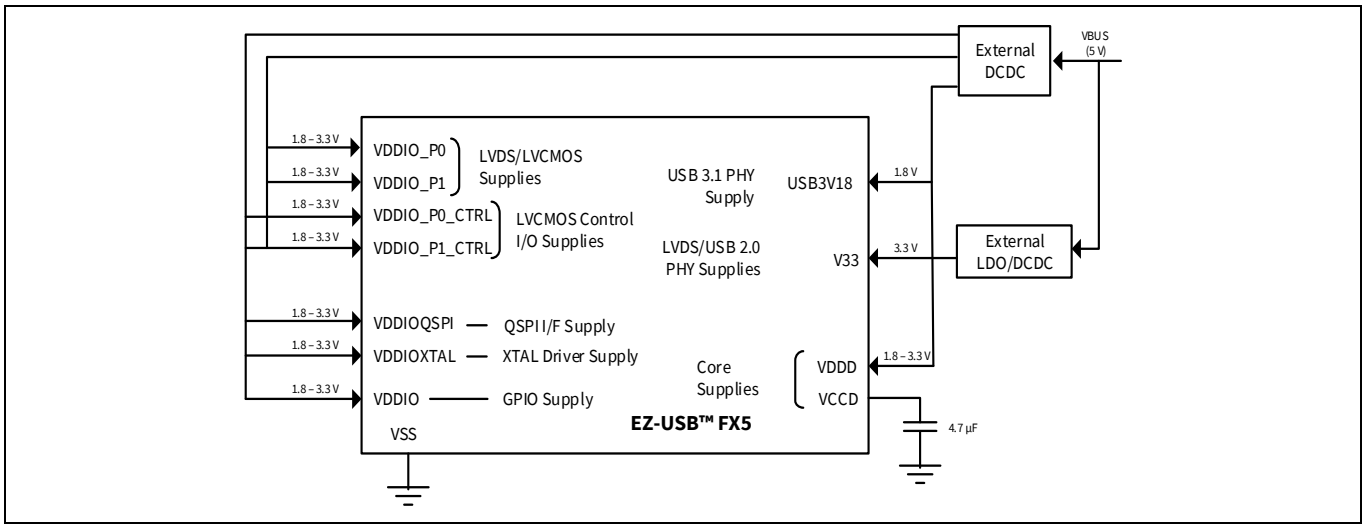


Figure 6 Power system requirement block diagram

4.1 Core power domains

- VDDD is the main digital supply input. It provides the inputs for the internal regulators.
- VCCD is the internal core logic supply and needs to be decoupled externally
- VDDIOQSPI is the power supply for the QSPI port
- VDDIOXTAL is the power supply for crystal
- VDDIO is the GPIO power supply
- VSS is the main ground for the entire chip

4.2 USB 3.2 and USB 2.0 PHY power supplies

- USB3V18 is the power supply for the USB 3.2 Gen 1 PHY
- V33 is the 3.3 V power supply for the USB 2 HS PHY, USB 2 FS PHY and LVDS PHY

4.3 LVDS port power supplies

- VDDIO_Px are the power supplies for LVDS/LVCMOS IOs

Note: For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can work in the entire 1.8 V–3.3 V range depending on the desired CTRL signal logic level.

- VDDIO_Px_CTRL are the power supplies for the LVCMOS control IOs

5 Electrical specifications

All specifications are valid for –40°C ≤ TA ≤ 85°C and for 1.71 V to 3.6 V except where noted.

5.1 Absolute maximum ratings

Table 21 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VDDD_ABS	Analog or digital supply relative to V_{SS}	–0.3	–	4.02	V	–
USB3V18_ABS	Max voltage on USB3V18 supply pins	–0.3	–	2.39	V	–
V33_ABS	Max voltage on V33 supply pin	–0.3	–	4.02	V	–
VDDD_ABS	Max voltage on VDDD supply pin	–0.3	–	4.02	V	–
VDDIO_ABS	Max voltage on VDDIO, VDDIO_* supply pins	–0.3	–	4.02	V	–
VGPIO_OVT_ABS	OVT GPIO voltage	–0.3	–	4.02	V	–
IGPIO_ABS_DS0	Current per GPIO at DS = 0	–7.5	–	7.5	mA	–
IGPIO_ABS_DS1	Current per GPIO at DS = 1	–5.6	–	5.6	mA	–
IGPIO_ABS_DS2	Current per GPIO at DS = 2	–3.8	–	3.8	mA	–
IGPIO_ABS_DS3	Current per GPIO at DS = 3	–1.9	–	1.9	mA	–
ESD_HBM	Electrostatic discharge human body model (ESD HBM) JEDEC JS-001-2017	2000	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model (ESD CDM) JS-002-2018	500	–	–	V	–
LU	Pin current for latch-up free operation	–100	–	100	mA	–
Tj	Junction Temperature	–	–	125	°C	–
TSTG	Storage Temperature	–65	–	150	°C	–
TA	Ambient Temperature	–40	–	85	°C	–

Table 22 Pin-based absolute maximum ratings

Category	Pin name	Absolute minimum (V)	Absolute maximum (V)
LVDS/LVCMOS	P[0,1][C,D,CLK,CTL]	–0.5	4.0
USB SS	USB3[RX,TX][1,2][N,P]	–0.5	2.06
USB HS	USBHS[DP,DN]	–0.5	4.0
USB FS	USBFS[DP,DN]	–0.5	4.0
CLOCK	XTAL[IN,OUT]	–0.5	4.0
RESET	XRES	–0.5	4.0
SPI /QSPI/Octal SPI	P[6,7]	–0.5	4.0
UART, I2S, PDM, GPIO, SWD, JTAG, CAN FD, USB Ctrl	P[0,1,4,8,9,11,13]	–0.5	4.0

5.2 DC specifications

Table 23 DC operating specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VDDD	Main analog / digital supply voltage	1.62	1.8 or 3.3	3.63	V	–
VDDD_EFUSE	VDDD supply when programming eFuse	2.38	2.5	2.62	V	eFuse programming voltage
USB3V18	Power supply voltage for USB3 ports	1.62	1.8	1.98	V	–
V33	Power supply voltage for 3.3 V supply	2.97	3.3	3.63	V	–
VDDIO_1P8	Power supply voltage for IO in the 1.8 V range	1.62	1.8	1.95	V	–
VDDIO_2P5	Power supply voltage for IO in the 2.5 V range	2.25	2.5	2.75	V	–
VDDIO_3P3	Power supply voltage for IO in the 3.3 V range	2.97	3.3	3.63	V	–
VCCD	Core logic supply output	–	1.1	–	V	–
CDEC1	Decoupling capacitor on VCCD	1.88	4.7	6.58	µF	Capacitor must have initial tolerance range of 4.7 µF ±20%

5.3 Power specifications

Table 24 Power specifications

Note: VDDD = 1.8 V (typ), 1.98 V (max).

Category	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Power specification	FX5_ACTIVE	USB 3.2 Gen 1x1 mode, LVCMOS at 100 MHz SDR	–	430	725	mW	–
	FX5_SUSPEND	U3 Suspend (Deep Sleep), USB3.2 Gen 1x1 in U3, LVDS Port in L3	–	2	–	mW	–
	USB3.2_G1_1_LVDS_1	USB 3.2 Gen 1x1 mode, LVDS at 0.625 Gbps	–	525	810	mW	–
	USB3.2_G1_1_LVCMOS_TX_2	USB 3.2 Gen 1x1 mode, 2x LVCMOS SDR TX Output at 100 MHz SDR	–	590	950	mW	–
	IDLE	Deep Sleep Mode	–	200	–	µW	–
	Power Down	XRES (RESET_N) asserted	–	100	–	µW	–

Table 25 Power specifications

Note: VDDD = 3.3 V (typ), 3.63 V (max).

Category	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Power specification	FX5_ACTIVE	USB 3.2 Gen 1x1 mode, LVCMOS at 100 MHz SDR	–	560	988	mW	–
	FX5_SUSPEND	U3 Suspend (Deep Sleep), USB3.2 Gen 1x1 in U3, LVDS Port shutdown	–	2	–	mW	–
	USB3.2_G1_1_LVDS_1	USB 3.2 Gen 1x1 mode, LVDS at 0.625 Gbps	–	680	1089	mW	–
	USB3.2_G1_1_LVCMOS_TX_2	USB 3.2 Gen 1x1 mode, 2x LVCMOS SDR TX Output at 100 MHz SDR		950	1500	mW	
	IDLE	Deep Sleep mode	–	300	–	µW	–
	Power Down	XRES(RESET_N) asserted	–	200	–	µW	–

5.4 RESETB requirements

Table 26 RESETB requirements

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Vih_RESETB	Input voltage high threshold on RESETB pin	65	–	–	%	CMOS Input, % of VDDD supply
Vil_RESETB	Input voltage low threshold on RESETB pin	–	–	35	%	CMOS Input, % of VDDD supply
Cin_RESETB	Input capacitance on RESETB pin	–	–	7	pF	–
TRESETB	External reset pulse width	1	–	–	µs	–40°C to +85°C TA, all VDDIO
TRESETB_GF	External reset glitch filter period	–	–	20	ns	–40°C to +85°C TA, all VDDIO
RPD_RESETB	Pull-down resistance of RESETB pin	60	85	110	kΩ	–
RESETB_TREADY	Time from RESETB deassertion to device being ready for USB traffic	–	–	32	ms	CMOS Input, % of VDDD supply

5.5 Standard GPIO DC specification

Table 27 Standard GPIO DC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
RPU	Pull-up resistor value	3.5	–	8.5	kΩ	–
RPD	Pull-down resistor value	3.5	–	8.5	kΩ	–
IIL	Input leakage current (absolute value)	-1	–	1	µA	–
CPIN	Maximum pin capacitance	–	–	9.5	pF	–
Vih_gpio	Input voltage HIGH level	0.65 × VDDIO	–		V	–
Vil_gpio	Input voltage LOW level	–	–	0.35 × VDDIO	V	–
FGPIO_OUT0_v1p8	Output frequency at 1.8 V, drive_sel<1:0>= 00, slow=0	–	–	30	MHz	Load 25 pF, 90%/10%

Table 27 Standard GPIO DC specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FGPIO_OUT1_v1p8	Output frequency at 1.8 V, drive_sel<1:0>= 01, slow=0	–	–	15	MHz	Load 25 pF, 90%/10%
FGPIO_OUT2_v1p8	Output frequency at 1.8 V, drive_sel<1:0>= 10, slow=0	–	–	7.5	MHz	Load 25 pF, 90%/10%
FGPIO_OUT3_v1p8	Output frequency at 1.8 V, drive_sel<1:0>= 11, slow=0	–	–	2.5	MHz	Load 25 pF, 90%/10%
FGPIO_OUT0_v2p5	Output frequency at 2.5 V, drive_sel<1:0>= 00, slow=0	–	–	40	MHz	Load 25 pF, 90%/10%
FGPIO_OUT1_v2p5	Output frequency at 2.5 V, drive_sel<1:0>= 01, slow=0	–	–	20	MHz	Load 25 pF, 90%/10%
FGPIO_OUT2_v2p5	Output frequency at 2.5 V, drive_sel<1:0>= 10, slow=0	–	–	12.5	MHz	Load 25 pF, 90%/10%
FGPIO_OUT3_v2p5	Output frequency at 2.5 V, drive_sel<1:0>= 11, slow=0	–	–	5	MHz	Load 25 pF, 90%/10%
FGPIO_OUT0_v3p3	Output frequency at 3.3 V, drive_sel<1:0>= 00, slow=0	–	–	50	MHz	Load 25 pF, 90%/10%
FGPIO_OUT1_v3p3	Output frequency at 3.3 V, drive_sel<1:0>= 01, slow=0	–	–	25	MHz	Load 25 pF, 90%/10%
FGPIO_OUT2_v3p3	Output frequency at 3.3 V, drive_sel<1:0>= 10, slow=0	–	–	15	MHz	Load 25 pF, 90%/10%
FGPIO_OUT3_v3p3	Output frequency at 3.3 V, drive_sel<1:0>= 11, slow=0	–	–	7.5	MHz	Load 25 pF, 90%/10%
FGPIO_IN	GPIO input operating frequency	–	–	50	MHz	–
IOH_v1p8_0	1.8 V pull-up current, DS=0	–2.12	–4	–5.88	mA	–
IOH_v1p8_1	1.8 V pull-up current, DS=1	–1.06	–2	–2.94	mA	–
IOH_v1p8_2	1.8 V pull-up current, DS=2	–0.8	–1.5	–2.2	mA	–
IOH_v1p8_3	1.8 V pull-up current, DS=3	–0.27	–0.5	–0.73	mA	–
IOH_v2p5_0	2.5 V pull-up current, DS=0	–3.18	–6	–8.82	mA	–
IOH_v2p5_1	2.5 V pull-up current, DS=1	–1.59	–3	–4.41	mA	–
IOH_v2p5_2	2.5 V pull-up current, DS=2	–1.06	–2	–2.94	mA	–
IOH_v2p5_3	2.5 V pull-up current, DS=3	–0.4	–0.75	–1.1	mA	–
IOH_v3p3_0	3.3 V pull-up current, DS=0	–4.24	–8	–11.76	mA	–
IOH_v3p3_1	3.3 V pull-up current, DS=1	–2.12	–4	–5.88	mA	–
IOH_v3p3_2	3.3 V pull-up current, DS=2	–1.59	–3	–4.41	mA	–
IOH_v3p3_3	3.3 V pull-up current, DS=3	–0.53	–1	–1.47	mA	–
IOL_v1p8_0	1.8 V pull-down current, DS=0	2.12	4	5.88	mA	–
IOL_v1p8_1	1.8 V pull-down current, DS=1	1.06	2	2.94	mA	–
IOL_v1p8_2	1.8 V pull-down current, DS=2	0.8	1.5	2.2	mA	–
IOL_v1p8_3	1.8 V pull-down current, DS=3	0.27	0.5	0.73	mA	–
IOL_v2p5_0	2.5 V pull-down current, DS=0	3.18	6	8.82	mA	–
IOL_v2p5_1	2.5 V pull-down current, DS=1	1.59	3	4.41	mA	–
IOL_v2p5_2	2.5 V pull-down current, DS=2	1.06	2	2.94	mA	–
IOL_v2p5_3	2.5 V pull-down current, DS=3	0.4	0.75	1.1	mA	–

Table 27 Standard GPIO DC specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
IOL_v3p3_0	3.3 V pull-down current, DS=0	4.24	8	11.76	mA	–
IOL_v3p3_1	3.3 V pull-down current, DS=1	2.12	4	5.88	mA	–
IOL_v3p3_2	3.3 V pull-down current, DS=2	1.59	3	4.41	mA	–
IOL_v3p3_3	3.3 V pull-down current, DS=3	0.53	1	1.47	mA	–
TRF_v1p8	Output rise/fall time at 1.8 V, drive_sel<1:0>= 11, slow=0	–	–	50	ns	–
TRF_v3p3	Output rise/fall time at 3.3 V, drive_sel<1:0>= 00, slow=0	–	–	7	ns	–
IIHS	IO pin current when Vpad is ramped up from 0 to 3.63 V and VDDIO = 0, T = 25°C	–	–	1	µA	–

5.6 SWD and trace interface specification

Table 28 SWD and trace interface specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
F_SWDCLK	SWD input clock frequency	–	–	25	MHz	1.62 V ≤ VDDIO ≤ 3.63 V
T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T_SWDO_VALID	T = 1/f SWDCLK		–	0.50 × T	ns	–
T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–
F_TRCLK_LP1	With trace data setup/hold times of 2/1 ns respectively	–	–	48	MHz	–
F_TRCLK_LP2	With trace data setup/hold times of 3/2 ns respectively	–	–	48	MHz	–
SWD_INPUT_ TRANSITION_TIME	SWD input transition time	–	–	5	ns	–
TRACE_CLKL	Trace clock LOW Period	2	–	–	ns	–
TRACE_CLKH	Trace clock HIGH Period	2	–	–	ns	–
TRACE_CLKL	Trace clock minimum pulse-width LOW	8	–	–	ns	–
TRACE_CLKH	Trace clock minimum pulse-width HIGH	8	–	–	ns	–

5.7 Precise power-on reset (POR) specification

Table 29 POR with brownout DC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VFALLPPOR	BOD trip voltage in Active and Sleep modes VDDD	1.45	–	–	V	BOD reset guaranteed for levels < 1.45 V
VFALLDPSLP	BOD trip voltage in Deep Sleep VDDD	1.45	–	–	V	–
VDDRAMP	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	Active mode

Table 30 POR with brownout AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VDDRAMP_DS	Maximum power supply ramp rate (any supply) in Deep Sleep	–	–	12.5	mV/µs	BOD operation guaranteed

5.8 XTAL / clock specification

Table 31 XTAL / clock specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
EXT_CRY_RES_FREQ	External crystal resonator frequency	–	24	–	MHz	Resonator reference clock frequency. Fundamental oscillation mode
EXT_CRY_RES_FREQ_TOL	External crystal resonator frequency tolerance	–30	–	30	ppm	Resonator reference clock accuracy
EXT_CRY_RES_CLOAD	External crystal resonator load capacitance	–	9.5	–	pF	PCB load
EXT_CRY_RES_CSHUNT	External crystal resonator shunt capacitance	–	0.4	1	pF	No ground connection
EXT_CRY_RESCMOTIONAL	External crystal resonator motional capacitance	–	–	3	pF	No ground connection
EXT_CRY_RES_ESR	External crystal resonator ESR	–	–	60	Ω	Equivalent sales resistance
EXT_CRY_RES_PDRIVE	Drive level for external crystal oscillator	–	50	200	µW	Resonator drive level
EXT_CRY_RES_START	External crystal resonator start-up time	–	–	1.6	ms	Maximum start-up time required by resonator to meet the USB 2.0 timing requirements.

5.9 Single-ended LVCMOS reference clock specification

Table 32 Single-ended LVCMOS reference clock input specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
LVCMOS_ REFCLK_FREQ	LVCMOS reference clock frequency	–	24	–	MHz	–
LVCMOS_ REFCLK_ FREQ_TOL	LVCMOS reference clock frequency tolerance	–30	–	30	ppm	–
LVCMOS_ REFCLK_ FREQ_DUTY	LVCMOS reference clock frequency duty cycle	40	–	60	%	–
LVCMOS_ REFCLK_VIH	Input voltage HIGH threshold for LVCMOS reference clock	0.65*VDDIO	–	–	V	–
LVCMOS_ REFCLK_VIL	Input voltage LOW threshold for LVCMOS reference clock	–	–	0.35*VDDIO	V	–
LVCMOS_ REFCLK_CIN	Input capacitance for LVCMOS reference clock	–	–	7	pF	–

Table 33 Single-ended CMOS reference clock input phase noise requirement

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
IN_PH_NOISE_100	Maximum input phase noise at 100-Hz offset	–	–	–75	dBc/Hz	–
IN_PH_NOISE_1K	Maximum input phase noise at 1-kHz offset	–	–	–104	dBc/Hz	–
IN_PH_NOISE_10K	Maximum input phase noise at 10-kHz offset	–	–	–120	dBc/Hz	–
IN_PH_NOISE_100K	Maximum input phase noise at 100-kHz offset	–	–	–128	dBc/Hz	–
IN_PH_NOISE_1M	Maximum input phase noise at 1-MHz offset	–	–	–130	dBc/Hz	–

5.10 USB 2.0 PHY specification

Table 34 USB 2.0 PHY HS TX pre-emphasis

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
USB_2_PHY_HS_TX_AMP_0011	USB 2.0 PHY HS TX amplitude for register setting = 0011	720	800	880	mV	–
USB_2_PHY_HS_TX_AMP_0101	USB 2.0 PHY HS TX amplitude for register setting = 0101	756	840	924	mV	–
USB_2_PHY_HS_TX_AMP_0111	USB 2.0 PHY HS TX amplitude for register setting = 0111	792	880	968	mV	–
USB_2_PHY_HS_TX_AMP_1011	USB 2.0 PHY HS TX amplitude for register setting = 1011	864	960	1056	mV	–
USB_2_PHY_HS_TX_PREMP_010	USB 2.0 PHY HS TX pre-emphasis for register setting = 010	0.83	1.5	1.78	dB	–
USB_2_PHY_HS_TX_PREMP_100	USB 2.0 PHY HS TX pre-emphasis for register setting = 100	2.28	2.9	3.52	dB	–
USB_2_PHY_HS_TX_PREMP_110	USB 2.0 PHY HS TX pre-emphasis for register setting = 110	3.23	4	4.6	dB	–

Table 35 USB 2.0 PHY HS TX pre-emphasis duration

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
USB_2_PHY_HS_TX_PREMP_D_00	USB 2.0 PHY HS TX pre-emphasis duration for register setting = 00	–	0	–	UI	0 = Disabled
USB_2_PHY_HS_TX_PREMP_D_01	USB 2.0 PHY HS TX pre-emphasis duration for register setting = 01	0.2	0.25	0.3	UI	–
USB_2_PHY_HS_TX_PREMP_D_10	USB 2.0 PHY HS TX pre-emphasis duration for register setting = 10	0.45	0.5	0.55	UI	–
USB_2_PHY_HS_TX_PREMP_D_11	USB 2.0 PHY HS TX pre-emphasis duration for register setting = 11	0.7	0.75	0.8	UI	–

Table 36 USB 2.0 PHY HS TX slew rate

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
USB_2_PHY_HS_TX_SLRA_00	USB 2.0 PHY HS TX slew rate for register setting = 00	100	300	460	ps	Guaranteed by characterization
USB_2_PHY_HS_TX_SLRA_01	USB 2.0 PHY HS TX slew rate for register setting = 01	–	375	560	ps	Guaranteed by characterization
USB_2_PHY_HS_TX_SLRA_10	USB 2.0 PHY HS TX slew rate for register setting = 10	–	450	680	ps	Guaranteed by characterization
USB_2_PHY_HS_TX_SLRA_11	USB 2.0 PHY HS TX slew rate for register setting = 11	–	525	800	ps	Guaranteed by characterization

Table 37 USB 2.0 PHY host disconnect thresholds

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
USB_2_PHY_DISC_TH_0000	USB 2.0 PHY host disconnect threshold for register setting = 0000	525	575	625	mV	%△ USB 2.0 spec = 0.0 mV
USB_2_PHY_DISC_TH_0100	USB 2.0 PHY host disconnect threshold for register setting = 0100	605	660	715	mV	%△ USB 2.0 spec = 15.2 mV
USB_2_PHY_DISC_TH_1000	USB 2.0 PHY host disconnect threshold for register setting = 1000	685	745	805	mV	%△ USB 2.0 spec = 30.4 mV
USB_2_PHY_DISC_TH_1100	USB 2.0 PHY host disconnect threshold for register setting = 1100	765	830	895	mV	%△ USB 2.0 spec = 45.6 mV

Table 38 USB 2.0 PHY squelch detection thresholds

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
USB_2_PHY_SQ_DET_1	USB 2.0 PHY squelch detection threshold for setting 1, Register = 1011	130	155	195	mV	–
USB_2_PHY_SQ_DET_3	USB 2.0 PHY squelch detection threshold for setting 3, Register = 1001	115	140	172.5	mV	–
USB_2_PHY_SQ_DET_5	USB 2.0 PHY squelch detection threshold for setting 5, Register = 0111	100	125	150	mV	–
USB_2_PHY_SQ_DET_7	USB 2.0 PHY squelch detection threshold for setting 7, Register = 0101	85	110	135	mV	–

Table 39 USB 2.0 PHY HS CTLE equalization

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
USB_2_PHY_HS_CTLE_000	USB 2.0 PHY HS CTLE equalization for register setting = 000	–0.2	0	0.2	dB	Typical value at 240 MHz. Guaranteed by characterization
USB_2_PHY_HS_CTLE_010	USB 2.0 PHY HS CTLE equalization for register setting = 010	0.7	1.1	1.75	dB	–
USB_2_PHY_HS_CTLE_100	USB 2.0 PHY HS CTLE equalization for register setting = 100	1.6	2.2	2.9	dB	–
USB_2_PHY_HS_CTLE_110	USB 2.0 PHY HS CTLE equalization for register setting = 110	2.8	3.4	4.4	dB	–

5.11 LVDS specifications

Table 40 LVDS electrical specifications

Note: For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can be at either 1.8 V or 3.3 V depending on the desired CTRL signal logic level.

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VCM	LVDS common mode voltage range	0.05	–	2.35	V	–
|VID|	LVDS differential input voltage (Magnitude)	100	–	–	mV	–
II	LVDS receiver input current (Magnitude)	–	–	20	µA	–
II_BALANCE	LVDS receiver input current balance (Magnitude)	–	–	6	µA	–
ZIP	LVDS receiver input impedance	90	–	132	Ω	–
VCM_SUB	SubLVDS common mode voltage range	0.4	–	1.4	V	–
|VID_SUB|	SubLVDS differential input voltage (Magnitude)	100	–	–	mV	–
ZIP	SubLVDS receiver input impedance	80	–	120	Ω	–

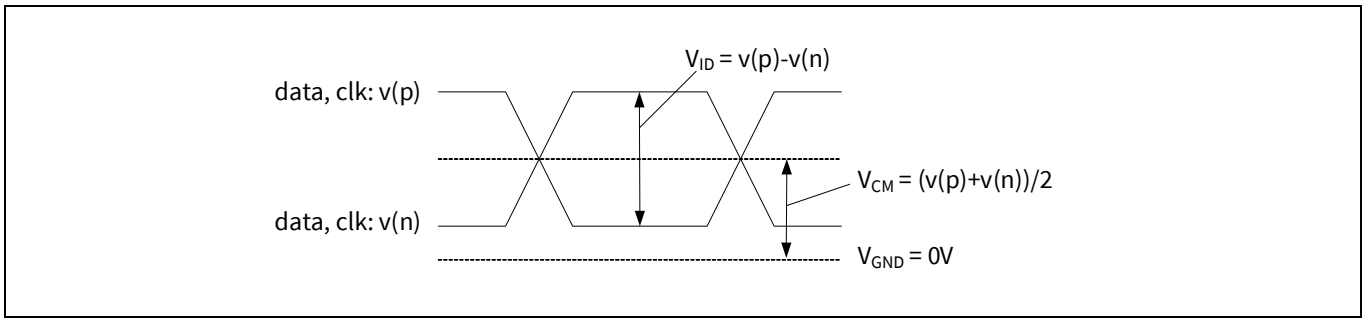


Figure 7 LVDS VCM and VID illustration

Table 41 LVDS timing specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
fLVDS_FREQ	LVDS RX clock input frequency	74.25		625	MHz	–
tLVDS_CLK	LVDS RX clock input period	1.6		13.46	ns	–
GR	Gearing ratio	1:1 2:1 4:1 8:1			–	–
tLVDS_UI	LVDS RX unit interval	tLVDS_CLK/GR			ns	Depends on GR
tLVDS_CH	LVDS RX clock HIGH time	45	–	55	%tLVDS_CLK	–
tLVDS_CD_skew_HF	LVDS RX clock-to-data skew, ≥ 400 Mbps per lane	–3	–	3	tLVDS_UI	Data unit interval, which is duration of 1-bit of lane interface data rate. Example: for 625 MHz, 2:1 gearing UI = 800 ps
tLVDS_CD_skew_LF	LVDS RX clock-to-data skew, < 200 Mbps per lane	–0.25	–	0.25	tLVDS_UI	
tLVDS_CD_skew_MF	LVDS RX clock-to-data skew, 200 Mbps ≤ data rate < 400 Mbps per lane	–3	–	3	tLVDS_UI	
tLVDS_CD_skew_MF_LP	LVDS RX clock-to-data skew, 200 Mbps ≤ data rate < 400 Mbps per lane, low-power mode	–0.25	–	0.25	tLVDS_UI	

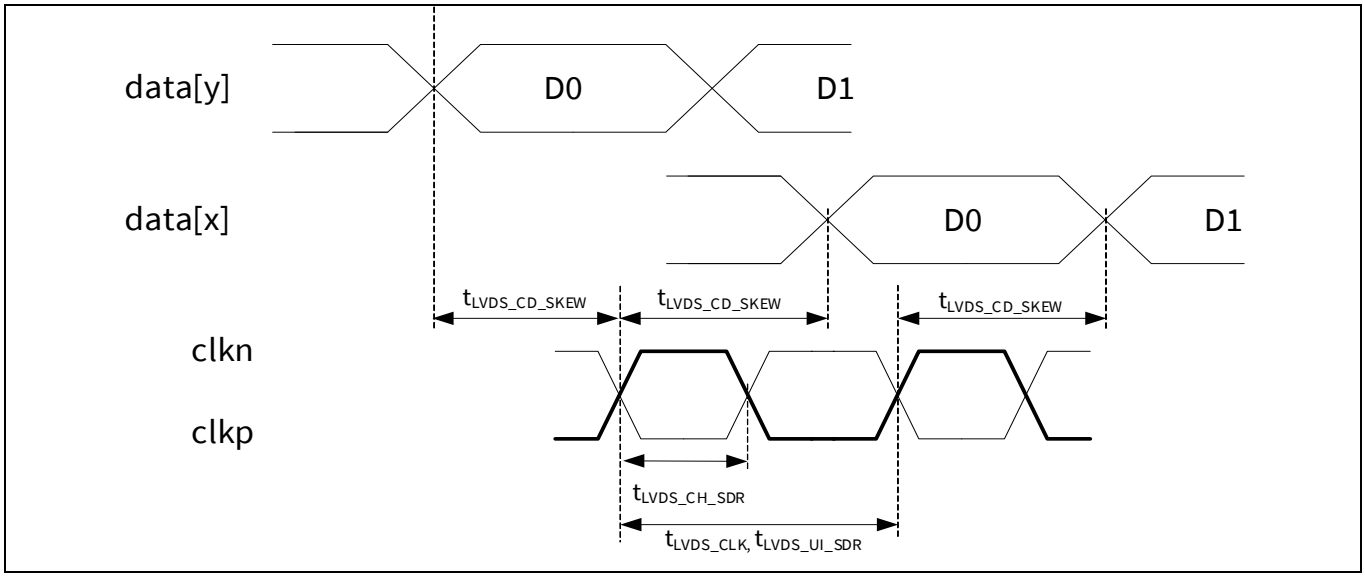


Figure 8 LVDS SDR clock and data timing

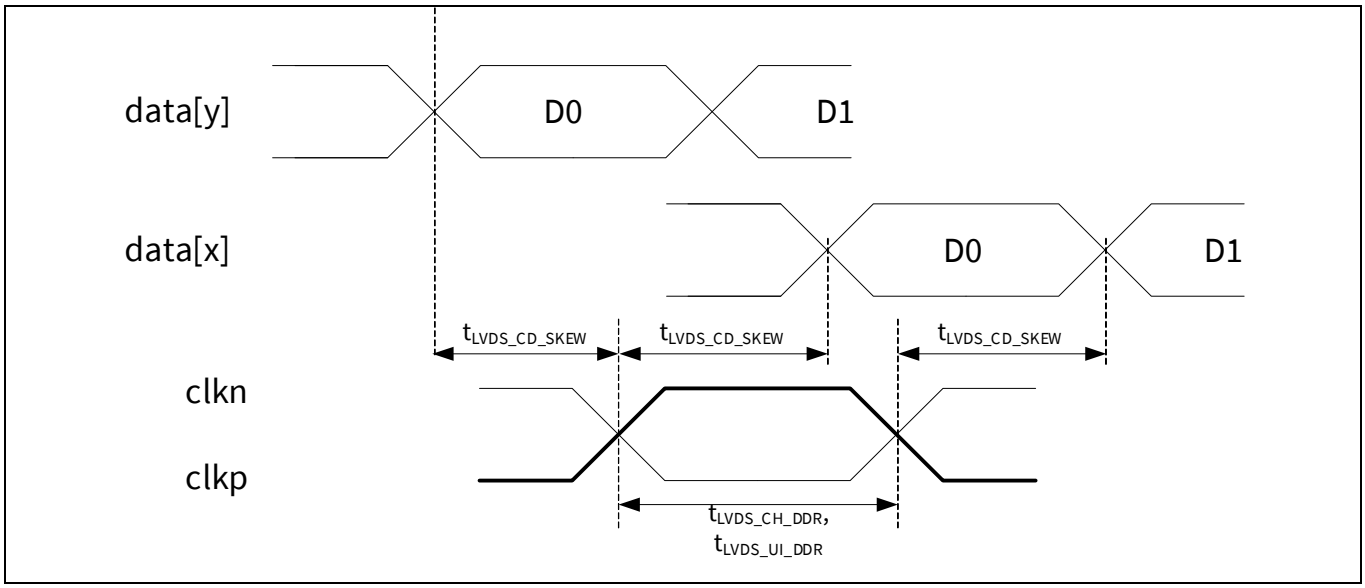


Figure 9 LVDS DDR clock and data timing

5.12 LVCMOS specification

Table 42 LVCMOS electrical parameter specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VOH_LVCMOS	Output HIGH voltage	75	–	–	%VDDIO	–
VOL_LVCMOS	Output LOW voltage	–	–	25	%VDDIO	–
IIH_LVCMOS	Input HIGH current	–	–	1	µA	–
IIL_LVCMOS	Input LOW current	–	–	1	µA	–
VIH_LVCMOS	Input HIGH level	65	–	–	%VDDIO	–
VIL_LVCMOS	Input LOW level	–	–	35	%VDDIO	–
RHIGH_Z0	Pull-up resistance	40	–	70	Ω	–
RLOW_Z0	Pull-down resistance	40	–	70	Ω	–
IOH_DS0	Output HIGH current at VOH, lowest drive DS0	1.5	–	7	mA	–
IOL_DS0	Output LOW current at VOL, lowest drive DS0	1.5	–	7	mA	–
IOH_DS1	Output HIGH current at VOH, mid drive DS1	3.4	–	14	mA	–
IOL_DS1	Output LOW current at VOL, mid drive DS1	3.4	–	14	mA	–
IOH_DS2	Output HIGH current at VOH, mid drive DS2	5.2	–	20	mA	–
IOL_DS2	Output LOW current at VOL, mid drive DS2	5.2	–	20	mA	–
IOH_DS3	Output HIGH current at VOH, highest drive DS3	7	–	30	mA	–
IOL_DS3	Output LOW current at VOL, highest drive DS3	7	–	30	mA	–

Table 43 LVCMOS SDR input only interface timing specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
fLVCMOS_SDR_I	Clock frequency	–	–	160	MHz	–
tCLK_SDR_I	Clock period	6.25	–	–	ns	–
tCLKH_SDR_I	Clock HIGH time	40	–	60	%tCLK_SDR_I	–
tS_SDR_I	CTL input to clock setup time	2	–	–	ns	–
tH_SDR_I	CTL input to clock hold time	0.5	–	–	ns	–
tDS_SDR_I	Data into clock setup Time	1.75	–	–	ns	–
tDH_SDR_I	Data into clock hold time	0.5	–	–	ns	–

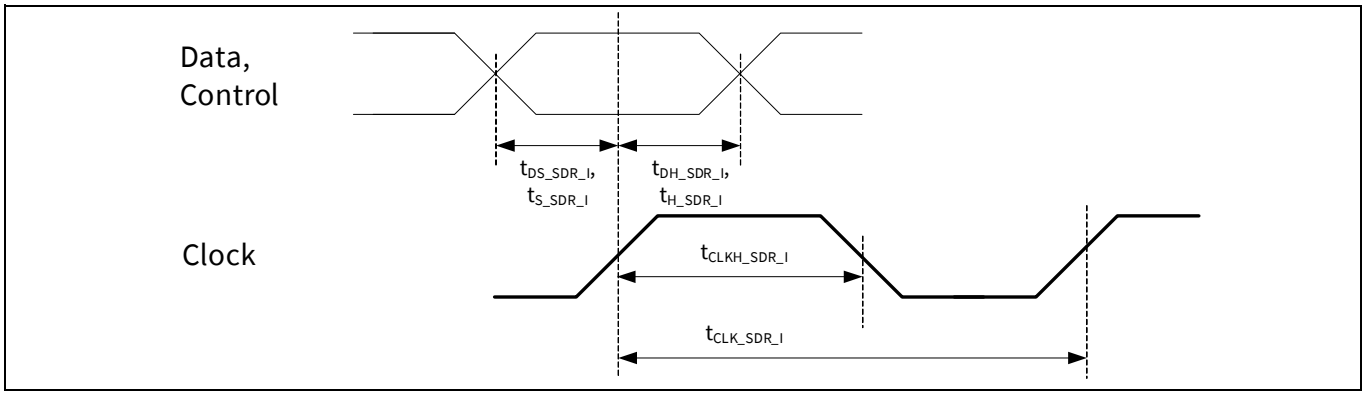


Figure 10 LVCMOS SDR input only clock and data timing

Table 44 LVCMOS DDR input only timing specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
fLVCMOS_DDR	Clock frequency	100	–	160	MHz	–
VIH_DDR_AC	AC Input HIGH level	75	–	–	%VDDIO	–
VIL_DDR_AC	AC Input LOW level	–	–	25	%VDDIO	–
|SR_DDR|	Input slew rate magnitude (VIL_DDR_AC to VIH_DDR_AC)	VDDIO/1.62	–	–	V/ns	–
tCLK_DDR	Clock period	6.25	–	10	ns	–
tCLKH_DDR	Clock HIGH time	45	–	55	%tCLK_DDR	–
tPW_DDR	Data input pulse width	40	–	60	%tCLK_DDR	–
tCD_skew_DDR	Input clock-to-data skew	–12.5	–	12.5	%tCLK_DDR	% OF tCLK_DDR

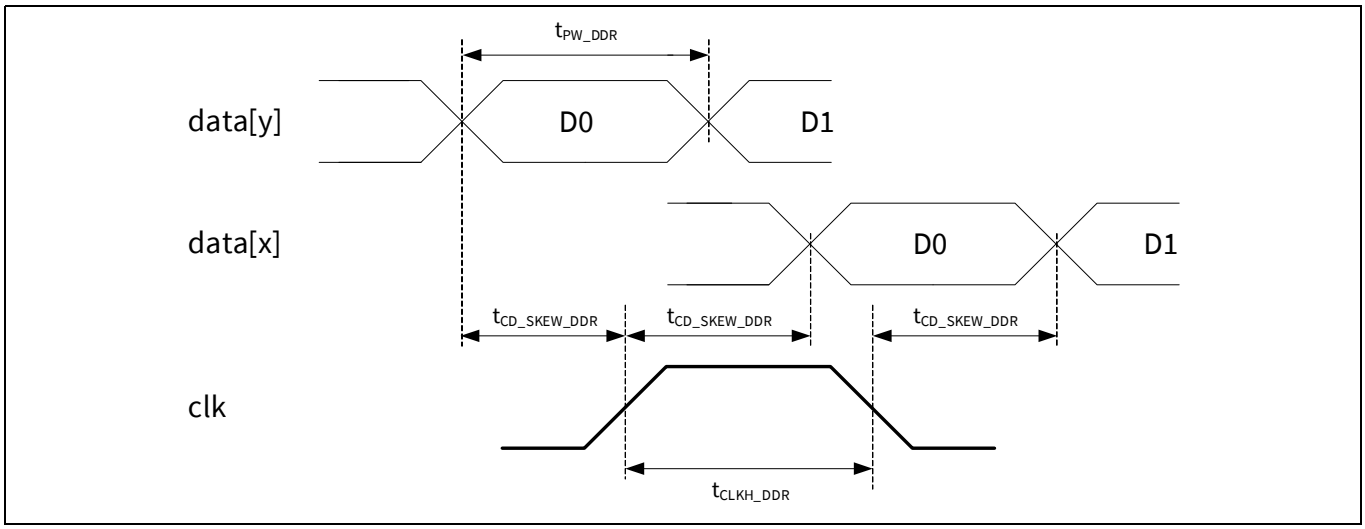


Figure 11 LVCMOS DDR clock and data timing

Table 45 LVCMOS SDR IO interface timing specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
fLVCMOS_SDR_IO	Clock frequency, when interface is used as I/O	–	–	100	MHz	–
tCLK_SDR_IO	Clock period, when interface is used as I/O	10	–	–	ns	–
tCLKH_SDR_IO	Clock high time, when interface is used as I/O	4	–	–	ns	–
tCLKL_SDR_IO	Clock Low time, when interface is used as I/O	4	–	–	ns	–
tS_SDR_IO	CTL Input to clock setup Time, when interface is used as I/O	2	–	–	ns	–
tH_SDR_IO	CTL Input to clock hold Time, when interface is used as I/O	0.5	–	–	ns	–
tDS_SDR_IO	Data in to clock setup time, when interface is used as I/O	2	–	–	ns	–
tDH_SDR_IO	Data in to clock hold time, when interface is used as I/O	0.5	–	–	ns	–
tDO_SDR_IO	Clock to data out propagation delay when DQ bus is already in output direction	–	–	8	ns	–
tCOE_SDR_IO	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus	–	–	8	ns	–
tCO_SDR_IO	Clock to CTL out propagation delay	–	–	8	ns	–
tDOH_SDR_IO	Clock to data out hold	2	–		ns	–
tCOH_SDR_IO	Clock to CTL out hold	2	–		ns	–
tHZ_SDR_IO	Clock to High-Z		–	8	ns	–
tLZ_SDR_IO	Clock to Low-Z	0	–		ns	–

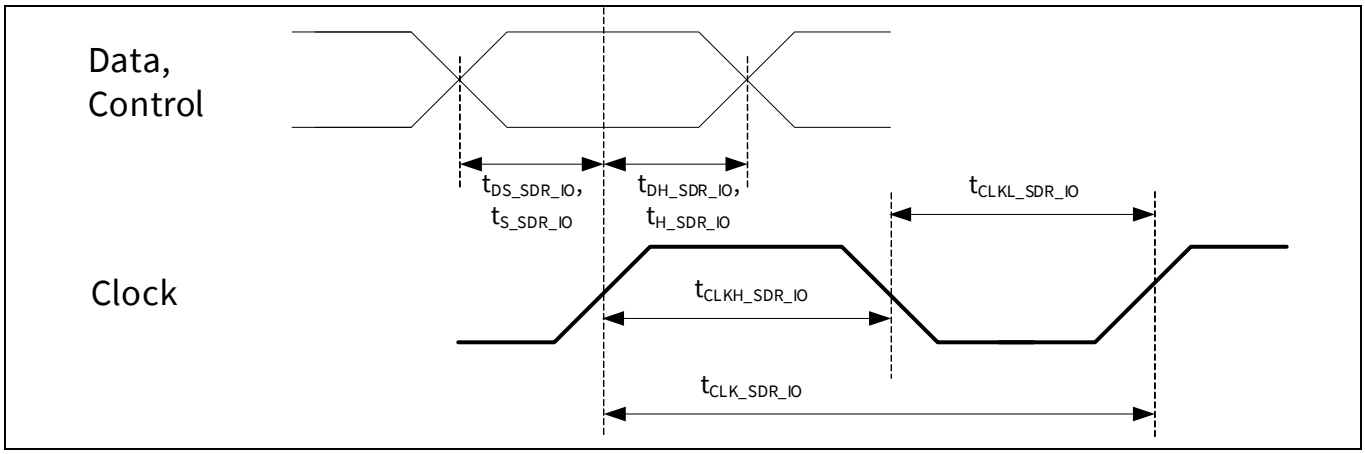


Figure 12 LVCMOS SDR IO clock and data timing

Table 46 LVCMOS SDR timing specifications (Master Mode)

Parameter	Description	Min	Max	Unit
tFREQ_SDR100_MSTR	Clock Frequency, when interface is used as I/O	–	100	MHz
tCLK_SDR100_MSTR	Clock Period, when interface is used as I/O	10	–	ns
tCLK_SDR100_MSTR	Clock High Time, when interface is used as I/O	4	–	ns
tCLK_SDR100_MSTR	Clock Low Time, when interface is used as I/O	4	–	ns
tS_SDR100_MSTR	CTL Input to Clock setup Time, when interface is used as I/O	2.5	–	ns
tH_SDR100_MSTR	CTL Input to Clock Hold Time, when interface is used as I/O	1.0	–	ns
tDS_SDR100_MSTR	Data in to Clock Setup Time, when interface is used as I/O	2.5	–	ns
tDH_SDR100_MSTR	Data in to Clock Hold Time, when interface is used as I/O	1.0	–	ns
tDO_SDR100_MSTR	Clock to data out propagation delay when DQ bus is already in output direction.	–	8	ns
tCOE_SDR100_MSTR	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus.	–	8	ns
tCO_SDR100_MSTR	Clock to CTL out propagation delay	–	8	ns
tDOH_SDR100_MSTR	Clock to data out hold	2	–	ns
tCOH_SDR100_MSTR	Clock to CTL out hold	2	–	ns
tHZ_SDR100_MSTR	Clock to High-Z	–	8	ns
tLZ_SDR100_MSTR	Clock to Low-Z	0	–	ns

Table 47 LVCMOS DDR timing specifications (Master Mode)

Parameter	Description	Min	Max	Unit
tFREQ_DDR80_MSTR	Clock Frequency, when interface is used as I/O	–	80	MHz
tCLK_DDR80_MSTR	Clock Period, when interface is used as I/O	12.5	–	ns
tCLK_DDR80_MSTR	Clock High Time, when interface is used as I/O	5	–	ns
tCLK_DDR80_MSTR	Clock Low Time, when interface is used as I/O	5	–	ns
tS_DDR80_MSTR	CTL Input to Clock Rise setup Time, when interface is used as I/O	2	–	ns
tH_DDR80_MSTR	CTL Input to Clock Rise Hold Time, when interface is used as I/O	0.5	–	ns
tDO_DDR80_MSTR	Clock to data out propagation delay (w.r.t to clock rise and fall edges) when DQ bus is already in output direction.	–	4	ns
tCOE_DDR80_MSTR	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus.	–	4	ns
tCO_DDR80_MSTR	Clock to CTL out propagation delay (w.r.t to clock rise and fall edges)	–	4	ns
tDOH_DDR80_MSTR	Clock to data out hold (w.r.t to clock rise and fall edges)	0.5	–	ns
tCOH_DDR80_MSTR	Clock to CTL out hold (w.r.t to clock rise and fall edges)	0.5	–	ns
tHZ_DDR80_MSTR	Clock to High-Z	–	8	ns
tLZ_DDR80_MSTR	Clock to Low-Z	0	–	ns

5.13 QSPI specifications

Table 48 QSPI specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Fsmifclk	SMIF QSPI output clock frequency	–	–	80	MHz	–
Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	–
Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	–
Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	–
Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	–
Tseloutvalid	Output select valid time with respect to clock rising edge	–	–	7.5	ns	–
Tselouthold	Output select hold time with respect to clock rising edge	0.5 × Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time
Tckpw	Clock pulse width	45	–	55	%	Related to Fsmifclk

5.14 Digital peripherals specifications

Table 49 TCPWM specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TCPWMFREQ	Operating frequency	–	–	100	MHz	Fc max = Fcpu. Maximum = 100 MHz
TPWMENEXT	Input trigger pulse width for all trigger events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected
TPWMEXT	Output trigger pulse widths	1.5/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
TCRES	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
PWMRES	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
QRES	Quadrature inputs resolution	2/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar.

Table 50 UART AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FUART2	Bit rate	–	–	8	Mbps	–

Table 51 SPI AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FSPI	SPI operating frequency master	–	–	25	MHz	–
FSPI_EXT	SPI operating frequency master (Fscb is SPI clock)	–	–	Fscb/4	MHz	Fscb max is 100 MHz
FSPI_IC	SPI slave internally clocked	–	–	15	MHz	–

Table 52 SPI master mode AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TDMO	MOSI valid after Sclock driving edge	–	–	12	ns	–
TDSI	MISO valid before Sclock capturing edge	20	–	–	ns	Full clock, late MISO sampling
THMO	MOSI data hold time	0	–	–	ns	Referred to slave capturing edge
TDHI	SPI master: MISO hold time after SCLK capturing edge	0	–	–	ns	–
TSSELMSCK1	SSEL valid to first SCK valid edge	18	–	–	ns	Referred to master clock edge
TSSELMCK2	SSEL valid to first SCK valid edge	18	–	–	ns	Referred to master clock edge

Table 53 SPI slave mode AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TDMI	MOSI valid before Sclock capturing edge	5	–	–	ns	–
SPI_FREQ	SPI frequency	–	–	25	MHz	–
TDSO_EXT	MISO valid after Sclock driving edge in Ext. Clk. mode	–	–	20	ns	–
TDSO	MISO valid after Sclock driving edge in Internally Clk. mode	–	–	TDSO_EXT + 3 × Tscb	ns	Tscb is serial comm block clock period
TDSO_FILT	MISO valid after Sclock driving edge in Internally Clk. mode with Median filter enabled.	–	–	TDSO_EXT + 4 × Tscb	ns	Tscb is serial comm block clock period
THSO	Previous MISO data hold time	5.5	–	–	ns	–
THIS	SPI MOSI hold from SCLK	–		14	ns	–
CSPI	SPI capacitive load		10	–	pF	–
TSSELSCK1	SSEL valid to first SCK valid edge	65	–	–	ns	–
TSSELSCK2	SSEL Hold after last SCK valid edge	65	–	–	ns	–

5.15 Audio subsystem specifications

Table 54 PDM specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Fmax_clk_if_srss	Clock frequency for audio clock reference clk_if_srss	–	48	–	MHz	–
T_SETUP	Receiver setup	–	–	10	ns	–
PDM_HOLD	Data input hold time to PDM_CLK edge	10	–	–	ns	–
CPDM	Load	–	10	–	pF	–
PDM_OUT	Audio sample rate	8	–	48	ksps	–
PDM_WL	Word length	16	–	24	bits	–
PDM_SNR	Signal-to-noise ratio (A-weighted)	–	100	–	dB	PDM input, 20 Hz to 20 kHz BW
PDM_DR	Dynamic Range (A-weighted)	–	100	–	dB	20 Hz to 20 kHz BW, –60 dB FS
PDM_SB	Stop band	–	0.566	–	f	DC to 0.45 f. DC blocking filter OFF
PDM_SBA	Stop band attenuation	–	60	–	dB	–
PDM_GAIN	Adjustable gain	–12	–	10.5	dB	–
PDM_ST	Start-up time	–	48	–	WS cycles	PDM to PCM, 1.5 dB/step

Table 55 I2S specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I2S_WORD	Length of I2S word	8	–	32	bits	–
I2S_BCK_F	Bit clock frequency	–	–	12.288	MHz	–
I2S_BCK_P	Bit clock period	–	1/I2S_BCK_F	–	ns	Guaranteed by design. No feature is used for low frequency I2S operation. DUT RX master: RX_IF_CTL.LATE_SAMPLE = 0 RX_IF_CTL.LATE_CAPTURE = “00” DUT TX Slave: No special configuration DUT RX slave: RX_IF_CTL.LATE_SAMPLE = 0
I2S_WS_FREQ	Word clock frequency	–	–	192	kHz	–
I2S_BCK_TL	Bit clock LOW period	0.35 × I2S_BCK_P	–	–	ns	–
I2S_BCK_TH	Bit clock HIGH period	0.35 × I2S_BCK_P	–	–	ns	–
I2S_MCKI_TL	Master clock IN LOW period	0.45 × tMCLK	–	–	ns	–

Table 55 I2S specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I2S_MCKI_TH	Master clock IN HIGH period	0.45 × tMCLK	–	–	ns	–
I2S_MCKO_TL	Master clock OUT LOW period	0.45 × tMCLK	–	–	ns	–
I2S_MCKO_TH	Master clock OUT HIGH period	0.45 × tMCLK	–	–	ns	–
TDM_ OUTPUT_ LOAD_MAX	Capacitive load	10	–	–	pF	–
tMCLK	Master clock period	20.83	–	–	ns	–

Table 56 I2S slave mode specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I2S_S_TS_WS	WS setup time before the first edge following the driving edge of Bit Clock for LP mode	0.2 × I2S_BCK_P	–	–	ns	Guaranteed by design. Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE or SCK_POLARITY setting
I2S_S_TH_WS	WS hold time after the first edge following the driving edge of Bit Clock, LP mode	0	–	–	ns	Guaranteed by design. Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 × tSCLK) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 00 RX-Slave: SCK_POLARITY = 0
I2S_S_SDO	SDO propagation delay from driving edge of Bit clock for LP mode	0	–	0.8 × I2S_BCK_P	ns	–

Table 57 I2S master mode specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I2S_M_WS	WS propagation delay from driving edge of Bit Clock for LP Mode	0	–	0.2 × I2S_BCK_P	ns	–
I2S_M_SDO	SDO Propagation delay from driving edge of Bit clock for LP mode	0	–	0.2 × I2S_BCK_P	ns	–

5.16 JTAG specifications

Table 58 JTAG specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TCKLOW	TCK LOW minimum	34	–	–	ns	–
TCKHIGH	TCK HIGH	10	–	–	ns	–
TCKPERIOD	CLK_JTAG_PERIOD, 30 pF load	–	44		MHz	–
TCK_TDO	TDO clock-to-out (maximum) from falling TCK	–	–	22	ns	–
TSU_TCK	TDI, TMS setup time before rising TCK	12	–	–	ns	–
TCk_THD	TDI, TMS hold time after rising TCK	10	–	–	ns	–
TCK_TDOV	TCK to TDO data valid (High-Z to active)	22	–	–	ns	–
TCK_TDOZ	TCK to TDO data valid (active to High-Z)	22	–	–	ns	–
JTAG_TDO _HOLD	JTAG TDO hold time	–	–	5	ns	–
JTAG_INPUT_ TRANSITION_ TIME	JTAG input transition time	–	–	5	ns	–

5.17 SSRS specifications

Table 59 IMO AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FIMOTOL1	Frequency variation centered on 8 MHz	–2	–	2	%	–
TJITR	Cycle-to-cycle and period jitter	–	–	250	ps	–

Table 60 ILO AC specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TSTARTILO1	ILO start-up time	–	–	7	µs	Start-up time to 95% of final frequency
TLIODUTY	ILO duty cycle	45	50	55	%	–
FILOTRIM1	32 kHz trimmed frequency	–10	–	10	%	28.8 kHz to 35.2 kHz (±10% variation)

Table 61 Frequency locked loop (FLL) specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FLL_RANGE	Input frequency range	0.04	–	96	MHz	Upper limit is for external input
FLL_OUT_DIV2	Output frequency range	24	–	96	MHz	Output range of FLL divided-by-2 output
FLL_DUTY_DIV2	Divided-by-2 output; HIGH or LOW	47	–	53	%	–
FLL_WAKEUP	Time from stable input clock to 1% of final value on Deep Sleep wakeup	–	–	11	µs	With IMO input, for <10°C change in temperature while in Deep Sleep and Fout ≥ 50 MHz
FLL_JITTER	Period jitter (1 sigma) at 96 MHz	–	–	45	ps	–

Table 62 External clock specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TSTARTILO1	ILO Start-up time	–	–	7	µs	–
TLIODUTY	ILO Duty cycle	45	50	55	%	–
FILOTRIM1	32 kHz trimmed frequency	–10	–	10	%	–

5.18 Flash specification

Table 63 Flash specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TROWWRITE	Row write item (erase and program)	–	–	16	ms	–
TROWERASE	Row erase time	–	–	11	ms	–
TROWPROGRAM	Row program time after erase	–	–	5	ms	–
TBULKERASE	Bulk erase time (2048 KB)	–	–	11	ms	–
TSECTORERASE	Sector erase time (256 KB)	–	–	11	ms	–
TSSERIAE	Sub-sector erase time	–	–	11	ms	–
TSSWRITE	Sub-sector erase time; 1 erase plus 8 program times	–	–	51	ms	–
TSWRITE	Total device write time	–	–	2.6	s	–
TDEVPROG	Sub-sector write time; 1 erase plus 512 program times	–	–	30	s	–
FEND	Flash endurance	100K	–	–	cycles	–
FRET1	Flash retention. TA <= 25°C, 100K P/E cycles	10	–	–	yrs	–
FRET2	Flash retention. TA <= 85°C, 10K P/E cycles	10	–	–	yrs	–
FRET3	Flash retention. TA <= 55°C, 20K P/E cycles	20	–	–	yrs	–
TWS100	Number of wait states at 100 MHz	300%	–	–	–	–

6 Timing and electrical diagrams

6.1 LVCMOS SDR IO synchronous mode GPIF III timing

This section describes the generic slave FIFO interface diagrams.

6.1.1 LVCMOS SDR IO GPIF III interface example

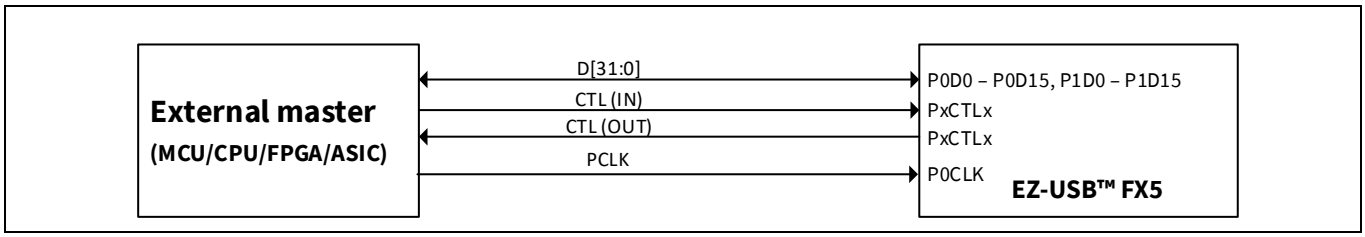


Figure 13 LVCMOS SDR IO GPIF III interface example

6.1.2 GPIF III timing in LVCMOS SDR IO synchronous mode

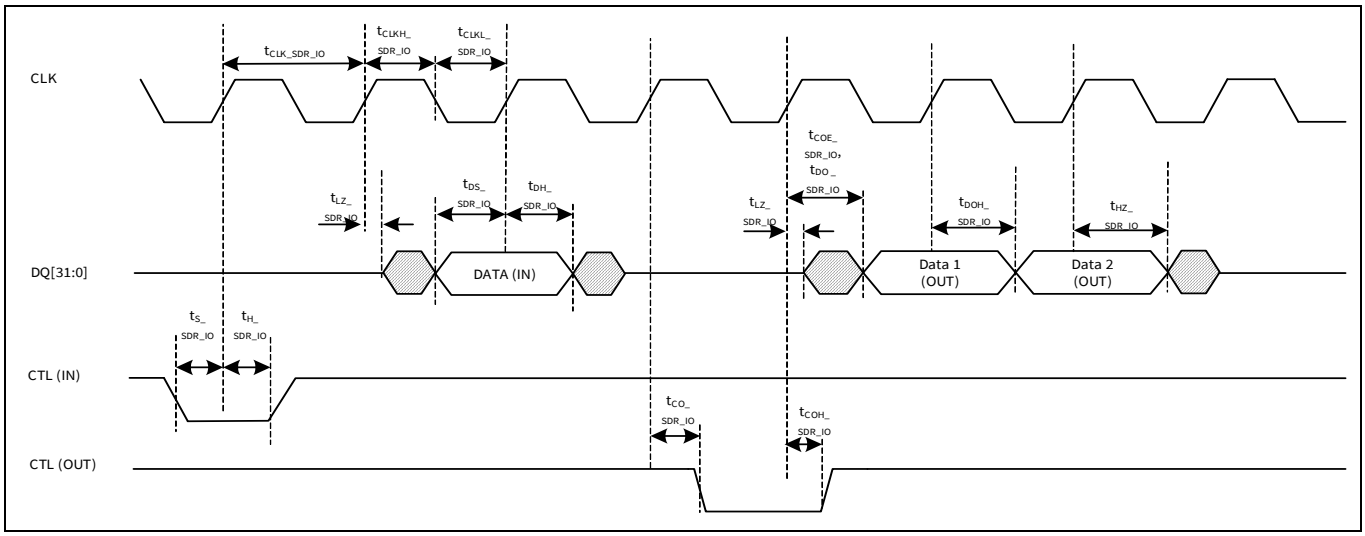
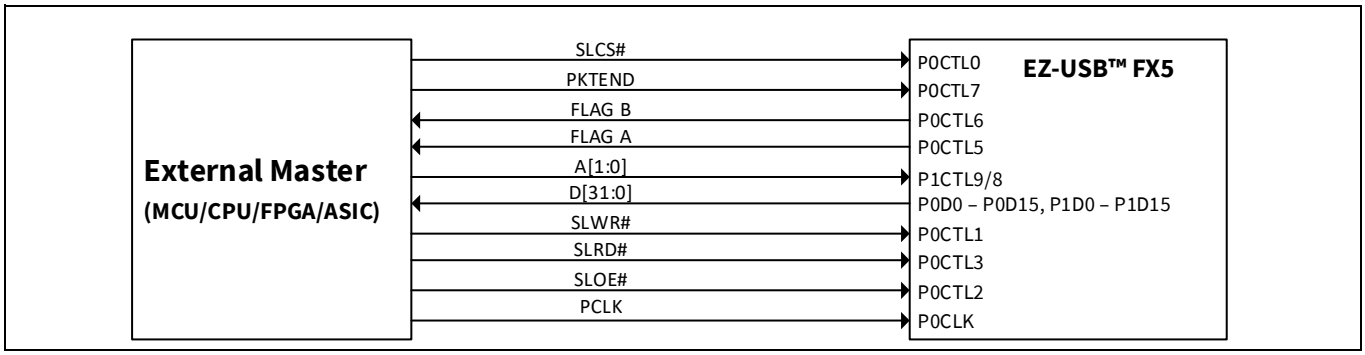


Figure 14 GPIF III timing in LVCMOS SDR IO synchronous mode (see Table 45)

6.1.3 Slave FIFO read interface example



6.1.4 Synchronous SDR slave FIFO read mode

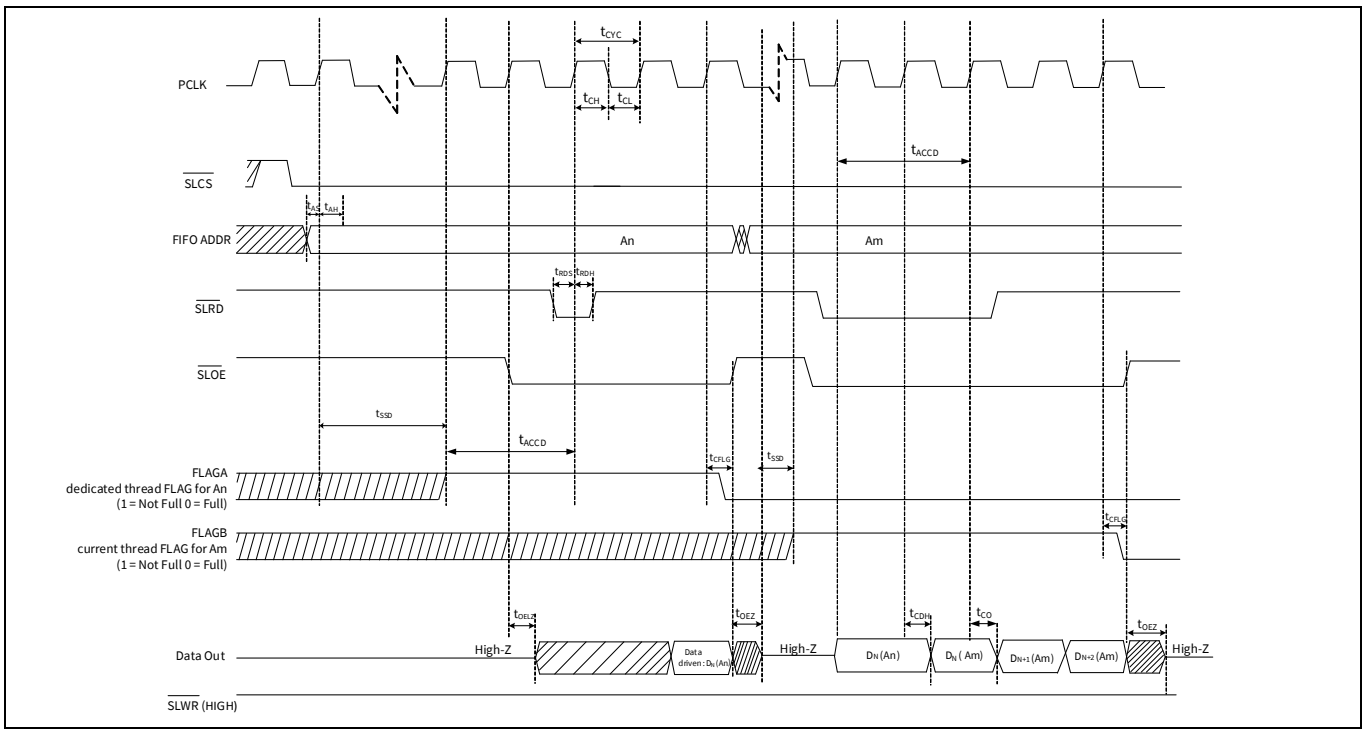


Figure 15 Synchronous SDR slave FIFO read cycle timing

6.1.5 Slave FIFO write interface example

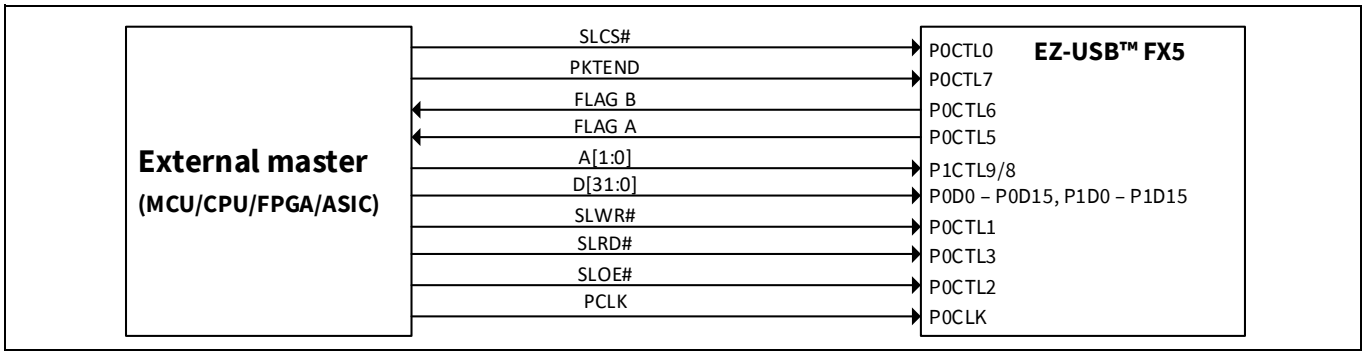


Figure 16 Slave FIFO write interface example

6.1.6 Synchronous SDR slave FIFO write mode

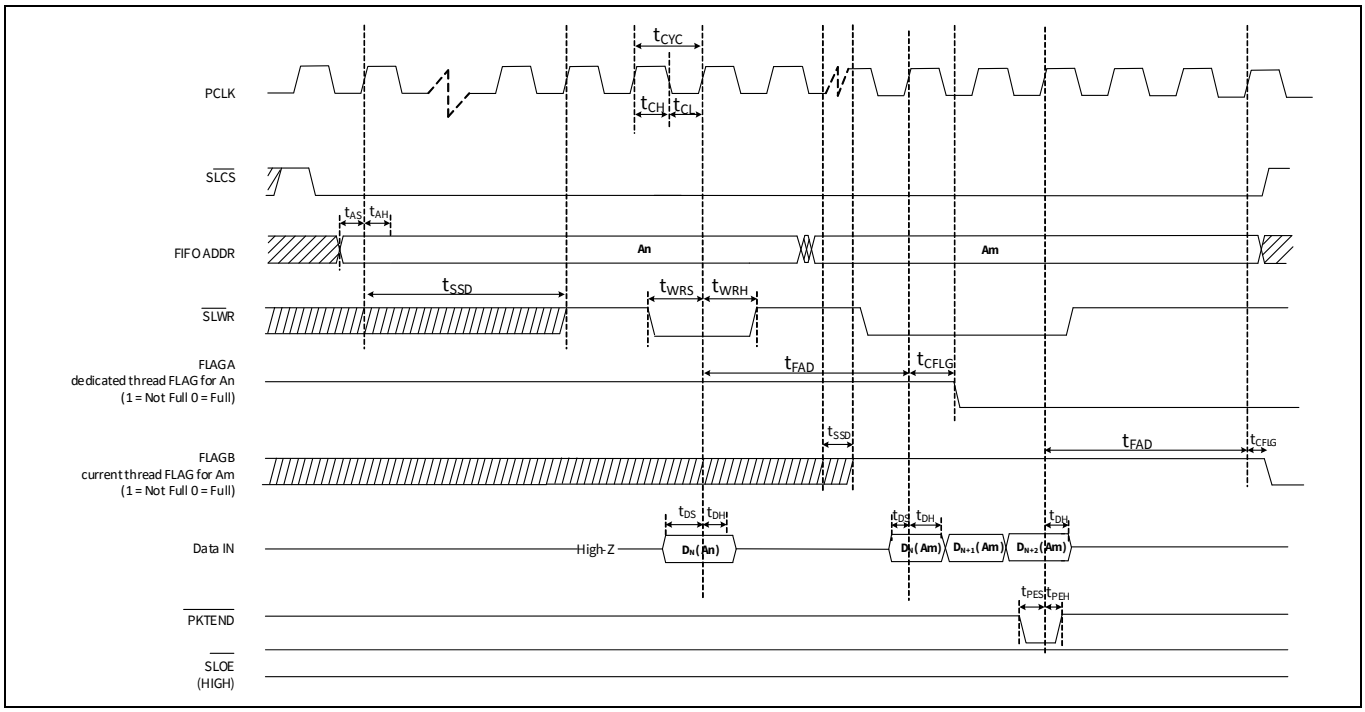


Figure 17 Synchronous SDR slave FIFO write cycle timing

6.1.7 Synchronous SDR slave FIFO ZLP write mode

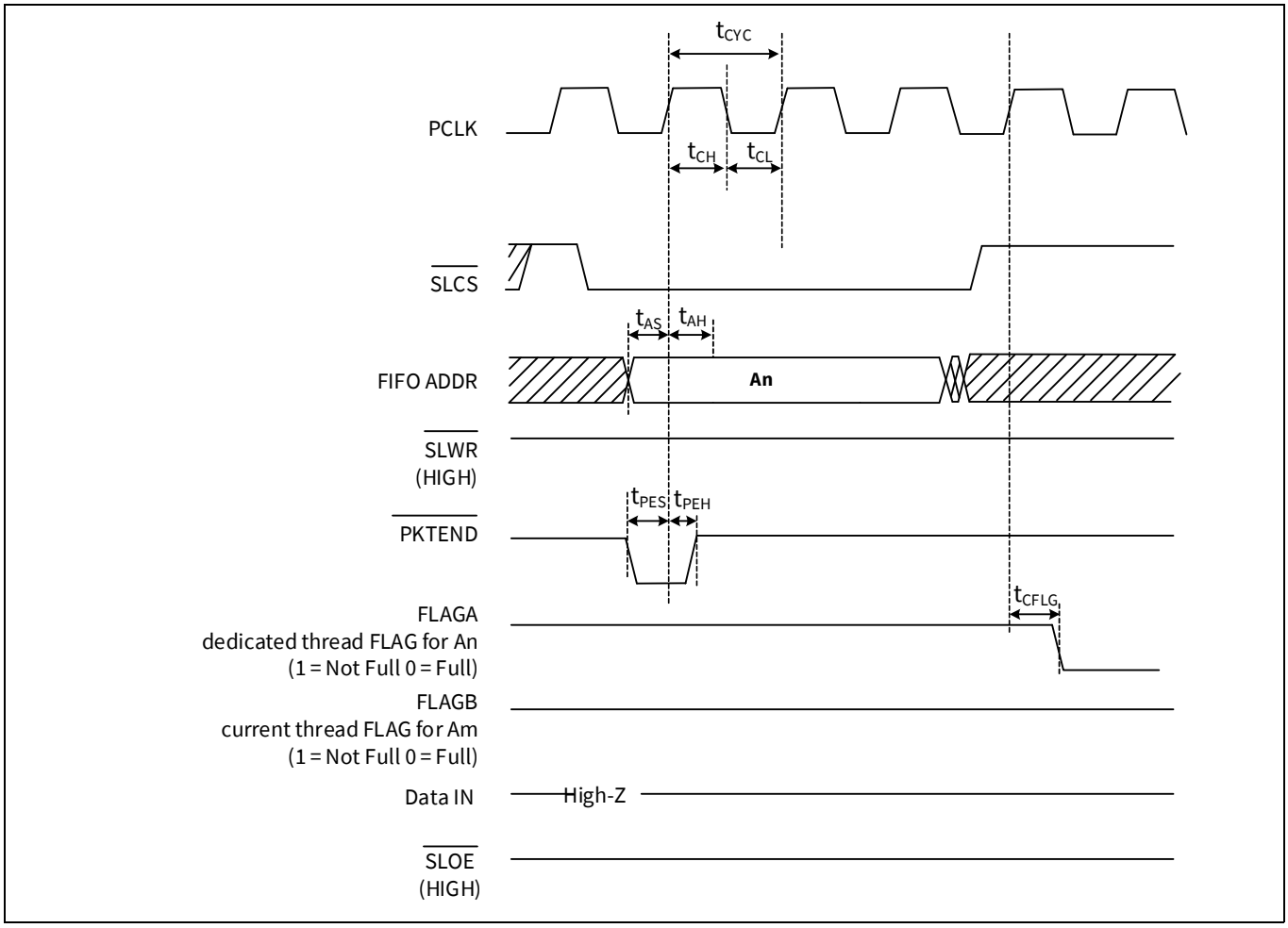


Figure 18 Synchronous SDR slave FIFO ZLP write cycle timing

Table 64 Synchronous SDR slave FIFO parameters[7]

Note: Three-cycle latency from ADDR to DATA/FLAGS.

Parameter	Description	Reference mapping	Min	Max	Unit
FREQ	Interface clock frequency	$f_{LVCMOS\_SDR\_IO}$	–	100	MHz
t_{CYC}	Clock period	$t_{CLK\_SDR\_IO}$	10	–	ns
t_{CH}	Clock high time+	$t_{CLKH\_SDR\_IO}$	4	–	ns
t_{CL}	Clock low time	$t_{CLKL\_SDR\_IO}$	4	–	ns
t_{RDS}	SLRD# to CLK setup time	$t_{S\_SDR\_IO}$	2	–	ns
t_{RDH}	SLRD# to CLK hold time	$t_{H\_SDR\_IO}$	0.5	–	ns
t_{WRS}	SLWR# to CLK setup time	$t_{S\_SDR\_IO}$	2	–	ns
t_{WRH}	SLWR# to CLK hold time	$t_{H\_SDR\_IO}$	0.5	–	ns
t_{CO}	Clock to valid data	$t_{DO\_SDR\_IO}$	–	8	ns
t_{DS}	Data input setup time	$t_{DS\_SDR\_IO}$	2	–	ns
t_{DH}	CLK to data input hold	$t_{DH\_SDR\_IO}$	0.5	–	ns
t_{AS}	Address to CLK setup time	$t_{DS\_SDR\_IO}$	2	–	ns
t_{AH}	CLK to address hold time	$t_{DH\_SDR\_IO}$	0.5	–	ns
t_{OELZ}	SLOE# to data Low-Z	$t_{LZ\_SDR\_IO}$	0	–	ns
t_{CFLG}	CLK to flag output propagation delay	$t_{CO\_SDR\_IO}$	–	8	ns
t_{OEZ}	SLOE# deassert to Data high-Z	$t_{HZ\_SDR\_IO}$	–	8	ns
t_{PES}	PKTEND# to CLK setup	$t_{S\_SDR\_IO}$	2	–	ns
t_{PEH}	CLK to PKTEND# hold	$t_{H\_SDR\_IO}$	0.5	–	ns
t_{CDH}	CLK to data output hold	$t_{DOH\_SDR\_IO}$	2	–	ns
t_{SSD}	Socket switching delay	–	2	68	Clock cycles
t_{ACCD}	Latency from SLRD# to Data	–	2	2	Clock cycles
t_{FAD}	Latency from SLWR# to FLAG	–	3	3	Clock cycles

Note
7. All parameters guaranteed by design and validated through characterization.

6.2 Synchronous DDR slave FIFO write cycle

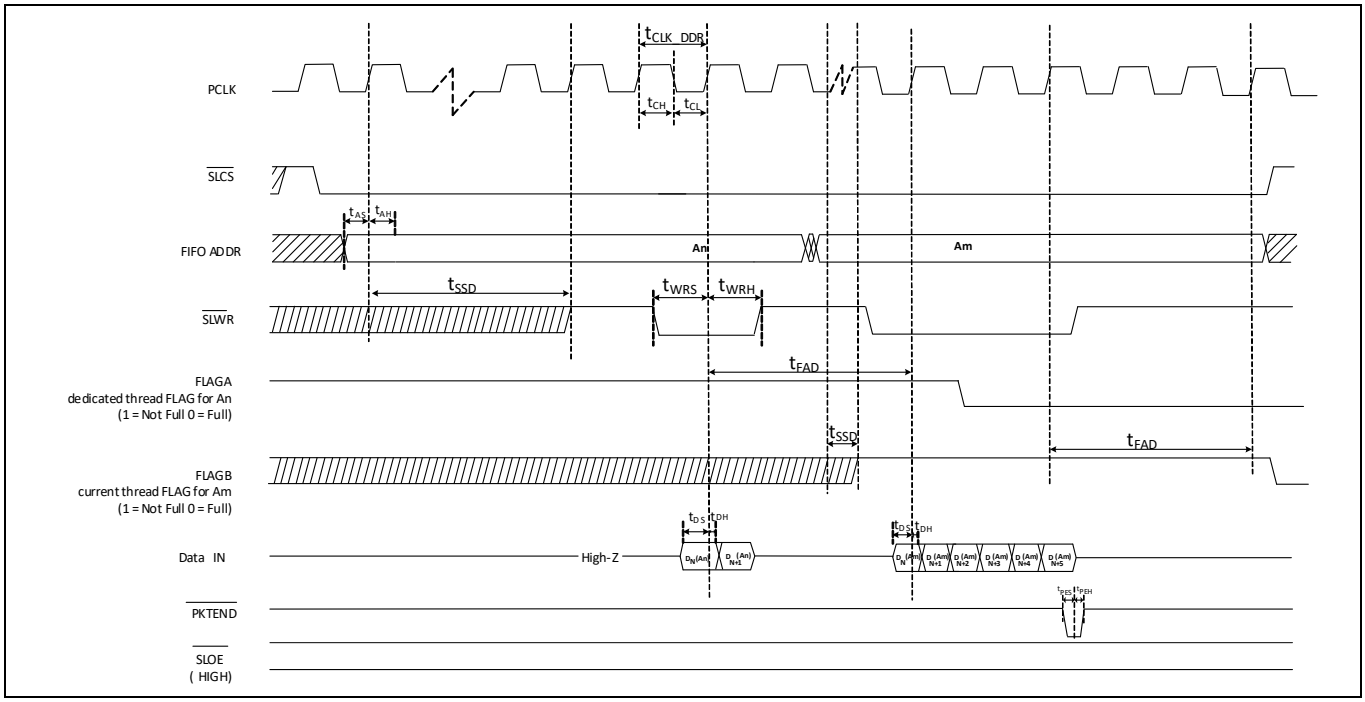


Figure 19 Synchronous DDR slave FIFO write cycle timing diagram

Table 65 Synchronous DDR slave FIFO write cycle timing

Paramter	Description	Mapping	Min	Max	Unit
fLVCMOS_DDR	Interface clock frequency	f_{LVCMOS_DDR}	100	160	MHz
t_{CLK_DDR}	Clock period	t_{CLK_DDR}	6.25	10	ns
t_{CH}	Clock high time	t_{CLKH_DDR}	45	55	% tCLK_DDR
t_{CL}	Clock low time	t_{CLKL_DDR}	45	55	% tCLK_DDR
t_{WRS}	CTL input (SLWR#) to CLK setup time	t_{S_DDR}	–12.5	12.5	% tCLK_DDR
t_{WRH}	CTL input (SLWR#) to CLK hold time	t_{H_DDR}	–12.5	12.5	% tCLK_DDR
t_{DS}	Data input to CLK setup time	t_{DS_DDR}	–12.5	12.5	% tCLK_DDR
t_{DH}	Data input to CLK hold time	t_{DH_DDR}	–12.5	12.5	% tCLK_DDR
t_{AS}	Address to CLK setup time	t_{DS_DDR}	–12.5	12.5	% tCLK_DDR
t_{AH}	CLK to address hold time	t_{DH_DDR}	–12.5	12.5	% tCLK_DDR
t_{PES}	PKTEND# to CLK setup	t_{S_DDR}	–12.5	12.5	% tCLK_DDR
t_{PEH}	CLK to PKTEND# hold	t_{H_DDR}	–12.5	12.5	% tCLK_DDR
t_{SSD}	Socket switching delay	t_{SSD}	2	68	Clock cycles
tACCD	Latency from SLRD# to Data	t_{ACCD}	2	2	Clock cycles
t_{FAD}	Latency from SLWR# to FLAG	t_{FAD}	3	3	Clock cycles

6.3 Slave FIFO pin mapping

Table 66 Slave FIFO pin mapping

Internal signals	Narrow link 0			Narrow link 1			Wide link-0 (2-ports combined)							
	8b wide bus		16b bus	8b wide bus		16b bus	8b	8b	16b	16b	24b	24b	32b	32b
	2 bit FIFO	5 bit FIFO	2 bit FIFO	2 bit FIFO	5 bit FIFO	2 bit FIFO	2 bit FIFO	5 bit FIFO	2 bit FIFO	5 bit FIFO	2 bit FIFO	5 bit FIFO	2bit FIFO	5 bit FIFO
CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK
DQ[0]	D0	D0	D0	–	–	–	D0	D0	D0	D0	D0	D0	D0	D0
DQ[1]	D1	D1	D1	–	–	–	D1	D1	D1	D1	D1	D1	D1	D1
DQ[2]	D2	D2	D2	–	–	–	D2	D2	D2	D2	D2	D2	D2	D2
DQ[3]	D3	D3	D3	–	–	–	D3	D3	D3	D3	D3	D3	D3	D3
DQ[4]	D4	D4	D4	–	–	–	D4	D4	D4	D4	D4	D4	D4	D4
DQ[5]	D5	D5	D5	–	–	–	D5	D5	D5	D5	D5	D5	D5	D5
DQ[6]	D6	D6	D6	–	–	–	D6	D6	D6	D6	D6	D6	D6	D6
DQ[7]	D7	D7	D7	–	–	–	D7	D7	D7	D7	D7	D7	D7	D7
DQ[8]	A0	A0	D8	–	–	–	A0	A0	D8	D8	D8	D8	D8	D8
DQ[9]	A1	A1	D9	–	–	–	A1	A1	D9	D9	D9	D9	D9	D9
DQ[10]	SPARE	A2	D10	–	–	–	SPARE	A2	D10	D10	D10	D10	D10	D10
DQ[11]	SPARE	A3	D11	–	–	–	SPARE	A3	D11	D11	D11	D11	D11	D11
DQ[12]	SPARE	A4	D12	–	–	–	SPARE	A4	D12	D12	D12	D12	D12	D12
DQ[13]	SPARE	SPARE	D13	–	–	–	SPARE	SPARE	D13	D13	D13	D13	D13	D13
DQ[14]	SPARE	SPARE	D14	–	–	–	SPARE	SPARE	D14	D14	D14	D14	D14	D14
DQ[15]	SPARE	SPARE	D15	–	–	–	SPARE	SPARE	D15	D15	D15	D15	D15	D15
DQ[16]	–	–	–	D0	D0	D0	SPARE	SPARE	A0	A0	D16	D16	D16	D16
DQ[17]	–	–	–	D1	D1	D1	SPARE	SPARE	A1	A1	D17	D17	D17	D17
DQ[18]	–	–	–	D2	D2	D2	SPARE	SPARE	SPARE	A2	D18	D18	D18	D18
DQ[19]	–	–	–	D3	D3	D3	SPARE	SPARE	SPARE	A3	D19	D19	D19	D19
DQ[20]	–	–	–	D4	D4	D4	SPARE	SPARE	SPARE	A4	D20	D20	D20	D20
DQ[21]	–	–	–	D5	D5	D5	SPARE	SPARE	SPARE	SPARE	D21	D21	D21	D21
DQ[22]	–	–	–	D6	D6	D6	SPARE	SPARE	SPARE	SPARE	D22	D22	D22	D22
DQ[23]	–	–	–	D7	D7	D7	SPARE	SPARE	SPARE	SPARE	D23	D23	D23	D23
DQ[24]	–	–	–	A0	A0	D8	SPARE	SPARE	SPARE	SPARE	A0	A0	D24	D24
DQ[25]	–	–	–	A1	A1	D9	SPARE	SPARE	SPARE	SPARE	A1	A1	D25	D25
DQ[26]	–	–	–	SPARE	A2	D10	SPARE	SPARE	SPARE	SPARE	SPARE	A2	D26	D26
DQ[27]	–	–	–	SPARE	A3	D11	SPARE	SPARE	SPARE	SPARE	SPARE	A3	D27	D27

Table 66 Slave FIFO pin mapping

Internal signals	Narrow link 0			Narrow link 1			Wide link-0 (2-ports combined)							
	8b wide bus		16b bus	8b wide bus		16b bus	8b	8b	16b	16b	24b	24b	32b	32b
	2 bit FIFO	5 bit FIFO	2 bit FIFO	2 bit FIFO	5 bit FIFO	2 bit FIFO	2 bit FIFO	5 bit FIFO	2 bit FIFO	5 bit FIFO	2 bit FIFO	5 bit FIFO	2bit FIFO	5 bit FIFO
DQ[28]	–	–	–	SPARE	A4	D12	SPARE	SPARE	SPARE	SPARE	SPARE	A4	D28	D28
DQ[29]	–	–	–	SPARE	SPARE	D13	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	D29	D29
DQ[30]	–	–	–	SPARE	SPARE	D14	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	D30	D30
DQ[31]	–	–	–	SPARE	SPARE	D15	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	D31	D31
CTL[19]	–	–	–	SPARE	SPARE	A0	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	A0	A0
CTL[18]	–	–	–	SPARE	EPSWITCH	A1	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	A1	A1
CTL[17]	–	–	–	L3_ENTRY	L3_ENTRY	L3_ENTRY	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	A2
CTL[16]	–	–	–	FLAG A	FLAG A	FLAG A	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	A3
CTL[15]	–	–	–	FLAG B	FLAG B	FLAG B	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	A4
CTL[14]	–	–	–	PKTEND	PKTEND	PKTEND	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE
CTL[13]	–	–	–	RD	RD	RD	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE
CTL[12]	–	–	–	OE	OE	OE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE
CTL[11]	–	–	–	WE	WE	WE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE
CTL[10]	–	–	–	CE	CE	CE	SPARE	EPSWITCH	SPARE	EPSWITCH	SPARE	EPSWITCH	SPARE	EPSWITCH
CTL[9]	SPARE	SPARE	A0	–	–	–	L3_ENTRY	L3_ENTRY	L3_ENTRY	L3_ENTRY	L3_ENTRY	L3_ENTRY	L3_ENTRY	L3_ENTRY
CTL[8]	SPARE	EPSWITCH	A1	–	–	–	FLAG A	FLAG A	FLAG A	FLAG A	FLAG A	FLAG A	FLAG A	FLAG A
CTL[7]	L3_ENTRY	L3_ENTRY	L3_ENTRY	–	–	–	FLAG B	FLAG B	FLAG B	FLAG B	FLAG B	FLAG B	FLAG B	FLAG B
CTL[6]	FLAG B	FLAG B	FLAG B	–	–	–	FLAG C	FLAG C	FLAG C	FLAG C	FLAG C	FLAG C	FLAG C	FLAG C
CTL[5]	FLAG A	FLAG A	FLAG A	–	–	–	FLAG D	FLAG D	FLAG D	FLAG D	FLAG D	FLAG D	FLAG D	FLAG D
CTL[4]	PKTEND	PKTEND	PKTEND	–	–	–	PKTEND	PKTEND	PKTEND	PKTEND	PKTEND	PKTEND	PKTEND	PKTEND
CTL[3]	RD	RD	RD	–	–	–	RD	RD	RD	RD	RD	RD	RD	RD
CTL[2]	OE	OE	OE	–	–	–	OE	OE	OE	OE	OE	OE	OE	OE
CTL[1]	WE	WE	WE	–	–	–	WE	WE	WE	WE	WE	WE	WE	WE
CTL[0]	CE	CE	CE	–	–	–	CE	CE	CE	CE	CE	CE	CE	CE

6.4 LVDS write cycle

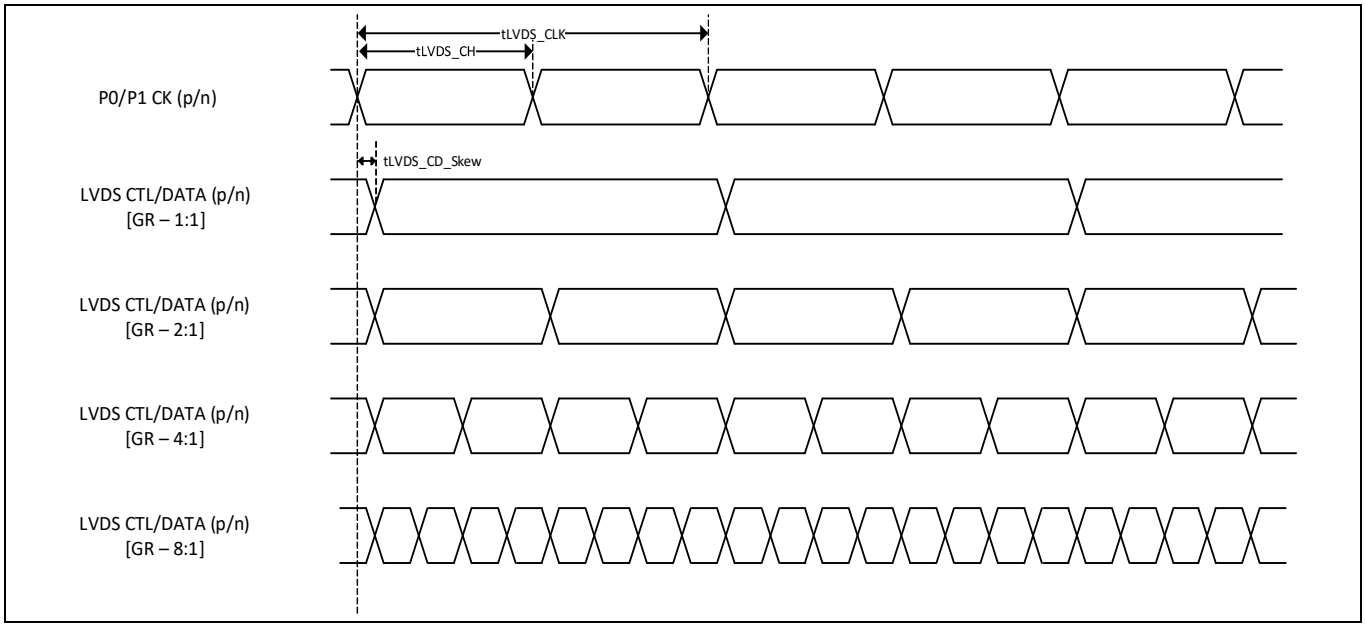


Figure 20 LVDS write cycle timing diagram (for the timing parameters, see Table 41)

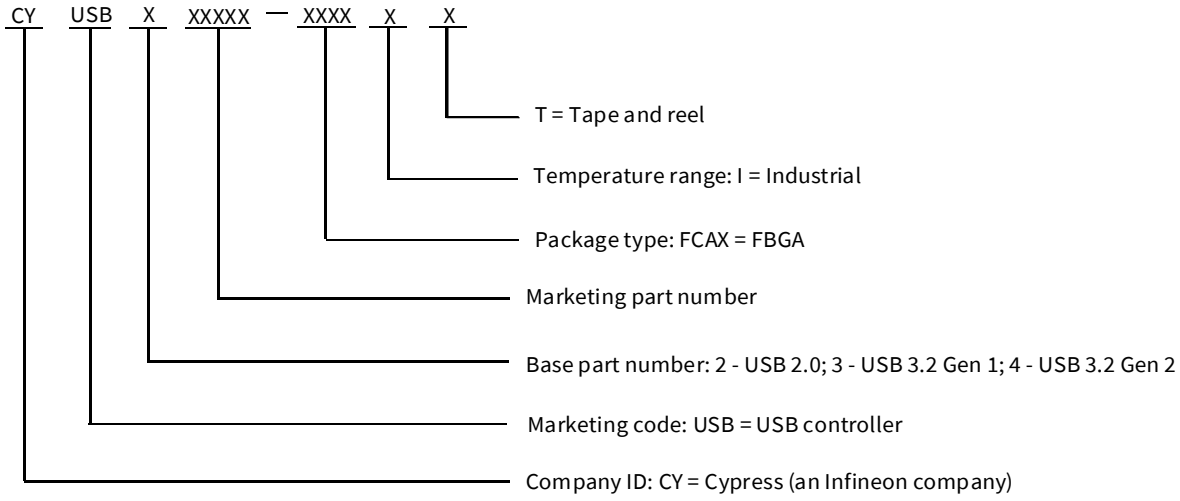
7 Ordering information

Table 67 lists the FX5 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative.

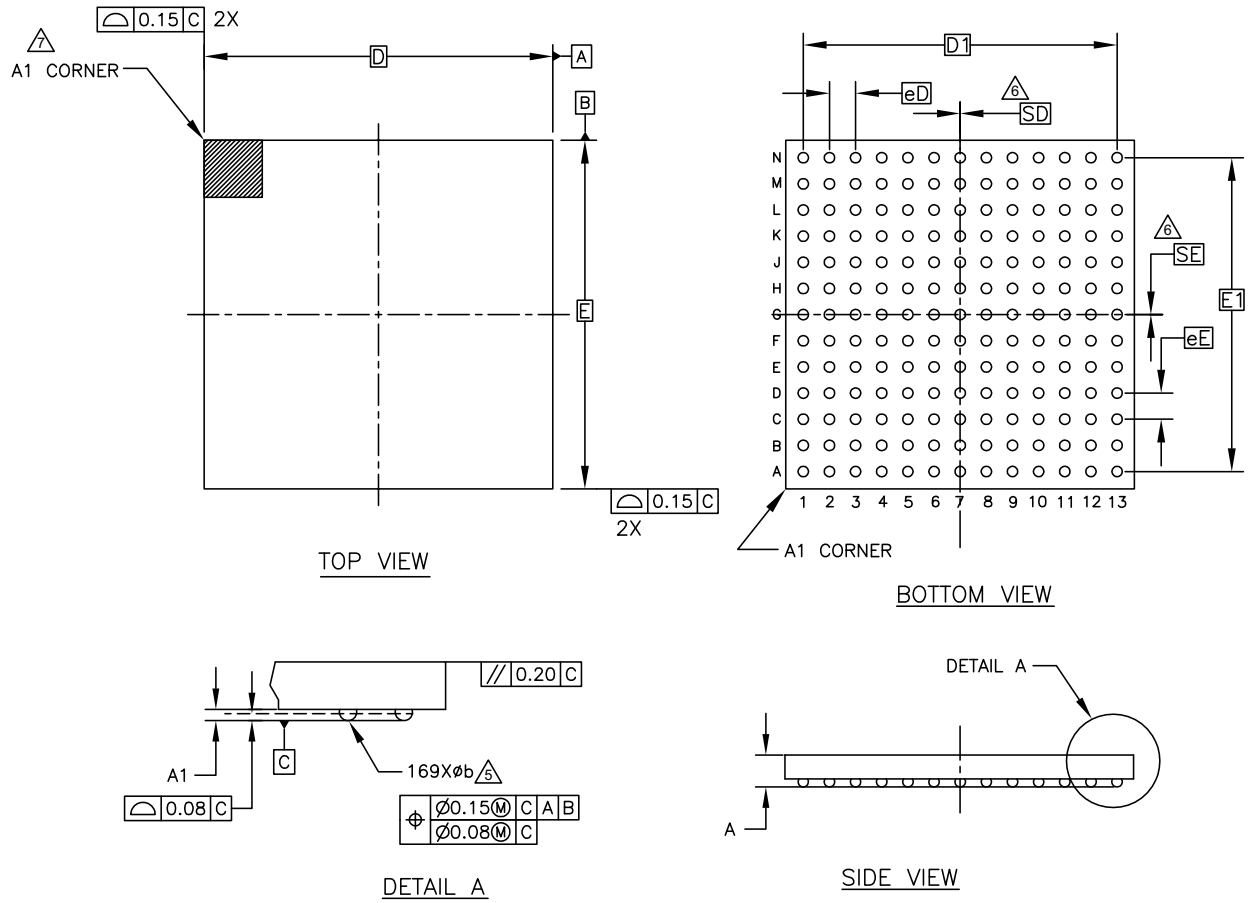
Table 67 FX5 key features and ordering information

Family	Product	Type-C	USB 3.2 Gen 1	CRYPTO	LVDS	LVCMOS	QSPI	Configurable	Flash	High- bandwidth data subsystem SRAM
EZ-USB™ FX5	CYUSB3082-FCAXI		X			X			256 KB	512 KB
	CYUSB3083-FCAXI	X	X		X	X	X		512 KB	1024 KB
	CYUSB3084-FCAXI	X	X	X	X	X	X		512 KB	1024 KB

7.1 Ordering code definitions



8 Package diagram



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.20	-	-
D	10.00 BSC		
E	10.00 BSC		
D1	9.00 BSC		
E1	9.00 BSC		
MD	13		
ME	13		
N	169		
Øb	0.25	0.30	0.35
eD	0.75 BSC		
eE	0.75 BSC		
SD	0.00 BSC		
SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MS-034

002-32511 *C

Figure 21 169-ball FBGA (10 × 10 × 1.2 mm) FCA169 package outline, 002-32511

9 Acronyms

Table 68 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA high-performance bus
AXI	advanced eXtensible interface
BB	bit banding
BOD	brown-out detection
BSDL	boundary scan description language
CAN	controller area network
CRC	cyclic redundancy check
CDC	communication device class
CRYPTO	cryptography accelerator
CTI	cross trigger interface
CTR	counter
DFT	design for testability
DMA	direct memory access
DW	data width
ECC	elliptic curve cryptography
ETM	embedded trace macrocell
FBGA	fine ball grid array
FLL	frequency-locked loop
FPU	floating point unit
FS	full-speed
GPIF	general programmable interface
GPIO	general-purpose I/O
HID	human-interface device
HS	high speed
I2C	inter integrated circuit
I2S	inter IC sound bus
IBIS	input output buffer information system
ILO	internal low-speed oscillator
IMO	internal main oscillator
IOSS	input output subsystem
IPC	inter-processor communication
ITM	instrumentation trace macrocell
LDO	low dropout regulator
LP	low power
LVD	low voltage detection
LVDS	low voltage differential signalling
LVCMOS	low voltage complementary metal oxide semiconductor
MCU	microcontroller unit
MPU	memory protection unit

Table 68 Acronyms used in this document *(continued)*

Acronym	Description
MMIO	memory-mapped IO
MTB	micro trace buffer
NVIC	nested vector interrupt control
OVP	overvoltage protection
PCLK	peripheral clock
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
PLL	phase-locked loop
POR	power-on reset
PPU	power policy unit
PWM	pulse-width modulation
PWRSYS	power system
QD	quadrature decoder
QSPI	quad SPI
REF	reference voltage
RSA	Rivest–Shamir–Adleman cryptography algorithm
RWW	read-while-write
SCB	serial communication block
SERDES	serializer deserializer
SHA	secure hash algorithm
SMPU	system memory protection unit
SPI	serial peripheral interface
SRAM	static random access memory
SWJ	SWD or JTAG debug port
TOF	time-of-flight
TRNG	true random number generation
UAC	USB audio class
UART	universal asynchronous receiver transmitter
USB	Universal Serial Bus
UVC	USB video class
WDT	watchdog timer
XRES	external reset

10 Document conventions

10.1 Unit of measure

Table 69 Unit of measure

Symbol	Unit of measure
°C	degree celsius
dB	decibel
fF	femto farad
Gbps	gigabits per second
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo-ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

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Document revision	Date	Description of changes
*A	2025-03-13	Publish to web.

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