

## IRS2183/IRS21834(S)PbF

### HALF-BRIDGE DRIVER

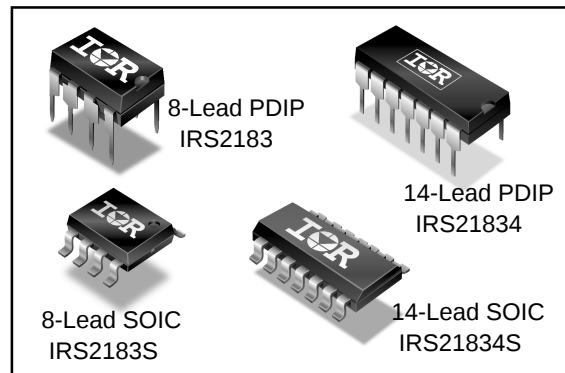
#### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage,  $dV/dt$  immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower  $di/dt$  gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A
- RoHS compliant

#### Description

The IRS2183/IRS21834 are high voltage, high speed power MOSFET and IGBT drivers with dependent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

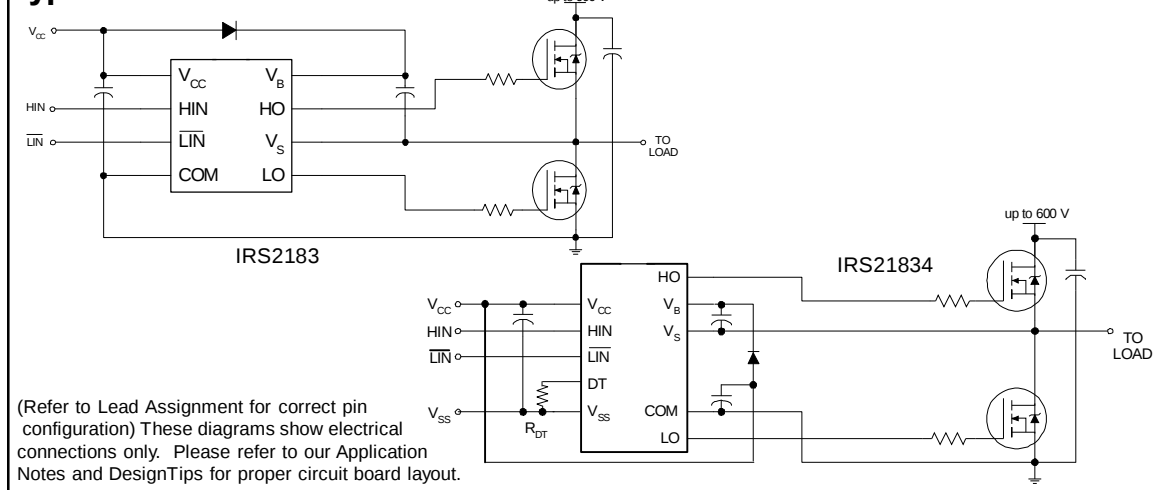
#### Packages



#### Feature Comparison

| Part  | Input logic           | Cross-conduction prevention logic | Deadtime (ns)    | Ground Pins  | $t_{on}/t_{off}$ (ns) |
|-------|-----------------------|-----------------------------------|------------------|--------------|-----------------------|
| 2181  | HIN/LIN               | no                                | none             | COM          | 180/220               |
| 21814 |                       |                                   |                  | $V_{SS}/COM$ |                       |
| 2183  | HIN/ $\overline{LIN}$ | yes                               | Internal 400     | COM          | 180/220               |
| 21834 |                       |                                   | Program 400-5000 | $V_{SS}/COM$ |                       |
| 2184  | IN/ $\overline{SD}$   | yes                               | Internal 400     | COM          | 680/270               |
| 21844 |                       |                                   | Program 400-5000 | $V_{SS}/COM$ |                       |

#### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol              | Definition                                          |                | Min.                  | Max.                  | Units |
|---------------------|-----------------------------------------------------|----------------|-----------------------|-----------------------|-------|
| V <sub>B</sub>      | High-side floating absolute voltage                 |                | -0.3                  | 620 (Note 1)          | V     |
| V <sub>S</sub>      | High-side floating supply offset voltage            |                | V <sub>B</sub> - 20   | V <sub>B</sub> + 0.3  |       |
| V <sub>HO</sub>     | High-side floating output voltage                   |                | V <sub>S</sub> - 0.3  | V <sub>B</sub> + 0.3  |       |
| V <sub>CC</sub>     | Low-side and logic fixed supply voltage             |                | -0.3                  | 20 (Note 1)           |       |
| V <sub>LO</sub>     | Low-side output voltage                             |                | -0.3                  | V <sub>CC</sub> + 0.3 |       |
| DT                  | Programmable deadtime pin voltage (IR21834 only)    |                | V <sub>SS</sub> - 0.3 | V <sub>CC</sub> + 0.3 |       |
| V <sub>IN</sub>     | Logic input voltage (HIN & LIN)                     |                | V <sub>SS</sub> - 0.3 | V <sub>CC</sub> + 0.3 |       |
| V <sub>SS</sub>     | Logic ground (IR21834 only)                         |                | V <sub>CC</sub> - 20  | V <sub>CC</sub> + 0.3 |       |
| dV <sub>S</sub> /dt | Allowable offset supply voltage transient           |                | —                     | 50                    | V/ns  |
| P <sub>D</sub>      | Package power dissipation @ T <sub>A</sub> ≤ +25 °C | (8-lead PDIP)  | —                     | 1.0                   | W     |
|                     |                                                     | (8-lead SOIC)  | —                     | 0.625                 |       |
|                     |                                                     | (14-lead PDIP) | —                     | 1.6                   |       |
|                     |                                                     | (14-lead SOIC) | —                     | 1.0                   |       |
| R <sub>thJA</sub>   | Thermal resistance, junction to ambient             | (8-lead PDIP)  | —                     | 125                   | °C/W  |
|                     |                                                     | (8-lead SOIC)  | —                     | 200                   |       |
|                     |                                                     | (14-lead PDIP) | —                     | 75                    |       |
|                     |                                                     | (14-lead SOIC) | —                     | 120                   |       |
| T <sub>J</sub>      | Junction temperature                                |                | —                     | 150                   | °C    |
| T <sub>S</sub>      | Storage temperature                                 |                | -50                   | 150                   |       |
| T <sub>L</sub>      | Lead temperature (soldering, 10 seconds)            |                | —                     | 300                   |       |

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset rating are tested with all supplies biased at 15 V differential.

| Symbol   | Definition                                       | Min.       | Max.       | Units            |
|----------|--------------------------------------------------|------------|------------|------------------|
| $V_B$    | High-side floating supply absolute voltage       | $V_S + 10$ | $V_S + 20$ | V                |
| $V_S$    | High-side floating supply offset voltage         | Note 2     | 600        |                  |
| $V_{HO}$ | High-side floating output voltage                | $V_S$      | $V_B$      |                  |
| $V_{CC}$ | Low-side and logic fixed supply voltage          | 10         | 20         |                  |
| $V_{LO}$ | Low-side output voltage                          | 0          | $V_{CC}$   |                  |
| $V_{IN}$ | Logic input voltage (HIN & LIN)                  | $V_{SS}$   | $V_{CC}$   |                  |
| DT       | Programmable deadtime pin voltage (IR21834 only) | $V_{SS}$   | $V_{CC}$   |                  |
| $V_{SS}$ | Logic ground (IR21834 only)                      | -5         | 5          | $^\circ\text{C}$ |
| $T_A$    | Ambient temperature                              | -40        | 125        |                  |

Note 2: Logic operational for  $V_S$  of -5 V to +600 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM,  $C_L$  = 1000 pF,  $T_A$  = 25 °C, DT =  $V_{SS}$  unless otherwise specified.

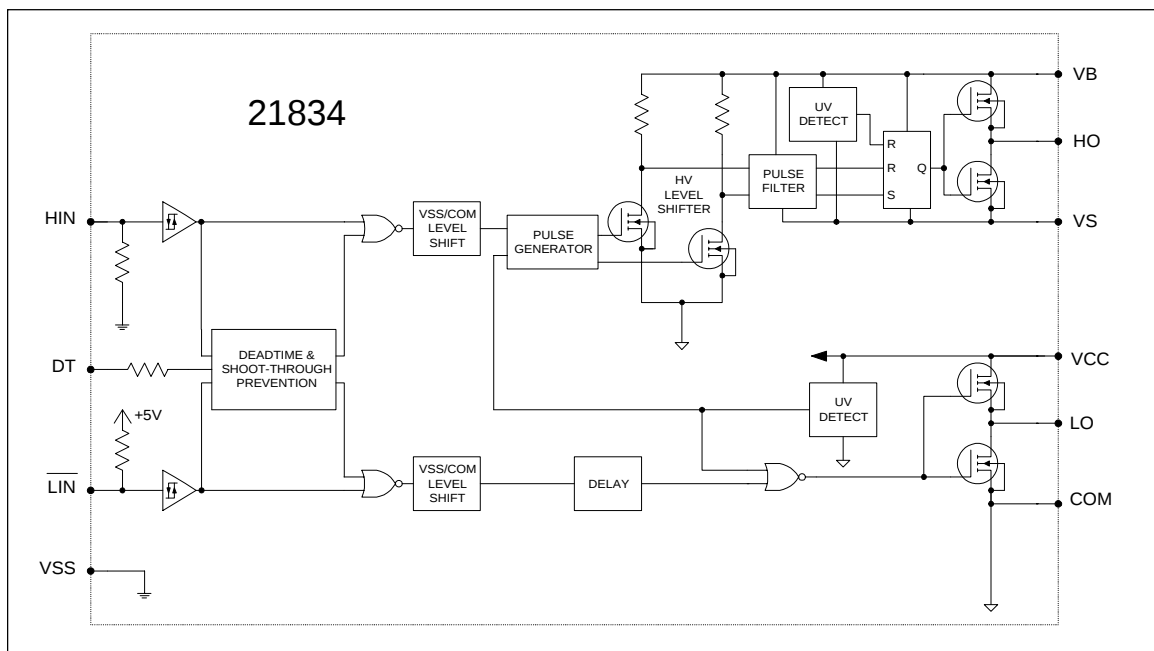
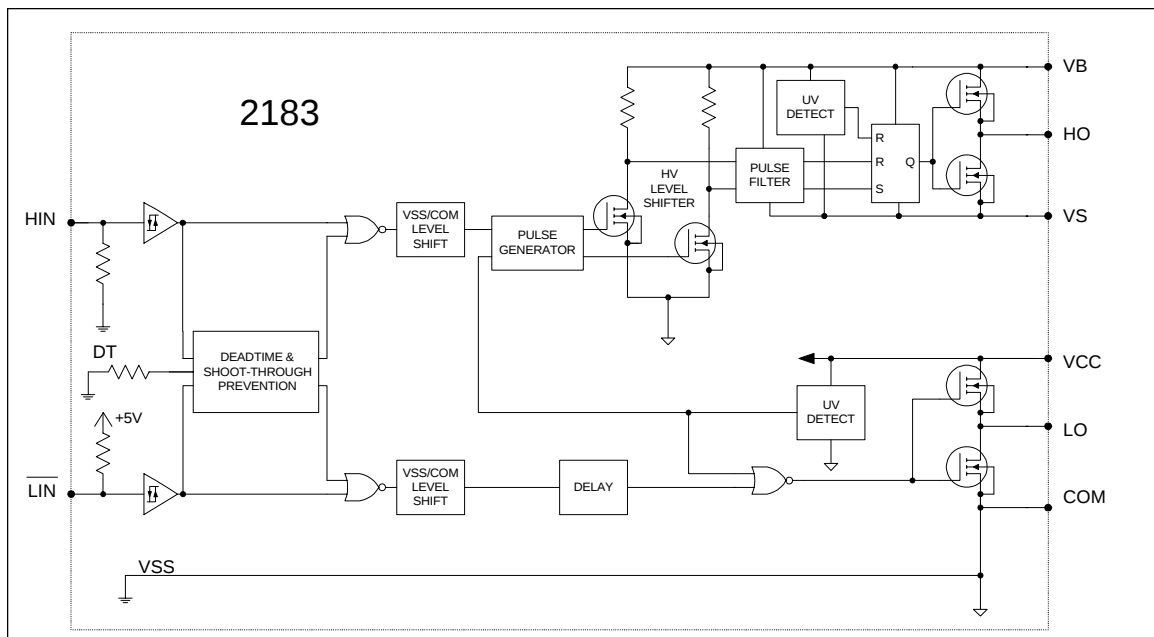
| Symbol    | Definition                                                                                                      | Min. | Typ. | Max. | Units | Test Conditions                 |
|-----------|-----------------------------------------------------------------------------------------------------------------|------|------|------|-------|---------------------------------|
| $t_{on}$  | Turn-on propagation delay                                                                                       | —    | 180  | 270  | ns    | $V_S = 0V$                      |
| $t_{off}$ | Turn-off propagation delay                                                                                      | —    | 220  | 330  |       | $V_S = 0V$ or 600V              |
| MT        | Delay matching $ t_{on} - t_{off} $                                                                             | —    | 0    | 35   |       |                                 |
| $t_r$     | Turn-on rise time                                                                                               | —    | 40   | 60   |       | $V_S = 0V$                      |
| $t_f$     | Turn-off fall time                                                                                              | —    | 20   | 35   |       |                                 |
| DT        | Deadtime: LO turn-off to HO turn-on(DT <sub>LO-HO</sub> ) &<br>HO turn-off to LO turn-on (DT <sub>HO-LO</sub> ) | 280  | 400  | 520  | μs    | $R_{DT} = 0\Omega$              |
|           |                                                                                                                 | 4    | 5    | 6    |       | $R_{DT} = 200k\Omega$ (IR21834) |
| MDT       | Deadtime matching = $ DT_{LO-HO} - DT_{HO-LO} $                                                                 | —    | 0    | 50   | ns    | $R_{DT}=0\Omega$                |
|           |                                                                                                                 | —    | 0    | 600  |       | $R_{DT} = 200k\Omega$ (IR21834) |

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM, DT=  $V_{SS}$  and  $T_A$  = 25 °C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}/COM$  and are applicable to the respective input leads: HIN and LIN. The  $V_O$ ,  $I_O$ , and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol                     | Definition                                                         | Min. | Typ. | Max. | Units | Test Conditions                    |
|----------------------------|--------------------------------------------------------------------|------|------|------|-------|------------------------------------|
| $V_{IH}$                   | Logic "1" input voltage for HIN & logic "0" for $\overline{LIN}$   | 2.5  | —    | —    | V     | $V_{CC} = 10V$ to 20 V             |
| $V_{IL}$                   | Logic "0" input voltage for HIN & logic "1" for $\overline{LIN}$   | —    | —    | 0.8  |       |                                    |
| $V_{OH}$                   | High level output voltage, $V_{BIAS} - V_O$                        | —    | —    | 1.4  |       | $I_O = 0A$                         |
| $V_{OL}$                   | Low level output voltage, $V_O$                                    | —    | —    | 0.2  |       | $I_O = 20mA$                       |
| $I_{LK}$                   | Offset supply leakage current                                      | —    | —    | 50   | μA    | $V_B = V_S = 600V$                 |
| $I_{QBS}$                  | Quiescent $V_{BS}$ supply current                                  | 20   | 60   | 150  |       | $V_{IN} = 0V$ or 5 V               |
| $I_{QCC}$                  | Quiescent $V_{CC}$ supply current                                  | 0.4  | 1.0  | 1.6  | mA    |                                    |
| $I_{IN+}$                  | Logic "1" input bias current                                       | —    | 25   | 60   | μA    | $HIN = 5V$ , $\overline{LIN} = 0V$ |
| $I_{IN-}$                  | Logic "0" input bias current                                       | —    | —    | 5.0  |       | $HIN = 0V$ , $\overline{LIN} = 5V$ |
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 8.0  | 8.9  | 9.8  | V     |                                    |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 7.4  | 8.2  | 9.0  |       |                                    |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | Hysteresis                                                         | 0.3  | 0.7  | —    |       |                                    |
| $I_{O+}$                   | Output high short circuit pulsed current                           | 1.4  | 1.9  | —    | A     | $V_O = 0V$ ,<br>$PW \leq 10\mu s$  |
| $I_{O-}$                   | Output low short circuit pulsed current                            | 1.8  | 2.3  | —    |       | $V_O = 15V$ ,<br>$PW \leq 10\mu s$ |

## Functional Block Diagrams



## Lead Definitions

| Symbol                  | Description                                                                                                         |
|-------------------------|---------------------------------------------------------------------------------------------------------------------|
| HIN                     | Logic input for high-side gate driver output (HO), in phase (referenced to COM for IRS2183 and VSS for IRS21834)    |
| $\overline{\text{LIN}}$ | Logic input for low-side gate driver output (LO), out of phase (referenced to COM for IRS2183 and VSS for IRS21834) |
| DT                      | Programmable deadtime lead, referenced to VSS (IRS21834 only)                                                       |
| VSS                     | Logic ground (IRS21834 only)                                                                                        |
| V <sub>B</sub>          | High-side floating supply                                                                                           |
| HO                      | High-side gate driver output                                                                                        |
| V <sub>S</sub>          | High-side floating supply return                                                                                    |
| V <sub>CC</sub>         | Low-side and logic fixed supply                                                                                     |
| LO                      | Low-side gate driver output                                                                                         |
| COM                     | Low-side return                                                                                                     |

## Lead Assignments

|                     |                     |
|---------------------|---------------------|
| <p>8-Lead PDIP</p>  | <p>8-Lead SOIC</p>  |
| <b>IRS2183PbF</b>   | <b>IRS2183SPbF</b>  |
| <p>14-Lead PDIP</p> | <p>14-Lead SOIC</p> |
| <b>IRS21834PbF</b>  | <b>IRS21834SPbF</b> |

## IRS2183/IRS21834(S)PbF

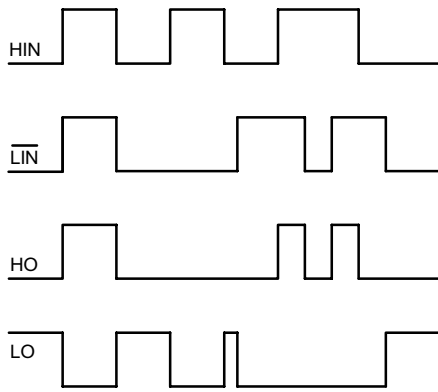


Figure 1. Input/Output Timing Diagram

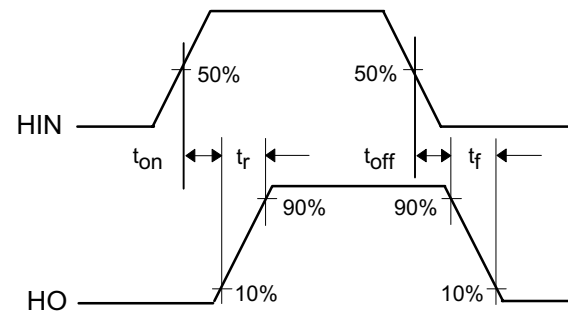
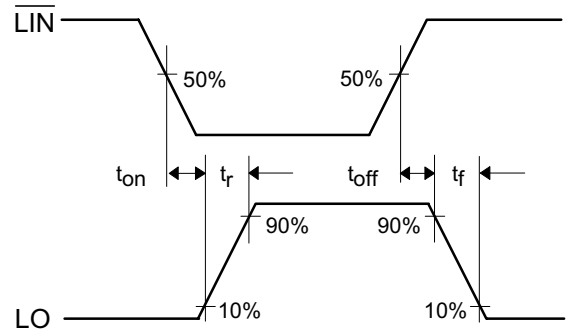


Figure 2. Switching Time Waveform Definitions

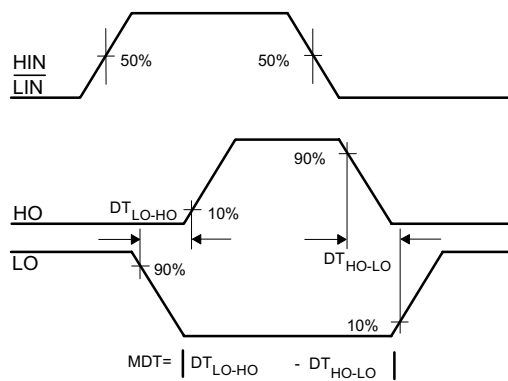
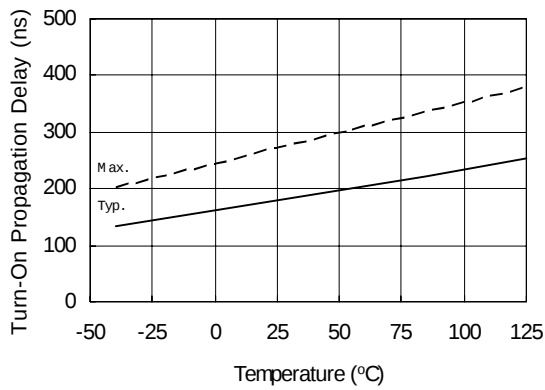
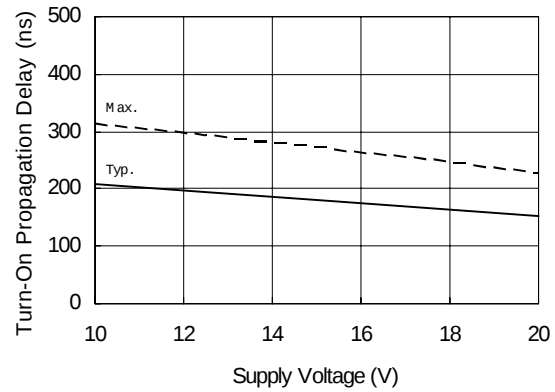


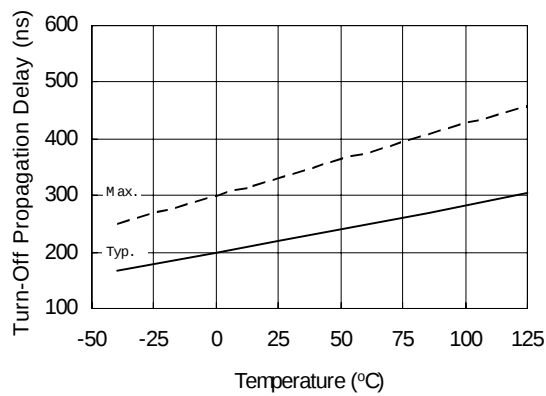
Figure 3. Deadtime Waveform Definitions



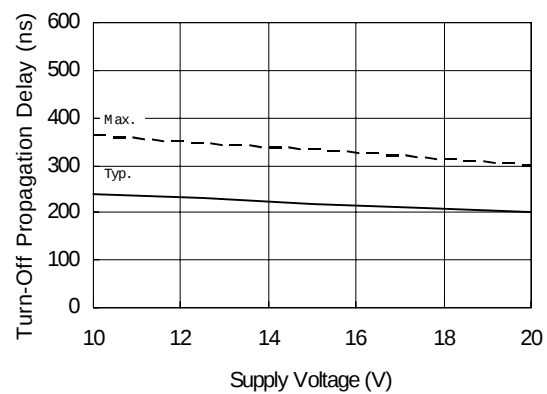
**Figure 4A. Turn-On Propagation Delay vs. Temperature**



**Figure 4B. Turn-On Propagation Delay vs. Supply Voltage**



**Figure 5A. Turn-Off Propagation Delay vs. Temperature**



**Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage**

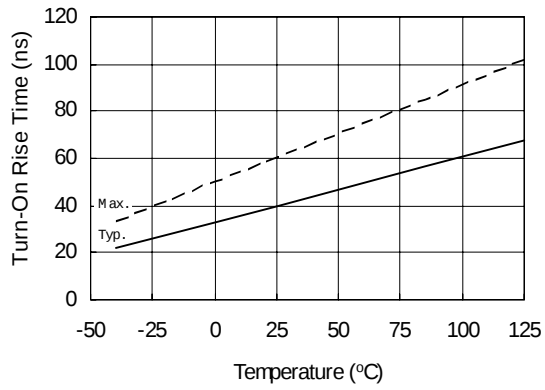


Figure 6A. Turn-On Rise Time vs. Temperature

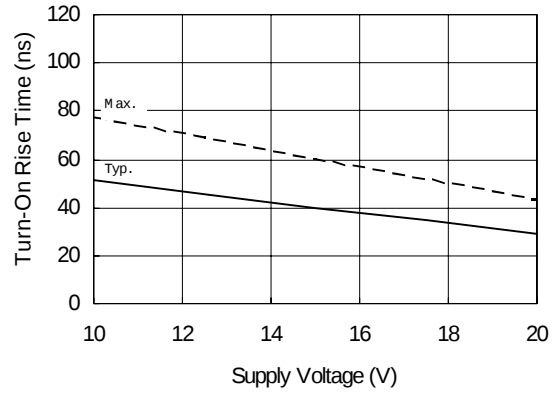


Figure 6B. Turn-On Rise Time vs. Supply Voltage

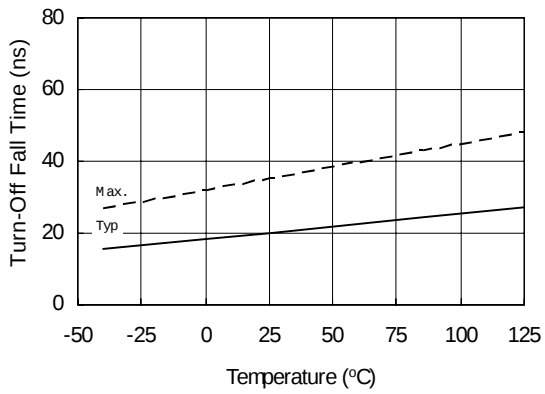


Figure 7A. Turn-Off Fall Time vs. Temperature

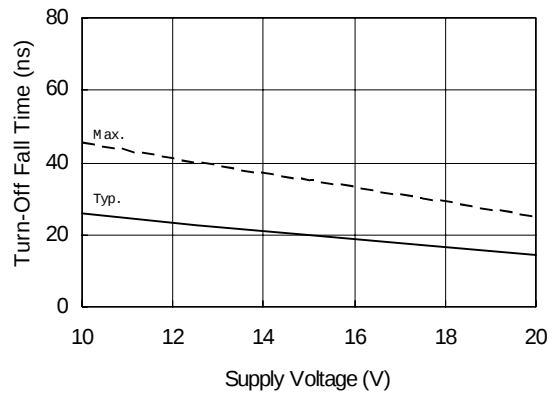


Figure 7B. Turn-Off Fall Time vs. Supply Voltage

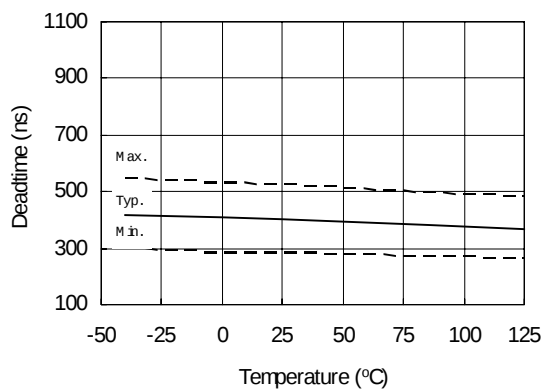


Figure 8A. Deadtime vs. Temperature

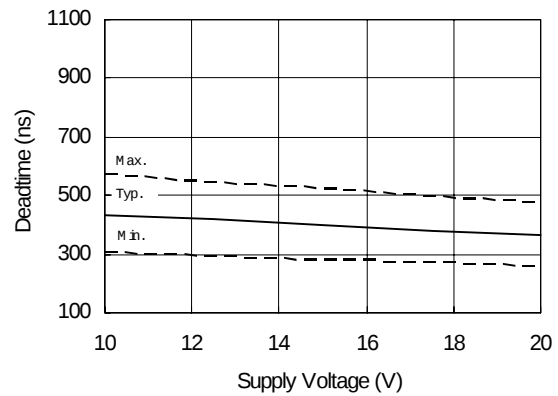


Figure 8B. Deadtime vs. Supply Voltage

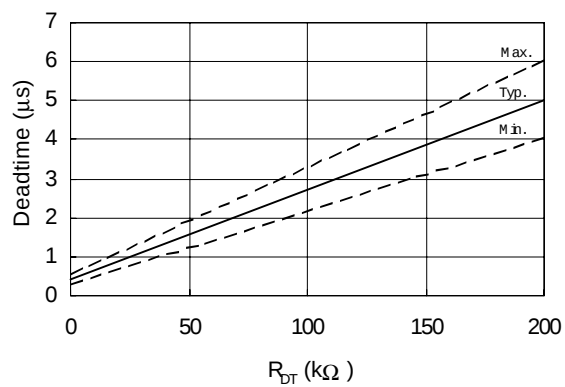


Figure 8C. Deadtime vs.  $R_{DT}$

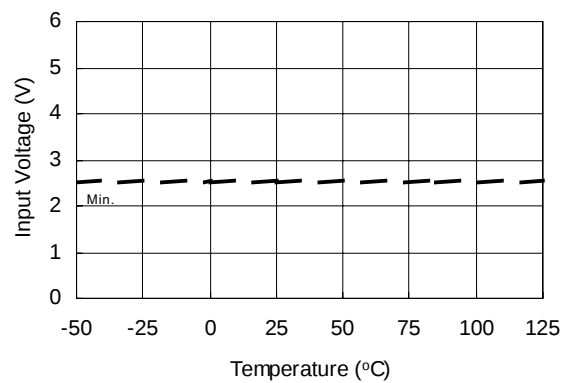
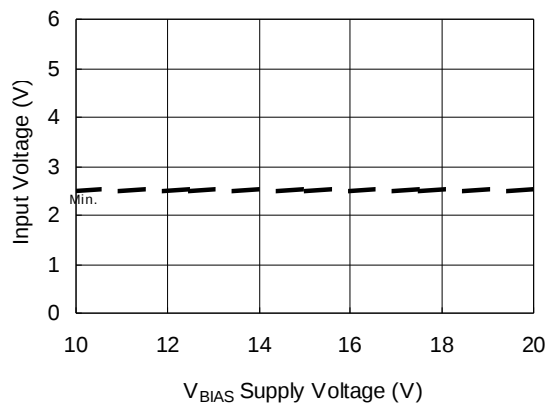
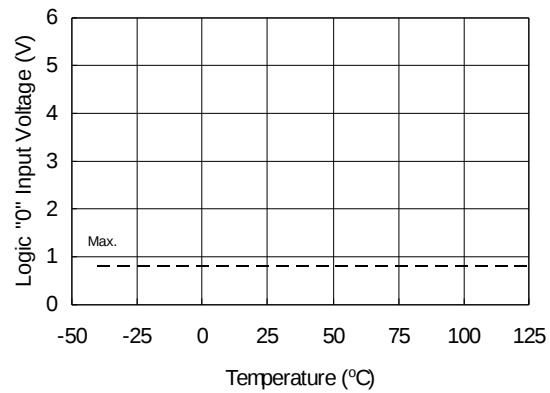


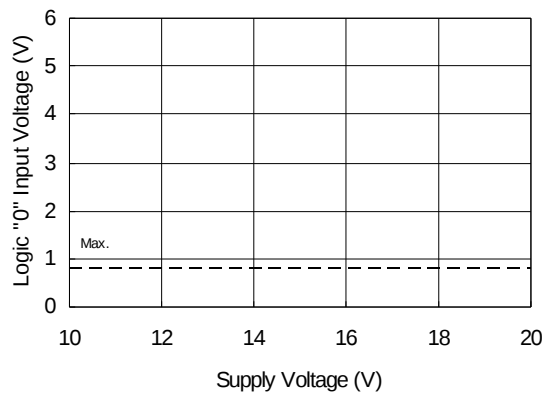
Figure 9A. Logic "1" Input Voltage vs. Temperature



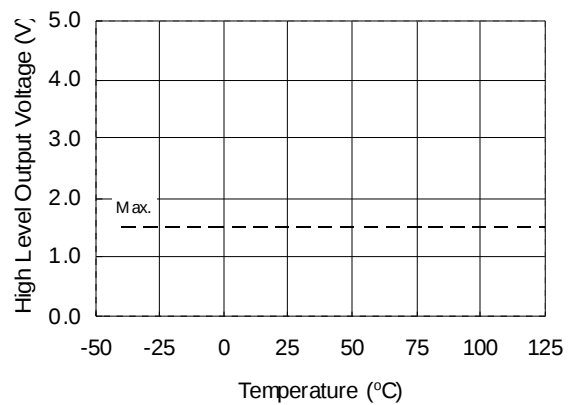
**Figure 9B. Logic "1" Input Voltage vs. Supply Voltage**



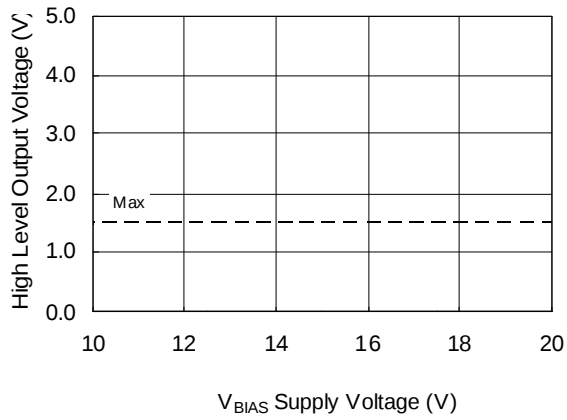
**Figure 10A. Logic "0" Input Voltage vs. Temperature**



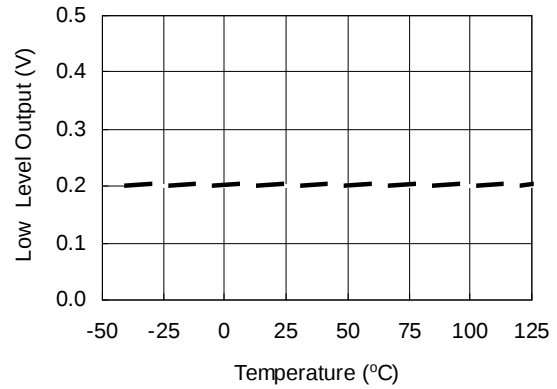
**Figure 10B. Logic "0" Input Voltage vs. Supply Voltage**



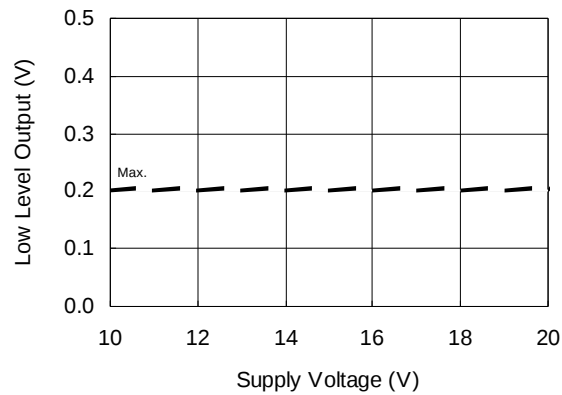
**Figure 11A. High Level Output Voltage vs. Temperature ( $I_o = 0$  mA)**



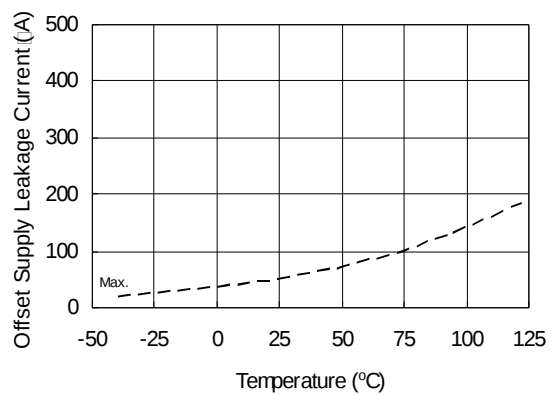
**Figure 11B. High Level Output Voltage vs. Supply Voltage ( $I_o = 0$  mA)**



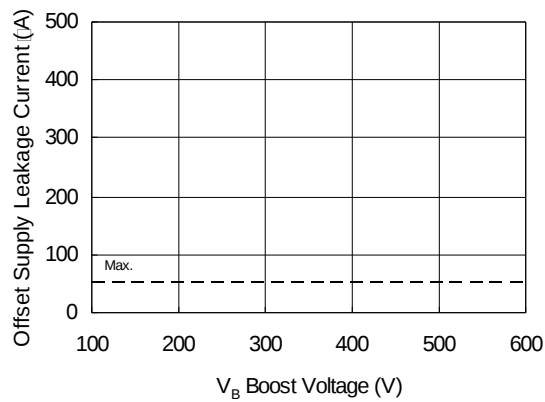
**Figure 12A. Low Level Output vs. Temperature**



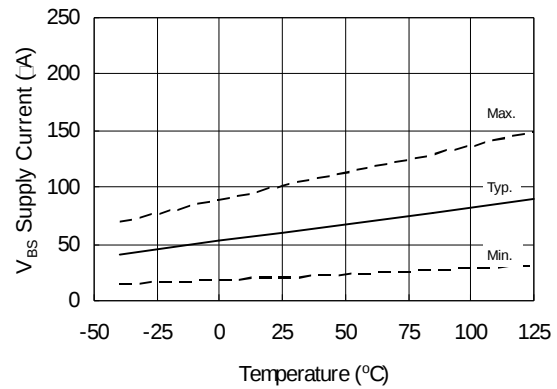
**Figure 12B. Low Level Output vs. Supply Voltage**



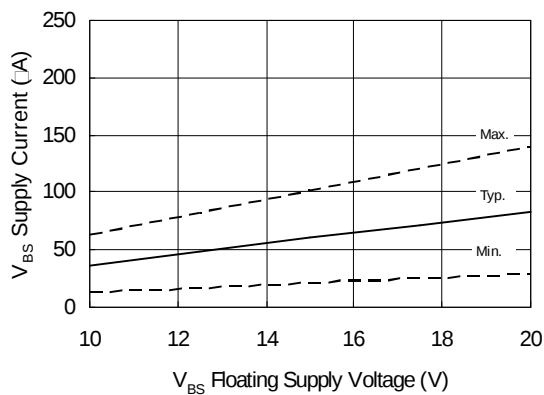
**Figure 13A. Offset Supply Leakage Current vs. Temperature**



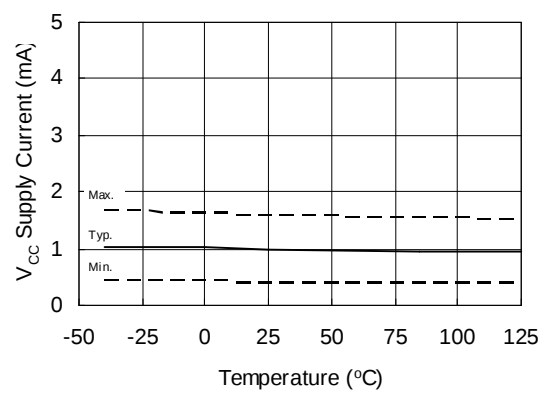
**Figure 13B. Offset Supply Leakage Current vs.  $V_B$  Boost Voltage**



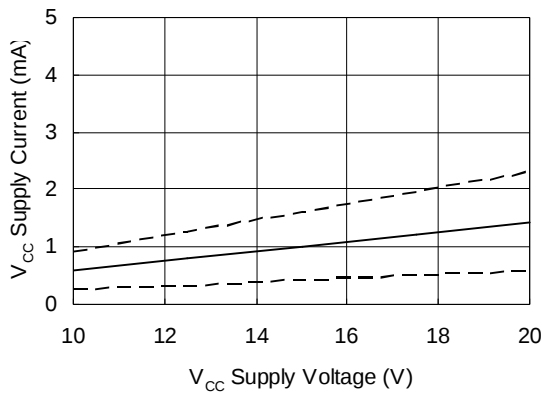
**Figure 14A.  $V_{BS}$  Supply Current vs. Temperature**



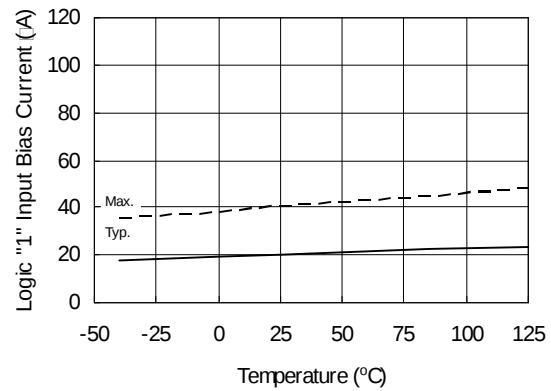
**Figure 14B.  $V_{BS}$  Supply Current vs.  $V_{BS}$  Floating Supply Voltage**



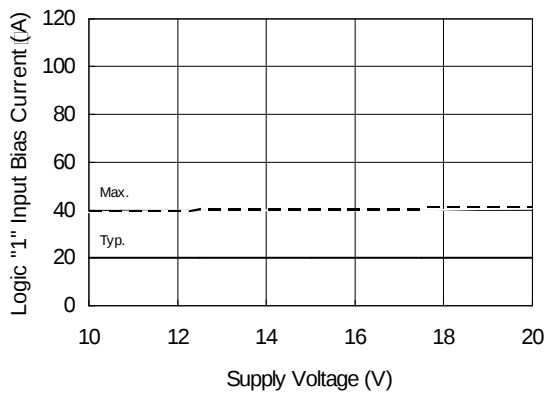
**Figure 15A.  $V_{CC}$  Supply Current vs. Temperature**



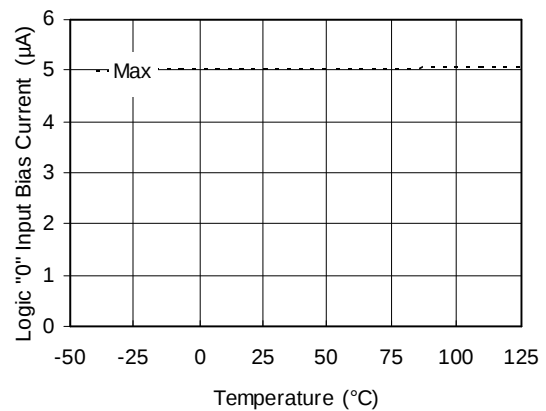
**Figure 15B. V<sub>CC</sub> Supply Current vs. V<sub>CC</sub> Supply Voltage**



**Figure 16A. Logic "1" Input Bias Current vs. Temperature**



**Figure 16B. Logic "1" Input Bias Current vs. Supply Voltage**



**Figure 17A. Logic "0" Input Bias Current vs. Temperature**

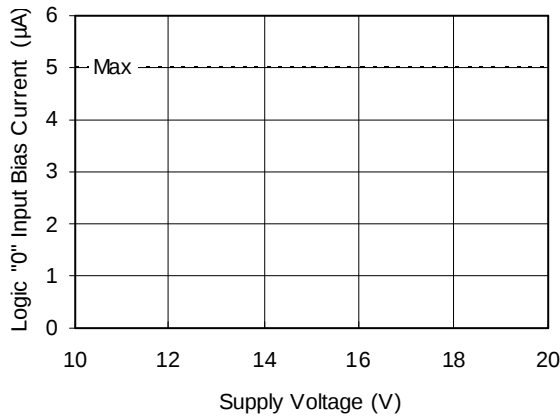


Figure 17B. Logic "0" Input Bias Current vs. Voltage

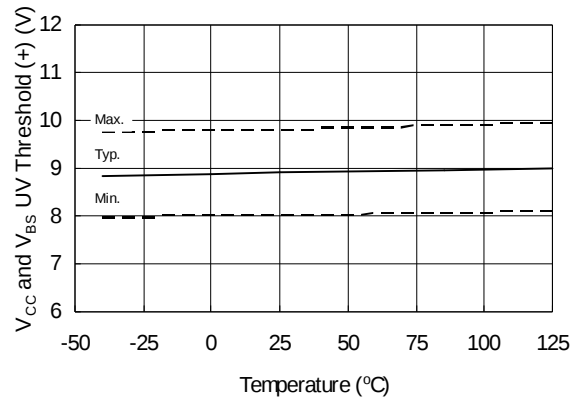


Figure 18.  $V_{CC}$  and  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature

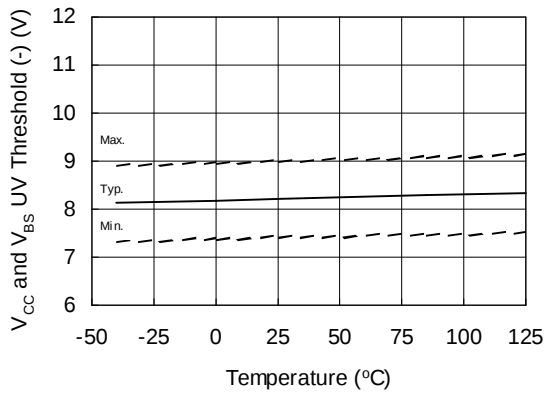


Figure 19.  $V_{CC}$  and  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature

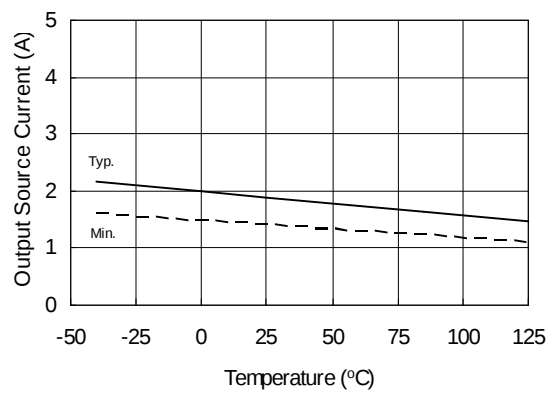
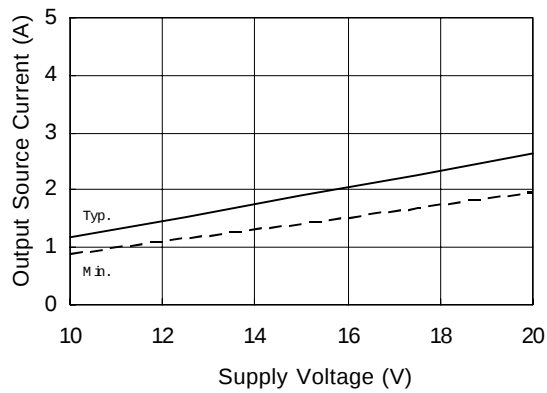
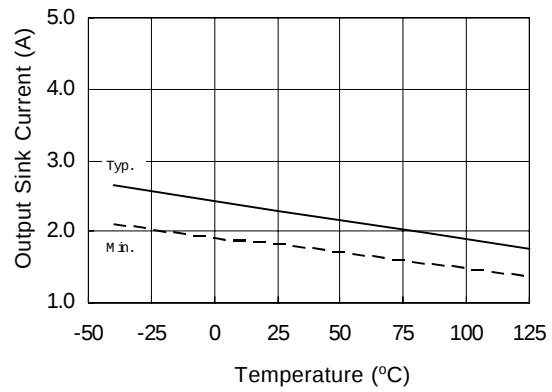


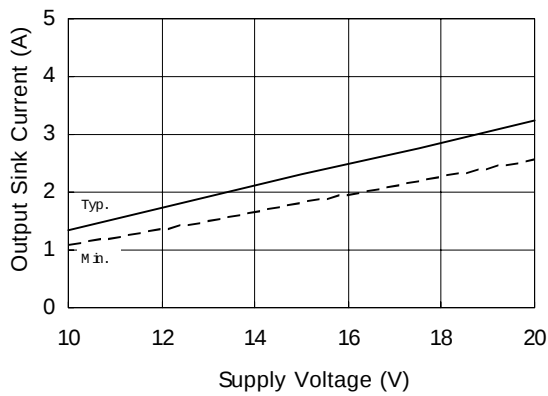
Figure 20A. Output Source Current vs. Temperature



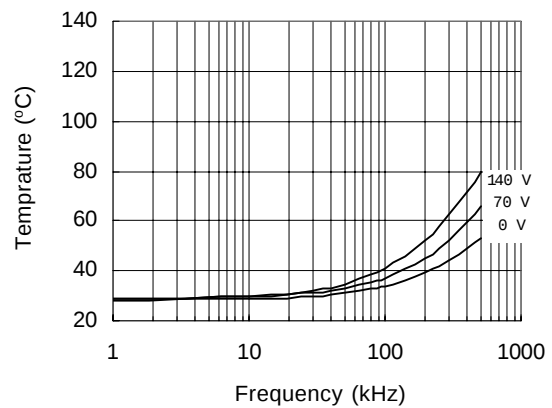
**Figure 20B. Output Source Current vs. Supply Voltage**



**Figure 21A. Output Sink Current vs. Temperature**



**Figure 21B. Output Sink Current vs. Supply Voltage**



**Figure 22. IRS2183 vs. Frequency (IRFBC20),  
 $R_{gate}=33\ \Omega$ ,  $V_{CC}=15\ V$**

## IRS2183/IRS21834(S)PbF

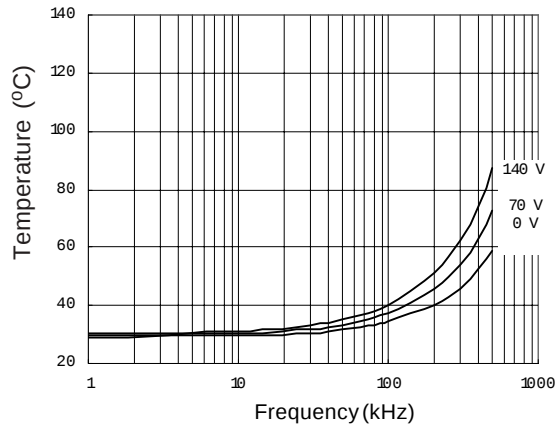


Figure 23. IRS2183 vs. Frequency (IRFBC30),  
 $R_{gate}=22\ \Omega$ ,  $V_{CC}=15\ V$

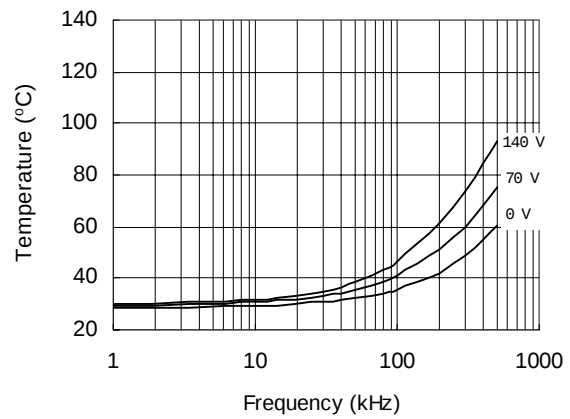


Figure 24. IRS2183 vs. Frequency (IRFBC40),  
 $R_{gate}=15\ \Omega$ ,  $V_{CC}=15\ V$

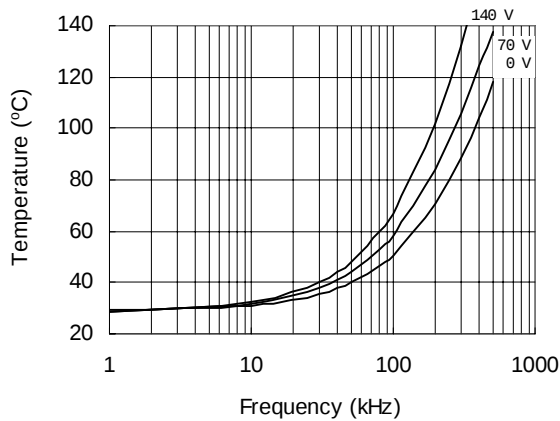


Figure 25. IRS2183 vs. Frequency (IRFPE50),  
 $R_{gate}=10\ \Omega$ ,  $V_{CC}=15\ V$

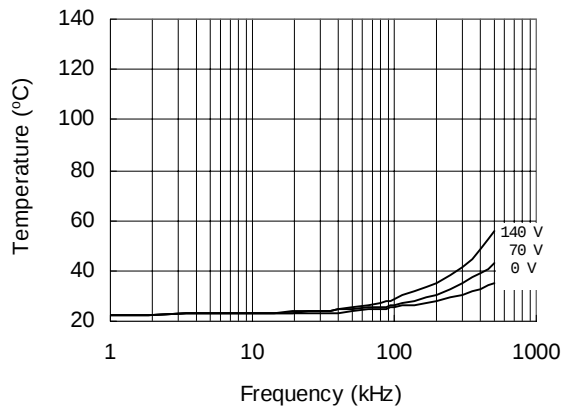


Figure 26. IRS21834 vs. Frequency (IRFBC20),  
 $R_{gate}=33\ \Omega$ ,  $V_{CC}=15\ V$

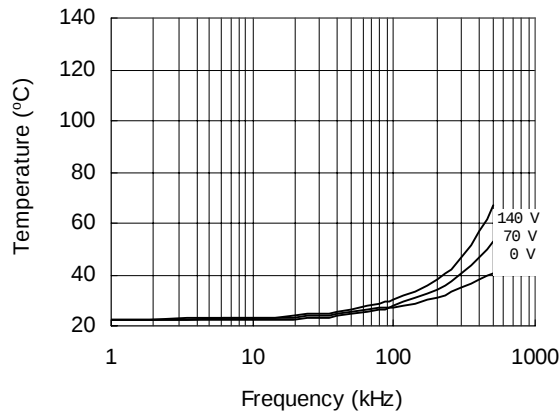


Figure 27. IRS21834 vs. Frequency (IRFBC30),  
 $R_{gate}=22\ \Omega$ ,  $V_{CC}=15\ V$

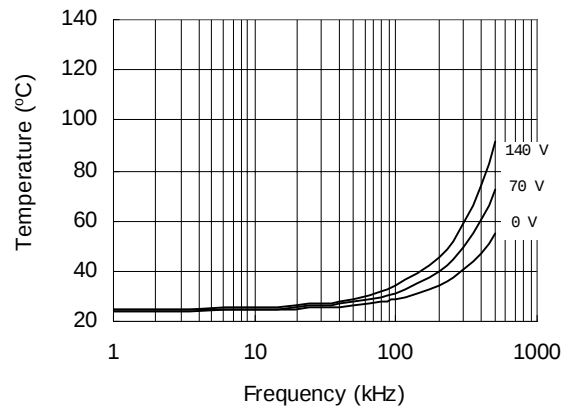


Figure 28. IRS21834 vs. Frequency (IRFBC40),  
 $R_{gate}=15\ \Omega$ ,  $V_{CC}=15\ V$

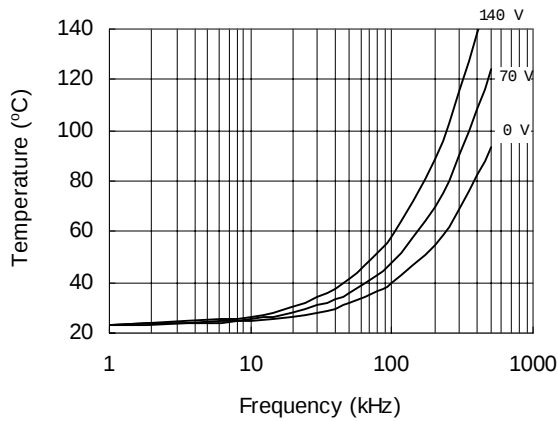


Figure 29. IRS21834 vs. Frequency (IRFPE50),  
 $R_{gate}=10\ \Omega$ ,  $V_{CC}=15\ V$

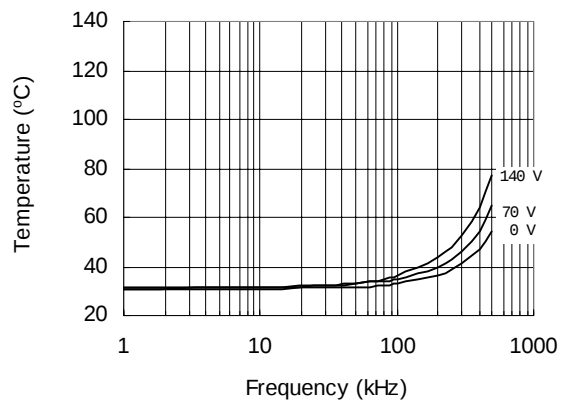
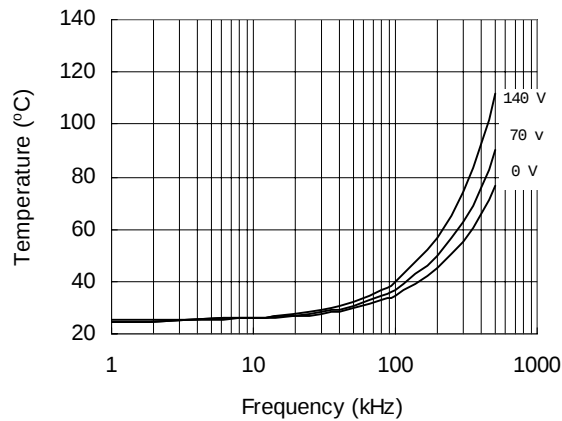
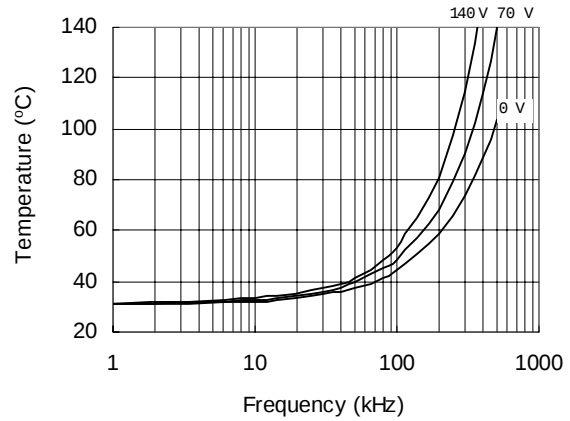


Figure 30. IRS2183S vs. Frequency (IRFBC20),  
 $R_{gate}=33\ \Omega$ ,  $V_{CC}=15\ V$

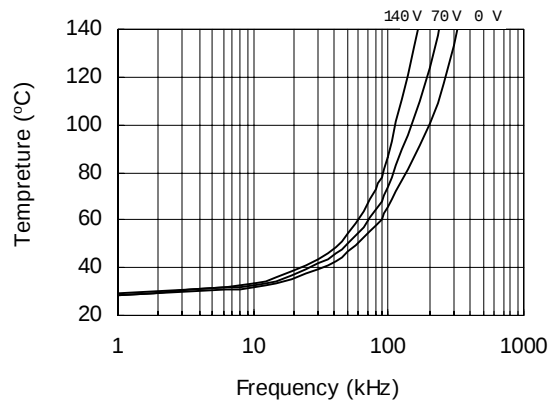
## IRS2183/IRS21834(S)PbF



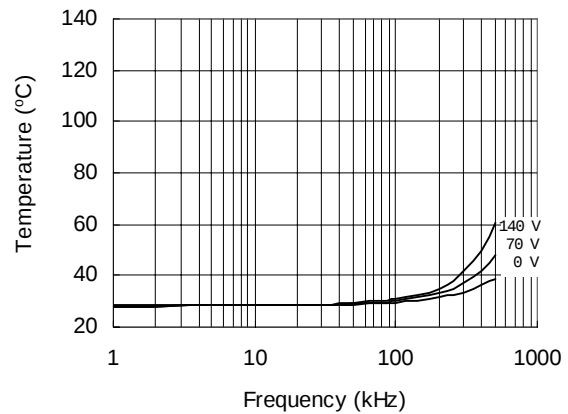
**Figure 31. IRS2183S vs. Frequency (IRFBC30),  
 $R_{gate}=22\ \Omega$ ,  $V_{CC}=15\ V$**



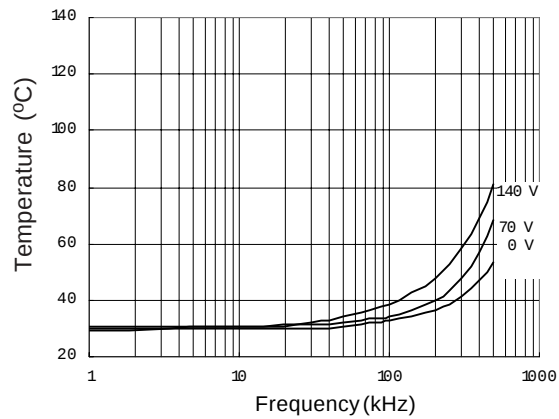
**Figure 32. IRS2183S vs. Frequency (IRFBC40),  
 $R_{gate}=15\ \Omega$ ,  $V_{CC}=15\ V$**



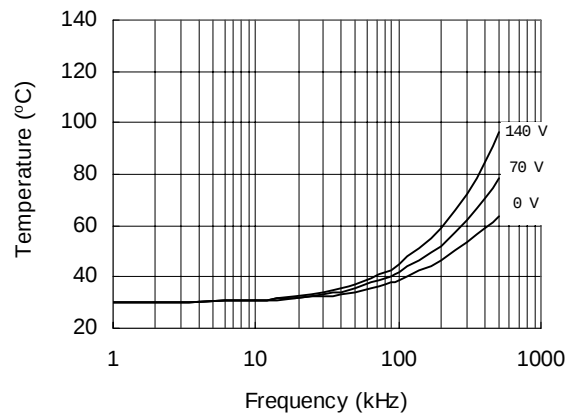
**Figure 33. IRS2183S vs. Frequency (IRFPE50),  
 $R_{gate}=10\ \Omega$ ,  $V_{CC}=15\ V$**



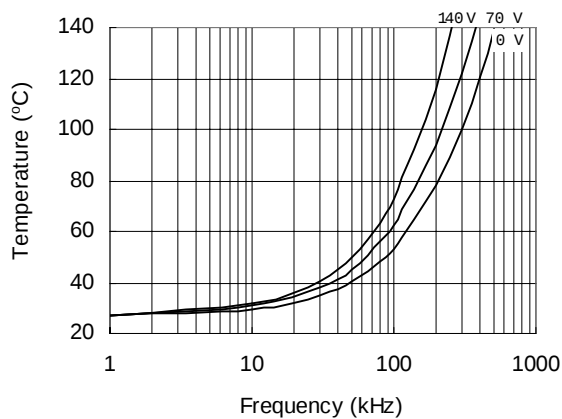
**Figure 34. IRS21834S vs. Frequency (IRFBC20),  
 $R_{gate}=33\ \Omega$ ,  $V_{CC}=15\ V$**



**Figure 35. IRS21834S vs. Frequency (IRFBC30),**  
 $R_{gate}=22\ \Omega$ ,  $V_{CC}=15\ V$

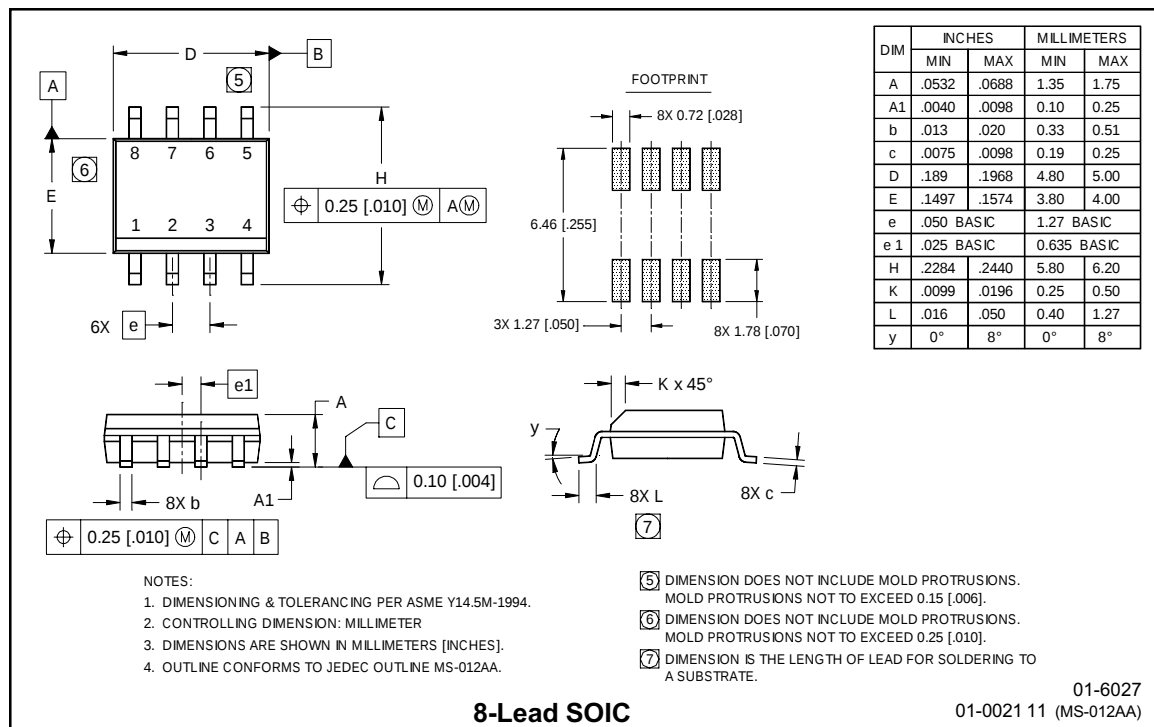
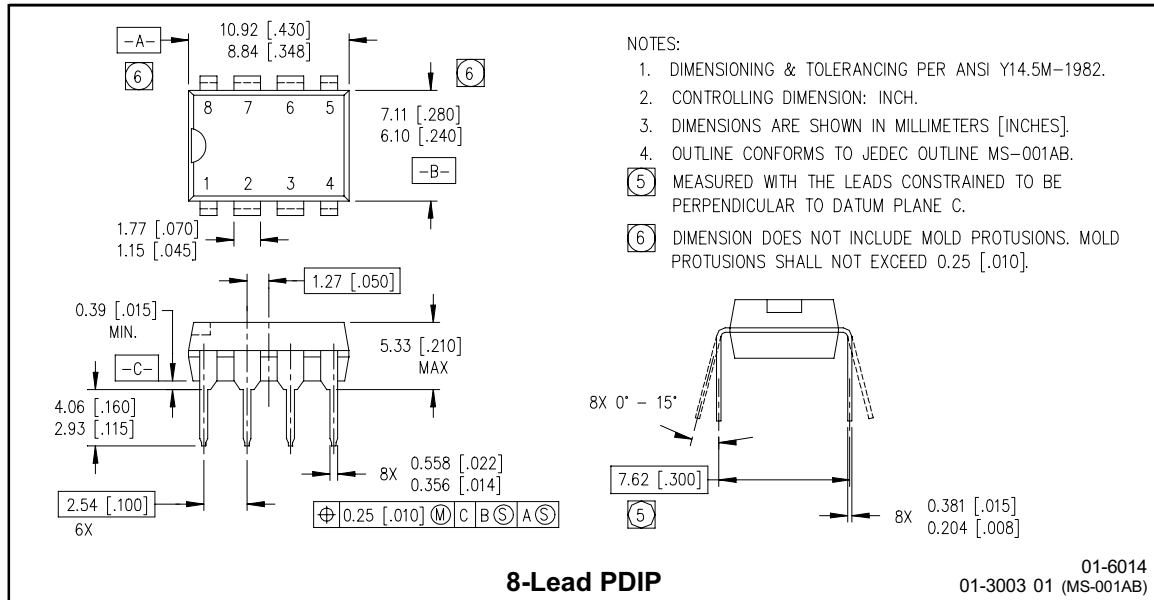


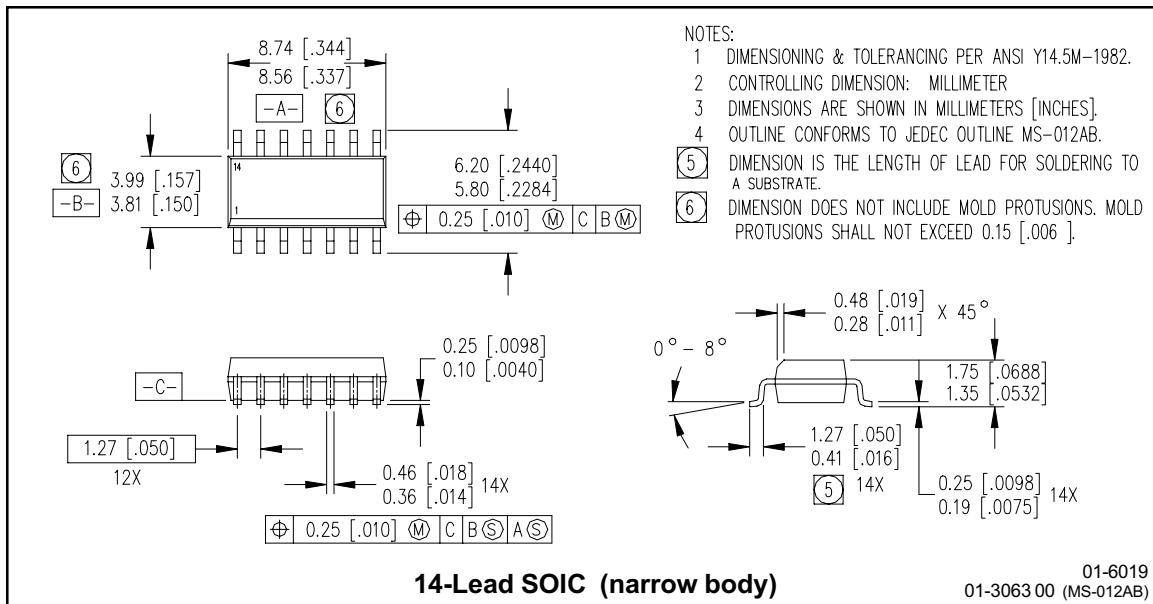
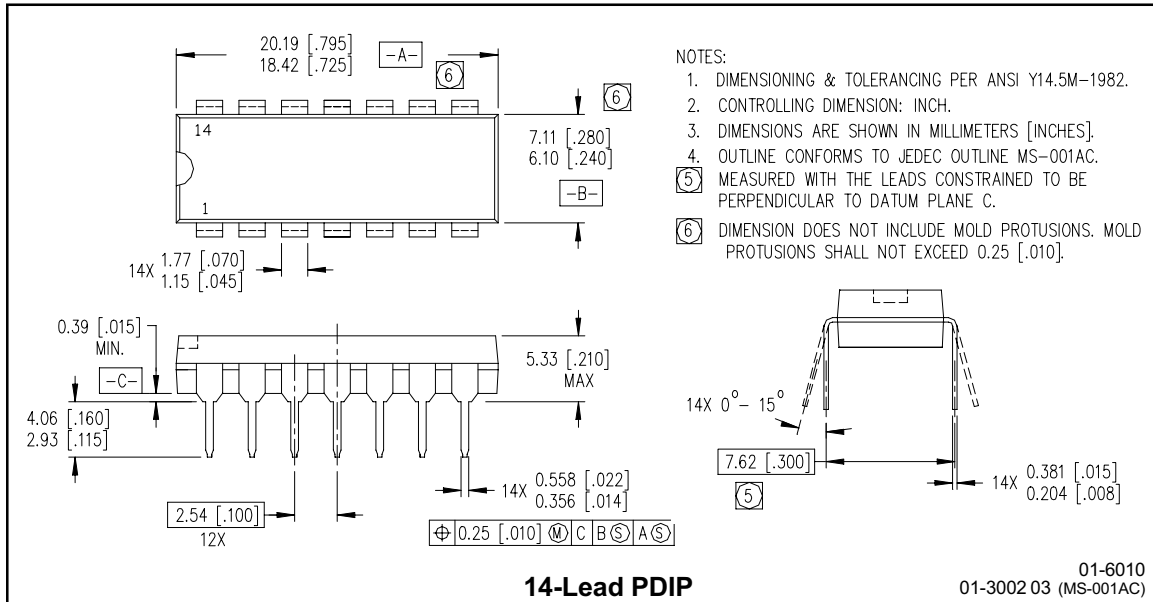
**Figure 36. IRS21834S vs. Frequency (IRFBC40),**  
 $R_{gate}=15\ \Omega$ ,  $V_{CC}=15\ V$



**Figure 37. IRS21834S vs. Frequency (IRFPE50),**  
 $R_{gate}=10\ \Omega$ ,  $V_{CC}=15\ V$

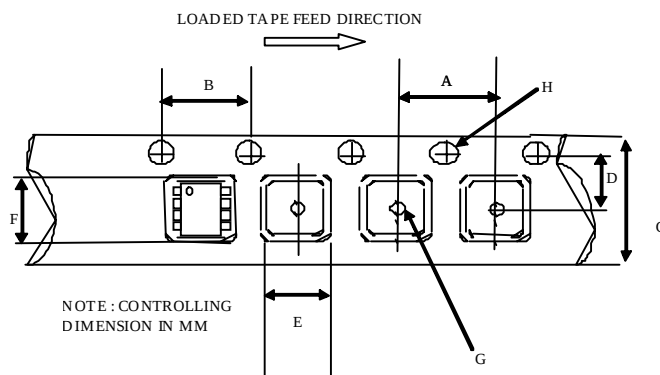
## Case outlines





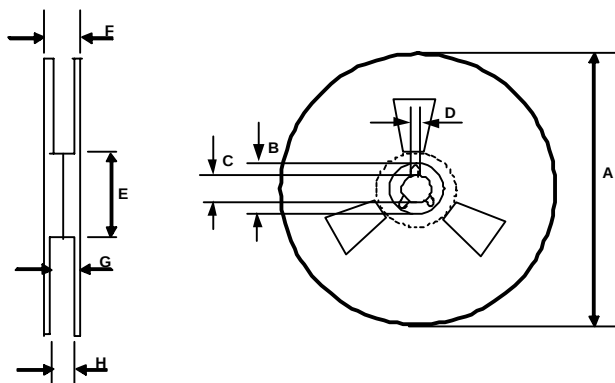
# IRS2183/IRS21834(S)PbF

## Tape & Reel 8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

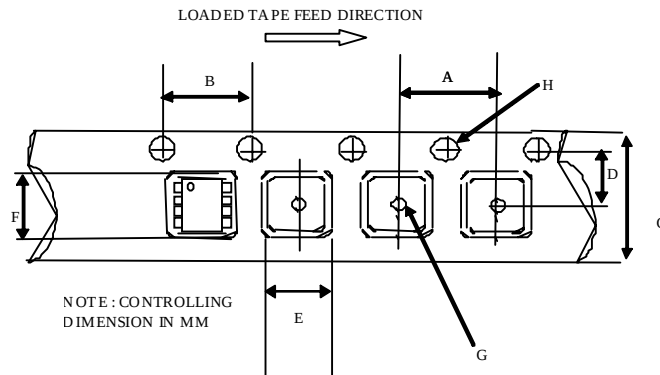
| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 7.90   | 8.10  | 0.311    | 0.318 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 11.70  | 12.30 | 0.46     | 0.484 |
| D    | 5.45   | 5.55  | 0.214    | 0.218 |
| E    | 6.30   | 6.50  | 0.248    | 0.255 |
| F    | 5.10   | 5.30  | 0.200    | 0.208 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |



REEL DIMENSIONS FOR 8SOICN

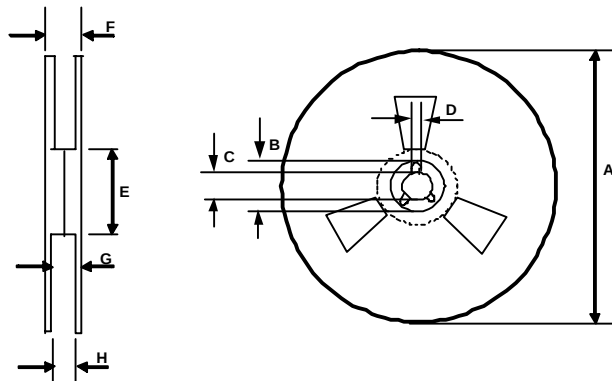
| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 18.40  | n/a      | 0.724  |
| G    | 14.50  | 17.10  | 0.570    | 0.673  |
| H    | 12.40  | 14.40  | 0.488    | 0.566  |

## Tape & Reel 14-lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 7.90   | 8.10  | 0.311    | 0.318 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 15.70  | 16.30 | 0.618    | 0.641 |
| D    | 7.40   | 7.60  | 0.291    | 0.299 |
| E    | 6.40   | 6.60  | 0.252    | 0.260 |
| F    | 9.40   | 9.60  | 0.370    | 0.378 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |

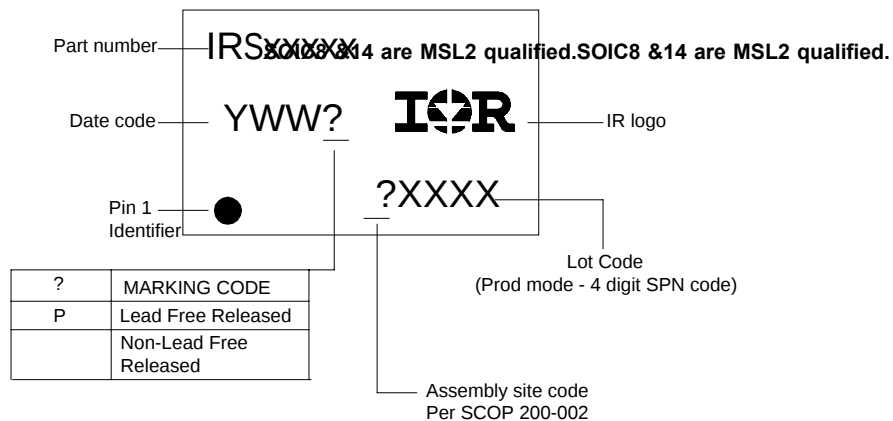


REEL DIMENSIONS FOR 14SOICN

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 22.40  | n/a      | 0.881  |
| G    | 18.50  | 21.10  | 0.728    | 0.830  |
| H    | 16.40  | 18.40  | 0.645    | 0.724  |

# IRS2183/IRS21834(S)PbF

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

8-Lead PDIP IRS2183PbF  
8-Lead SOIC IRS2183SPbF  
8-Lead SOIC Tape & Reel IRS2183STRPbF

14-Lead PDIP IRS21834PbF  
14-Lead SOIC IRS21834SPbF  
14-Lead SOIC Tape & Reel IRS21834STRPbF

**SOIC8 & 14 are MSL2 qualified.**

**This product has been designed and qualified for the industrial level.**

**Qualification standards can be found at [www.irf.com](http://www.irf.com)**

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105  
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