

# TLD5542-1

## H-Bridge DC/DC Controller with SPI Interface

Infineon® LITIX™ Power Flex



<b>Package</b>	PG-VQFN-48	PG-TQFP-48
<b>Marking</b>	TLD55421QV	TLD55421QU
<b>Sales Name</b>	TLD5542-1QV	TLD5542-1QU

## 1 Overview

### Features

- Single inductor high power Buck-Boost controller
- Wide LED forward voltage range (2 V up to 55 V)
- Wide VIN range (IC 4.5 V to 40 V, power 4.5 V to 55 V)
- Switching frequency range from 200 kHz to 700 kHz
- SPI for diagnostics and control
- Maximum efficiency in every condition (up to 96%)
- Constant current (LED) and constant voltage regulation
- Drives multiple loads with a single IC thanks to the Fast Output Discharge operation
- Limp Home function (fail safe mode)
- EMC optimized device: features an Auto Spread Spectrum
- LED and input current sense with dedicated monitor outputs
- Advanced protection features for device and load
- Enhanced dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48 or PG-TQFP-48 package
- Automotive AEC Qualified

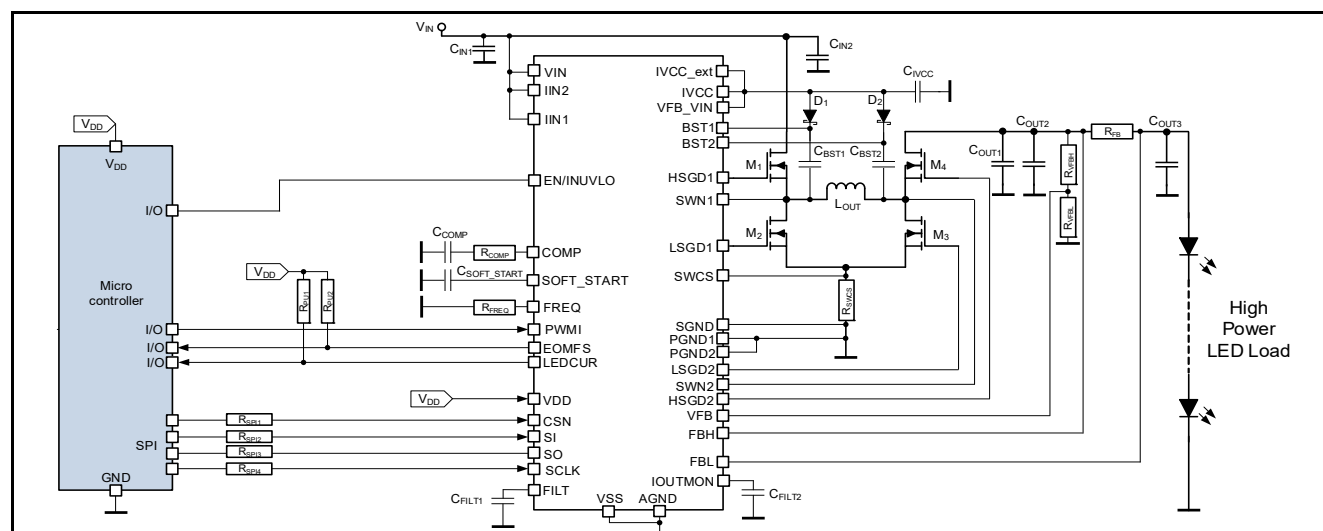
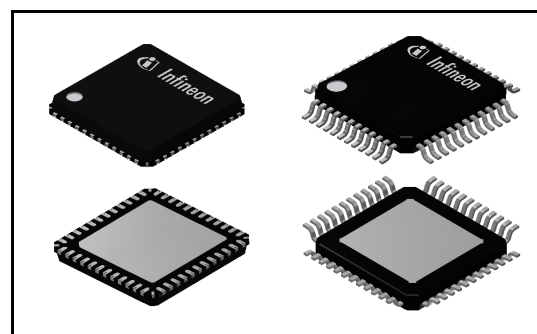


Figure 1 Application Drawing - TLD5542-1 as current regulator

## Overview

### Description

The TLD5542-1 is a synchronous MOSFET H-Bridge DC/DC controller with built in protection features and SPI interface. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5542-1 offers both analog and digital (PWM) dimming. The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programmable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5542-1 is suitable for use in the harsh automotive environment.

**Table 1 Product Summary**

Power Stage input voltage range	$V_{POW}$	4.5 V ... 55 V
Device Input supply voltage range	$V_{VIN}$	4.5 V ... 40 V
Maximum output voltage (depending by the application conditions)	$V_{OUT(max)}$	55 V as LED Driver Boost Mode 50 V as LED Driver Buck Mode 50 V as Voltage regulator
Switching Frequency range	$f_{SW}$	200 kHz... 700 kHz
Typical NMOS driver on-state resistance at $T_j = 25^\circ\text{C}$ (Gate Pull Up)	$R_{DS(ON\_PU)}$	2.3 $\Omega$
Typical NMOS driver on-state resistance at $T_j = 25^\circ\text{C}$ (Gate Pull Down)	$R_{DS(ON\_PD)}$	1.2 $\Omega$
SPI clock frequency	$f_{SCLK(MAX)}$	5 MHz

### Protective Functions

- Over load protection of external MOSFETs
- Shorted load, output overvoltage protection
- Input undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

### Diagnostic Functions

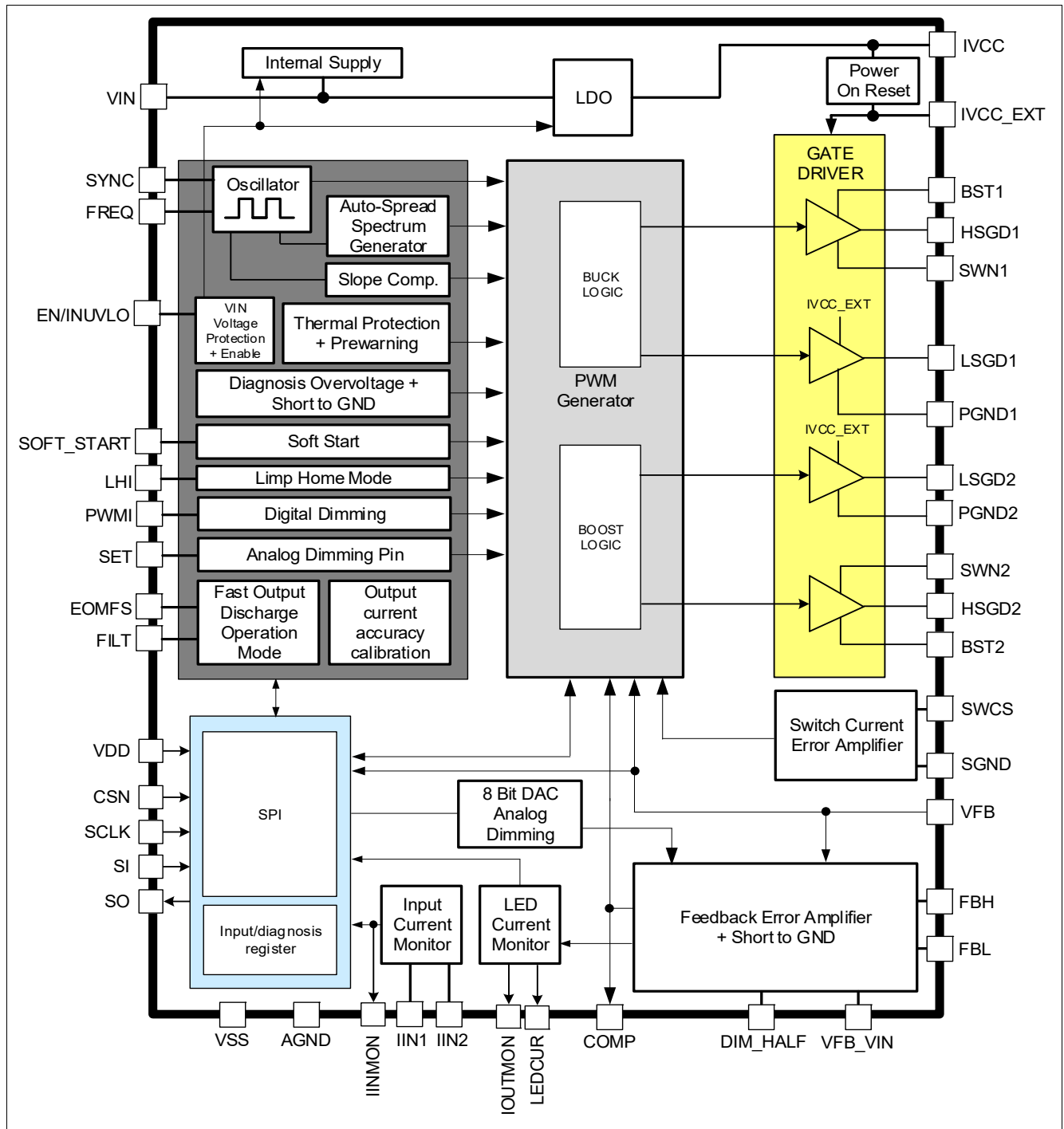
- Latched diagnostic information via SPI
- Device Overtemperature shutdown and Temperature Prewarning
- Smart monitoring and advanced functions provide  $I_{LED}$  and  $I_{IN}$  information

### Limp Home Function

- Limp Home activation via LHI pin

### Applications

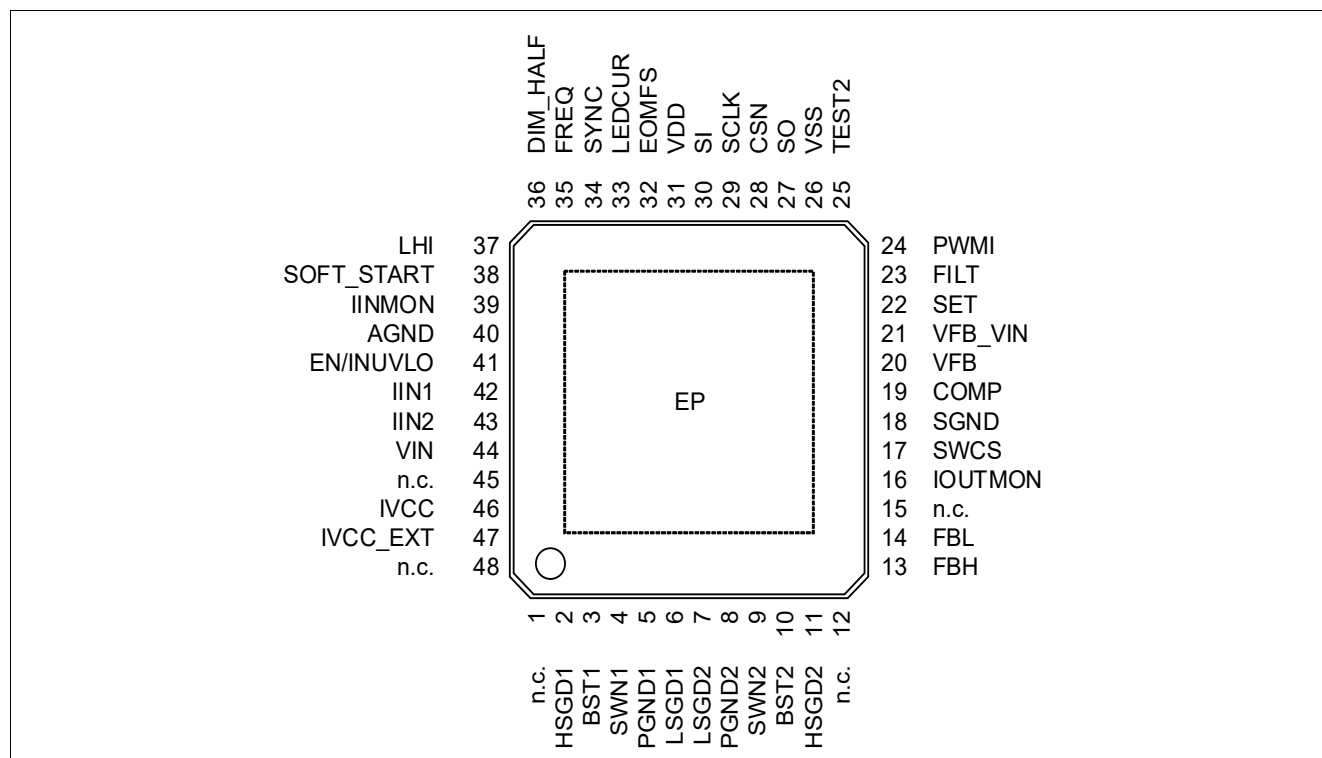
- Especially designed for driving multiple high power LED functions (I.E. Low Beam, High Beam, DRL)
- Automotive Exterior Lighting: full LED headlamp assemblies
- General purpose DC/DC voltage regulator



## Pin Configuration

### 3 Pin Configuration

#### 3.1 Pin Assignment



**Figure 3 Pin Configuration - TLD5542-1**

## Pin Configuration

### 3.2 Pin Definitions and Functions

**Table 2 Pin Definitions and Functions**

Pin	Symbol	I/O <sup>1)</sup>		Function
Power Supply				
1, 12, 15, 45, 48	n.c.	-		Not connected, tie to AGND on the Layout;
44	VIN	-		Power Supply Voltage; Supply for internal biasing.
31	VDD	-		Digital GPIO Supply Voltage; Connect to reverse voltage protected 5 V or 3.3 V supply.
47	IVCC_EXT	I	PD	External LDO input; Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open.
5, 8	PGND1, 2	-		Power Ground; Ground for power potential. Connect externally close to the chip.
26	VSS	-		Digital GPIO Ground; Ground for GPIO pins.
40	AGND	-		Analog Ground; Ground Reference
-	EP	-		Exposed Pad; Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).
Gate Driver Stages				
2	HSGD1	O		Highside Gate Driver Output 1; Drives the top n-channel MOSFET with a voltage equal to $V_{IVCC\_EXT}$ superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET.
11	HSGD2	O		Highside Gate Driver Output 2; Drives the top n-channel MOSFET with a voltage equal to $V_{IVCC\_EXT}$ superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET.
6	LSGD1	O		Lowside Gate Driver Output 1; Drives the lowside n-channel MOSFET between GND and $V_{IVCC\_EXT}$ . Connect to gate of external switching MOSFET.
7	LSGD2	O		Lowside Gate Driver Output 2; Drives the lowside n-channel MOSFET between GND and $V_{IVCC\_EXT}$ . Connect to gate of external switching MOSFET.
4	SWN1	IO		Switch Node 1; SWN1 pin swings from a diode voltage drop below ground up to $V_{IN}$ .
9	SWN2	IO		Switch Node 2; SWN2 pin swings from ground up to a diode voltage drop above $V_{OUT}$ .

**Pin Configuration**

**Table 2 Pin Definitions and Functions**

Pin	Symbol	I/O <sup>1)</sup>		Function
46	IVCC	O		<b>Internal LDO output;</b> Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open.
<b>Inputs and Outputs</b>				
37	LHI	I	PD	<b>Limp Home Input Pin;</b> Used to enter in Limp Home state during Fail Safe condition.
23	FILT	-		<b>MFS Filter;</b> Connect with a 220pF capacitor to GND to filter MFS reference Voltage.
25	TEST2	-		<b>Test Pin;</b> Used for Infineon end of line test, connect to GND in application.
41	EN/INUVLO	I	PD	<b>Enable/Input Under Voltage Lock Out;</b> Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open.
35	FREQ	I		<b>Frequency Select Input;</b> Connect external resistor to GND to set frequency.
34	SYNC	I	PD	<b>Synchronization Input;</b> Apply external clock signal for synchronization.
24	PWMI	I	PD	<b>Control Input;</b> Digital input 5 V or 3.3 V.
13	FBH	I		<b>Output current Feedback Positive;</b> Non inverting Input (+).
14	FBL	I		<b>Output current Feedback Negative;</b> Inverting Input (-).
3	BST1	IO		<b>Bootstrap capacitor;</b> Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open.
10	BST2	IO		<b>Bootstrap capacitor;</b> Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open.
17	SWCS	I		<b>Current Sense Input;</b> Inductor current measurement - Non Inverting Input (+).
18	SGND	I		<b>Current Sense Ground;</b> Inductor current sense - Inverting Input (-). Route as Differential net with SWCS on the Layout.
42	IIN1	I		<b>Input Current Monitor Positive;</b> Non Inverting Input (+), connect to VIN if input current monitor is not needed.
43	IIN2	I		<b>Input Current Monitor Negative;</b> Inverting Input (-), connect to VIN if input current monitor is not needed.
19	COMP	O		<b>Compensation Network Pin;</b> Connect R and C network to pin for stability phase margin adjustment.

## Pin Configuration

**Table 2 Pin Definitions and Functions**

Pin	Symbol	I/O <sup>1)</sup>	Function
38	SOFT_START	O	<b>Softstart configuration Pin;</b> Connect a capacitor $C_{SOFT\_START}$ to GND to fix a soft start ramp default time.
21	VFB_VIN	I	<b>Input Voltage Feedback for analog dimming compensation;</b> Connect with a Resistor divider to Vin. If not used, short to IVCC
36	DIM_HALF	I	<b>Dual Range Output Current;</b> Double the analog dimming compensation when High.
20	VFB	I	<b>Voltage Loop Feedback Pin;</b> VFB is intended to set output overvoltage protection and F.D. output voltage sensing.
22	SET	I	<b>Analog current sense adjustment Pin;</b>
39	IINMON	O	<b>Input current monitor output;</b> Monitor pin that produces a voltage proportional to $V_{IIN1-IIN2}$ . Typical IINMON will be equal 1 V when $V_{IIN1}-V_{IIN2} = 50$ mV.
16	IOUTMON	O	<b>Output current monitor output;</b> Monitor pin that produces a voltage proportional to $V_{FBH-FBL}$ plus an offset. Connect with a bypass capacitor to ground
33	LEDCUR	O	<b>LED current Flag;</b> An open drain output used to detect the presence of load current on MFS topologies
32	EOMFS	O	<b>End of MFS routine Flag;</b> An open drain output which is pulled to LOW when MFS routine is ongoing, released to high when complete.

### SPI

30	SI	I	PD	<b>Serial data in;</b> Digital input 5 V or 3.3 V.
29	SCLK	I	PD	<b>Serial clock;</b> Digital input 5 V or 3.3 V.
28	CSN	I	PU	<b>SPI chip select;</b> Digital input 5 V or 3.3 V. Active LOW.
27	SO	O		<b>Serial data out;</b> Digital output, referenced to $V_{DD}$ .

- 1) O: Output, I: Input,  
PD: pull-down circuit integrated,  
PU: pull-up circuit integrated

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings<sup>1)</sup>**

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
VIN Supply Input	V <sub>VIN</sub>	-0.3	–	60	V	–	P_4.1.1
VDD Digital supply voltage	V <sub>VDD</sub>	-0.3	–	6	V	–	P_4.1.2
IVCC Internal Linear Voltage Regulator Output voltage	V <sub>IVCC</sub>	-0.3	–	6	V	–	P_4.1.3
IVCC_EXT External Linear Voltage Regulator Input voltage	V <sub>IVCC_EXT</sub>	-0.3	–	6	V	–	P_4.1.4
Gate Driver Stages							
LSGD1,2 - PGND1,2 Lowside Gatedriver voltage	V <sub>LSGD1,2- PGND1,2</sub>	-0.3	–	5.5	V	–	P_4.1.54
HSGD1,2 - SWN1,2 Highside Gatedriver voltage	V <sub>HSGD1,2- SWN1,2</sub>	-0.3	–	5.5	V	2)	P_4.1.55
SWN1, SWN2 switching node voltage	V <sub>SWN1, 2</sub>	-1	–	60	V	–	P_4.1.6
(BST1-SWN1), (BST2-SWN2) Bootstrap voltage	V <sub>BST1,2- SWN1,2</sub>	-0.3	–	6	V	2)	P_4.1.7
BST1, BST2 Bootstrap voltage related to GND	V <sub>BST1, 2</sub>	-0.3	–	65	V	–	P_4.1.8
SWCS Switch Current Sense Input voltage	V <sub>SWCS</sub>	-0.3	–	0.3	V	–	P_4.1.9
SGND Switch Current Sense GND voltage	V <sub>SGND</sub>	-0.3	–	0.3	V	–	P_4.1.10
SWCS-SGND Switch Current Sense differential voltage	V <sub>SWCS- SGND</sub>	-0.5	–	0.5	V	–	P_4.1.11
PGND1,2 Power GND voltage	V <sub>PGND1,2</sub>	-0.3	–	0.3	V	–	P_4.1.28
High voltage Pins							
IIN1, IIN2 Input Current monitor voltage	V <sub>IIN1, 2</sub>	-0.3	–	60	V	–	P_4.1.12



**General Product Characteristics**

**Table 3 Absolute Maximum Ratings<sup>1)</sup> (cont'd)**  
 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IIN1-IIN2 Input Current monitor differential voltage	$V_{\text{IIN1-IIN2}}$	-0.5	–	0.5	V	2)	P_4.1.13
FBH, FBL Feedback Error Amplifier voltage	$V_{\text{FBH, FBL}}$	-0.3	–	60	V	–	P_4.1.14
FBH-FBL Feedback Error Amplifier differential voltage	$V_{\text{FBH-FBL}}$	-0.5	–	0.5	V	2)	P_4.1.15
EN/INUVLO Device enable/input undervoltage lockout	$V_{\text{EN/INUVLO}}$	-0.3	–	60	V	–	P_4.1.16

**Digital (I/O) Pins**

PWMI Digital Input voltage	$V_{\text{PWMI}}$	-0.3	–	5.5	V	–	P_4.1.17
CSN Voltage at Chip Select pin	$V_{\text{CSN}}$	-0.3	–	5.5	V	–	P_4.1.18
SCLK Voltage at Serial Clock pin	$V_{\text{SCLK}}$	-0.3	–	5.5	V	–	P_4.1.19
SI Voltage at Serial Input pin	$V_{\text{SI}}$	-0.3	–	5.5	V	–	P_4.1.20
SO Voltage at Serial Output pin	$V_{\text{SO}}$	-0.3	–	5.5	V	–	P_4.1.21
SYNC Synchronization Input voltage	$V_{\text{SYNC}}$	-0.3	–	5.5	V	–	P_4.1.22
LHI Limp Home Input Voltage	$V_{\text{LHI}}$	-0.3	–	5.5	V	–	P_4.1.58

**Analog Pins**

VFB, VFB_VIN Output and Input Voltage feedback pins	$V_{\text{VFB}}, V_{\text{VFB\_VIN}}$	-0.3	–	5.5	V	–	P_4.1.25
DIM_HALF Dual Range Output Current	$V_{\text{DIM\_HALF}}$	-0.3	–	5.5	V	–	P_4.1.26
FILT MFS Filter pin voltage	$V_{\text{FILT}}$	-0.3	–	3	V	–	P_4.1.62
EOMFS, LEDCUR Flags output voltage	$V_{\text{FLAGS}}$	-0.3	–	5.5	V	–	P_4.1.61
SET Analog dimming Input voltage	$V_{\text{SET}}$	-0.3	–	5.5	V	–	P_4.1.29
COMP Compensation Input voltage	$V_{\text{COMP}}$	-0.3	–	3.6	V	–	P_4.1.30

**General Product Characteristics**

**Table 3 Absolute Maximum Ratings<sup>1)</sup> (cont'd)**  
 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SOFT_START Softstart Voltage	$V_{\text{SOFT\_STAR T}}$	-0.3	–	3.6	V	–	P_4.1.31
FREQ Voltage at frequency selection pin	$V_{\text{FREQ}}$	-0.3	–	3.6	V	–	P_4.1.32
IINMON Voltage at input monitor pin	$V_{\text{IINMON}}$	-0.3	–	3.6	V	–	P_4.1.33
IOUTMON Voltage at output monitor pin	$V_{\text{IOUTMON}}$	-0.3	–	5.5	V	–	P_4.1.34

**Temperatures**

Junction Temperature	$T_J$	-40	–	150	$^{\circ}\text{C}$	–	P_4.1.35
Storage Temperature	$T_{\text{stg}}$	-55	–	150	$^{\circ}\text{C}$	–	P_4.1.36

**ESD Susceptibility**

ESD Resistivity of all Pins	$V_{\text{ESD,HBM}}$	-2	–	2	kV	HBM <sup>3)</sup>	P_4.1.37
ESD Resistivity to GND	$V_{\text{ESD,CDM}}$	-500	–	500	V	CDM <sup>4)</sup>	P_4.1.38
ESD Resistivity of corner Pins to GND	$V_{\text{ESD,CDM\_corner}}$	-750	–	750	V	CDM <sup>4)</sup>	P_4.1.39

1) Not subject to production test, specified by design.

2) Does not refer to GND

3) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002

4) ESD susceptibility, Charged Device Model “CDM” AECQ100-011 Rev. D

**Note:** Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4.2 Functional Range

**Table 4 Functional Range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Device Extended Supply Voltage Range	$V_{\text{VIN}}$	4.5	–	40	V	<sup>1)</sup> (parameter deviations possible)	P_4.2.1
Device Nominal Supply Voltage Range	$V_{\text{VIN}}$	8	–	36	V	–	P_4.2.2
Power Stage Voltage Range	$V_{\text{POW}}$	4.5	–	55	V	<sup>1)</sup>	P_4.2.5

**General Product Characteristics**

**Table 4 Functional Range** (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Supply Voltage	$V_{DD}$	3	–	5.5	V	–	P_4.2.3
Junction Temperature	$T_j$	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 5**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	$R_{thJC}$	–	0.9	–	K/W	<sup>1) 2)</sup>	P_4.3.1
Junction to Ambient	$R_{thJA}$	–	25	–	K/W	<sup>3)</sup> 2s2p	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature).  $T_a = 25^\circ\text{C}$ ; The IC is dissipating 1 W.

3) Specified  $R_{thJA}$  value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70  $\mu\text{m}$  Cu) and 2 inner copper layers (2 x 35  $\mu\text{m}$  Cu). A thermal via (diameter = 0.3 mm and 25  $\mu\text{m}$  plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB.  $T_a = 25^\circ\text{C}$ ; The IC is dissipating 1 W.

## Power Supply

### 5 Power Supply

The TLD5542-1 is supplied by the following pins:

- VIN (main supply voltage)
- VDD (digital supply voltage)
- IVCC\_EXT (supply for internal gate driver stages)

The VIN supply, in combination with the VDD supply, provides internal supply voltages for the analog and digital blocks. In situations where VIN voltage drops below VDD voltage, an increased current consumption may be observed at the VDD pin.

The SPI and IO interfaces are supplied by the VDD pin.

IVCC\_EXT is the supply for the low side driver stages, which is also used to charge, by means of external Schottky diodes, the bootstrap capacitors. These capacitors provide power to the high side driver stages. If no external voltage is available, IVCC\_EXT pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

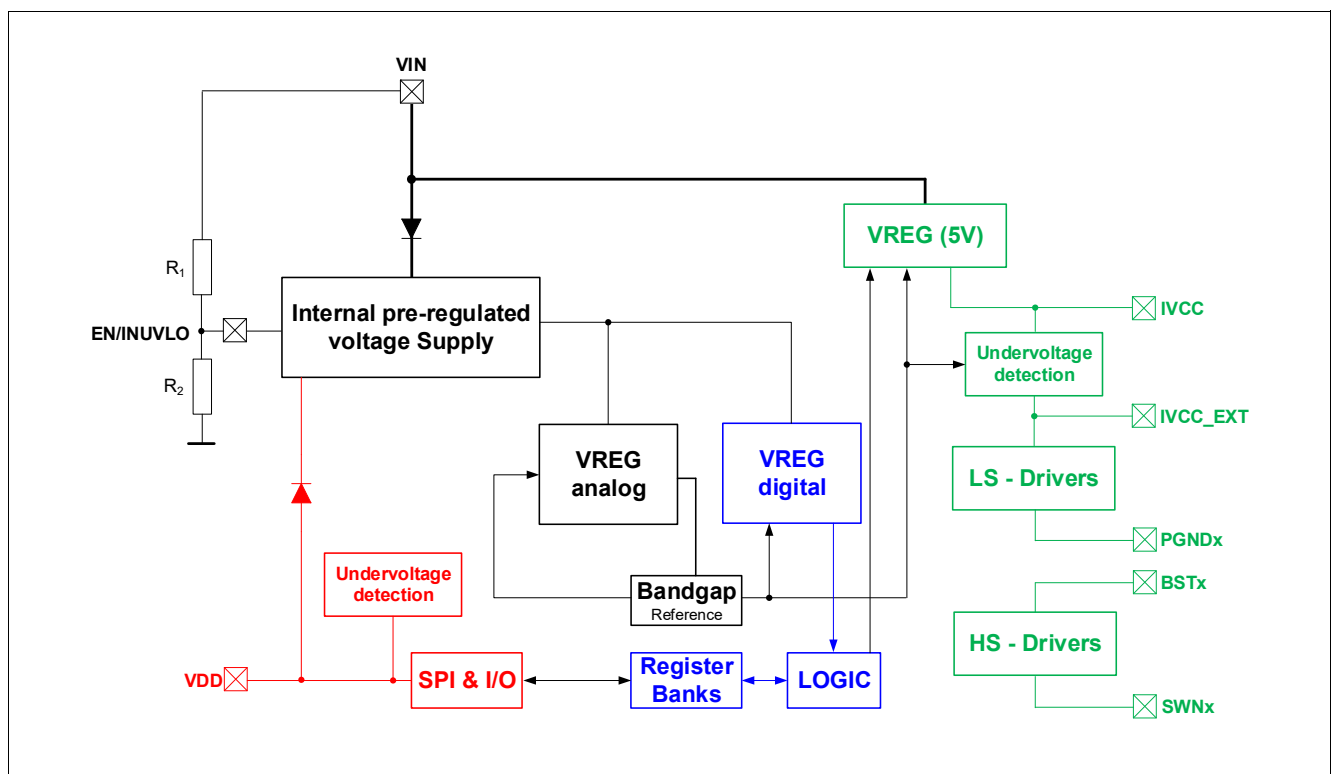
The supply pins VIN, VDD and IVCC\_EXT have undervoltage detections.

Undervoltage on VDD prevents the activation of the gate driver stages and any SPI communication (the SPI registers are reset). Undervoltage on IVCC\_EXT or IVCC pins forces a deactivation of the driver stages, thus stopping the switching activity, but has no effect on the SPI register settings.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND (refer to [Chapter 10.3](#)).

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator, stop switching, stop communications and reset all the registers.

**Figure 4** shows a basic concept drawing of the supply domains and interactions among pins VIN, VDD and IVCC/IVCC\_EXT.

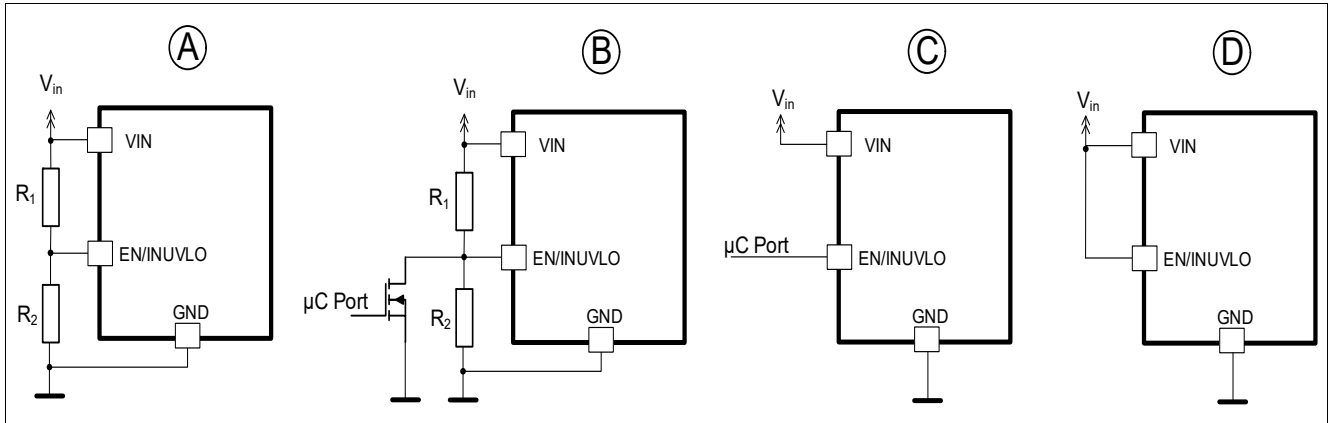


**Figure 4 Power Supply Concept Drawing**

## Power Supply

### Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold is fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a  $\mu\text{C}$ -port as shown in (B) (C).



**Figure 5** Usage of EN/INUVLO pin in different applications

## Power Supply

### 5.1 Different Power States

TLD5542-1 has the following power states:

- SLEEP state
- IDLE state
- LIMP HOME state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC\_EXT level
- VDD level
- LHI level
- DVCTRL.IDLE bit state

The state diagram including the possible transitions is shown in [Figure 6](#).

The Power-up condition is entered when the supply voltage  $V_{VIN}$  exceed its minimum supply voltage threshold  $V_{VIN(ON)}$ .

#### SLEEP

When the device is powered it enters the SLEEP state, all outputs are OFF and the SPI registers are reset, independently from the supply voltages at the pins VIN , VDD, IVCC, and IVCC\_EXT. The current consumption is low. Refer to parameters:  $I_{VDD(SLEEP)}$  and  $I_{VIN(SLEEP)}$ .

The transition from SLEEP to ACTIVE state requires a specified time:  $t_{ACTIVE}$ .

#### IDLE

In IDLE state, the current consumption of the device can reach the limits given by parameter  $I_{VDD}$  (P\_5.3.4). The internal voltage regulator and IVCC linear regulator are working. Not all diagnosis functions are available (refer to [Chapter 10](#) for additional informations). In this state there is no switching activity, independently from the supply voltages  $V_{IN}$ ,  $V_{DD}$ , IVCC and IVCC\_EXT. When  $V_{DD}$  is available, the SPI registers are working and SPI communication is possible.

#### Limp Home

The Limp Home state is beneficial to fulfill system safety requirements and provides the possibility to maintain a defined current/voltage level on the output via a backup control circuitry. The backup control circuitry turns on required loads during a malfunction of the  $\mu C$ . For detailed info, refer to [Chapter 8](#).

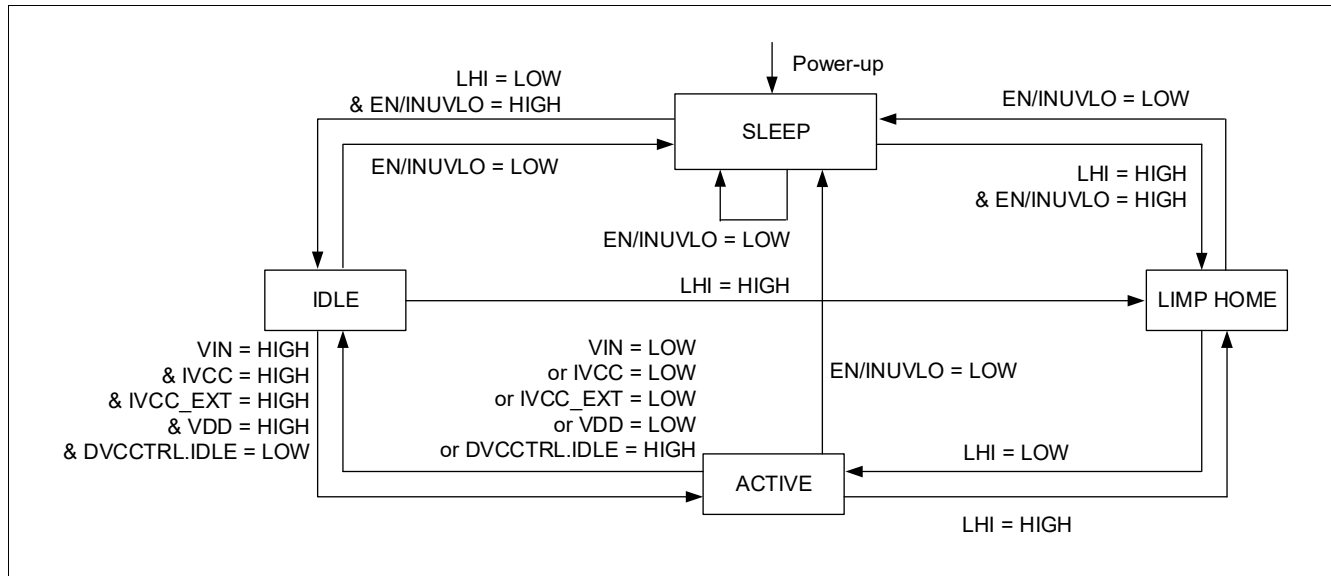
When Limp Home state is entered, SPI registers are reset to their default values and SPI communication is possible but only in read mode (SPI registers can be read but cannot be written). In order to regulate the output current/voltage, it is necessary that  $V_{IN}$  and IVCC\_EXT are present and above their undervoltage threshold.

#### ACTIVE

In active state the device will start switching activity to provide power at the output only when PWM1 = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level  $V_{BST1,2} - V_{SWN1,2}$  needs to be above the threshold

## Power Supply

$V_{BST1,2} - V_{SWN1,2\_UVth}$ . In ACTIVE state the device current consumption via  $V_{IN}$  and  $V_{DD}$  is dependent on the external MOSFET used and the switching frequency  $f_{SW}$ .



**Figure 6 Simplified State Diagram**

## 5.2 Different Possibilities to RESET the device

There are several reset triggers implemented in the device.

After any kind of reset, the Transmission Error Flag (TER) is set to HIGH.

### Under Voltage Reset:

**EN/INUVLO:** When EN/INUVLO is below  $V_{EN/INUVLOth}$  (P\_5.3.7), the SPI interface is not working and all the registers are reset to their default values. In addition, the device enters SLEEP mode and the current consumption is minimized.

**VDD:** When  $V_{VDD}$  is below  $V_{VDD(UV)}$  (P\_5.3.6), the SPI interface is not working and all the registers are reset to their default values.

### Reset via SPI command:

There is a command (DVCCTRL.SWRST = HIGH) available to RESET all writeable registers with the exception of MUXCTRL, to their default values. Note that the result coming from the Calibration routine, which is readable by the SPI when DVCCTRL.ENCAL = HIGH, is not reset by the SWRST.

### Reset via Limp Home:

When Limp Home state is detected the registers are reset to the default values.

**Power Supply**

**5.3 Electrical Characteristics**

**Table 6 EC Power Supply**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply $V_{IN}$							
Input Voltage Startup	$V_{VIN(ON)}$	–	–	4.7	V	$V_{IN}$ increasing; $V_{EN/INUVLO}$ = HIGH; $V_{DD}$ = 5 V; $IVCC$ = $IVCC\_EXT$ = 10 mA;	P_5.3.1
Input Undervoltage switch OFF	$V_{VIN(OFF)}$	–	–	4.5	V	$V_{IN}$ decreasing; $V_{EN/INUVLO}$ = HIGH; $V_{DD}$ = 5 V; $IVCC$ = $IVCC\_EXT$ = 10 mA;	P_5.3.14
Device operating current	$I_{VIN(ACTIVE)}$	–	5	7	mA	<sup>1)</sup> ACTIVE mode; $V_{PWMI}$ = 0 V; $V_{VFB\_VIN}$ = $1/(51+1)*V_{VIN}$ ; $V_{VFB}$ =0.7V	P_5.3.2
$V_{IN}$ Sleep mode supply current	$I_{VIN(SLEEP)}$	–	–	1.5	μA	$V_{EN/INUVLO}$ = 0 V; $V_{CSN}$ = $V_{DD}$ = 5 V; $V_{IN}$ = 13.5 V; $V_{IVCC}$ = $V_{IVCC\_EXT}$ = 0 V;	P_5.3.3
Digital Power Supply $V_{DD}$							
Digital supply current	$I_{VDD}$	–	–	0.5	mA	$V_{IN}$ = 13.5 V; $f_{SCLK}$ = 0 Hz; $V_{PWMI}$ = 0 V; $V_{EN}$ = $V_{CSN}$ = $V_{DD}$ = 5 V;	P_5.3.4
Digital Supply Sleep mode current	$I_{VDD(SLEEP)}$	–	–	1.5	μA	$V_{EN/INUVLO}$ = 0 V; $V_{CSN}$ = $V_{DD}$ = 5 V; $V_{IN}$ = 13.5 V; $V_{IVCC}$ = $V_{IVCC\_EXT}$ = 0 V;	P_5.3.5
Undervoltage shutdown threshold voltage	$V_{VDD(UV)}$	1	–	3	V	$V_{CSN}$ = $V_{DD}$ ; $V_{SI}$ = $V_{SCLK}$ = 0 V; SO from LOW to HIGH impedance;	P_5.3.6
EN/INUVLO Pin characteristics							
Input Undervoltage falling Threshold	$V_{EN/INUVLOth}$	1.6	1.75	1.9	V	–	P_5.3.7



**Power Supply**

**Table 6 EC Power Supply (cont'd)**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN/INUVLO Rising Hysteresis	$V_{EN/INUVLO(hyst)}$	–	90	–	mV	<sup>1)</sup>	P_5.3.8
EN/INUVLO input Current LOW	$I_{EN/INUVLO(LOW)}$	0.45	0.89	1.34	$\mu\text{A}$	$V_{EN/INUVLO} = 0.8\text{ V};$	P_5.3.9
EN/INUVLO input Current HIGH	$I_{EN/INUVLO(HIGH)}$	1.1	2.2	3.3	$\mu\text{A}$	$V_{EN/INUVLO} = 2\text{ V};$	P_5.3.10

**LHI Pin characteristics**

LOW level	$V_{LHI(L)}$	0	–	0.8	V	–	P_5.3.16
HIGH level	$V_{LHI(H)}$	2.0	–	5.5	V	–	P_5.3.17
L-Input pull-down current	$I_{LHI(L)}$	6	12	18	$\mu\text{A}$	$V_{LHI} = 0.8\text{ V};$	P_5.3.18
H-Input pull-down current	$I_{LHI(H)}$	15	30	45	$\mu\text{A}$	$V_{LHI} = 2.0\text{ V};$	P_5.3.19

**Timings**

SLEEP mode to ACTIVE time	$t_{ACTIVE}$	–	–	0.7	ms	<sup>1)</sup> $V_{IVCC} = V_{IVCC\_EXT};$ $C_{IVCC} = 10\text{ }\mu\text{F};$ $V_{IN} = 13.5\text{ V};$ $V_{DD} = 5\text{ V};$	P_5.3.11
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1) Not subject to production test, specified by design.

## Regulator Description

### 6 Regulator Description

The TLD5542-1 includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to [Chapter 6.6](#)).

It is designed to control 4 gate driver outputs in a H-Bridge topology by using only one inductor and 4 external MOSFETs. This topology is able to operate in high power Boost, Buck-Boost and Buck mode applications with maximum efficiency.

The transition between the different regulation modes is done automatically by the device itself, with respect to the application boundary conditions.

The Buck-Boost to Boost transition can be smoothed by mean of BB\_BST\_CMP bitfield.

A SPI flag provides mode feedback to the  $\mu\text{C}$  (refer to SPI bits REGUSETMON . REGUMODFB).

#### 6.1 Regulator Diagram Description

The analog current control loop (A5, A6 with compressive gain =  $IFBx_{gm}$ ) connected to the sensing pins FBL, FBH regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network ( $R_{COMP}$ ,  $C_{COMP}$ ) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the  $R_{SWCS}$  resistor.

$R_{SWCS}$  is used also to limit the maximum external switches / inductor current.

If the Voltage across  $R_{SWCS}$  exceeds its overcurrent threshold ( $V_{SWCS\_buck}$  or  $V_{SWCS\_boost}$  for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

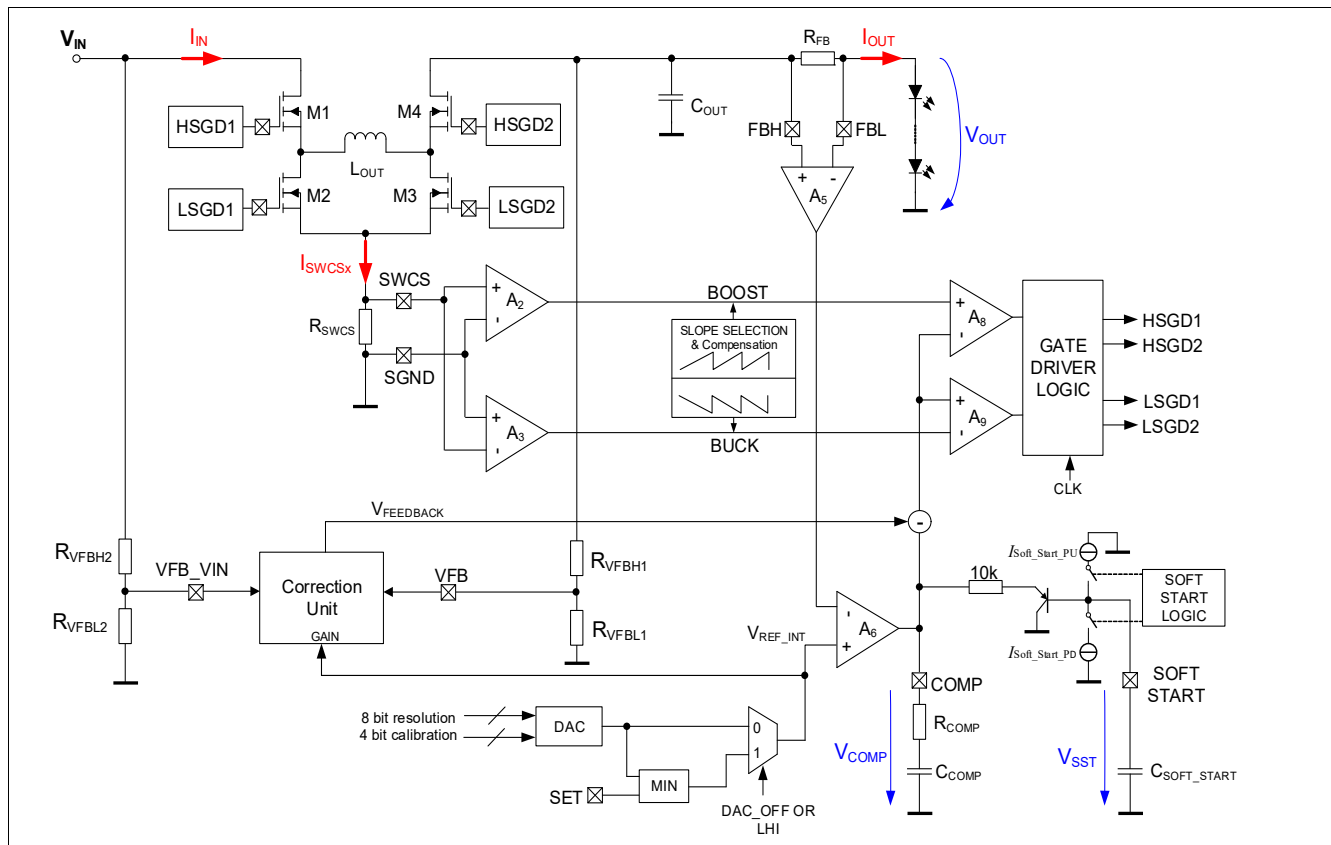
The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC) provides a PWM signal to four internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in an H-Bridge setup . Once the soft start expires a forced CCM regulation mode is performed.

The control loop block diagram displayed in [Figure 7](#) shows a typical constant current application. The voltage across  $R_{FB}$  sets the output current.

The output current is adjusted via the SPI register LEDCURRADIM.ADIMVAL plus an offset trimming on LEDCURRCAL . CALIBVAL register. Refer to [Chapter 8.1](#) for more details.

## Regulator Description



**Figure 7 Regulator Block Diagram - TLD5542-1**

An Infineon proprietary correction unit (see [Figure 7](#)) ensures optimum performance on MFS architecture, minimizing dependency of comp voltage by the analog dimming value, and reduces overshoots during load jump up.

The correction unit provides an input voltage feedback to the regulator loop, proportional to  $V_{out}/V_{in}$  through the VFB/VFB\_VIN signals. Therefore, the 2 voltage dividers at VFB and VIN\_VFB are related to each other, and their ratio is setting the feedback amount. Correction unit feedback can be disabled by setting SWTMOD.VFB\_VIN\_OFF bitfield.

The negative feedback applied to  $V_{COMP}$  is also proportional to the analog dimming value. The smaller the analog dimming value, the larger is the feedback voltage:

$$V_{FEEDBACK} \approx 0.05 \cdot \frac{V_{VFB}}{V_{VFB_{VIN}}} \cdot (100\% - ADIM[\%]) \quad [V] \quad (6.1)$$

In order to ensure good accuracy on VFB\_VIN reading, the total resistance on the divider should be less than 100kΩ. It is recommended to have VFB\_VIN / VFB voltage dividers ratio equal to 1 / 1.5 (I.E. RVFBH2=RVFBH1=51kΩ, RVFBL2=1kΩ, RVFBL1=1.5kΩ).

If the input voltage feedback is too high (I.E. RVFBL2 is too low),  $V_{COMP}$  may saturate toward the operating range limit ( 2V ) and the output current regulation would be affected. Minimum temperature, maximum  $V_{out}/V_{in}$  ratio and minimum ADIM value shall be considered as worst case condition when checking for  $V_{COMP}$  dynamic operating range.

## Regulator Description

### 6.2 Adjustable Soft Start Ramp

The soft start routine has 2 functionalities:

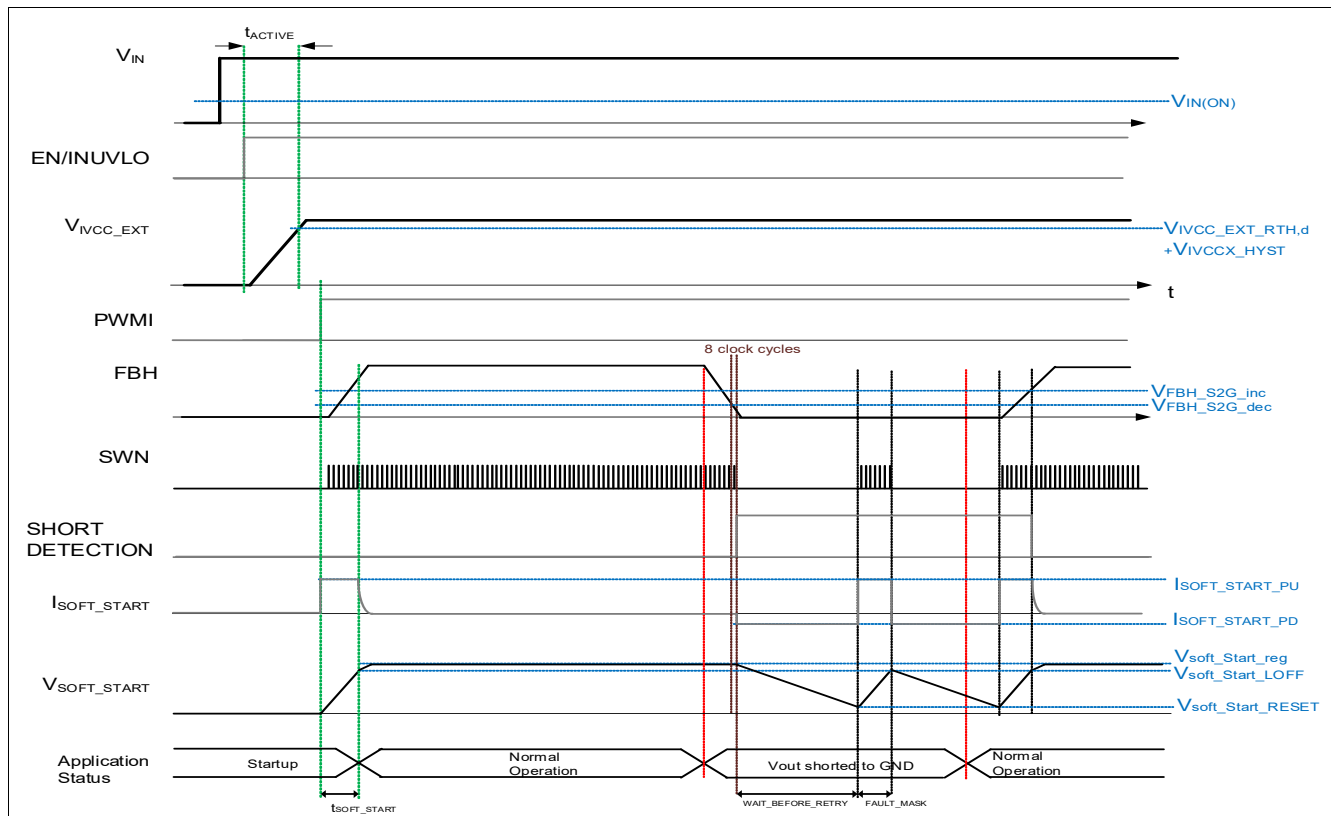
- Fault management: fault mask and wait-before-retry time (**Figure 8** and chapter **Chapter 10.2**)
- Limit input inrush current and output overshoots by limiting Vcomp (**Figure 7**) in boost mode

The soft start routine is applied in two cases:

- At startup (first PWM rise after IDLE to ACTIVE transition)
- After output short to GND detection

The soft start routine is active during the rising and falling edges of the VSST. The soft start timing is defined by a capacitor placed at the SOFT\_START pin and the pull-up and pull down current sources ( $I_{\text{Soft\_Start\_PU}}$ ,  $I_{\text{Soft\_Start\_PD}}$ ).

Minimum value for soft start capacitor has to be designed such that, at startup, the output voltage exceeds the short to ground threshold ( $V_{\text{FBH\_S2G\_inc}}$ ), before the soft start voltage reaches  $V_{\text{SOFT\_START\_LOFF}}$ . Minimum temperature and minimum input voltage shall be considered as worst case condition for previously mentioned dimensioning.



**Figure 8** Soft Start timing diagram on a short to ground detected by the FBH pin

Soft Start rising edge time is approximately:

$$t_{\text{SOFT\_START}} = V_{\text{Soft\_Start\_LOFF}} \cdot \frac{C_{\text{Soft\_Start}}}{I_{\text{Soft\_Start\_PU}}} \quad (6.2)$$

The Soft Start routine limits the inrush current during boost mode by clamping the COMP pin through a buffer as in **Figure 7**. Therefore this functionality is effective only when Soft Start capacitor is sufficiently larger than the comp capacitor.

## Regulator Description

If the inductor current is low during the soft start rising edge, DCM is enabled and MOSFET M4 is disabled. If the inductor current increases then M4 may get enabled.

After the soft start has been completed ( $V_{\text{SOFT\_START}} > V_{\text{SOFT\_START\_LOFF}}$ ) CCM is forced and M4 is permanently enabled, independently from the inductor current level.

To avoid overshoot at startup on voltage regulators, may be useful to keep CCM forced also during soft start by setting CCM\_4EVER bitfield.

If a short circuit on the output is detected, a pull-down current source  $I_{\text{SOFT\_START\_PD}}$  (P\_6.4.20) is activated. This current brings down the  $V_{\text{SOFT\_START}}$  until  $V_{\text{SOFT\_START\_RESET}}$  (P\_6.4.22) is reached. Afterwards the pull-up current source  $I_{\text{SOFT\_START\_PU}}$  (P\_6.4.19) turns on again. If the fault condition hasn't been removed until  $V_{\text{SOFT\_START\_LOFF}}$  (P\_6.4.21) is reached, the pull-down current source turns back on again, initiating a new cycle. This will continue until the fault is removed.

If a low duty cycle PWM is applied at startup, the output voltage may be still below the short to ground threshold once the soft start fault mask is expired. Therefore the TLD5542-1 has a special feature in order to prevent short to ground in case of startup with low duty cycle PWM.

At first PWM rise after IDLE to ACTIVE transition, the internal PWM signal is extended if the following conditions are met:

- A capacitor is connected to the IOUTMON pin (suggested 220pF)
- IDLE mode is kept for less than 10ms
- PWM rise is provided within 10ms from IDLE to ACTIVE transition

The PWM extension last until one of the two following conditions is reached:

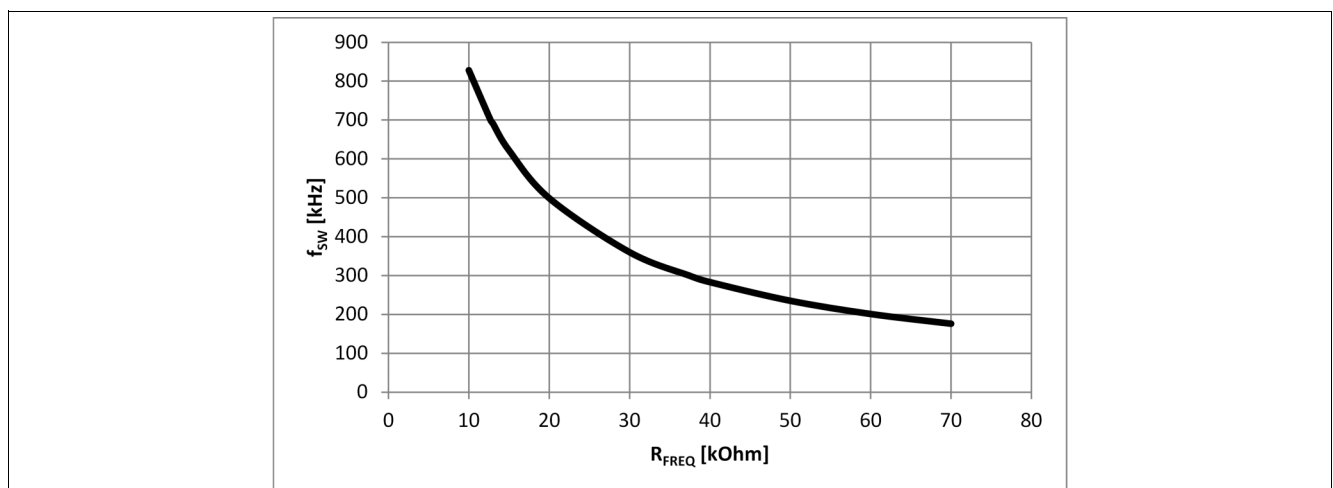
- Until  $V_{\text{SOFT\_START}}$  exceeds  $V_{\text{SOFT\_START\_LOFF}}$
- Until  $V_{\text{FBH\_FBL}}$  exceeds  $V_{\text{FBH\_FBL\_IN}}$

## 6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter [Chapter 11.2](#). Select the switching frequency with an external resistor according to the graph in [Figure 9](#) or the following approximate formulas.

$$f_{\text{SW}}[\text{kHz}] = 5375 * (R_{\text{FREQ}}[\text{k}\Omega])^{-0.8} \quad (6.3)$$

$$R_{\text{FREQ}}[\text{k}\Omega] = 46023 * (f_{\text{SW}}[\text{kHz}])^{-1.25} \quad (6.4)$$



**Figure 9** Switching Frequency  $f_{\text{SW}}$  versus Frequency Select Resistor to GND  $R_{\text{FREQ}}$

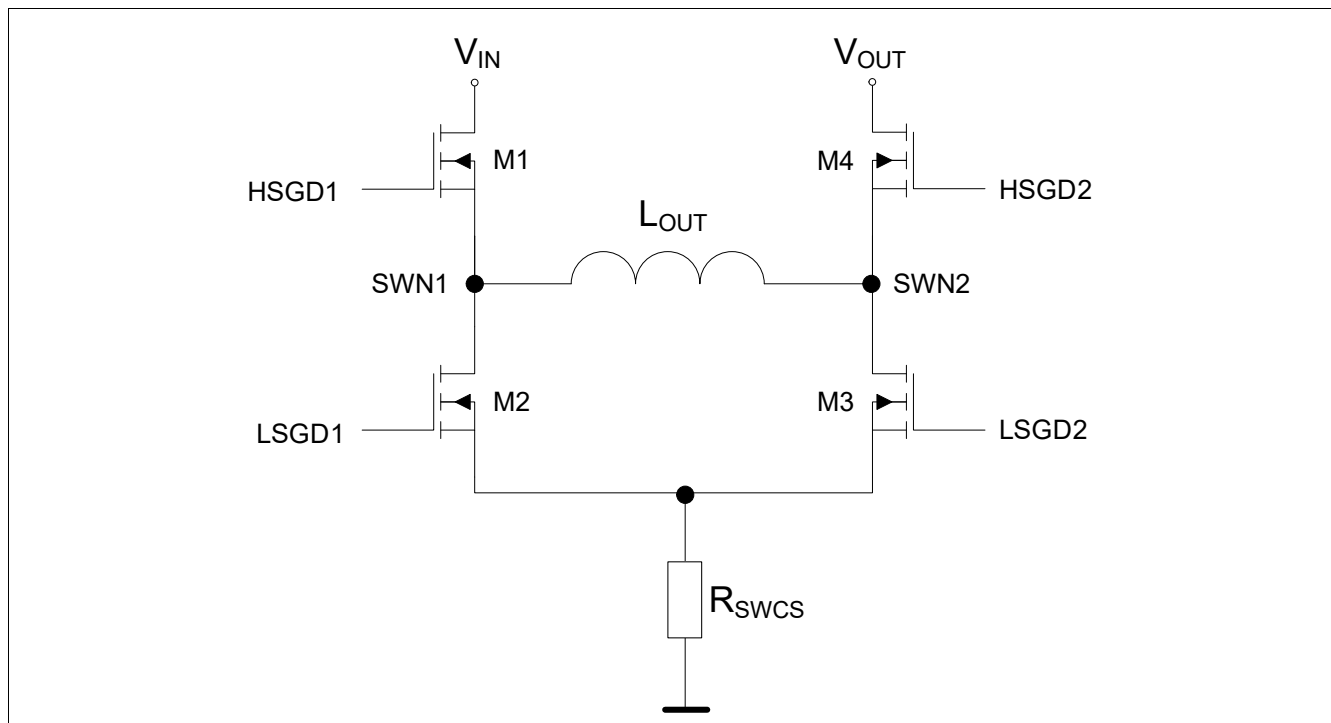
## Regulator Description

### 6.4 Operation of 4 switches H-Bridge architecture

Inductor  $L_{OUT}$  connects in an H-Bridge configuration with 4 external N channel MOSFETs (M1, M2, M3 & M4)

	BOOST MODE	BUCK-BOOST MODE	BUCK MODE
M1	ON	PWM	PWM
M2	OFF	PWM	PWM
M3	PWM	PWM	OFF
M4	PWM	PWM	ON

**Figure 10 4 switches H-Bridge architecture Transistor Status summary**



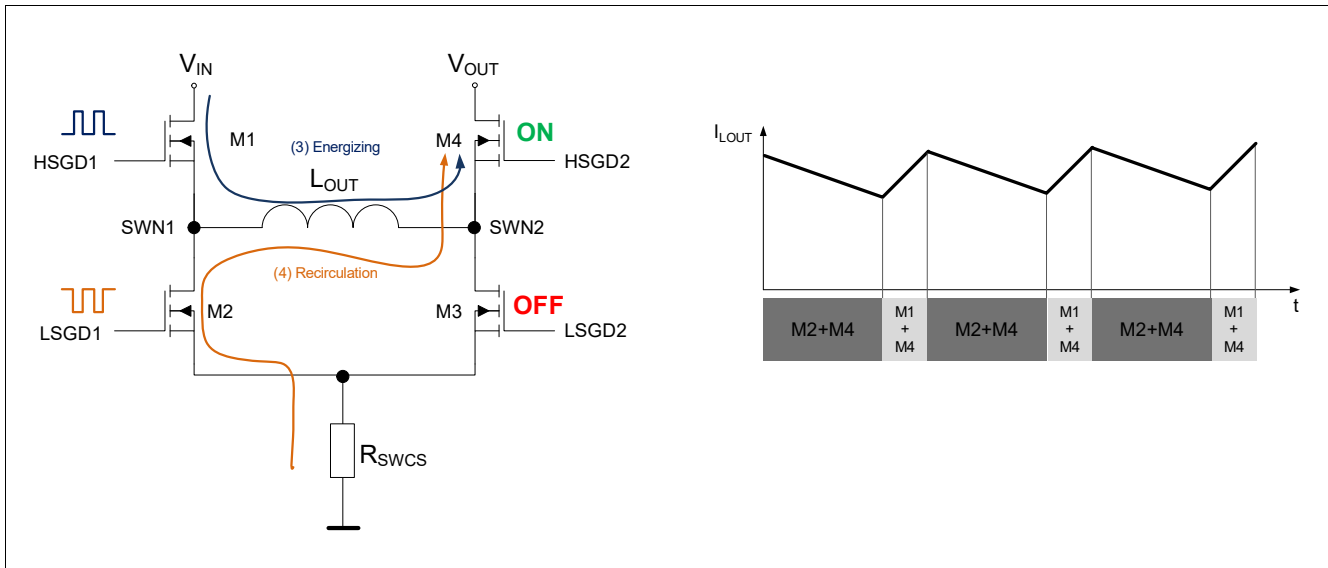
**Figure 11 4 switches H-Bridge architecture overview**

#### 6.4.1 Boost mode ( $V_{IN} < V_{OUT}$ )

- M1 is always ON, M2 is always OFF
- Every cycle M3 turns ON first and inductor current is sensed (peak current control)
- M3 stays ON until the upper reference threshold is reached across  $R_{SWCS}$  (Energizing)
- M3 turns OFF, M4 turns ON until the end of the cycle (Recirculation)
- Switches M3 and M4 alternate, behaving like a typical synchronous boost Regulator (see [Figure 12](#))



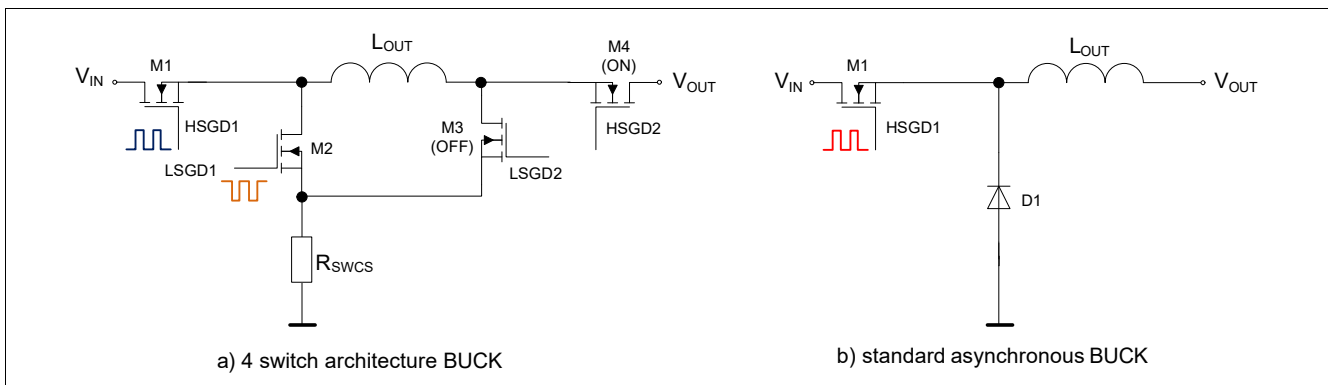
## Regulator Description



**Figure 14 4 switches H-Bridge architecture in BUCK mode**

### Simplified comparison of 4 switches architecture to traditional asynchronous Buck approach.

- M3 is always OFF in this mode (open).
- M4 is always ON in this mode (closed connection inductor to  $V_{OUT}$ ).
- M2 acts as a synchronous diode, with significantly lower conduction losses ( $I^2 \times R_{DS(on)}$  vs.  $0.7\text{ V} \times I$ )



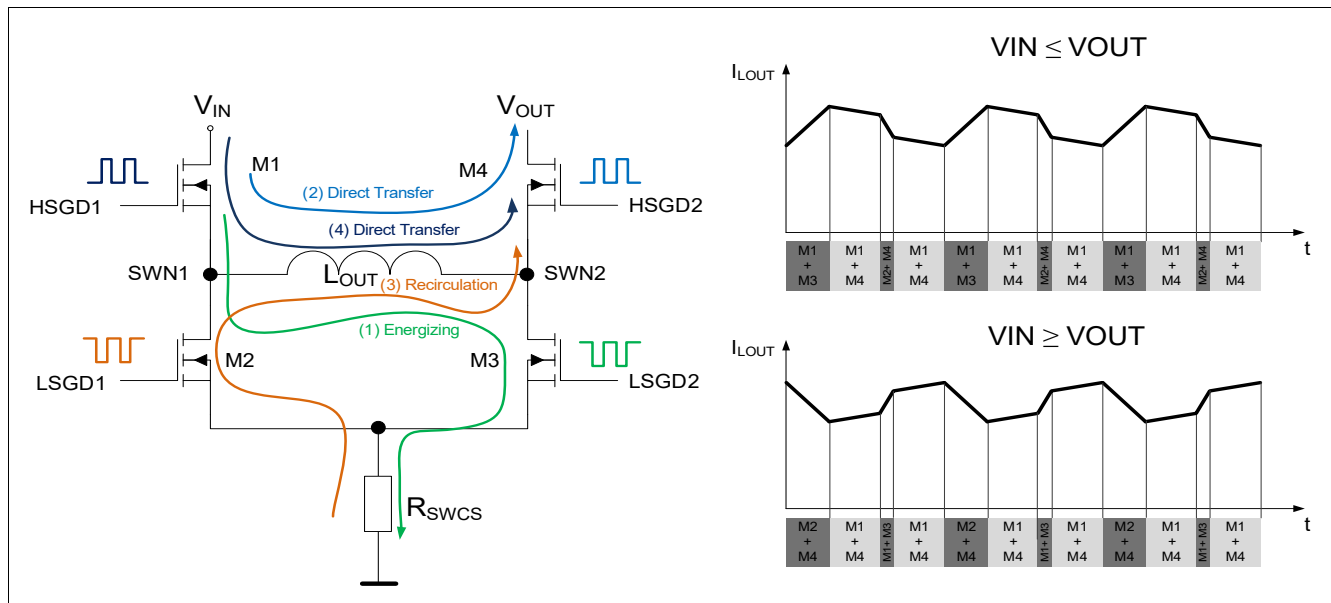
**Figure 15 4 switches H-Bridge architecture in BUCK mode compared to standard async BUCK**

### 6.4.3 Buck-Boost mode ( $V_{IN} \sim V_{OUT}$ )

- When  $V_{IN}$  is close to  $V_{OUT}$  the controller is in Buck-Boost operation
- All switches are switching in buck-boost operation. The direct energy transfer from the Input to the output ( $M1+M4 = ON$ ) is beneficial to reduce ripple current and improves the energy efficiency of the Buck-Boost control scheme
- The two buck boost waveforms and switching behaviors are displayed in [Figure 16](#) below



## Regulator Description



**Figure 16 4 switches H-Bridge architecture in BUCK-BOOST mode**

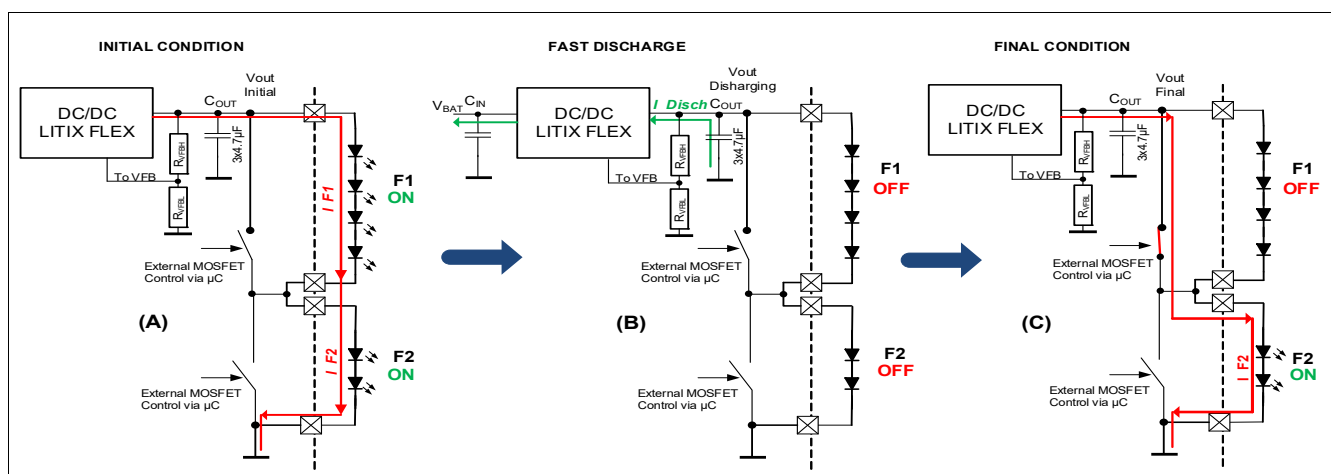
## 6.5 Fast Output Discharge Operation Mode - Multi Floating Switches Topology

Multiple light functions can be driven by a single DC/DC converter adopting a Multi Floating Switch (MFS) topology. In a MFS topology, each LED Function is connected in series and can be independently turned off via a bypass switch. Because of the series connections, all the functions are driven with the same current (except for Loads with complementary duty cycle I.E. DRL, LB ). Different brightness can be achieved with individual PWM duty cycles.

In order to drive different LED functions in this topology, a Buck Boost converter is probably needed. A single stage buck boost topology has high efficiency but requires several  $\mu\text{F}$  of output capacitance ( $C_{\text{OUT}}$ ). The extra voltage present on this capacitor, when shorting one function to turn it off, may create a current spike in the LEDs that have to remain on.

The TLD5542-1 has a dedicated state machine which controls a fast discharge of the output cap to a desired fraction of the initial output voltage. This Fast Output Discharge feature (F.D.), if carefully configured, limits the current spike during load jump events preventing LED damage.

An Example of the Multi Floating Switch topology architecture and operation are shown in [Figure 17](#)



**Figure 17 Multi Floating Switch topology: operation sequence on 2 Functions: (F1+F2) to (F2)**

## Regulator Description

The F.D. operation consists of discharging the capacitor  $C_{OUT}$  to the final load voltage (**Figure 17-B**) before the bypass switch closure. The external Microcontroller Software has to take care of the synchronization between the TLD5542-1 F.D. operation and the bypass Switches activation.

The discharged energy from  $C_{OUT}$  is recovered back to the Input capacitor  $C_{IN}$  which could cause a small overshoot on the  $C_{IN}$  itself. This feature allows high efficiency designs also when PWM operation with repetitive Load Jumps is needed.

The F.D. feature is needed when a negative  $V_{OUT}$  step is performed, so when one or more LED functions are switched off. If additional LED functions are turned on, increasing the output voltage, the F.D. does not have to be used.

In case analog dimming is performed during a load Jump (I.E. from 1A LB to 300mA DRL), even with a positive  $V_{OUT}$  step, a discharge of the COMP capacitor could be necessary.

In MFS topologies, a short interruption of the current is observed during the Load Transitions (either positive or negative) in all the functions, until  $V_{OUT}$  is stable and the device control loop is able to provide the target output current.

We will refer to any Voltage-Current or Load configuration just before the Load Jump as "Initial" (**Figure 17-A**), while we will refer to any value after the system is in the new Load configuration as "Final" (**Figure 17-C**).

### Set the Target $C_{OUT}$ discharge voltage

The Target output voltage ( $V_{OUTFinal}$ ) of an F.D. operation is communicated to the TLD5542-1 as a fraction of the  $V_{OUT}$  at the beginning of the Jump ( $V_{OUTInitial}$ ), and not as an absolute Value.

In order to F.D. the output Capacitor to a desired Ratio of the initial voltage, two SPI commands have to be sent to the TLD5542-1 register MFSSETUP1.

- The first is to write in the MFSSETUP1.LEDCHAIN the Ratio Denominator
- The second is to write in the MFSSETUP1 register the Ratio Numerator and the Start Of Multi Floating Switch, respectively in the LEDCHAIN and SOMFS bitfields

The time interval between the Ratio Denominator and Numerator SPI commands, needs to be long enough to sample the Initial Voltage of the F.D. in the FILT capacitor.

After the second command, as soon as the Chip select is raised the F.D. begins. The final output voltage of the F.D. operation, after a MFS routine is correctly performed, will be approximately:

$$V_{OUTFinal} = \frac{RatioNumerator}{RatioDenominator} \cdot V_{OUTInitial} \quad (6.5)$$

If RatioNumerator is bigger than RatioDenominator, the output voltage remains constant, but the COMP capacitor is discharged during all the TPREP

F.D. operation will exit if the output voltage reaches  $V_{FBH\_S2G\_dec}$ .

Example:

In order to jump from 6LED (18 V) to 2LEDs (6 V), the Ratio is 1/3 of initial voltage.

So the 2 SPI commands that have to be sent are:

Spi command 1: set MFSSETUP1 to 0x06 (Ratio Denominator = 6)

Spi command 2: set MFSSETUP1 to 0x22 (Ratio Numerator+SOMFS = 0x02+0x20)

### Preparation Time $t_{prep}$ :

The TLD5542-1 enables the user to set a period  $t_{prep}$  on the load jump, where  $C_{COMP}$  is discharged continuously with a constant current (IEA\_neg).

## Regulator Description

The Preparation Time has to be sufficient for the capacitor  $C_{COMP}$  to be discharged the desired value.

(6.6)

$$t_{DiscComp} = Dvcomp \frac{C_{COMP}}{I_{EA\_neg}} = t_{prep}$$

In order to set a preparation time on the TLD5542-1, a SPI command has to be sent to the register MFSSETUP2.MFSDLY).

The **Equation (6.7)** below describes the relationship between the switching frequency  $f_{SW}$  and the MFSSETUP2.MFSDLY register value.

$$t_{prep} = \frac{1}{f_{SW}} \cdot [2 + (MFSDLY)_{dec}] \quad (6.7)$$

For SPI command details refer to **Chapter 12.6**.

The F.D. procedure is automatically extended until Cout capacitor is discharged to the target value, and Tprep is expired. If there is the need to do not discharge the CCOMP, but Discharge only the Vout, is possible to set MFSSETUP2.MFSDLY to 0 on a F.D. routine, Cout will be anyway discharged to the target voltage.

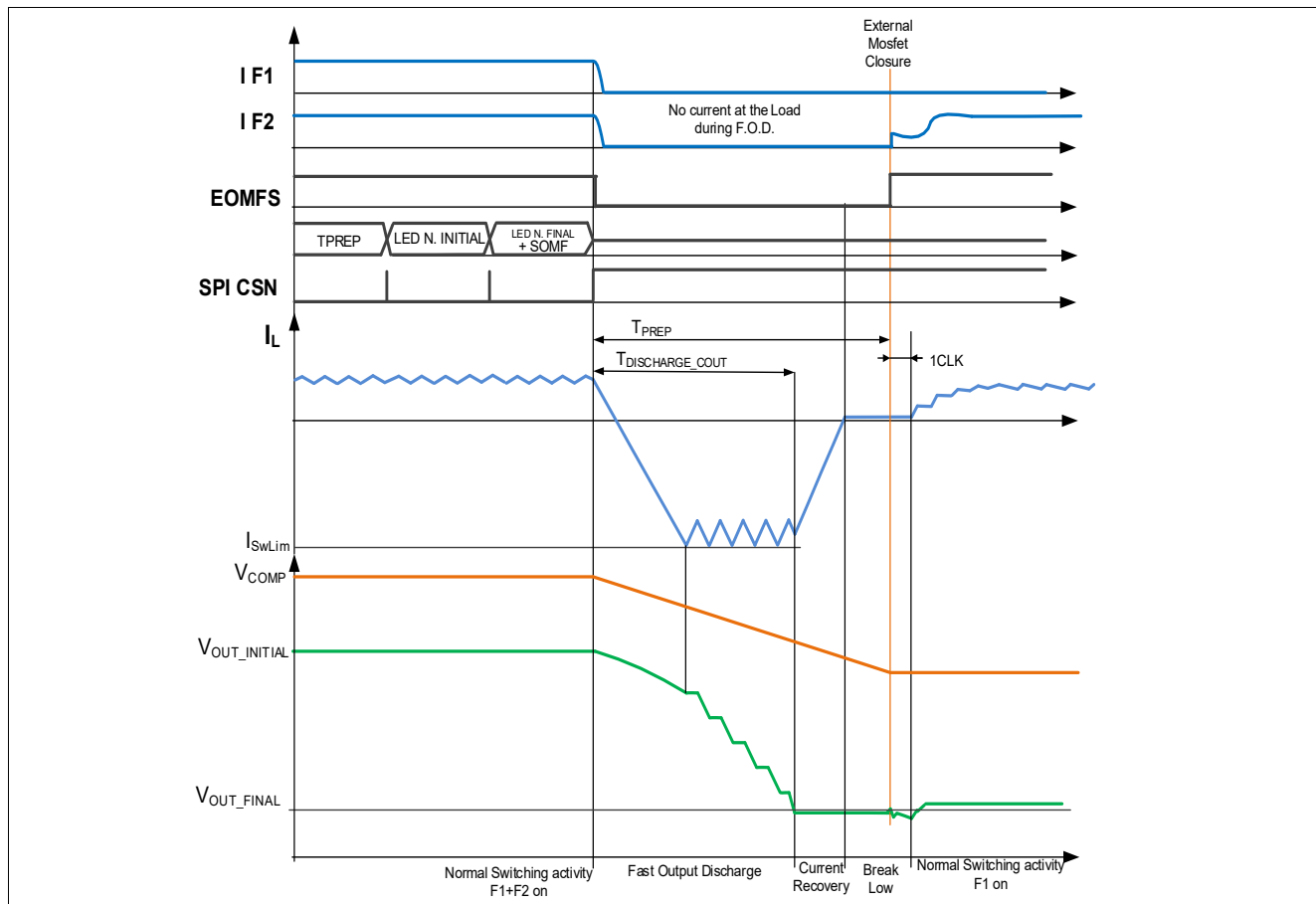
### Fast Discharge Phase

After programming the desired output voltage Ratio via SPI, the right Preparation Time and activating the state machine (MFSSETUP1.SOMFS = HIGH) the TLD5542-1 inverts the inductor current  $I_L$  and keeps its negative peak at a reduced switch current limit  $I_{SwLim}$  until the  $V_{OUT}$  reaches the desired target.

$$I_{SwLim} \approx \frac{V_{SWCS\_boost}}{R_{SWCS}} \cdot \frac{2}{3} \quad (6.8)$$

**Figure 18** displays the relation of inductor current  $I_L$  and the output voltage  $V_{OUT}$  during a fast output discharge operation mode.

## Regulator Description



**Figure 18 Fast Output Discharge timing diagram**

If the discharge current limit  $I_{SwLim}$  needs to be reduced further, the `MFSSETUP1 . ILIM_HALF_MFS` bit can be used to reduce it to the [Equation \(6.9\)](#) (only during the F.D. phase and not in normal operation), see SPI Chapter for further details [Chapter 12.6](#).

$$I_{SwLim} \approx \frac{V_{SWCS\_boost}}{R_{SWCS}} \cdot \frac{1}{2} \quad (6.9)$$

Setting the `EA_IOUT_MFS` bit will reduce (only during the F.D. phase) the saturation current of the error amplifier A6 (IEA\_neg) that discharges the Comp capacitor.

Once  $V_{OUT}$  reaches the desired target, the current recovery phase brings  $I_L$  from a negative value back to 0 A and the device stays in “Brake-Low condition” (both Lowside gatedrivers = ON) until the programmed preparation time (`MFSSETUP2 . MFSDLY`) expires.

Only when both the current recovery phase has ended and  $t_{prep}$  is expired an SPI flag( STD bit EOMFS) and the pin EOMFS are set to HIGH. One clock cycle after EOMFS is asserted, the TLD5542-1 starts automatically switching again.

**Figure 18** displays one Fast Output Discharge cycle.

### Sequence of operations to perform a Fast Output Discharge

In order to perform a F.D .operation, the user has to :

- Send via SPI to `MFSSETUP1 . LEDCHAIN` the Ratio Denominator.
- Set via SPI an adequate Preparation Time
- Send via SPI to `MFSSETUP1 . LEDCHAIN` the Ration Numerator + SOMFS

### **Regulator Description**

- Wait until preparation time is expired and Vout has reached the target value (EOMFS is asserted)
- Adjust the Floating switches to the new configuration

In case of short to GND the routine is not executed or it is aborted.

At startup (after EN = High), if PWM has never been set to HIGH, F.D. routine can not be executed.

If a F.D. is needed just after device enable (for instance to lower the output voltage after a low battery reset), PWMI has to be set to 1 before the SOMFS command, and the F.D. procedure will be executed only once the SS is expired.

Other than for the 2 above exceptions, it is always possible to perform F.D. independently from PWM signal and output overvoltage condition.

## Regulator Description

### 6.6 Programming Output Voltage (Constant Voltage Regulation)

For a voltage regulator, the output voltage can be set by selecting the values  $R_{FB1}$ ,  $R_{FB2}$  according to the following **Equation (6.10)**:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \cdot V_{FBH-FBL} \quad (6.10)$$

Refer to the voltage regulator application drawing on **Figure 45**.

After the output voltage is fixed via the resistor divider, the value can be changed via the Analog Dimming bits ADIMVAL.

## Regulator Description

### 6.7 Electrical Characteristics

**Table 7 EC Regulator**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator:							
$V_{FBH-FBL\_REF}$ reference voltage	$V_{FBH-FBL\_REF}$	145.5	150	154.5	mV	ADIMVAL = 240;	P_6.4.1
$V_{FBH-FBL\_REF}$ reference voltage	$V_{FBH-FBL\_REF}$	12	15	18	mV	ADIMVAL =24; Calibration Procedure not performed	P_6.4.5
FBH Bias current @ highside sensing setup	$I_{FBH\_HSS}$	65	110	155	μA	<sup>1)</sup> $V_{FBL} = 7\text{ V}$ ; $V_{FBH} - FBL = 150\text{ mV}$ ;	P_6.4.8
FBL Bias current @ highside sensing setup	$I_{FBL\_HSS}$	17	30	43	μA	<sup>1)</sup> $V_{FBL} = 7\text{ V}$ ; $V_{FBH} - FBL = 150\text{ mV}$ ;	P_6.4.9
A6 sense Amp +sat current	$I_{EA\_pos}$	25	29	33	μA	<sup>1)</sup> VCOMP = 1V; ADIMVAL = 240; $V_{FBH} - FBL = 0\text{ mV}$	P_6.10.2
A6 sense Amp -sat current	$I_{EA\_neg}$	-63	-56	-49	μA	<sup>1)</sup> VCOMP = 1V; ADIMVAL = 240; $V_{FBH} - FBL = 500\text{ mV}$	P_6.10.3
A5A6 sense Amp $g_m$	$IFBx_{gm}$	–	890	–	μS	<sup>1)</sup> EA_GM=0	P_6.4.10
Output Monitor Voltage	$V_{IOUTMON}$	1.33	1.4	1.47	V	$V_{FBH} - FBL = 150\text{ mV}$ ;	P_6.4.11
Maximum BOOST Duty Cycle	$D_{BOOST\_MAX}$	89	91	93	%	<sup>1)</sup> $f_{sw} = 300\text{ kHz}$ ;	P_6.4.12
Input current Monitor Voltage	$V_{IINMON}$	0.95	1	1.05	V	<sup>1)</sup> $V_{IIN1} - IIN2 = 50\text{ mV}$ ; $V_{IIN1} = V_{VIN(ON)}$ to 55 V;	P_6.4.15
Switch Peak Over Current Threshold - BOOST	$V_{SWCS\_boost}$	70	76	82	mV	<sup>1)</sup>	P_10.8.1 5
Switch Peak Over Current Threshold - BUCK	$V_{SWCS\_buck}$	-60	-50	-40	mV	<sup>1)</sup>	P_10.8.1 6
Soft Start							
Soft Start pull up current	$I_{Soft\_Start\_PU}$	22	26	32	μA	$V_{Soft\_Start} = 1\text{ V}$ ;	P_6.4.19
Soft Start pull down current	$I_{Soft\_Start\_PD}$	2.2	2.6	3.2	μA	$V_{Soft\_Start} = 1\text{ V}$ ;	P_6.4.20
Soft Start Latch-OFF Threshold	$V_{Soft\_Start\_LOFF}$	1.65	1.75	1.85	V	–	P_6.4.21
Soft Start Reset Threshold	$V_{Soft\_Start\_RESET}$	0.1	0.2	0.3	V	–	P_6.4.22

## Regulator Description

**Table 7 EC Regulator (cont'd)**

$V_{IN} = 8\text{ V to } 36\text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Soft Start Voltage during regulation	$V_{\text{Soft\_Start\_reg}}$	1.9	2	2.1	V	<sup>1)</sup> No Faults	P_6.9.3
Output Current init reference Voltage $V_{\text{FBH-FBL}}$	$V_{\text{FBH\_FBL\_IN}}$	11	17.5	24	mV	$V_{\text{FB}} = 1.4\text{ V}$ ;	P_10.8.10
Output Current EA_GM boost reference Voltage $V_{\text{FBH-FBL}}$	$V_{\text{FBH\_FBL\_EA}}$	–	120	–	mV	<sup>1)</sup> $V_{\text{FB}} = 1.4\text{ V}$ ; $\text{ADIMVAL} = 240$ ;	P_6.10.4

## Oscillator

Switching Frequency	$f_{\text{SW}}$	285	300	315	kHz	$T_J = 25^\circ\text{C}$ ; $R_{\text{FREQ}} = 37.4\text{ k}\Omega$ ;	P_6.4.23
SYNC Frequency	$f_{\text{SYNC}}$	200	–	700	kHz	–	P_6.4.24
SYNC Turn On Threshold	$V_{\text{SYNC,ON}}$	2	–	–	V	–	P_6.4.25
SYNC Turn Off Threshold	$V_{\text{SYNC,OFF}}$	–	–	0.8	V	–	P_6.4.26
SYNC High Input Current	$I_{\text{SYNC,H}}$	15	30	45	$\mu\text{A}$	$V_{\text{SYNC}} = 2.0\text{ V}$ ;	P_6.4.62
SYNC Low Input Current	$I_{\text{SYNC,L}}$	6	12	18	$\mu\text{A}$	$V_{\text{SYNC}} = 0.8\text{ V}$ ;	P_6.4.63

## Gate Driver for external Switch

Gate Driver undervoltage threshold $V_{\text{BST1,2}} - V_{\text{SWN1,2\_UVth}}$	$V_{\text{BST1,2}} - V_{\text{SWN1,2\_UVth}}$	3.4	–	4	V	$V_{\text{BST1,2}} - V_{\text{SWN1,2}}$ decreasing;	P_6.4.64
HSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{\text{DS(ON\_PU)HS}}$	1.4	2.3	3.7	$\Omega$	$V_{\text{BST1,2}} - V_{\text{SWN1,2}} = 5\text{ V}$ ; $I_{\text{source}} = 100\text{ mA}$ ;	P_6.4.28
HSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{\text{DS(ON\_PD)HS}}$	0.6	1.2	2.2	$\Omega$	$V_{\text{BST1,2}} - V_{\text{SWN1,2}} = 5\text{ V}$ ; $I_{\text{sink}} = 100\text{ mA}$ ;	P_6.4.29
LSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{\text{DS(ON\_PU)LS}}$	1.4	2.3	3.7	$\Omega$	$V_{\text{IVCC\_EXT}} = 5\text{ V}$ ; $I_{\text{source}} = 100\text{ mA}$ ;	P_6.4.30
LSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{\text{DS(ON\_PD)LS}}$	0.4	1.2	1.8	$\Omega$	$V_{\text{IVCC\_EXT}} = 5\text{ V}$ ; $I_{\text{sink}} = 100\text{ mA}$ ;	P_6.4.31
HSGD1,2 Gate Driver peak sourcing current	$I_{\text{HSGD1,2\_SRC}}$	380	–	–	mA	<sup>1)</sup> $V_{\text{HSGD1,2}} - V_{\text{SWN1,2}} = 1\text{ V to } 4\text{ V}$ ; $V_{\text{BST1,2}} - V_{\text{SWN1,2}} = 5\text{ V}$	P_6.4.32
HSGD1,2 Gate Driver peak sinking current	$I_{\text{HSGD1,2\_SNK}}$	410	–	–	mA	<sup>1)</sup> $V_{\text{HSGD1,2}} - V_{\text{SWN1,2}} = 4\text{ V to } 1\text{ V}$ ; $V_{\text{BST1,2}} - V_{\text{SWN1,2}} = 5\text{ V}$	P_6.4.33



## Regulator Description

**Table 7 EC Regulator** (cont'd)

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^{\circ}\text{C to }+150^{\circ}\text{C}$ , all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LSGD1,2 Gate Driver peak sourcing current	$I_{\text{LSGD1,2\_SRC}}$	370	–	–	mA	<sup>1)</sup> $V_{\text{LSGD1,2}} = 1\text{ V to }4\text{ V};$ $V_{\text{IVCC\_EXT}} = 5\text{ V};$	P_6.4.34
LSGD1,2 Gate Driver peak sinking current	$I_{\text{LSGD1,2\_SNK}}$	550	–	–	mA	<sup>1)</sup> $V_{\text{LSGD1,2}} = 4\text{ V to }1\text{ V};$ $V_{\text{IVCC\_EXT}} = 5\text{ V};$	P_6.4.35
LSGD1,2 OFF to HSGD1,2 ON delay	$t_{\text{LSOFF-HSON\_delay}}$	15	30	40	ns	<sup>1)</sup>	P_6.4.36
HSGD1,2 OFF to LSGD1,2 ON delay	$t_{\text{HSOFF-LSON\_delay}}$	35	60	75	ns	<sup>1)</sup>	P_6.4.37

<sup>1)</sup> Not subject to production test, specified by design

## Digital Dimming Function

### 7 Digital Dimming Function

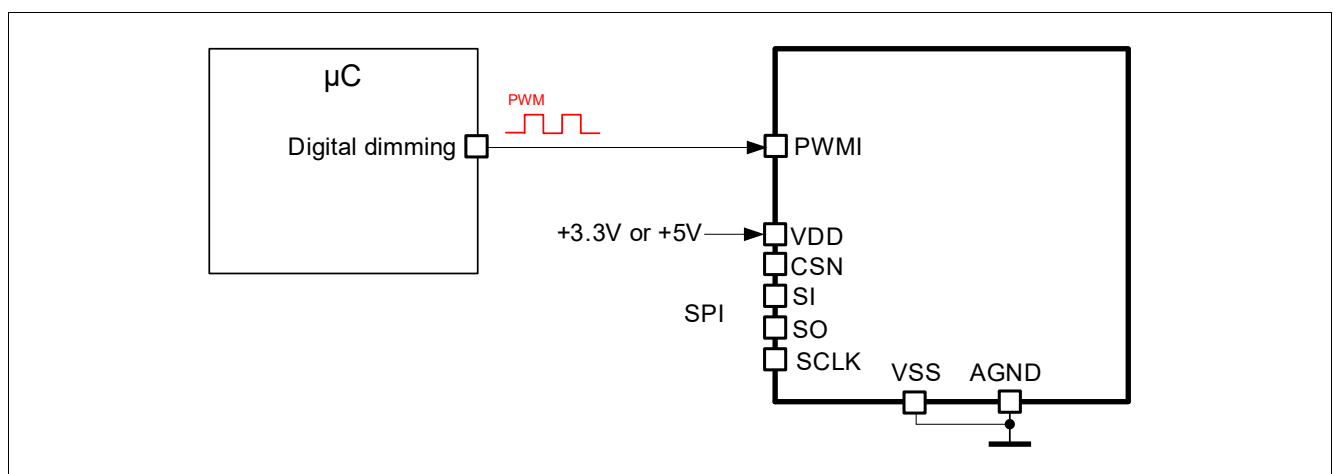
PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

#### 7.1 Description

A PWM signal can be transmitted to the TLD5542-1 as described below.

##### PWM via direct interface

The PWMI pin can be fed with a pulse width modulated (PWM) signals, this enables when HIGH and disables when LOW the gate drivers of the main switches.

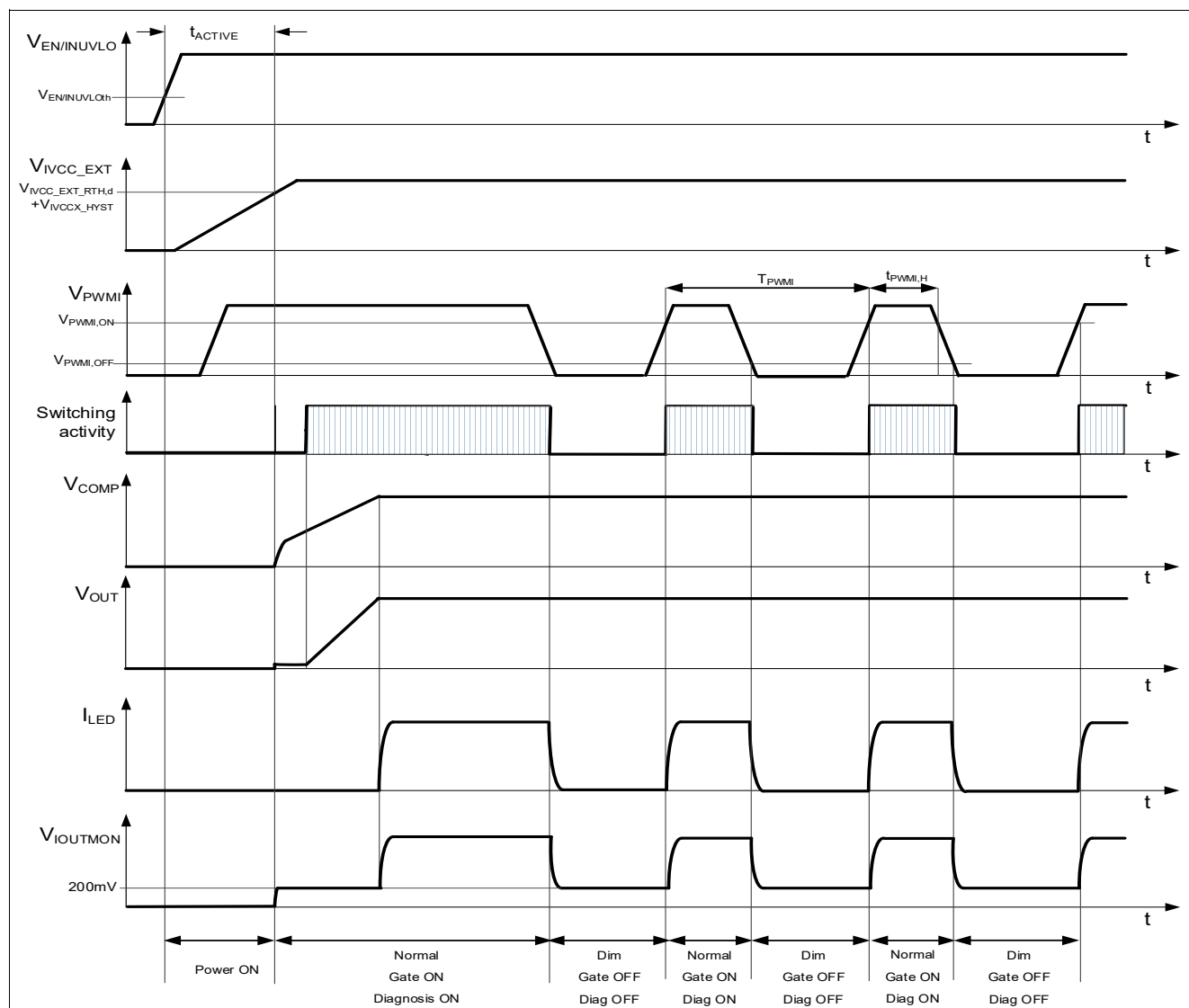


**Figure 19** Digital Dimming Overview

*Note:* In Register `REGUSETMON.REGUMODFB` the regulation mode can be read. During `PWMI = LOW` the SPI will always deliver the Regulation mode which was present at `PWMI = HIGH` as actual regulation mode, instead of “no Regulation”.

To avoid unwanted output overshoots due to not soft start assisted startups, PWM dimming in LOW state should not be used to suspend the output current for long time intervals. To stop in a safe manner `DVCCTRL.IDLE=HIGH` or `EN/INUVLO=LOW` can be used.

## Digital Dimming Function



**Figure 20** Timing Diagram LED Dimming and Start up behavior example ( $V_{VDD}$  and  $V_{VIN}$  stable in the functional range and not during startup)

**Digital Dimming Function**

## 7.2 Electrical Characteristics

**Table 8 EC Digital Dimming**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^{\circ}\text{C to }+150^{\circ}\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI Input:							
PWMI Turn On Threshold	$V_{PWMI,ON}$	2	–	–	V	–	P_7.2.1
PWMI Turn Off Threshold	$V_{PWMI,OFF}$	–	–	0.8	V	–	P_7.2.2
PWMI High Input Current	$I_{PWMI,H}$	15	30	45	μA	$V_{PWMI} = 2.0\text{ V};$	P_7.2.4
PWMI Low Input Current	$I_{PWMI,L}$	6	12	18	μA	$V_{PWMI} = 0.8\text{ V};$	P_7.2.5

## 8 Analog Dimming and Limp Home

If the TLD5542-1 is used as current regulator, the analog dimming feature allows control of the LED peak current level from the default maximum value. If the device is used as voltage regulator, then the analog dimming can be used to reduce the output voltage. In this chapter the assumption is to have it as a current regulator.

### 8.1 Description

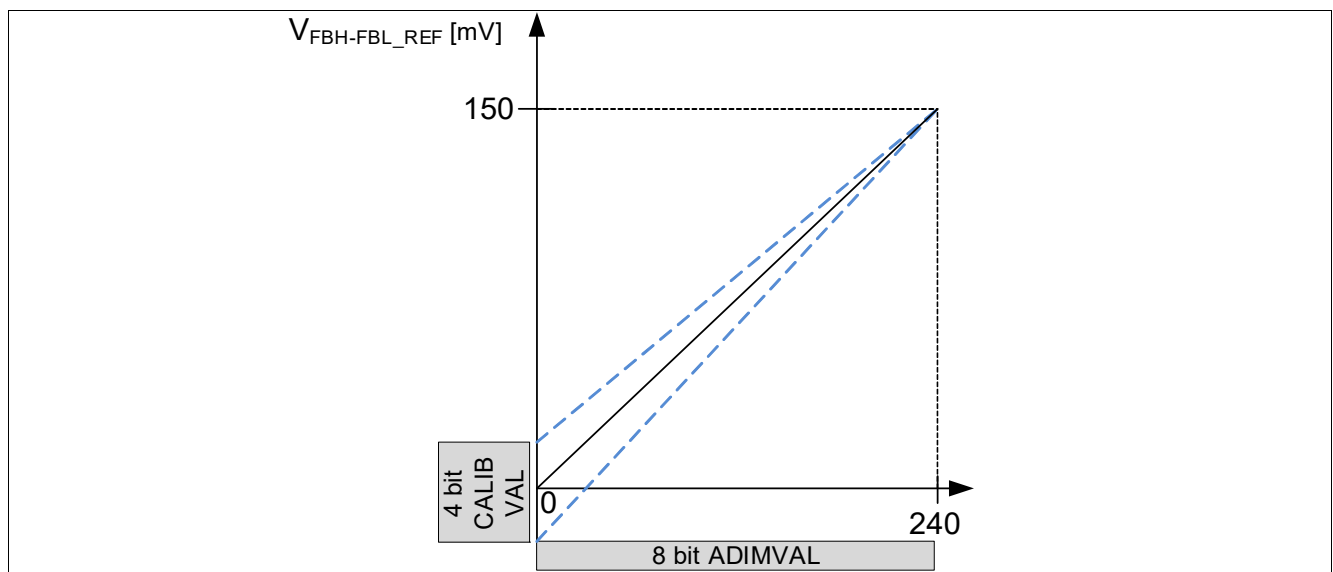
For the calculation of the output current  $I_{OUT}$  the following **Equation (8.1)** is used:

$$I_{OUT} = \frac{V_{FBH} - V_{FBL}}{R_{FB}} \quad (8.1)$$

The analog dimming feature is adjusting the average LED current level via the control of the feedback error amplifier reference voltage  $V_{FBH-FBL\_REF}$ .

In the default state (DAC\_OFF=0 and LHI=LOW), the current adjustment is done via a 8BIT SPI parameter (LEDCURRADIM.ADIMVAL) as shown on **Figure 21**.

If DAC\_OFF = 1 then the error amplifier reference voltage is the minimum between SET pin and DAC value. Therefore, in order to have a full scale dimming via SET pin, ADIMVAL has to be set to 240.



**Figure 21 Analog Dimming Overview**

#### Analog dimming adjustment during Limp Home state:

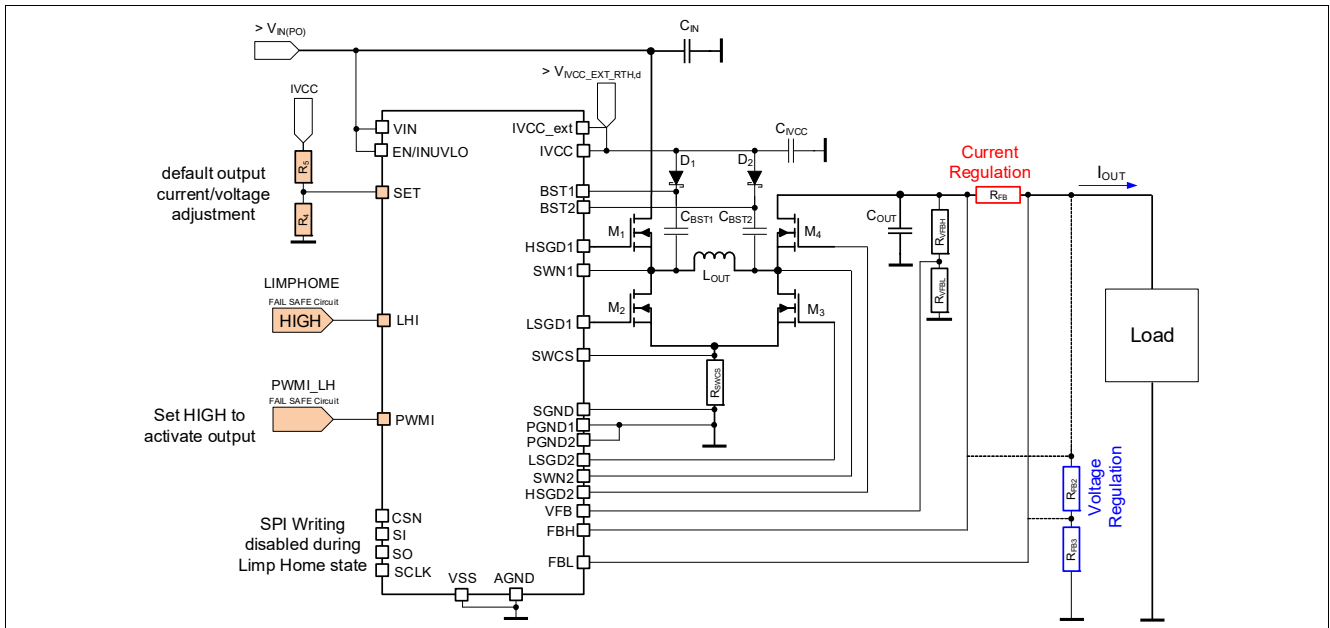
To enter in Limp Home state the LHI pin must be HIGH.

*Note: If the PWM1 and the EN/INUVLO are not set to HIGH, it is not possible to enable switching, even during Limp Home state.*

In Limp Home state, or if DAC\_OFF=1, the analog dimming control is done via the SET pin. A resistor divider between IVCC/IVCC\_EXT, SET and GND can be used to fix a load current/voltage value (refer to below).

When Limp Home is entered, the device will discharge the output capacitor with a F.D. Routine down to  $V_{FBH\_S2G\_dec}$  (MFSDLY set to the default Value). At the end of the F.D. routine, if the PWM1 is kept HIGH, the device will start regulating with the analog dimming level provided by the SET pin.

## Analog Dimming and Limp Home



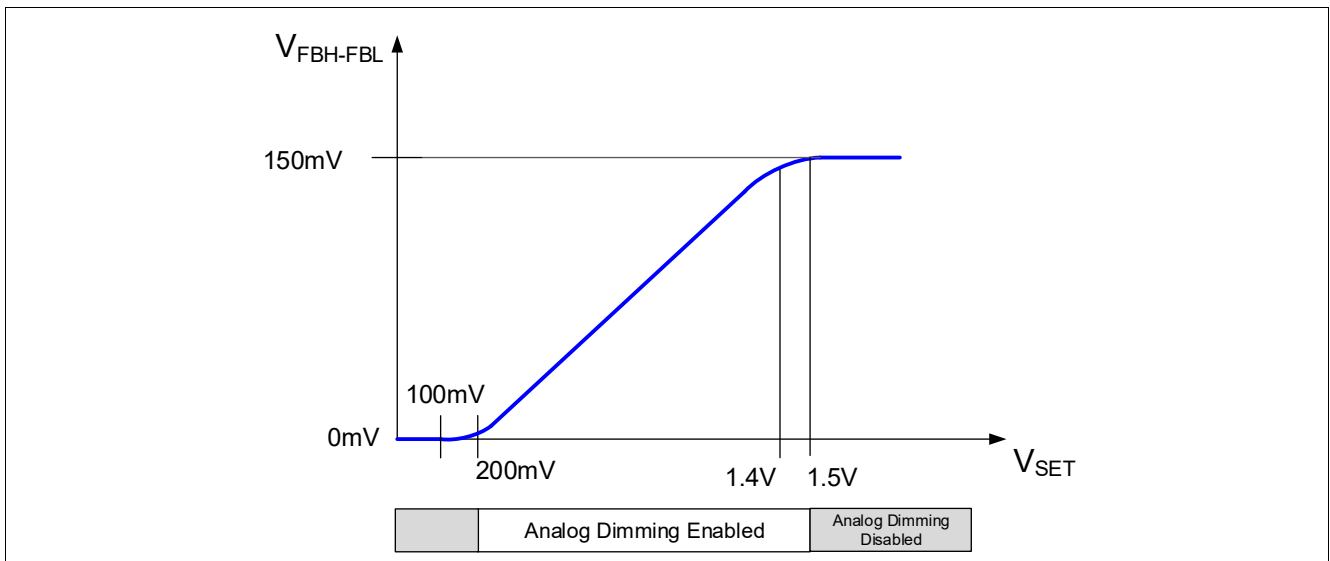
**Figure 22 Limp Home state schematic overview**

### Using the SET pin to adjust the output current:

During Limp Home state or if DAC\_OFF = 1, the average  $I_{OUT}$  can be adjusted by controlling the voltage at the SET pin ( $V_{SET}$ ) between 0.2 V and 1.4 V. The typical  $I_{OUT}$  behaviour is described by [Equation \(8.2\)](#) below:

$$I_{OUT} = \frac{V_{SET} - 200 \text{ mV}}{R_{FB} \cdot 8} \quad (8.2)$$

If  $V_{SET}$  is 200 mV (typ.) the LED current is only determined by the internal offset voltages of the comparators. To assure the switching activity is stopped and  $I_{OUT} = 0$ ,  $V_{SET}$  has to be < 100 mV, see [Figure 23](#).



**Figure 23 Analog Dimming Overview**

## 8.2 LED current calibration procedure

The LED current calibration procedure improves the accuracy during analog dimming. In order to be most effective, this routine has to be performed in the application, when the TLD5542-1 temperature and the output

## Analog Dimming and Limp Home

voltage are the ones in which the driver has to be accurate. The output current must be 0 during the procedure run. The optimum should be to re-calibrate the output periodically every time the application has PWMI=LOW for a sufficient long time.

Current calibration procedure:

- Power the load with a low analog dimming value (for example 10%)
- Set PWMI = LOW and disconnect the Load at the same time (to avoid Vout drifts from operating conditions and bring the output current to 0)
- Quickly (to avoid Vout drifts)  $\mu\text{C}$  enables the calibration routine:  $\text{DVCCTRL} . \text{ENCAL} = \text{HIGH}$
- Quickly (to avoid Vout drifts)  $\mu\text{C}$  starts the calibration:  $\text{LEDCURRCAL} . \text{SOCAL} = \text{HIGH}$
- Waiting time (needed to internally perform the calibration routine)  $\rightarrow$  aprox. 200  $\mu\text{s}$
- TLD5542-1 will set the FLAG:  $\text{LEDCURRCAL} . \text{EOCAL} = \text{HIGH}$ , when calibration routine has finished
- Reconnect the load
- The output current is automatically adjusted to a low offset and more accurate analog dimming value

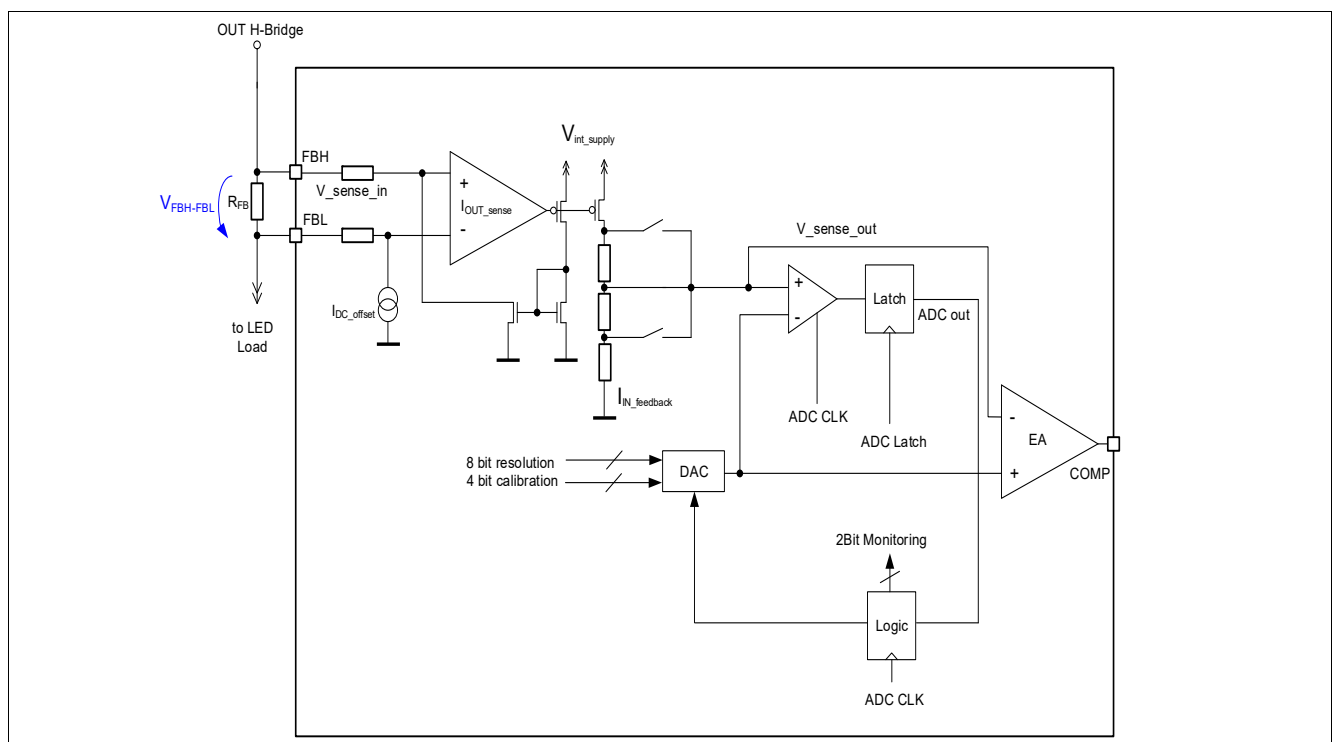
Once the calibration routine is correctly performed, the output current accuracy with analog dimming = 10% ( $\text{LEDCURRADIM} . \text{ADIMVAL} = 24$ ) is 10%.

The Calibration routine is not affecting the accuracy at 100% analog dimming.

The ENCAL Bits affect both device operation and CALIBVAL reading result:

- ENCAL = HIGH: the calibration result coming from the routine is used by internal circuitry and can be read back from CALIBVAL
- ENCAL = LOW: SPI value written in CALIBVAL is used by internal circuitry and can be read back; calibration routine start is inhibited

As a result,  $\mu\text{C}$  can use a stored result from a previously performed calibration to directly impose the desired value without waiting for a new routine to finish.



**Figure 24 LED current accuracy calibration overview**

### 8.3 Electrical Characteristics

**Table 9 EC Analog Dimming**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^{\circ}\text{C to }+150^{\circ}\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Source current on SET Pin	$I_{SET\_source}$	–	–	1	$\mu\text{A}$	<sup>1)</sup> $V_{SET} = 0.2\text{ V to }1.4\text{ V}$ ; <b>P_8.3.4</b>	

1) Specified by design: not subject to production test.



## 9 Linear Regulator

The TLD5542-1 features an integrated voltage regulator for the supply of the internal gate driver stages. Furthermore an external voltage regulator can be connected to the IVCC\_EXT pin to achieve an alternative gate driver supply if required.

### 9.1 IVCC Description

When the IVCC pin is connected to the IVCC\_EXT pin, the internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to  $I_{LIM}$  (P\_9.2.2). An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor (Figure 25, drawing A). Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches. A minimum capacitance value is given in parameter  $C_{IVCC}$  (P\_9.2.4).

#### Alternative IVCC\_EXT Supply Concept:

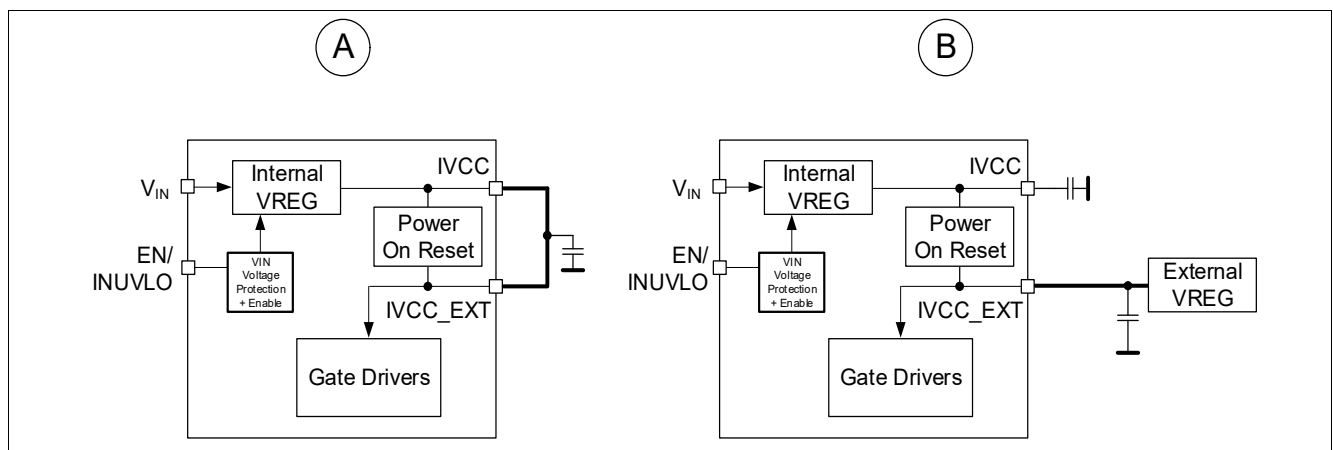
The IVCC\_EXT pin can be used for an external voltage supply to alternatively supply the MOSFET Gate drivers. This concept is beneficial in the high input voltage range to avoid power losses in the IC (Figure 25, drawing B).

#### Integrated undervoltage protection for the external switching MOSFET:

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage. This undervoltage reset threshold circuit will turn OFF the gate drivers in case the IVCC or IVCC\_EXT voltage falls below their undervoltage Reset switch OFF Thresholds  $V_{IVCC\_RTH,d}$  (P\_9.2.9) and  $V_{IVCC\_EXT\_RTH,d}$  (P\_9.2.5).

In Limp Home state the Undervoltage Reset switch OFF threshold for the IVCC has no impact on the switching activity.

The Undervoltage Reset threshold for the IVCC and the IVCC\_EXT pins help to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of the external logic level N-channel MOSFETs.



**Figure 25 Voltage Regulator Configurations**

**Linear Regulator**

**9.2 Electrical Characteristics**

**Table 10 EC Line Regulator**

$V_{IN} = 8\text{ V to } 36\text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IVCC							
Output Voltage	V <sub>IVCC</sub>	4.8	5	5.2	V	V <sub>IN</sub> = 13.5 V; 0.1 mA ≤ I <sub>IVCC</sub> ≤ 50 mA;	P_9.2.1
Output Current Limitation	I <sub>LIM</sub>	70	90	110	mA	1) V <sub>IVCC</sub> = 4 V;	P_9.2.2
Drop out Voltage (V <sub>IN</sub> - V <sub>IVCC</sub> )	V <sub>DR</sub>	–	200	350	mV	V <sub>IN</sub> = 5 V; I <sub>IVCC</sub> = 10 mA;	P_9.2.3
IVCC Buffer Capacitor	C <sub>IVCC</sub>	10	–	–	μF	1) 2)	P_9.2.4
IVCC_EXT Undervoltage Reset switch OFF Threshold	V <sub>IVCC_EXT_RTH,d</sub>	3.6	3.8	4.0	V	3) V <sub>IVCC_EXT</sub> decreasing;	P_9.2.5
IVCC Undervoltage Reset switch OFF Threshold	V <sub>IVCC_RTH,d</sub>	3.6	3.8	4.0	V	3) V <sub>IVCC</sub> decreasing;	P_9.2.9
IVCC and IVCC_EXT Undervoltage Hysterisis	V <sub>IVCCX_HYST</sub>	0.315	0.365	0.395	V	V <sub>IVCC</sub> increasing; V <sub>IVCC_EXT</sub> increasing;	P_9.2.6

1) Not subject to production test, specified by design

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum. Use capacitors with LOW ESR.

3) Selection of external switching MOSFET is crucial.  $V_{IVCC\_EXT\_RTH,d}$  and  $V_{IVCC\_RTH,d}$  min. as worst case  $V_{GS}$  must be considered.

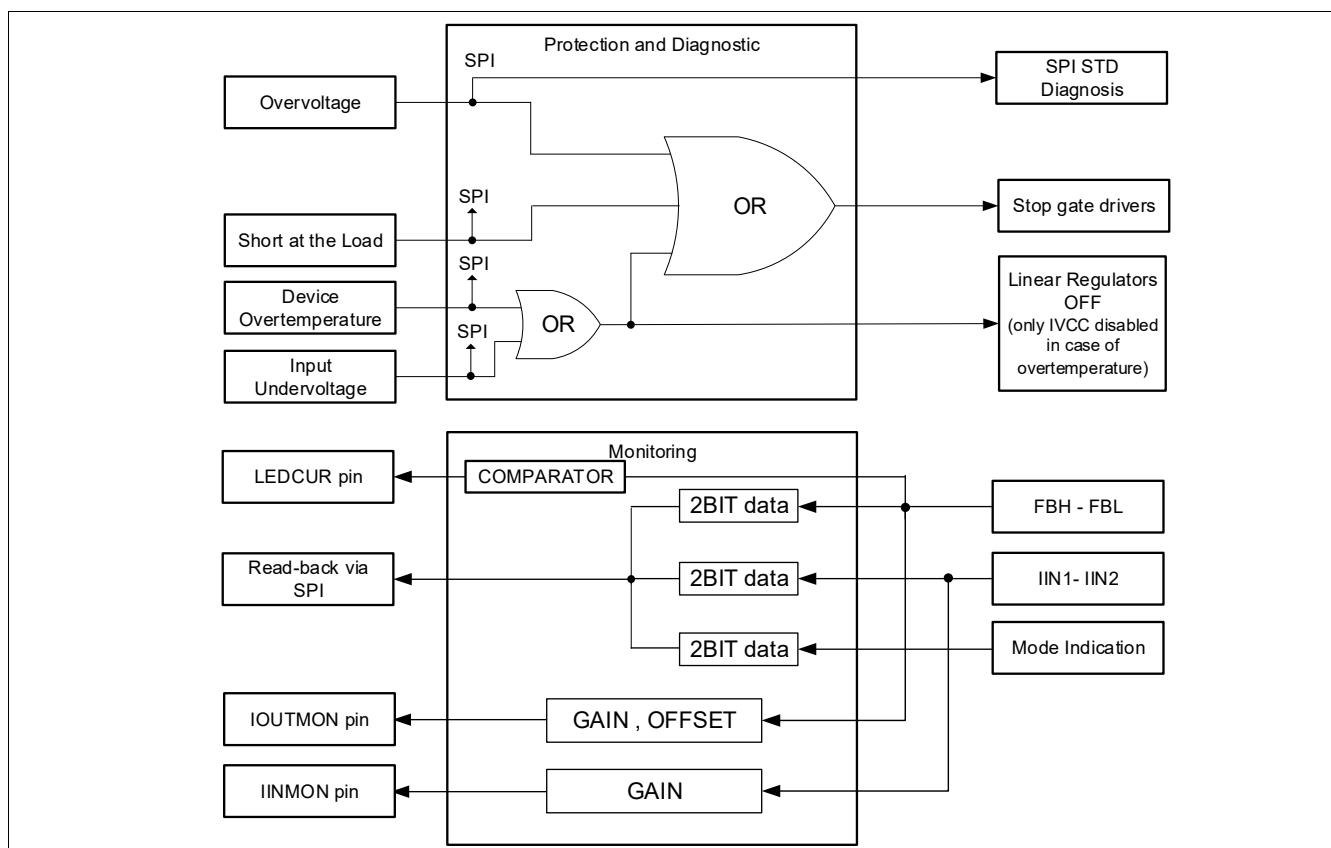
## 10 Protection and Diagnostic Functions

### 10.1 Description

The TLD5542-1 has integrated circuits to diagnose and protect against overvoltage, short circuits of the load and overtemperature faults. Furthermore, the device provides a 2 Bit information of  $I_{LED}$ ,  $I_{IN}$  by the SPI to the  $\mu C$ .

In IDLE state, only the overtemperature Shut Down, overtemperature warning, IVCC or IVCC\_EXT undervoltage monitor,  $V_{DD}$  or  $V_{EN/INUVLO}$  undervoltage monitor are reported according to specifications.

In a summary of the protection, diagnostic and monitor functions is displayed.



**Figure 26 Protection, Diagnostic and Monitoring Overview - TLD5542-1**

*Note: A device Overtemperature event overrules all other fault events!*



## Protection and Diagnostic Functions

### 10.2.2 Overvoltage Protection

A voltage divider between  $V_{OUT}$ , VFB pin and AGND is used to adjust  $V_{OUT}$  overvoltage protection threshold ( $V_{OUT\_OV}$ ), refer to **Figure 27** and **Equation (10.1)**:

$$V_{OUT\_OV} = V_{VFB\_OVTH} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad (10.1)$$

If  $V_{VFB}$  gets higher than its overvoltage threshold  $V_{VFB\_OVTH}$ , the SPI flag (OUTOV) in the STD diagnosis set to HIGH and the gate drivers stop switching for output regulation (Brake-Low condition both LS MOSFETs ON). When  $V_{VFB\_OVTH} - V_{VFB\_OVTH,HYS}$  threshold is reached the device will auto restart. The dedicated diagnosis flag (OUTOV) will be cleared after the next reading cycle of the STD diagnosis.

If the overvoltage threshold  $V_{OUT\_OV}$  is set below the maximum  $V_{IN}$  application operating range, then attention needs to be paid to the overvoltage behavior.

If load current persists during overvoltage event, repetitive overvoltage triggering may occur with a high frequency. This prevents inductor current regulation and the output current may even increase. To avoid this condition, proper sizing of the external components is needed (i.e. increase the output capacitance or the overvoltage threshold in order to delay the overvoltage trigger).

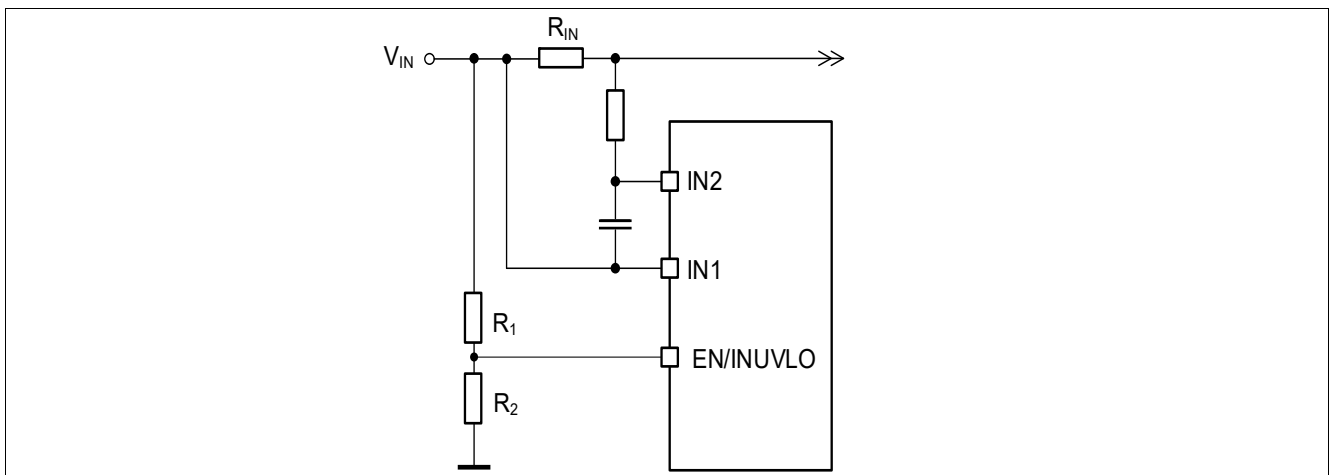
### 10.3 Input voltage monitoring, protection

Input undervoltage shutdown level can be defined through an external resistor divider, as shown in .

EN/INUVLO pin voltages are internally compared to their respective thresholds by means of hysteretic comparators.

Neglecting the hysteresis, the following equations hold:

$$UV_{th} = \frac{R_1 + R_2}{R_2} \cdot EN/INUVLO_{th} \quad (10.2)$$



**Figure 28 Input Voltage Protection**

### 10.4 Input current Monitoring

The two inputs (IIN1, IIN2) can be used to monitor the Input current.

The input current, measured via IIN1 and IIN2 pins, can be monitored through an analog output pin and an SPI routine.

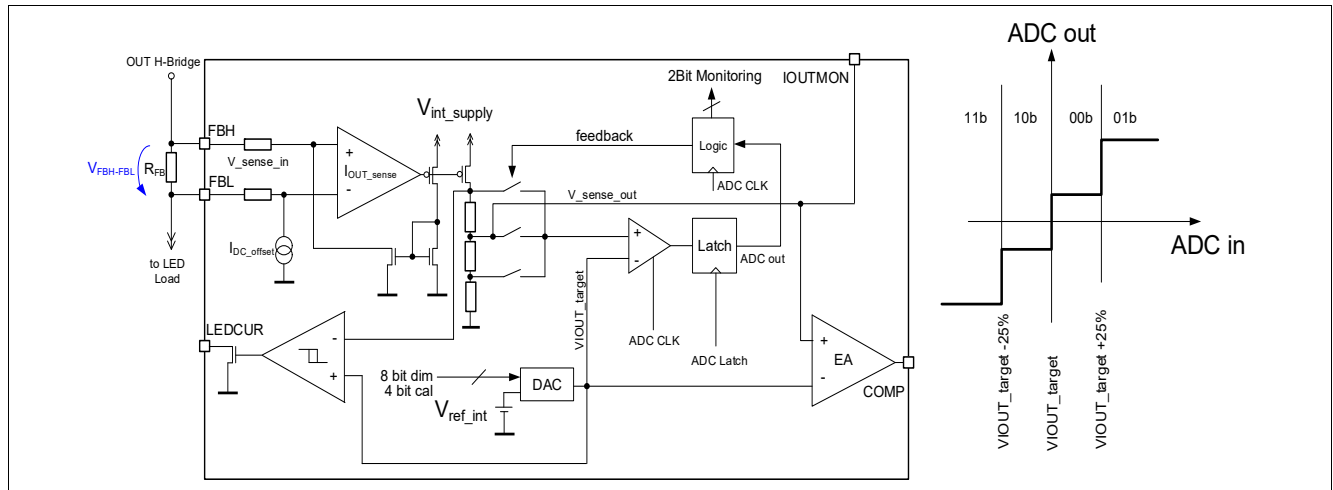


## Protection and Diagnostic Functions

The IOUTMON pin provides a linear indication of the current flowing through the LEDs. The typical IOUTMON behaviour follows [Equation \(10.4\)](#) :

$$V_{IOUTMON} = 200 \text{ mV} + I_{OUT} \cdot R_{FB} \cdot 8 \quad (10.4)$$

The typical output impedance of the IOUTMON is 24k Ohm.



**Figure 30 Output Current Monitoring General Overview**

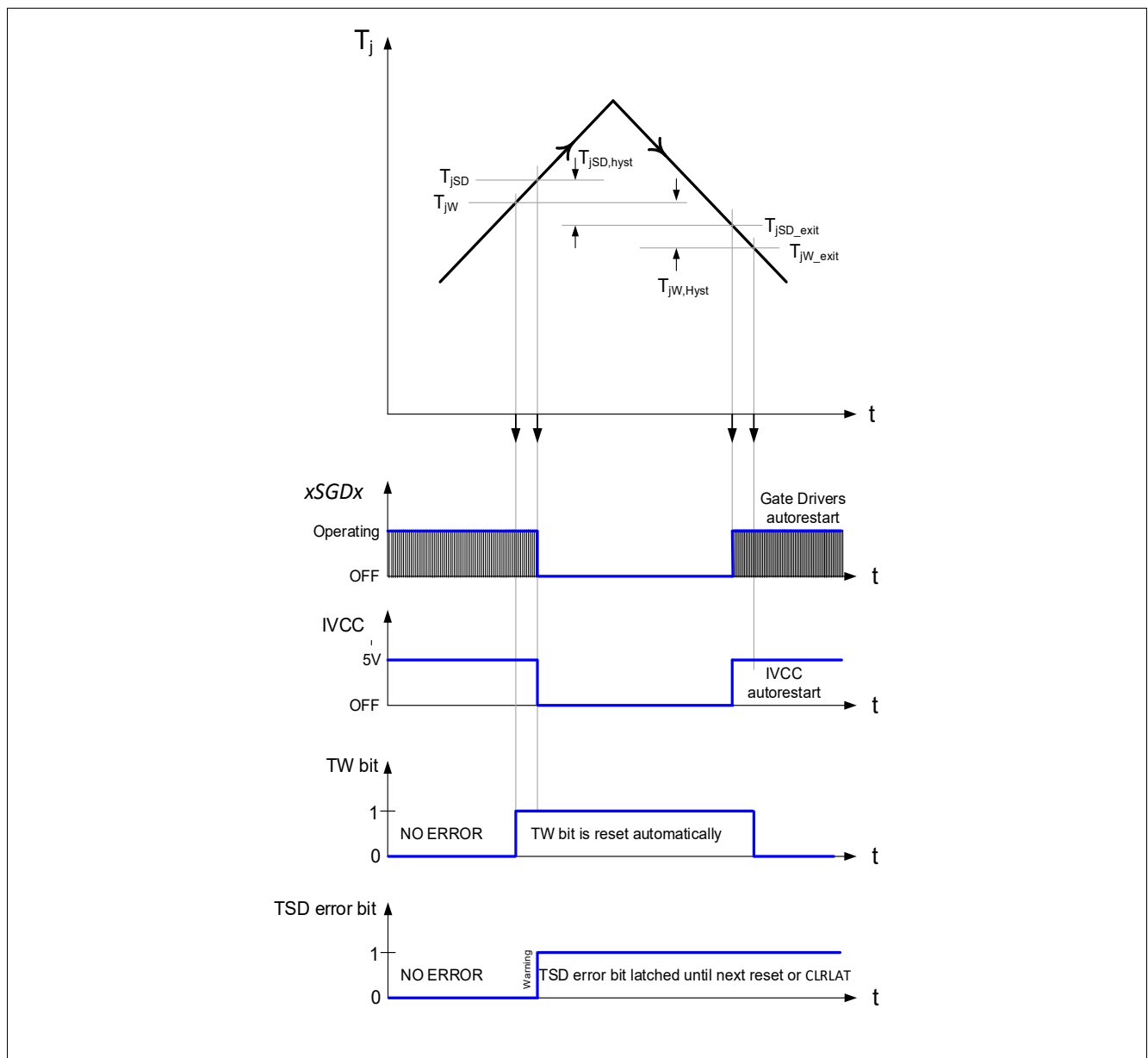
**Protection and Diagnostic Functions**

## 10.6 Device Temperature Monitoring

A temperature sensor is integrated on the chip. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If the internal temperature sensor reaches the warning temperature, the temperature warning bit  $TW$  is set to HIGH. This bit is not latched (i.e. if the temperature falls below the warning threshold (with hysteresis), the  $TW$  bit is reset to LOW again).

If the internal temperature sensor reaches the shut-down temperature, the Gate Drivers plus the IVCC regulator are shut down as described in [Figure 31](#) and the temperature shut-down bit:  $TSD$  is set to HIGH. The  $TSD$  bit is latched while the Gate Drivers plus the IVCC regulator have an auto restart behavior.

*Note: The Device will start up with a soft start routine after a TSD condition disappear.*



**Figure 31 Device Overtemperature Protection Behavior**



**Protection and Diagnostic Functions**

**10.7 Electrical Characteristics**

**Table 11 EC Protection and Diagnosis**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Short Circuit Protection							
Short to GND exit threshold	$V_{FBH\_S2G\_inc}$	1.95	2.05	2.15	V	<sup>1)</sup> $V_{FBH}$ increasing;	P_6.9.1
Short to GND entry threshold	$V_{FBH\_S2G\_dec}$	1.65	1.75	1.85	V	<sup>1)</sup> $V_{FBH}$ decreasing;	P_6.9.2
LEDCUR detect threshold increasing	$k_{LEDC\_INC}$	60	70	80	%	<sup>1)</sup> ADIMVAL = 240 $V_{FBH-FBL}$ increasing;	P_10.7.1
LEDCUR detect threshold increasing	$k_{LEDC\_INC}$	45	55	65	%	<sup>1)</sup> ADIMVAL = 48 $V_{FBH-FBL}$ increasing;	P_10.7.2
LEDCUR detect threshold decreasing	$k_{LEDC\_DEC}$	50	60	70	%	<sup>1)</sup> ADIMVAL = 240 $V_{FBH-FBL}$ decreasing;	P_10.7.3
LEDCUR detect threshold decreasing	$k_{LEDC\_DEC}$	30	40	50	%	<sup>1)</sup> ADIMVAL = 48 $V_{FBH-FBL}$ decreasing;	P_10.7.4
LEDCUR detect hysteresys	$k_{LEDCUR\_HYS}$	-	12	-	%	<sup>1)</sup> ADIMVAL = 48 to 240	P_10.7.5
Temperature Protection:							
Thermal Warning junction temperature	$T_{j,W}$	125	140	155	°C	<sup>1)</sup>	P_10.8.2
Temperature warning Hysteresis	$T_{j,W,hyst}$	–	10	–	°C	<sup>1)</sup>	P_10.8.3
Over Temperature Shutdown	$T_{j,SD}$	160	175	190	°C	<sup>1)</sup>	P_10.8.4
Over Temperature Shutdown Hysteresis	$T_{j,SD,hyst}$	–	10	–	°C	<sup>1)</sup>	P_10.8.5
Overvoltage Protection:							
VFB Over Voltage Feedback Threshold	$V_{VFB\_OVTH}$	1.42	1.46	1.50	V		P_10.8.6
Output Over Voltage Feedback Hysteresis	$V_{VFB\_OVTH,HYS}$	25	40	58	mV	Output Voltage decreasing;	P_10.8.7
Flags							
LEDCUR, EOMFS Pin Output Impedance	$R_{F12}$	–	2.1	–	kΩ	<sup>1)</sup> When Pull Down is active I=100uA	P_10.8.14

1) Specified by design; not subject to production test.

**Note:** *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 11 Infineon FLAT SPECTRUM Feature set

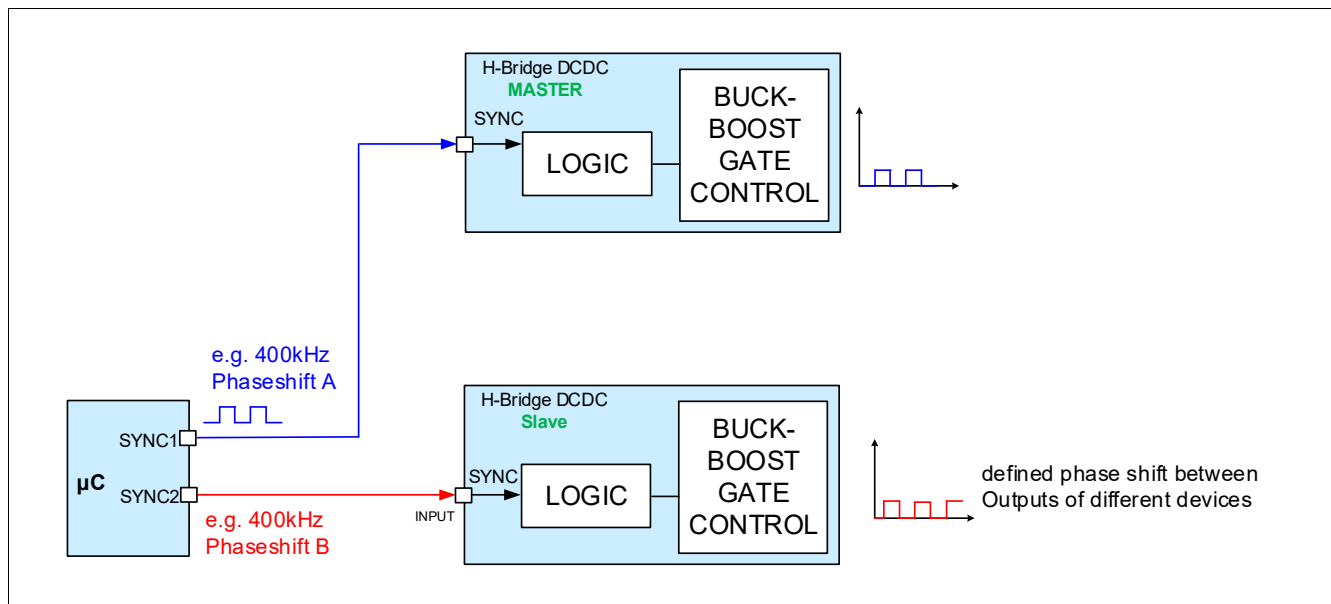
### 11.1 Description

The Infineon FLAT SPECTRUM feature set has the target to minimize external additional filter circuits. The goal is to provide several beneficial concepts to provide easy adjustments for EMC improvements after the layout is already done and the HW designed.

### 11.2 Synchronization Function

The TLD5542-1 features a SYNC input pin which can be used by a  $\mu\text{C}$  pin to define an oscillator switching frequency. The  $\mu\text{C}$  is responsible to synchronize with various devices by applying appropriate SYNC signals to the dedicated DC/DC devices in the system. Refer to [Figure 32](#)

*Note: The Synchronization function can not be used when the Spread Spectrum is active.*



**Figure 32 Synchronization Overview**

### 11.3 Spread Spectrum

The Spread Spectrum modulation technique significantly improves the lower frequency range of the spectrum ( $f < 30$  MHz).

By using the spread spectrum technique, it is possible to optimize the input filter only for the peak limits, and also pass the average limits (average emission limits are -20dB lower than the peak emission limits). By using spread spectrum, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits.

The TLD5542-1 features a built in Spread Spectrum function which can be enabled (SWTMOD. ENSPREAD) and adjusted via the SPI interface. Dedicated SPI-Bits are used to adjust the modulation frequency  $f_{FM}$ , (P\_11.6.3) and (P\_11.6.4) (SWTMOD. FMSPREAD) and the deviation frequency  $f_{dev}$ , (P\_11.6.1) and (P\_11.6.2) (SWTMOD. FDEVSPREAD) accordingly to specific application needs. Refer to [Figure 33](#) for more details.

**The following adjustments can be programmed when SWTMOD. ENSPREAD = HIGH:**

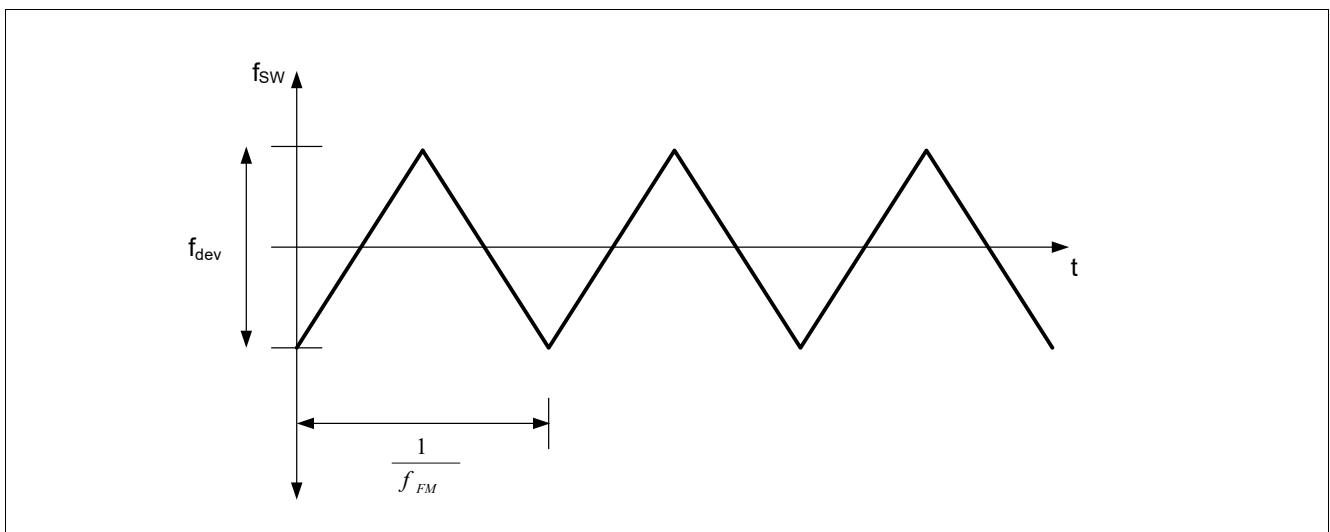
SWTMOD. FMSPREAD = LOW: 12 kHz

SWTMOD. FMSPREAD = HIGH: 18 kHz

SWTMOD. FDEVSPREAD = HIGH:  $\pm 8\%$  of  $f_{SW}$

SWTMOD. FDEVSPREAD = LOW:  $\pm 16\%$  of  $f_{SW}$

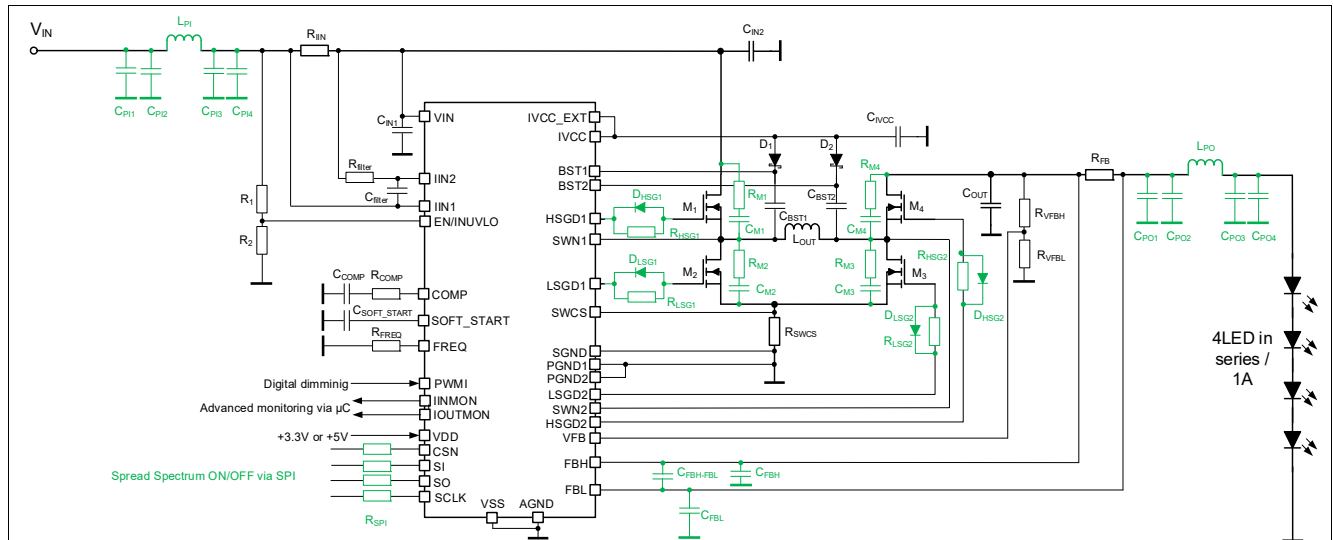
*Note: The Spread Spectrum function can not be used when the synchronization pin is used.*



**Figure 33 Spread Spectrum Overview**

## 11.4 EMC optimized schematic

**Figure 34** below displays the Application circuit with additional external components for improved EMC behavior.



**Figure 34 Application Drawing Including Additional Components for an Improved EMC Behavior**

**Note:** The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

## 11.5 Electrical Characteristics

**Table 12 EC Spread Spectrum**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

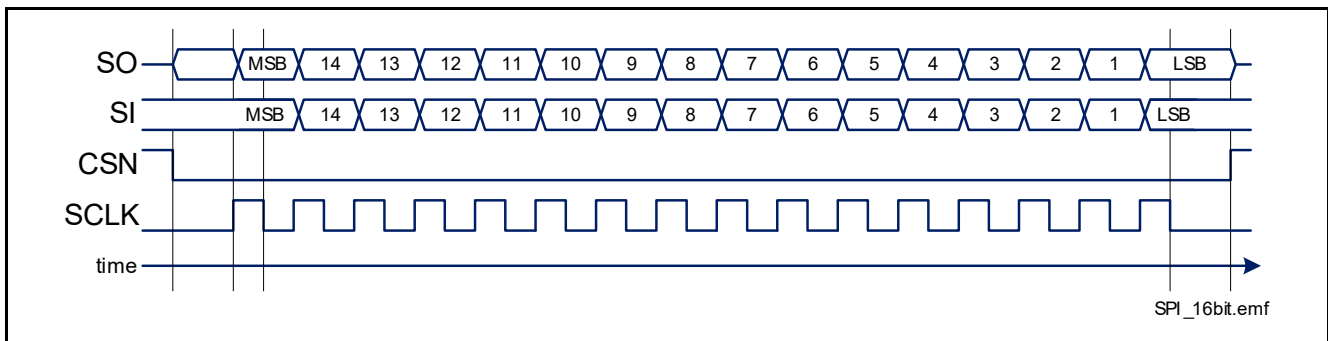
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Spread Spectrum Parameters							
Frequency Deviation	$f_{\text{dev}}$	–	±8	–	%	1) SWTMOD . FDEV SPREAD = HIGH;	P_11.6.1
Frequency Deviation	$f_{\text{dev}}$	–	±16	–	%	1) SWTMOD . FDEV SPREAD = LOW;	P_11.6.2
Frequency Modulation	$f_{\text{FM}}$	–	12	–	kHz	1) SWTMOD . FMSP READ = LOW;	P_11.6.3
Frequency Modulation	$f_{\text{FM}}$	–	18	–	kHz	1) SWTMOD . FMSP READ = HIGH;	P_11.6.4

1) Specified by design; not subject to production test.

## Serial Peripheral Interface (SPI)

## 12 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CSN indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CSN. A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bit has been transferred after the first 16 bits. Otherwise, a TER (i.e. Transmission Error) bit is asserted. In this way the interface provides daisy chain capability with 16 bit as well as with 8 bit SPI devices.



**Figure 35 Serial Peripheral Interface**

### 12.1 SPI Signal Description

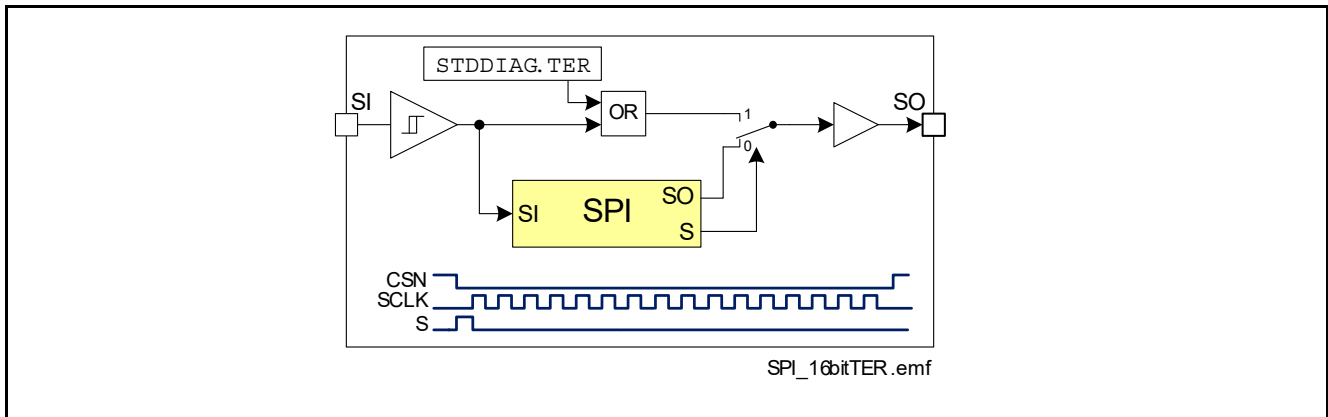
#### CSN - Chip Select

The system microcontroller selects the TLD5542-1 by means of the CSN pin. Whenever the pin is in LOW state, data transfer can take place. When CSN is in HIGH state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

#### CSN HIGH to LOW Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to HIGH or LOW state depending on the signal level at pin SI.
- If the device is in SLEEP mode, the SO pin remains in high impedance state and no SPI transmission will occur.
- TER Flag will set the Bit number 10 in the STD diagnosis Frame. This Bit is set to HIGH after an undervoltage condition, reset via SPI command, on Limp Home state entering or after an incorrect SPI transmission. TER Flag can be read also directly on the SO line between the falling edge of the CSN and the first rising edge of the SCLK according to the [Figure 36](#).

## Serial Peripheral Interface (SPI)



**Figure 36 Combinatorial Logic for TER bit**

### CSN LOW to HIGH Transition

- Command decoding is only done, when after the falling edge of CSN exactly a multiple (0,1, 2, 3, ...) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

### SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in LOW state whenever chip select CSN makes any transition, otherwise the command may be not accepted.

### SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to [Chapter 12.5](#) for further information.

### SO Serial Output

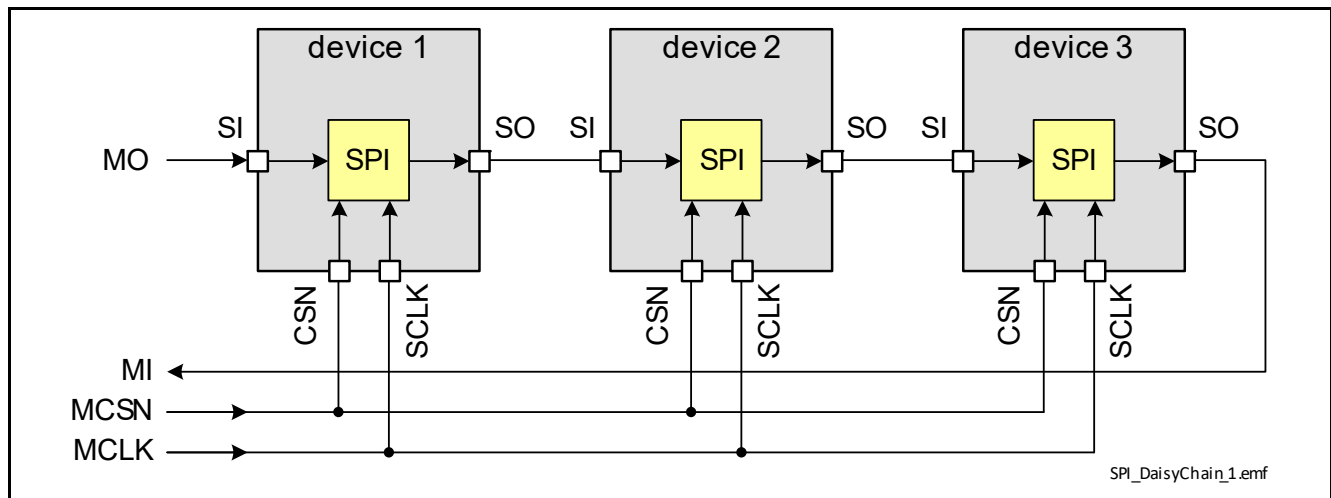
Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CSN pin goes to LOW state. New data will appear at the SO pin following the rising edge of SCLK.

Please refer to [Chapter 12.5](#) for further information.

## 12.2 Daisy Chain Capability

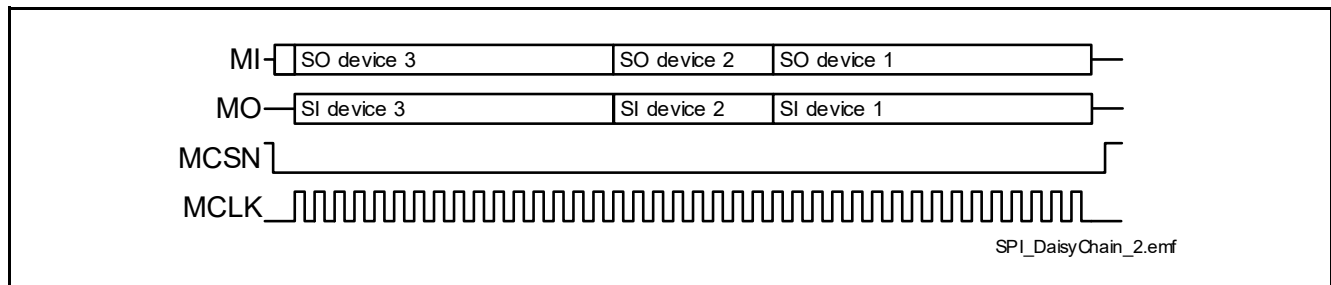
The SPI of the TLD5542-1 provides daisy chain capability. In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device (see [Figure 37](#)), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

## Serial Peripheral Interface (SPI)



**Figure 37** Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from the SI line is shifted in with each SCLK. The bit shifted out occurs at the SO pin. After sixteen SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CSN line must turn HIGH to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices (depending on how many devices with 8 bit SPI and how many with 16 bit SPI). After that, the MCSN line must turn HIGH (see [Figure 38](#)).

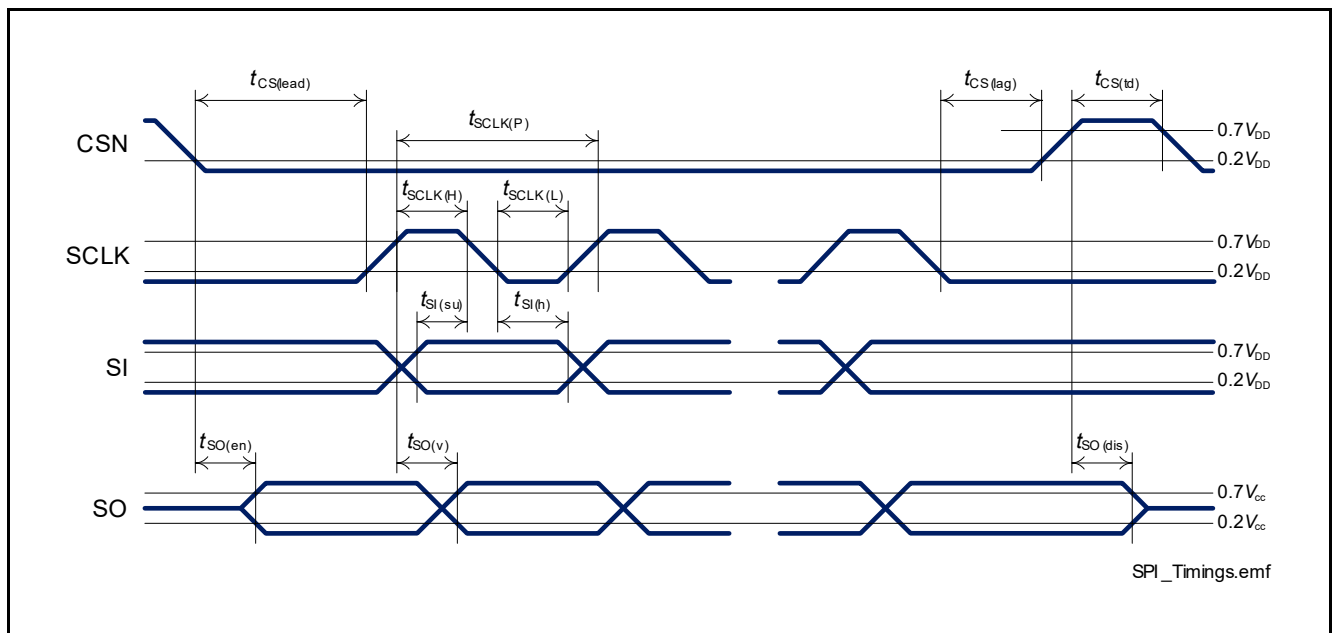


**Figure 38** Data Transfer in Daisy Chain Configuration



## Serial Peripheral Interface (SPI)

### 12.3 Timing Diagrams



**Figure 39 Timing Diagram SPI Access**

**Serial Peripheral Interface (SPI)**

**12.4 Electrical Characteristics**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^{\circ}\text{C to }+150^{\circ}\text{C}$ ,  $V_{DD} = 3\text{ V to }5.5\text{ V}$ , all voltages with respect to ground; (unless otherwise specified)

**Table 13 EC Serial Peripheral Interface (SPI)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CSN, SCLK, SI) - LOW level of pin							
CSN	$V_{\text{CSN(L)}}$	0	–	0.8	V	–	P_12.4.1
SCLK	$V_{\text{SCLK(L)}}$	0	–	0.8	V	–	P_12.4.2
SI	$V_{\text{SI(L)}}$	0	–	0.8	V	–	P_12.4.3
Input Characteristics (CSN, SCLK, SI) - HIGH level of pin							
CSN	$V_{\text{CSN(H)}}$	2	–	$V_{\text{DD}}$	V	–	P_12.4.4
SCLK	$V_{\text{SCLK(H)}}$	2	–	$V_{\text{DD}}$	V	–	P_12.4.5
SI	$V_{\text{SI(H)}}$	2	–	$V_{\text{DD}}$	V	–	P_12.4.6
L-input pull-up current at CSN pin	$-I_{\text{CSN(L)}}$	31	63	94	μA	$V_{\text{DD}} = 5\text{ V};$ $V_{\text{CSN}} = 0.8\text{ V};$	P_12.4.7
H-input pull-up current at CSN pin	$-I_{\text{CSN(H)}}$	22	45	67	μA	$V_{\text{DD}} = 5\text{ V};$ $V_{\text{CSN}} = 2\text{ V};$	P_12.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{\text{SCLK(L)}}$	6	12	18	μA	$V_{\text{SCLK}} = 0.8\text{ V};$	P_12.4.9
SI	$I_{\text{SI(L)}}$	6	12	18	μA	$V_{\text{SI}} = 0.8\text{ V};$	P_12.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{\text{SCLK(H)}}$	15	30	45	μA	$V_{\text{SCLK}} = 2\text{ V};$	P_12.4.11
SI	$I_{\text{SI(H)}}$	15	30	45	μA	$V_{\text{SI}} = 2\text{ V};$	P_12.4.12
Output Characteristics (SO)							
L level output voltage	$V_{\text{SO(L)}}$	0	–	0.4	V	$I_{\text{SO}} = -2\text{ mA};$	P_12.4.13
H level output voltage	$V_{\text{SO(H)}}$	$V_{\text{DD}} - 0.4\text{ V}$	–	$V_{\text{DD}}$	V	$I_{\text{SO}} = 2\text{ mA};$ $V_{\text{DD}} = 5\text{ V};$	P_12.4.14
Output tristate leakage current	$I_{\text{SO(OFF)}}$	-1	–	1	μA	$V_{\text{CSN}} = V_{\text{DD}};$ $V_{\text{SO}} = 0\text{ V or}$ $V_{\text{SO}} = V_{\text{DD}};$	P_12.4.15
Timings							
Enable lead time (falling CSN to rising SCLK)	$t_{\text{CSN(lead)}}$	200	–	–	ns	<sup>1)</sup>	P_12.4.17
Enable lag time (falling SCLK to rising CSN)	$t_{\text{CSN(lag)}}$	200	–	–	ns	<sup>1)</sup>	P_12.4.18
Transfer delay time (rising CSN to falling CSN)	$t_{\text{CSN(td)}}$	250	–	–	ns	<sup>1)</sup>	P_12.4.19
Output enable time (falling CSN to SO valid)	$t_{\text{SO(en)}}$	–	–	200	ns	<sup>1)</sup> $C_{\text{L}} = 20\text{ pF at SO pin};$	P_12.4.20

**Serial Peripheral Interface (SPI)**

**Table 13 EC Serial Peripheral Interface (SPI) (cont'd)**

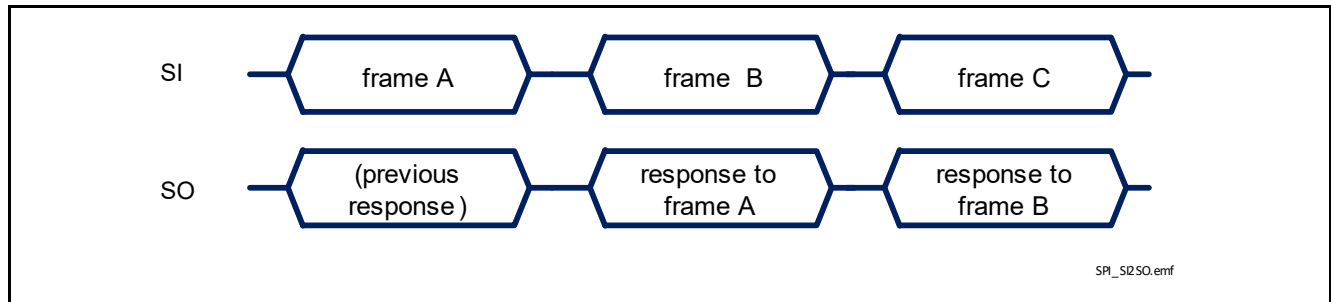
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	200	ns	<sup>1)</sup> $C_L = 20 \text{ pF}$ at SO pin;	P_12.4.21
Serial clock frequency	$f_{SCLK}$	–	–	5	MHz	<sup>1)</sup>	P_12.4.22
Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	<sup>1)</sup>	P_12.4.24
Serial clock HIGH time	$t_{SCLK(H)}$	75	–	–	ns	<sup>1)</sup>	P_12.4.25
Serial clock LOW time	$t_{SCLK(L)}$	75	–	–	ns	<sup>1)</sup>	P_12.4.26
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	<sup>1)</sup>	P_12.4.27
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	<sup>1)</sup>	P_12.4.28
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	<sup>1)</sup> $C_L = 20 \text{ pF}$ ;	P_12.4.29

1) Not subject to production test, specified by design

## Serial Peripheral Interface (SPI)

### 12.5 SPI Protocol

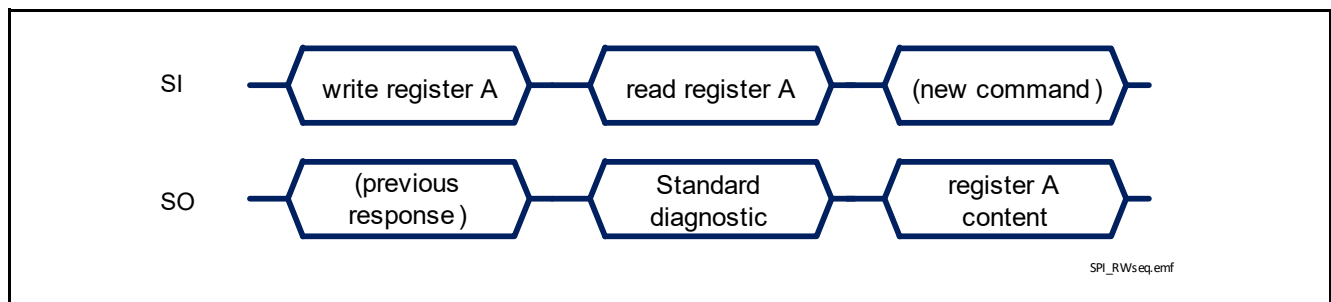
The relationship between SI and SO content during SPI communication is shown in **Figure 40**. The SI line represents the frame sent from the  $\mu\text{C}$  and the SO line is the answer provided by the TLD5542-1. The first SO response is the response from the previous command.



**Figure 40 Relationship between SI and SO during SPI communication**

The SPI protocol will provide the answer to a command frame only with the next transmission triggered by the  $\mu\text{C}$ . Although the biggest majority of commands and frames implemented in TLD5542-1 can be decoded without the knowledge of what happened before, it is advisable to consider what the  $\mu\text{C}$  sent in the previous transmission to decode TLD5542-1 response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register will look as follows:



**Figure 41 Register content sent back to  $\mu\text{C}$**

There are 3 special situations where the frame sent back to the  $\mu\text{C}$  doesn't depend on the previously received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 42**
- when TLD5542-1 logic supply comes out of an Undervoltage reset condition ( $V_{\text{DD}} < V_{\text{DD(UV)}}$ ) as shown in **Figure 43** or  $\text{EN/INUVLO} < V_{\text{EN/INUVLOth}}$
- in case of a read or write command for a “not used” or “reserved” register (in this case TLD5542-1 answers with Standard Diagnosis at the next SPI transmission)

Serial Peripheral Interface (SPI)

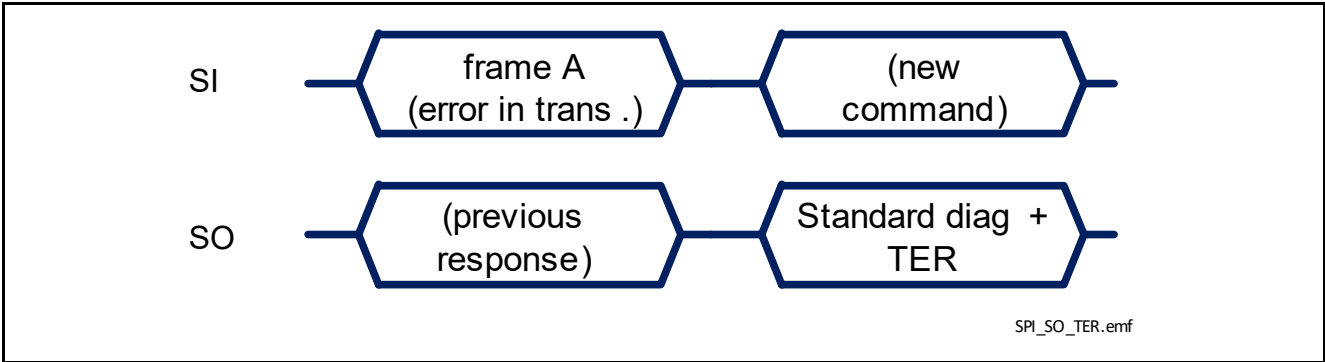


Figure 42 TLD5542-1 response after an error in transmission

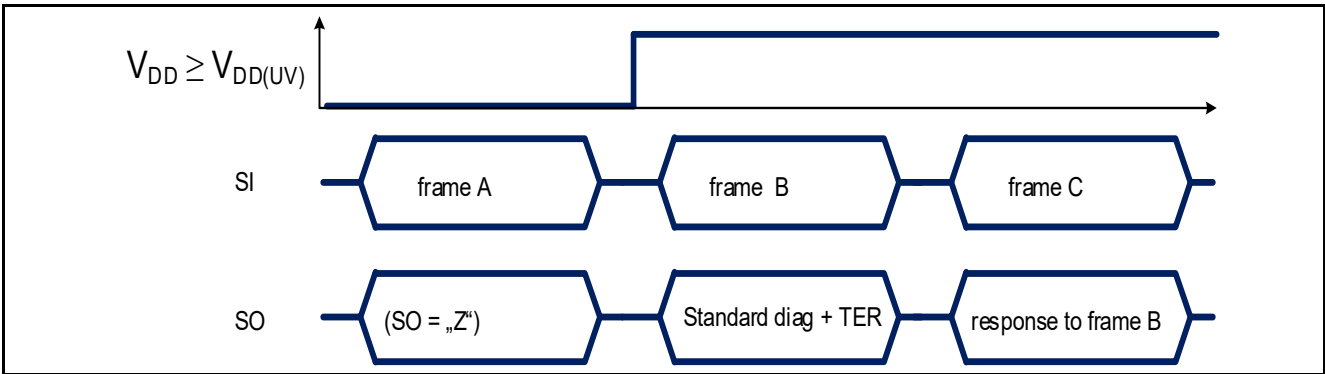


Figure 43 TLD5542-1 response after coming out of Power-On reset at  $V_{DD}$

**Serial Peripheral Interface (SPI)**

## 12.6 SPI Registers Overview

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame	W/R	RB	ADDR						Data							
Write Register in bank 0																
SI	1	0	ADDR						Data							
Read Register in bank 0																
SI	0	0	ADDR						x	x	x	x	x	x	x	0
Read Standard Diagnosis																
SI	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

Reading a register needs two SPI frames. In the first frame the read command is sent. In the second frame the output at SPI signal SO will contain the requested information. The MSB will be HIGH (while in case of standard diagnosis is LOW). A new command can be executed in the second frame.

### 12.6.1 Standard Diagnosis

The Standard Diagnosis reports several diagnostic informations and the status of the device and the utility routines.

The bits UVLORST, TER, OUTOV, IVCCUVLO and SHRTLED are latched and automatically cleared after a STD diagnosis reading.

A CLRLAT command resets the diagnostic Latched Flag TSD bit.

The TSD bit is always latched and clearable only via explicit CLRLAT command.

The STD bits which are real time status monitors or mirror of internal registers are not cleared after a STD diagnosis reading or via explicit CLRLAT command:

- The STATE bits and TW are real time status flags
- The bits EOMON, EOMFS and EOCAL are mirror of internal register
- The SWRST\_BSTUV bit is the logic OR of:
  - latched SWRST flag after a DVCSTRL.SWRST command (clearable via STD Diagnosis reading)
  - real time monitor of gate driver undervoltage (VBSTx-VSWNx\_UVth)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SWRST_BSTUV	UVLO_RST	STATE	TER	EO MON	EOM FS	EOC AL	0	OUTOV	IVCCU VLO	LED CUR	SHRT LED	TSD	TW	

**Serial Peripheral Interface (SPI)**

Field	Bits	Type	Description
SWRST_BSTUV	14	r	<b>SWRST OR VBSTx-VSWNx_UVth Monitor</b> $0_B$ , no SWRST or undervoltage on the Gate Drivers occurred $1_B$ , there was at least one SWRST since last readout OR an undervoltage condition at the gate drivers is occurring
UVLORST	13	r	<b><math>V_{DD}</math> OR <math>V_{EN/INUVLO}</math> Undervoltage Monitor</b> $0_B$ , there was no $V_{DD}$ OR $V_{EN/INUVLO}$ undervoltage since last readout $1_B$ , there was at least one $V_{DD}$ undervoltage OR $V_{EN/INUVLO}$ undervoltage condition since last readout
STATE	12:11	r	<b>Operative State Monitor</b> $00_B$ , (reserved) $01_B$ , Limp Home Mode $10_B$ , Active Mode $11_B$ , Idle Mode
TER	10	r	<b>Transmission Error</b> $0_B$ , Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) $1_B$ , Previous transmission failed or first transmission after reset
EOMON	9	r	<b>End of LED/Input Current Monitor Routine Bit</b> $0_B$ , Current monitoring routine not completed, not successfully performed or never run. $1_B$ , Current Monitor routine successfully performed (is reset to $0_B$ when SOMON is set to $1_B$ )
EOMFS	8	r	<b>End of MFS Routine Bit</b> $0_B$ , MFS routine not completed, not successfully performed or never run. $1_B$ , MFS routine successfully performed (is reset to $0_B$ when SOMOFS is set to $1_B$ )
EOCAL	7	r	<b>End of Calibration Routine</b> $0_B$ , Calibration routine not completed, not successfully performed or never run. $1_B$ , Calibration routine successfully performed (is reset to $0_B$ when SOCAL is set to $1_B$ )
OUTOV	5	r	<b>Output overvoltage Monitor</b> $0_B$ , Output overvoltage not detected since last readout $1_B$ , Output overvoltage was detected since last readout
IVCCUVLO	4	r	<b>IVCC or IVCC_EXT Undervoltage Lockout Monitor</b> $0_B$ , IVCC and IVCC_EXT above $V_{IVCC\_RTH,d}$ or $V_{IVCC\_EXT\_RTH,d}$ threshold since last readout $1_B$ , Undervoltage on IVCC or IVCC_EXT occurred since last readout
LEDCUR	3	r	<b>LED Current Flag (see LEDCUR pin description <a href="#">Chapter 10.5</a>)</b> $0_B$ , LED current not detected $1_B$ , LED current detected

**Serial Peripheral Interface (SPI)**

Field	Bits	Type	Description
SHRTLED	2	r	<b>Shorted LED Diagnosis</b> $0_B$ , Short circuit condition not detected since last readout $1_B$ , Short circuit condition detected since last readout
TSD	1	r	<b>Over Temperature Shutdown</b> $0_B$ , $T_j$ below temperature shutdown threshold $1_B$ , Overtemperature condition detected since last readout
TW	0	r	<b>Over Temperature Warning</b> $0_B$ , $T_j$ below temperature warning threshold $1_B$ , $T_j$ exceeds temperature warning threshold



## Serial Peripheral Interface (SPI)

### 12.6.2 Register structure

**Table 15** describes in detail the available registers with their bit-fields function, size and position

**Table 14** shows register addresses and summarize bit-field position inside each register

**Table 14 Register Bank 0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W/ R	R B	ADDR						Data							
LEDCURR ADIM	W/ R	0	0	0	0	0	0	0	ADIMVAL							
LEDCURR CAL	W/ R	0	0	0	0	0	1	1	x	DAC_ OFF	SOCAL	EOCAL	CALIBVAL			
SWTMOD	W/ R	0	0	0	0	1	0	1	x	DCM_ EN	CCM4E VER	VFB_VI N_OFF	S2G_O FF	ENSP READ	FMSP READ	FDEVSP READ
DVCCTRL	W/ R	0	0	0	0	1	1	0	EA_IO UT	EA_G M	SLOPE		ENCAL	CLRLA T	SWRS T	IDLE
MFSSETU P1	W/ R	0	0	0	1	0	0	1	EA_IO UT_MF S	ILIM_ HALF _MFS	SOMFS	EOMFS	LEDCHAIN			
MFSSETU P2	W/ R	0	0	0	1	0	1	0	MFSDLY							
CURRMON	W/ R	0	0	0	1	1	0	0	x	x	SOMO N	EOMON	INCURR		LEDCURR	
REGUSET MON	W/ R	0	0	0	1	1	1	1	x	x	x		REGUMODFB		BB_BST_CMP	
MUXCTRL	W/ R	1	1	1	1	1	1	0	MFS_R EF	AMUX _EN	SO_MUX_SEL					

A write to a non existing address is ignored, a read to a non existing register is ignored and the STD Diagnosis Frame is send out.

**Serial Peripheral Interface (SPI)**

**Table 15 Register description**

Register name	Field	Bits	Type	Purpose
LEDCURRADIM	ADIMVAL	7:0	r/w	<b>LED Current Configuration Register</b> 00000000 <sub>B</sub> , analog dimming @ 0% of LED current fixed via $R_{FB}$ 11110000 <sub>B</sub> , (default) analog dimming @ 100% of LED current fixed via $R_{FB}$
LEDCURRCAL	CALIBVAL	3:0	r/w	<b>LED Current Accuracy Trimming Configuration Register</b> LED current calibration value definition, the first bit is the calibration sign: 0000 <sub>B</sub> , (default) Initial state in the middle of the range 0111 <sub>B</sub> , maximum calibration value positive 1111 <sub>B</sub> , maximum calibration value negative
	EOCAL	4	r	End of calibration routine signalling bit: 0 <sub>B</sub> , (default) calibration routine not completed, not successfully performed or never run. 1 <sub>B</sub> , calibration successfully performed (is reset to 0 <sub>B</sub> when SOCAL is set to 1 <sub>B</sub> )
	SOCAL	5	r/w	Start of calibration routine signalling bit: 0 <sub>B</sub> , (default) no calibration routine started 1 <sub>B</sub> , calibration routine start (autoclear)
	DAC_OFF	6	r/w	Switch OFF internal analog dimming DAC bit: 0 <sub>B</sub> , (default) internal DAC active 1 <sub>B</sub> , internal DAC inactive and analog dimming error amplifier mapped to SET pin

**Serial Peripheral Interface (SPI)**

**Table 15 Register description (cont'd)**

Register name	Field	Bits	Type	Purpose
SWTMOD	FDEVSPREAD	0	r/w	<b>Switching Mode Configuration Register</b> Deviation Frequency $f_{DEV}$ definition: 0 <sub>B</sub> , (default) $\pm 16\%$ of $f_{SW}$ 1 <sub>B</sub> , $\pm 8\%$ of $f_{SW}$
	FMSPREAD	1	r/w	Frequency Modulation Frequency $f_{FM}$ definition: 0 <sub>B</sub> , (default) 12 kHz 1 <sub>B</sub> , 18 kHz
	ENSPREAD	2	r/w	Enable Spread Spectrum feature: 0 <sub>B</sub> , (default) Spread Spectrum modulation disabled 1 <sub>B</sub> , Spread Spectrum modulation enabled
	S2G_OFF	3	r/w	Short to GND protection enable Bit 0 <sub>B</sub> , (default) Short to ground protection enabled 1 <sub>B</sub> , Short to ground protection disabled
	VFB_VIN_OFF	4	r/w	Vin Feedback Enable on VFB_VIN pin 0 <sub>B</sub> , (default) Enable Vin Feedback 1 <sub>B</sub> , Disable Vin Feedback
	CCM_4EVER	5	r/w	Forced Continuous Conduction Mode 0 <sub>B</sub> , (default) Forced CCM after soft start finish 1 <sub>B</sub> , Forced CCM even during soft start ramp up
	DCM_EN	6	r/w	Enable Bit to allow DCM regulation (MOSFET M4 control) 0 <sub>B</sub> , (default) DCM is disabled (M4 alternately switching), 1 <sub>B</sub> , DCM is enabled (M4 is permanently OFF)

**Serial Peripheral Interface (SPI)**

**Table 15 Register description (cont'd)**

Register name	Field	Bits	Type	Purpose
DVCCTRL	IDLE	0	r/w	<b>Device Control Register</b> IDLE mode configuration bit: 0 <sub>B</sub> , ACTIVE mode (default) 1 <sub>B</sub> , IDLE mode
	SWRST	1	r/w	Software reset bit: 0 <sub>B</sub> , (default) normal operation 1 <sub>B</sub> , execute reset command
	CLRLAT	2	r/w	Clear Latch bit: 0 <sub>B</sub> , (default) normal operation 1 <sub>B</sub> , execute CLRLAT command
	ENCAL	3	r/w	Enable automatic output current calibration bit: 0 <sub>B</sub> , (default) DAC takes CALIBVAL from SPI registers 1 <sub>B</sub> , DAC takes CALIBVAL from last completed automatic calibration procedure; SOCAL Bit can be set.
	SLOPE	5:4	r/w	slope compensation strenght: 00 <sub>B</sub> , (default) Nominal 01 <sub>B</sub> , +25% 10 <sub>B</sub> , -50% 11 <sub>B</sub> , -25%
	EA_GM	6	r/w	Increase the gain of the error amplifier, active only when output current is below 80% of target (i.e. < VFBH_FBL_EA): 0 <sub>B</sub> , (default) inactive 1 <sub>B</sub> , $IFBx_{gm}$ boosted to 1420μS
	EA_IOUT	7	r/w	Bit to decrease the saturation current of the error amplifier in current mode control loop: 0 <sub>B</sub> , (default) inactive 1 <sub>B</sub> , active: error amplifier saturation current reduced to 10uA

**Serial Peripheral Interface (SPI)**

**Table 15 Register description (cont'd)**

Register name	Field	Bits	Type	Purpose
MFSSETUP1	LEDCHAIN	3:0	r/w	<b>Multifloat Switch configuration Register</b> MFS ratio bits: set MFS jump ratio 0001 <sub>B</sub> , smallest Value 1 Step 0010 <sub>B</sub> , 2 Steps 1000 <sub>B</sub> , (default) 8 Steps 1111 <sub>B</sub> , 15 Steps 0000 <sub>B</sub> , largest Value 16 Steps
	EOMFS	4	r	End of MFS routine bit: 0 <sub>B</sub> , (default) MFS routine not completed, not successfully performed or never run. 1 <sub>B</sub> , MFS routine successfully performed (is reset to 0 <sub>B</sub> when SOMFS is set to 1 <sub>B</sub> ).
	SOMFS	5	r/w	Start of MFS routine bit: 0 <sub>B</sub> , (default) MFS routine not activated 1 <sub>B</sub> , MFS routine activated
	ILIM_HALF	6	r/w	Bit to decrease the Switch Current Limit ( $I_{SwLim}$ ) during F.D. operation: 0 <sub>B</sub> , (default) inactive $I_{SwLim} = 2/3$ of default value 1 <sub>B</sub> , $I_{SwLim}$ reduced to $1/2$ of default value
	EA_IOUT_MFS	7	r/w	Bit to decrease the saturation current of the error amplifier (A6) in current mode control loop only during MFS routine: 0 <sub>B</sub> , (default) inactive 1 <sub>B</sub> , active: error amplifier current reduced to 20%
MFSSETUP2	MFSDLY	7:0	r/w	<b>Multifloat switch configuration register 2 (delay time programming)</b> 00000000 <sub>B</sub> , smallest delay time in respect to $f_{SW}$ 11111111 <sub>B</sub> , largest delay time in respect to $f_{SW}$ 10000000 <sub>B</sub> , (default) delay time in respect to $f_{SW}$

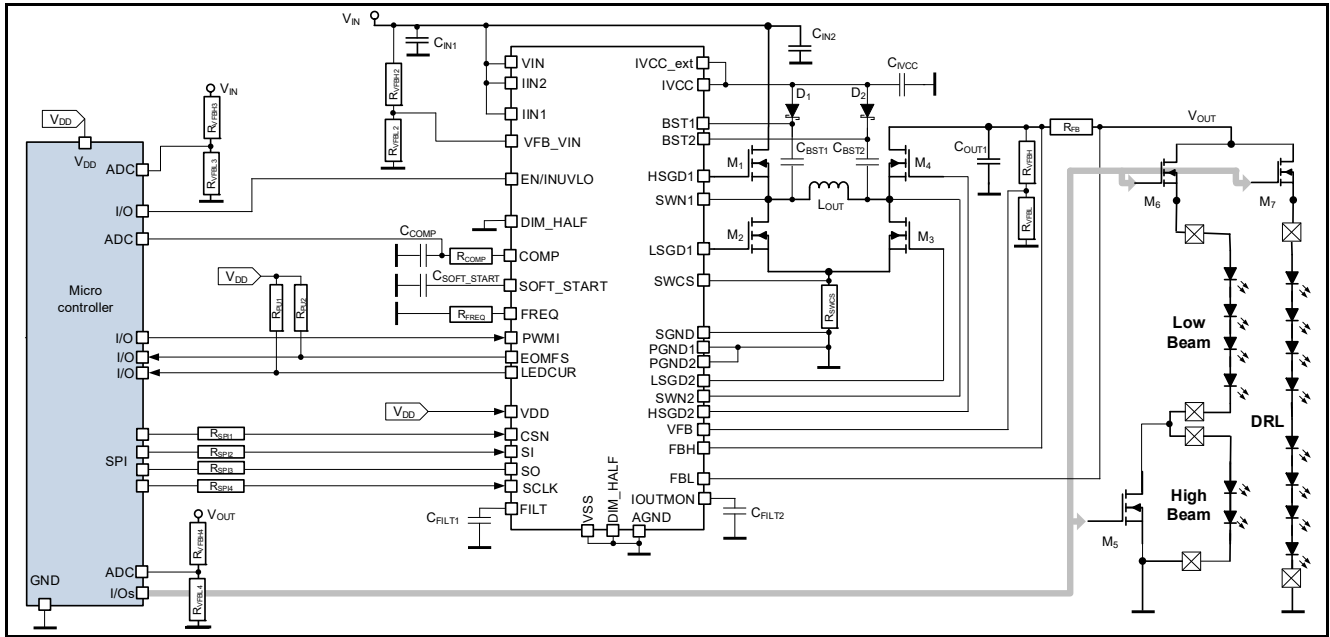
**Serial Peripheral Interface (SPI)**

**Table 15 Register description (cont'd)**

Register name	Field	Bits	Type	Purpose
CURRMON	LEDCURR	1:0	r	<b>Current Monitor Register</b> Status of the LED Current bits: 00 <sub>B</sub> , (default) LED current between Target and +25% 01 <sub>B</sub> , LED current above +25% of Target 10 <sub>B</sub> , LED current between Target and -25% 11 <sub>B</sub> , LED current below -25% of Target
	INCURR	3:2	r	Status of the Input Current bits: 00 <sub>B</sub> , (default) Input current between 75% and 90% of Limit 01 <sub>B</sub> , Input current between 90% and the Limit 10 <sub>B</sub> , Input current between 60% and 75% of Limit 11 <sub>B</sub> , Input current below 60% of Limit
	EOMON	4	r	End of LED/Input Current Monitoring bit: 0 <sub>B</sub> , (default) Current monitoring routine not completed, not successfully performed or never run. 1 <sub>B</sub> , Current Monitor routine successfully performed (is reset to 0 <sub>B</sub> when SOMON is set to 1 <sub>B</sub> )
	SOMON	5	r/w	Start of LED/Input Current Monitoring bit: 0 <sub>B</sub> , (default) Current monitor routine not started 1 <sub>B</sub> , Start of the current monitor routine
REGUSETMON	REGUMODFB	3:2	r	<b>Regulation Setup And Monitor Register</b> Feedback of Regulation Mode bits: 01 <sub>B</sub> , (default) Buck 10 <sub>B</sub> , Boost 11 <sub>B</sub> , Buck-Boost
	BB_BST_CMP	1 : 0	r/w	Buck boost to Boost transition compensation level: 00 <sub>B</sub> , (default) Min compensation: useful when low switching frequencies are selected 01 <sub>B</sub> , Low compensation: I.E. adopted @ $f_{SW}=250\text{kHz}$ 10 <sub>B</sub> , Mid compensation: I.E. adopted @ $f_{SW}=400\text{kHz}$ 11 <sub>B</sub> , Max compensation: useful when high switching frequencies are selected I.E. @ $f_{SW}=500\text{kHz}$
MUXCTRL	SO_MUX_SEL	5:0	r/w	<b>Internal Muxes Configuration Register</b> Digital Multiplexer selector, output on SO pin: 000000 <sub>B</sub> , (default) SO pin configured as normal SPI output 000100 <sub>B</sub> , as default with in addition internal oscillator clock available when CS_N is high
	AMUX_EN	6	r/w	Analog Mux enable, output on FILT pin: 0 <sub>B</sub> , (default) Analog Mux disabled 1 <sub>B</sub> , Analog Mux enabled
	MFS_REF	7	r/w	MFS reference to FILT pin Path Enable: 0 <sub>B</sub> , (default) path disabled 1 <sub>B</sub> , Path Enabled

## 13 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 44 Application Drawing - TLD5542-1 on a 3 functions LED Driver Module**

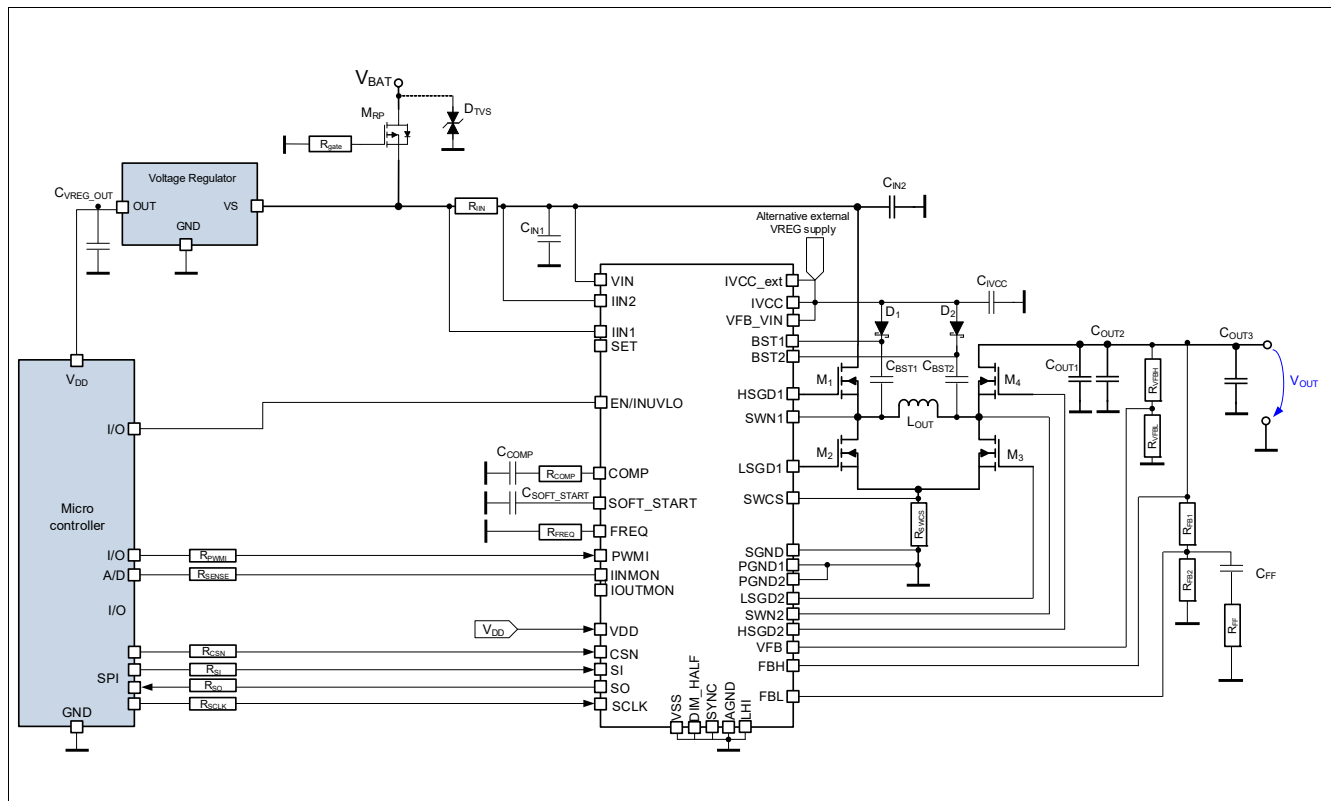
**Table 16 BOM - TLD5542-1 as current regulator ( $I_{OUT} = 1\text{ A}$ ,  $f_{SW} = 300\text{ kHz}$ )**

Reference Designator	Value	Manufacturer	Part Number	Type
$D_1, D_2$	BAT46WJ	--	BAT46WJ	Diode
$C_{IN1}$	10 $\mu\text{F}$ , 50 V	TDK	X7R	Capacitor
$C_{IN2}$	4.7 $\mu\text{F}$ , 50 V	TDK	X7R	Capacitor
$C_{FILT1,2}$	220 pF, 10 V	TDK	X7R	Capacitor
$C_{COMP}$	15 nF, 16 V	TDK	X7R	Capacitor
$C_{SOFT\_START}$	15 nF, 16 V	TDK	X7R	Capacitor
$C_{OUT1}$	3x3.3 $\mu\text{F}$ , 100 V	TDK	X7R	Capacitor
$C_{IVCC}$	10 $\mu\text{F}$ , 16 V	TDK	X7R	Capacitor
$C_{BST1}, C_{BST2}$	100 nF, 16 V	TDK	X7R	Capacitor
$IC_1$	--	Infineon	TLD5542-1	IC
$L_{OUT}$	10 $\mu\text{H}$	TDK	SPM10065VT-100M	Inductor
$R_{FB}$	0.100 $\Omega$ , 1%	Panasonic	--	Resistor
$R_1, R_2, R_3, R_{PD}, R_{EN}, R_{PWM1}, R_{SENSE1}, R_{SENSE2}, R_{SYNC}, R_{SCLK}, R_{SI}, R_{SO}, R_{CSN}$	xx k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{VFBL}, R_{VFBH}$	1k $\Omega$ , 51k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{VFBL2}, R_{VFBH2}$	1k $\Omega$ , 51k $\Omega$ , 1%	Panasonic	--	Resistor

**Application Information**

**Table 16 BOM - TLD5542-1 as current regulator ( $I_{OUT} = 1\text{ A}$ ,  $f_{SW} = 300\text{ kHz}$ )**

Reference Designator	Value	Manufacturer	Part Number	Type
$R_{COMP}$	1k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{FREQ}$	24 k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{SWCS}$	0.007 $\Omega$ , 1%	Panasonic	ERJB1CFR05U	Resistor
$M_1, M_2, M_3, M_4, M_5, M_6, M_7$	Dual MOSFET: 60V / 26 m $\Omega$ N-ch	Infineon	IPG20N10S4L-26	Transistor



**Figure 45 Application Drawing - TLD5542-1 as adjustable voltage regulator**

**Table 17 BOM - TLD5542-1 as voltage regulator**

Reference Designator	Value	Manufacturer	Part Number	Type
$D_1, D_2$	BAT46WJ	--	BAT46WJ	Diode
$C_{IN1}$	1 $\mu\text{F}$ , 100 V	TDK	X7R	Capacitor
$C_{IN2}$	4.7 $\mu\text{F}$ , 100 V	TDK	X7R	Capacitor
$C_{COMP}$	22 nF, 16 V	TDK	X7R	Capacitor
$C_{FF}$	10 nF, 50 V	TDK	X7R	Capacitor
$C_{SOFT\_START}$	22 nF, 16 V	TDK	X7R	Capacitor
$C_{OUT1}$	3x4.7 $\mu\text{F}$ , 100 V	TDK	X7R	Capacitor
$C_{OUT2}, C_{OUT3}$	100 nF, 100 V	TDK	X7R	Capacitor
$C_{IVCC}$	10 $\mu\text{F}$ , 16 V	TDK	X7R	Capacitor
$C_{BST1}, C_{BST2}$	100 nF, 16 V	TDK	X7R	Capacitor
$I/C_1$	--	Infineon	TLD5542-1	IC



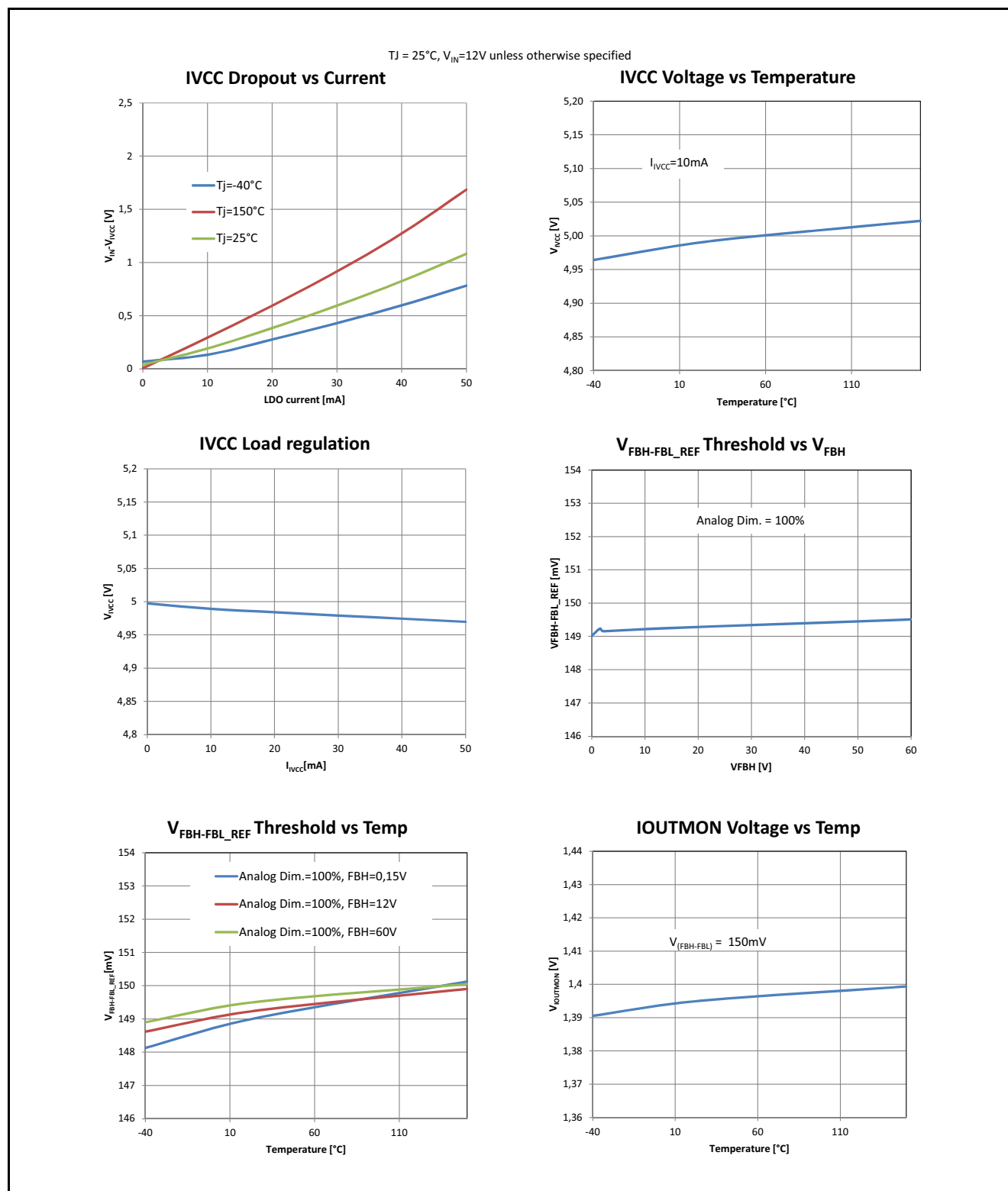
**Application Information**

**Table 17 BOM - TLD5542-1 as voltage regulator**

Reference Designator	Value	Manufacturer	Part Number	Type
$L_{OUT}$	10 $\mu$ H	Coilcraft	XAL1010-103MEC	Inductor
$R_{FF}$	1.5 k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{FB1}$ , $R_{FB2}$	150 $\Omega$ , 20.5k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{IN}$	0.005 $\Omega$ , 1%	Panasonic	--	Resistor
$R_{PWM1}$ , $R_{Sense1}$ , $R_{Sense2}$ , $R_{SYNC}$ , $R_{SCLK}$ , $R_{SI}$ , $R_{SO}$ , $R_{CSN}$	xx k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{VFBL}$ , $R_{VFBH}$	1.5 k $\Omega$ , 24 k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{COMP}$	0 $\Omega$ , 1%	Panasonic	--	Resistor
$R_{FREQ}$	37.4 k $\Omega$ , 1%	Panasonic	--	Resistor
$R_{SWCS}$	0.007 $\Omega$ , 2%	--	--	Resistor
$M_1$ , $M_2$ , $M_3$ , $M_4$	Dual MOSFET: 100 V / 35 m $\Omega$ N-ch	Infineon	IPG20N10S4L-35	Transistor

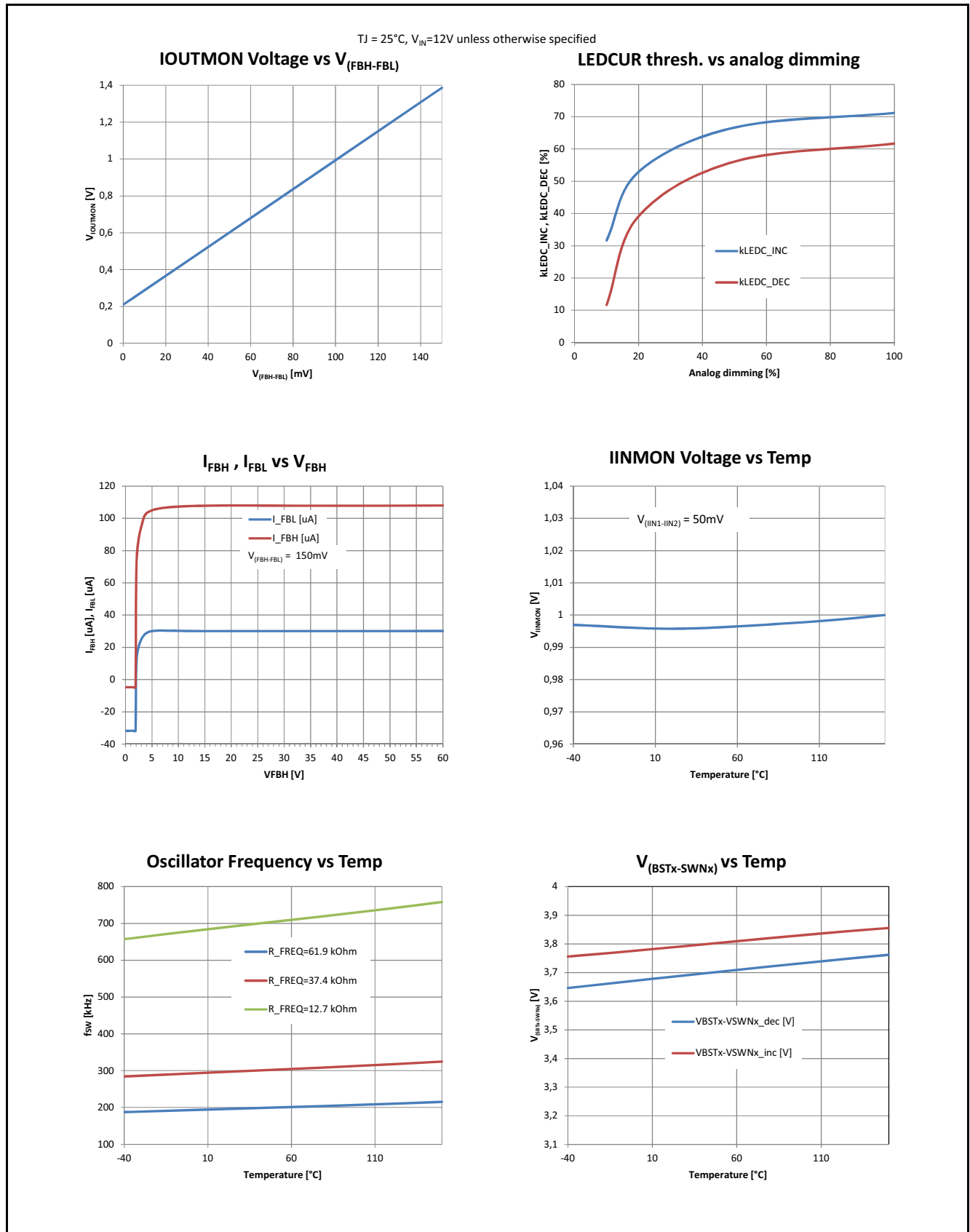
## 13.1 Further Application Information

### Typical Performance Characteristics of Device



**Figure 46 Characterization Diagrams 1**

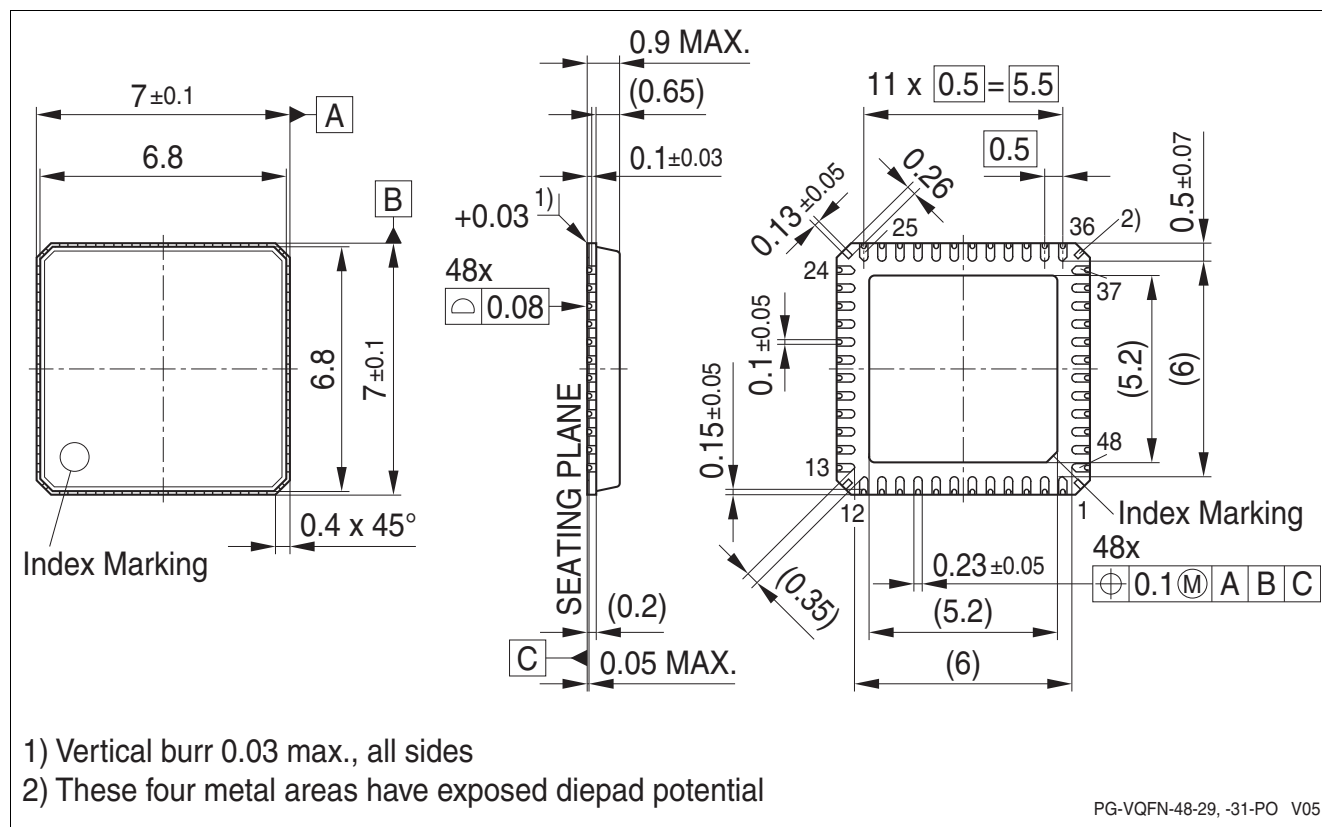
**Application Information**



**Figure 47 Characterization Diagrams 2**

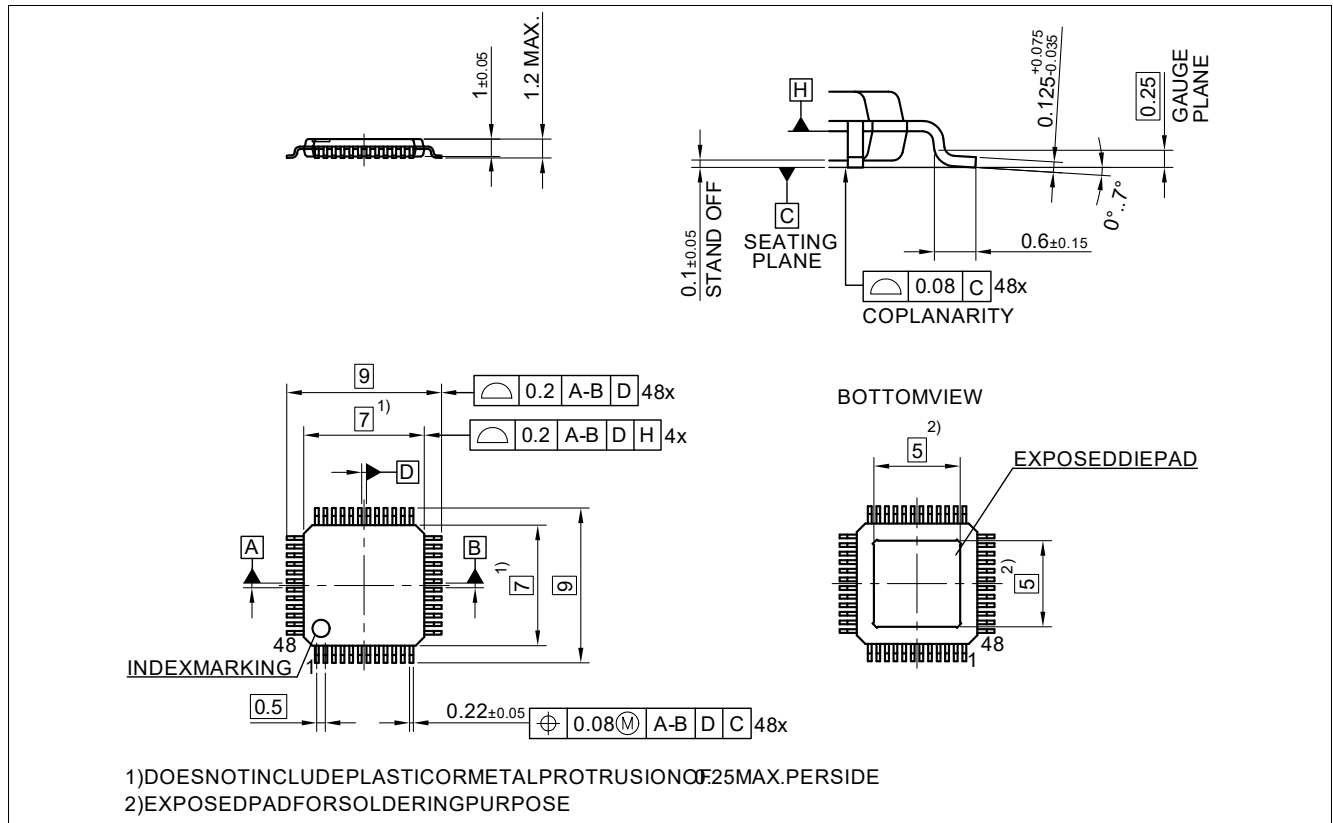
- For further information you may contact <http://www.infineon.com/>

## 14 Package Outlines



**Figure 48 PG-VQFN-48 (with LTI)**

**Package Outlines**



**Figure 49 PG-TQFP-48**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Revision History**

## **15 Revision History**

**Table 18 Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
Rev. 1.0	2019-11-21	Released datasheet
Rev. 1.10	2019-12-11	changed ESD in to “CDM” AECQ100-011 including revision : Rev. D
Rev. 1.10	2019-12-11	Updated Vout Overvoltage description <a href="#">Chapter 10.2</a>

## Table of Content

<b>1</b>	<b>Overview</b>	<b>1</b>
<b>2</b>	<b>Block Diagram</b>	<b>3</b>
<b>3</b>	<b>Pin Configuration</b>	<b>4</b>
3.1	Pin Assignment	4
3.2	Pin Definitions and Functions	5
<b>4</b>	<b>General Product Characteristics</b>	<b>8</b>
4.1	Absolute Maximum Ratings	8
4.2	Functional Range	10
4.3	Thermal Resistance	11
<b>5</b>	<b>Power Supply</b>	<b>12</b>
5.1	Different Power States	14
5.2	Different Possibilities to RESET the device	15
5.3	Electrical Characteristics	16
<b>6</b>	<b>Regulator Description</b>	<b>18</b>
6.1	Regulator Diagram Description	18
6.2	Adjustable Soft Start Ramp	20
6.3	Switching Frequency setup	21
6.4	Operation of 4 switches H-Bridge architecture	22
6.4.1	Boost mode ( $V_{IN} < V_{OUT}$ )	22
6.4.2	Buck mode ( $V_{IN} > V_{OUT}$ )	23
6.4.3	Buck-Boost mode ( $V_{IN} \sim V_{OUT}$ )	24
6.5	Fast Output Discharge Operation Mode - Multi Floating Switches Topology	25
6.6	Programming Output Voltage (Constant Voltage Regulation)	30
6.7	Electrical Characteristics	31
<b>7</b>	<b>Digital Dimming Function</b>	<b>34</b>
7.1	Description	34
7.2	Electrical Characteristics	36
<b>8</b>	<b>Analog Dimming and Limp Home</b>	<b>37</b>
8.1	Description	37
8.2	LED current calibration procedure	38
8.3	Electrical Characteristics	40
<b>9</b>	<b>Linear Regulator</b>	<b>41</b>
9.1	IVCC Description	41
9.2	Electrical Characteristics	42
<b>10</b>	<b>Protection and Diagnostic Functions</b>	<b>43</b>
10.1	Description	43
10.2	Output Overvoltage, Short circuit protection	44
10.2.1	Short Circuit protection	44
10.2.2	Overvoltage Protection	45
10.3	Input voltage monitoring, protection	45
10.4	Input current Monitoring	45
10.5	Output current Monitoring	46
10.6	Device Temperature Monitoring	48
10.7	Electrical Characteristics	49
<b>11</b>	<b>Infineon FLAT SPECTRUM Feature set</b>	<b>50</b>

11.1	Description .....	50
11.2	Synchronization Function .....	50
11.3	Spread Spectrum .....	51
11.4	EMC optimized schematic .....	52
11.5	Electrical Characteristics .....	53
<b>12</b>	<b>Serial Peripheral Interface (SPI) .....</b>	<b>54</b>
12.1	SPI Signal Description .....	54
12.2	Daisy Chain Capability .....	55
12.3	Timing Diagrams .....	57
12.4	Electrical Characteristics .....	58
12.5	SPI Protocol .....	60
12.6	SPI Registers Overview .....	62
12.6.1	Standard Diagnosis .....	62
12.6.2	Register structure .....	65
<b>13</b>	<b>Application Information .....</b>	<b>71</b>
13.1	Further Application Information .....	74
<b>14</b>	<b>Package Outlines .....</b>	<b>76</b>
<b>15</b>	<b>Revision History .....</b>	<b>78</b>
	<b>Table of Content .....</b>	<b>79</b>



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