Lite SBC Family

User’s Guide

About this document

The intention of this User's Guide is to provide relevant design-in information for automotive applications with the Infineon Lite SBC family. The document is complementary to the datasheet.

Scope and purpose

This User’s Guide covers the following products of the Lite SBC device family (with/without CAN Partial Networking, with 5 V or 3.3 V, LDO or SMPS main supply output):

- TLE9461ES
- TLE9461ESV33
- TLE9461-3ES
- TLE9461-3ESV33
- TLE9471ES
- TLE9471ESV33
- TLE9471-3ES
- TLE9471-3ESV33

Intended audience

This document is aimed at hardware engineers integrating devices of the Lite SBC family into their applications.

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1 Hardware configuration

1.1 Introduction and initial setup

The Lite SBC device behavior in reaction to a watchdog trigger failure and/or a main supply (VCC1) overvoltage can be initially configured depending on the specific requirements of the application.

This individual configuration is selected by setting the voltage level at the INT pin (CFPG) during the power-on phase in combination with setting the SPI bit CFG in the HW_CTRL register. Combining these two bits, four configurations (for each failure event) are available.

Connecting an external pull-up resistor between INT and VCC1 ensures a logic High level of CFGP. If the pin is left floating, an internal pull-down resistor automatically ensures a logic Low level.

The configuration chosen is stored for all conditions, and can be changed only by powering down ($V_S < V_{POR,f}$) and restarting the device again.

Table 1 Response on watchdog trigger

Configuration	CFGP logic level	CFG logic level	SBC Mode activated	Failure event	FO activation
1	1	1	Restart Mode	watchdog trigger	after 1st WD trigger
2	0	1	Fail-Safe Mode	watchdog trigger	after 1st WD trigger
3	1	0	Restart Mode	watchdog trigger	after 2nd WD trigger
4	0	0	Fail-Safe Mode	watchdog trigger	after 2nd WD trigger

See also ***Chapter 1.3.2*** on page 13.

Table 2 Response on VCC1 overvoltage

Configuration	CFGP logic level	CFG logic level	SBC Mode activated	Failure event	FO activation
1	1	1	Restart Mode	VCC1 overvoltage	yes
2	0	1	Fail-Safe Mode	VCC1 overvoltage	yes
3	1	0	Restart Mode	VCC1 overvoltage	yes
4	0	0	Fail-Safe Mode	VCC1 overvoltage	yes

See also ***Chapter 1.3.3*** on page 15.

1.2 Pin structures

Table 3 Pin overview

Pin	Symbol	Input / output structure
1	VCAN	Power supply for internal CAN cell
2	TXDCAN	CAN transmitter output line
3	RXDCAN	CAN receiver input line
4	CLK	SPI clock input
5	SDI	SPI data input (MOSI)
6	SDO	SPI data output (MISO)
7	CSN	SPI chip select, active Low
8	INTN	Interrupt, active Low
9	RSTN	Reset, active Low
10	TEST	Connect to VCC1 to enter SBC Development Mode, connect to ground for typical operation
11	GND	Power ground VCC1, connect on PCB with common GND and Exposed Pad
12	VIO	Power supply for digital I/O, must be connected to VCC1
13	VCC1	Main power supply output
14	NC	Internally not connected; leave floating or connected to GND plane
15	VS	Main supply voltage, pins must be connected together
16	VS	Main supply voltage, pins must be connected together
17	VCP	Charge pump output: drives gate of external n-channel HS-MOSFET, use 1kΩ serial resistor for protection
18	WK/SENSE	Wake input; Sense input: Alternative function as input for HV measurement function
19	FO/GPIO	Fail output: open drain, active Low, default setting; GPIO: Alternative function configurable as WK, HS/LS driver; Sense output: Alternative function as output for HV measurement function
20	VCC2	Secondary power supply output
21	GND	Power ground VCC2, connect on PCB with common GND and Exposed Pad
22	GND	CAN ground pin
23	CANH	CAN high line bus
24	CANL	CAN low line bus
	Exposed Pad	Must be connected with GND pins and common GND

1.3 Response on system failures

1.3.1 Loss of system GND

A loss of the electronic control unit's (ECU) ground connection is a state-of-the-art test in automotive applications. It is important to know and to understand the behavior of the system for such case, specifically the System Basis Chip (SBC). Different scenarios are possible and considered for such loss of module ground:

It is important to know and to understand the behavior of the ECU in this case, specifically the SBC.

Certain scenarios are possible for a loss-of-GND of the module:

- Loss of ECU module ground and no connections to external ground, see ***Chapter 1.3.1.1*** on page 6
- Loss of ECU module ground and connections to external ground via external ESD diode, see ***Chapter 1.3.1.2*** on page 7
- Loss of ECU module ground and connections to external ground via internal ESD diode, see ***Chapter 1.3.1.3*** on page 8
- Loss of ECU module ground and short circuit at High-side switches, see ***Chapter 1.3.1.4*** on page 9

1.3.1.1 Scenario 1: Loss of module GND and no connections to external GND

Behavior description:

- All individual SBC ground pins are connected on the module PCB.
- No external ground connection is present (e.g. all loads are on the ECU board).
- A loss of module ground creates a floating GND structure (floats towards VS level).
- If the voltage difference across VS and GND disappears, the SBC becomes disabled (no unintended current, no activity).

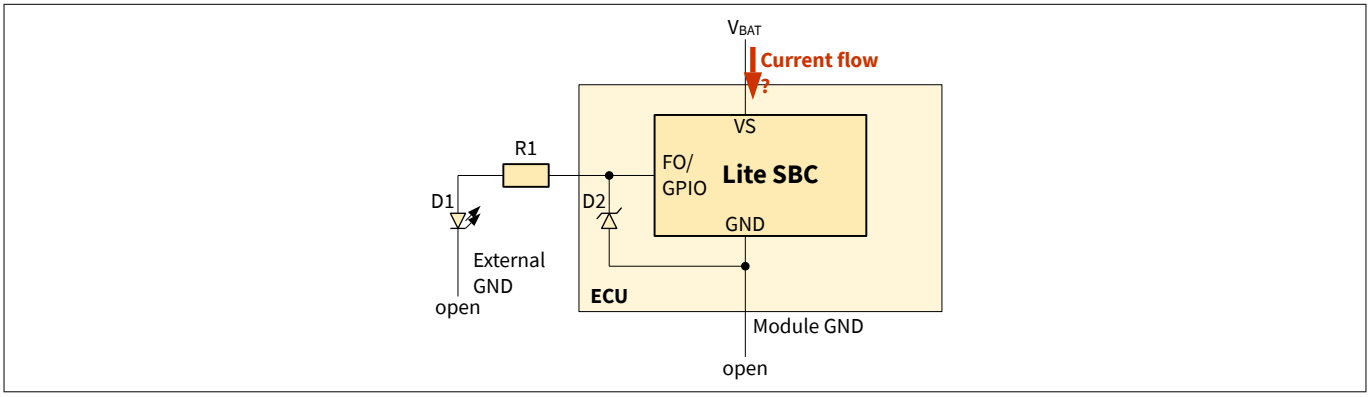

Figure 1 Scenario 1: Loss of module GND, no connections to external GND

1.3.1.2 Scenario 2: Loss of module GND and connection to external GND via external ESD diode

Behavior description:

- All individual SBC ground pins are connected on the module PCB.
- An external load (with ground connection) can provide a current path from V_{BAT} through the SBC and an ESD structure into external ground (see figure below).
- Other scenarios with similar configurations are possible.
- A current can flow even if ground of the module got lost.
- These load current(s) might exceed the current capability of the ESD structures, and therewith be destructive within the ECU.
- The SBC operates as long as V_S is above $V_{POR,f}$.

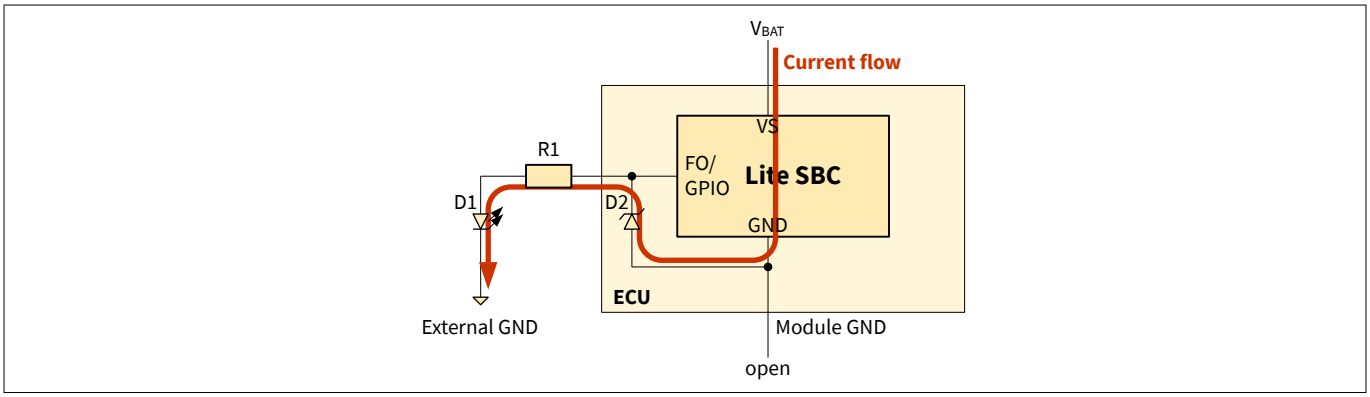

Figure 2 Scenario 2: Loss of module GND, connections to external GND, external ESD diode

1.3.1.3 Scenario 3: Loss of module GND and connection to external GND via internal ESD diode

Behavior description:

- All individual SBC ground pins are connected on the module PCB.
- Since ground of the module is lost, the GND structure is floating towards VS level.
- The ESD protection diode of the pin that is shorted to external ground is forward biased as soon as the GND structure is biased sufficiently above ground level (ESD diode forward voltage).
- The SBC still works, though the whole current is now flowing through the ESD diode into external ground.
- Since the ESD structures are not made for larger and permanent currents, lifetime decreases and destruction might happen.

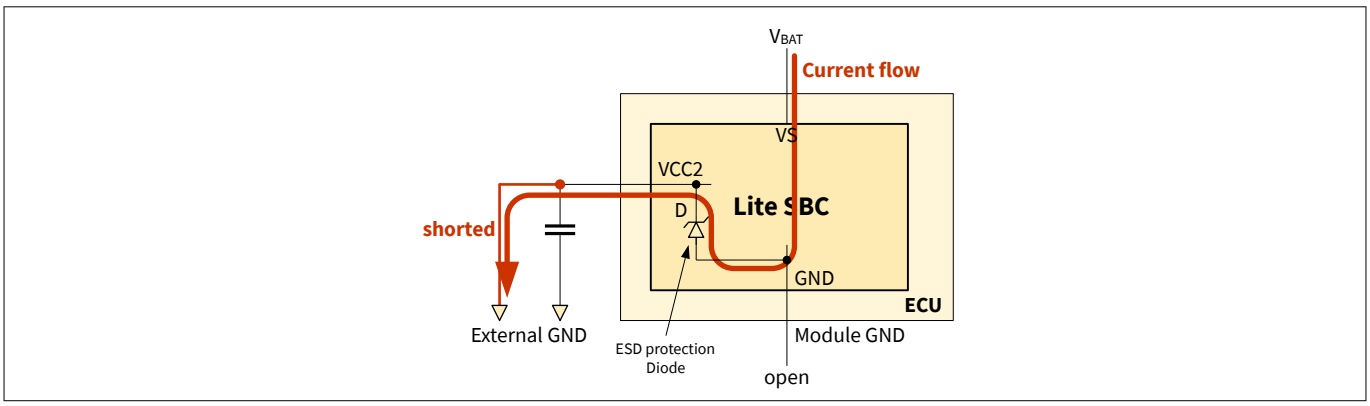

Figure 3 Scenario 3: Loss of module GND, connections to external GND, internal ESD diode

1.3.1.4 Short-circuit scenarios at the High-Side output (FO/GPIO)

The following scenarios are analyzed in this section (with KL30 = VBAT and KL31= GND connection):

- KL30 connected, KL31 NOT connected, short circuit of HS output to V_{BAT}, see ***Chapter 1.3.1.4.1***
- KL30 connected, KL31 NOT connected, short circuit of HS output to GND, see ***Chapter 1.3.1.4.2***
- KL30 NOT connected, KL31 connected, short circuit of HS output to V_{BAT}, see ***Chapter 1.3.1.4.3***
- KL30 NOT connected, KL31 connected, short circuit of HS output to GND, see ***Chapter 1.3.1.4.4***

Note: In case all ground connections are present, the device shuts down completely, and no unintended current flows.

1.3.1.4.1 Scenario 1: KL30 connected, KL31 open, short circuit of HS output to V_{BAT}

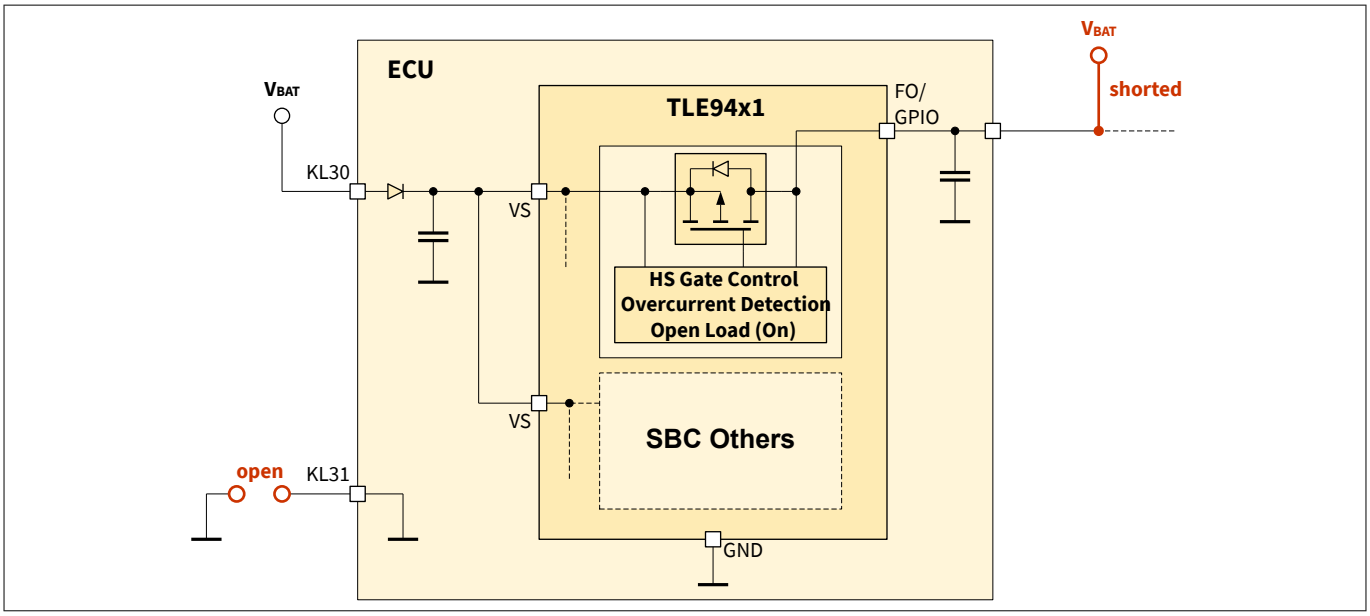

Figure 4 Simplified circuitry for scenario 1

Description of the device behavior:

- The device stays enabled and functional as long as the voltage across VS and the floating GND structure is sufficient.
- The specification might be violated.
- This behavior is true as long as:
  - Loads don't establish a path to external ground (see ***Figure 3*** on page 8).
  - $V_{BAT} > V_{BATHS}$ (reverse current path).

1.3.1.4.2 Scenario 2: KL30 connected, KL31 open, short circuit of HS output to GND

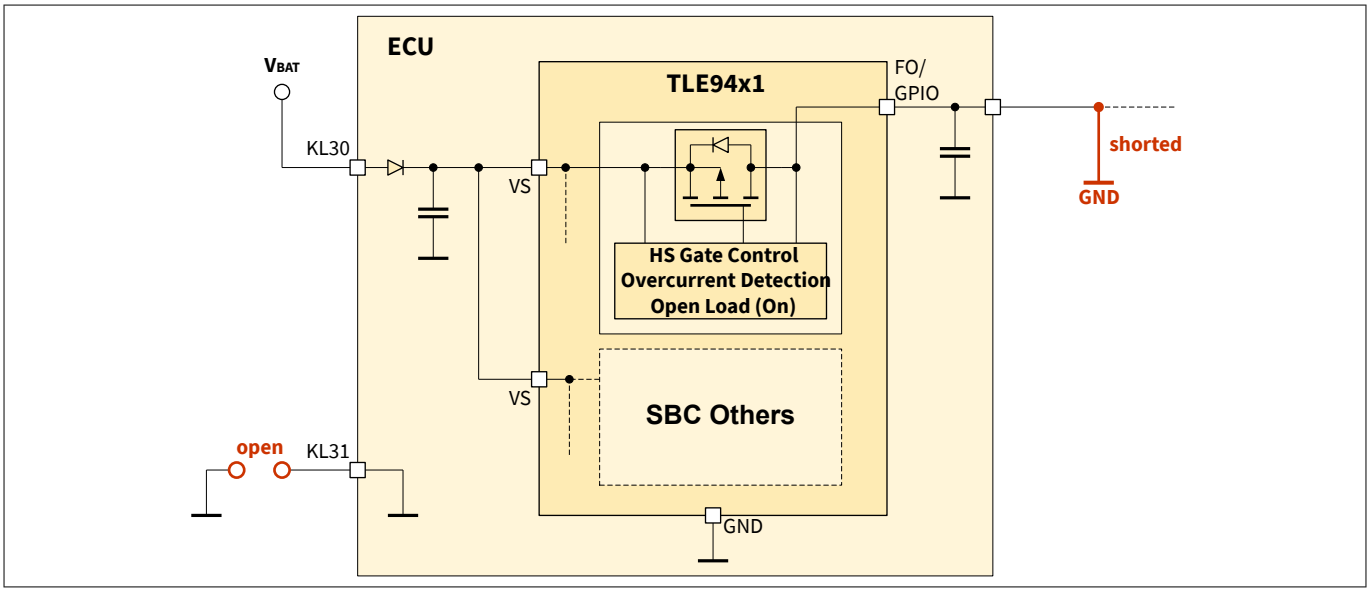

Figure 5 Simplified circuitry for scenario 2

Description of the device behavior:

- Since ground is floating, on-board ESD diodes of the ECU might become forward biased.
- If the respective pin is loaded or shorted to GND, a current from VBAT passes the diode flowing through the short into external ground.
- Since this current is not specifically limited, it might exceed the current capability of the ESD structure and be destructive.
- The SBC may operate as long as V_S is above $V_{POR,f}$.

1.3.1.4.3 Scenario 3: KL30 open, KL31 connected, short circuit of HS output to V_{BAT}

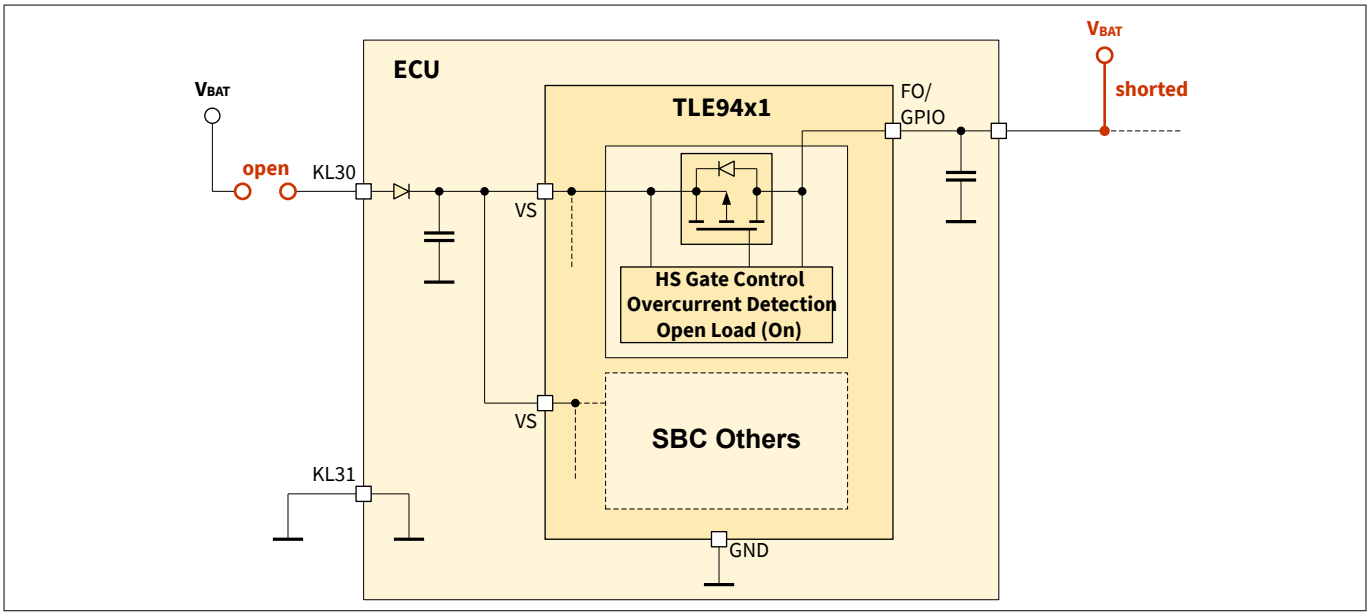

Figure 6 Simplified circuitry for scenario 3

Description of the device behavior:

- SBC is disabled, since KL30 is open (no supply).
- A reverse current can flow from the High-Side pin, shorted to V_{BAT}, once the floating supply structure is sufficiently lower than V_{BAT} to (forward) bias the body diode of the High-Side switch.
- Different scenarios are possible for the current to find its way to GND.
- The reverse current can be limited or even prevented by using an (external) series resistor or a reverse biased diode, respectively.

1.3.1.4.4 Scenario 4: KL30 open, KL31 connected, short circuit of HS output to GND

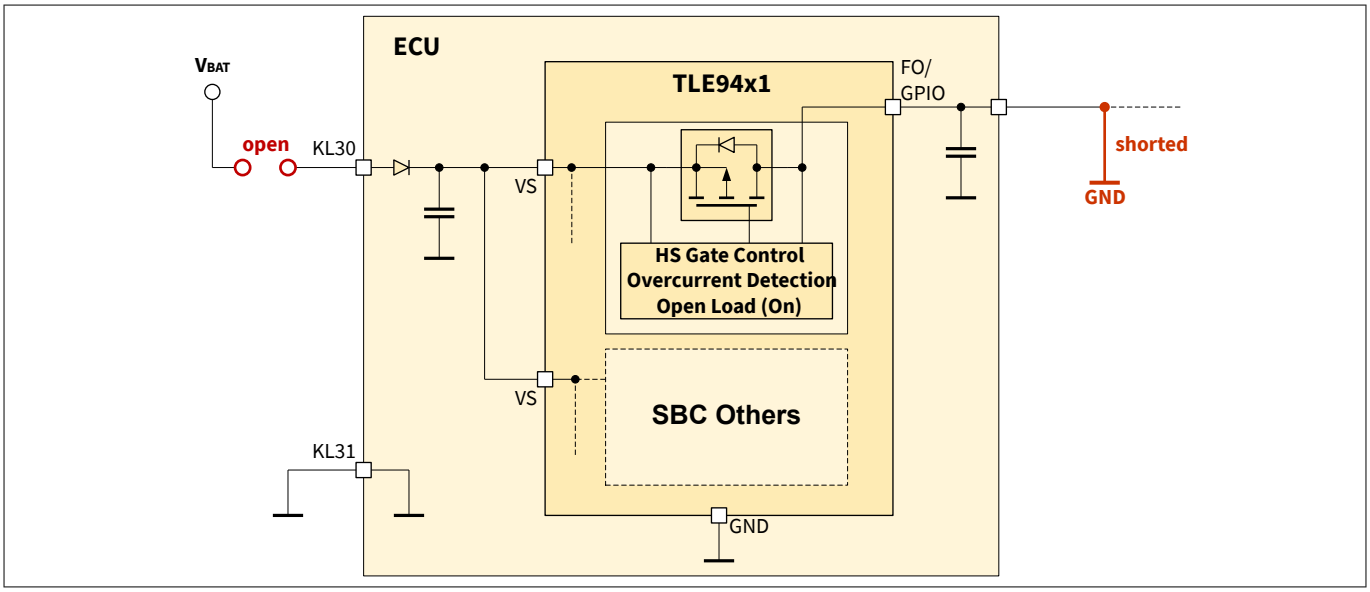

Figure 7 Simplified circuitry for scenario 4

Description of the device behavior:

- SBC is disabled, since KL30 is open (no supply).
- No reverse current as long as common GND potential is ensured.

1.3.1.4.5 Conclusion

In general, a combination of loss of the ECU's module ground and any output short circuit is considered to be a double failure, and therefore not covered by the SBC by default.

Depending on the specific failure case, the SBC can be biased to undesirable behavior. This may lead, in the worst case, to the destruction of external components or (more unlikely) the device itself.

A case by case analysis of the actual application is required to determine:

- The specific device behavior.
- Whether and how external components can protect the device and the application.

1.3.2 Watchdog trigger failure

The four different configurations (depending on the CFPG and CFG bit settings) are described in ***Table 1*** on page 4. A watchdog trigger failure leads to either an SBC Restart of Fail-Safe Mode entry (after the first or after the second trigger failure). The Failure Output (FO/GPIO) is activated respectively if configured as fail output.

The specific behavior is illustrated in the following timing diagrams.

1.3.2.1 Watchdog trigger failure (CFG_STATE=1, CFG=1), Config1

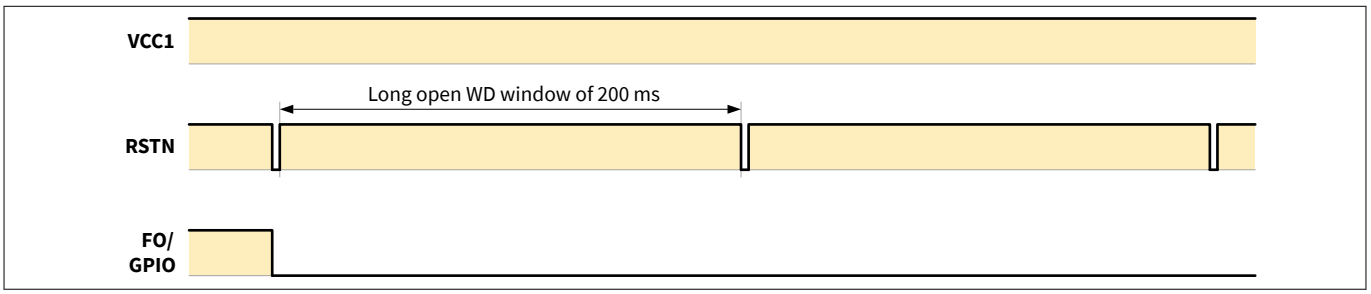

Figure 8 SBC Restart Mode entry and FOx activation after 1st WD trigger failure

1.3.2.2 Watchdog trigger failure (CFG_STATE=0, CFG=1), Config2

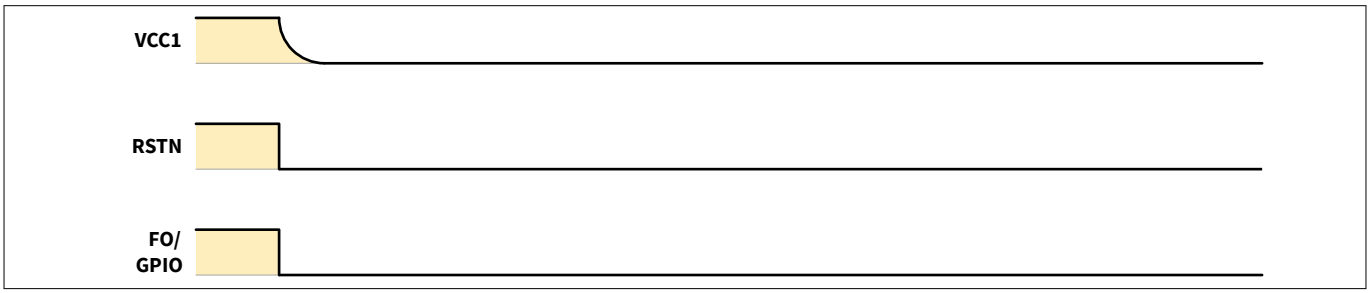

Figure 9 SBC Fail-Safe Mode entry and FOx activation after 1st WD trigger failure

1.3.2.3 Watchdog trigger failure (CFG_STATE=1, CFG=0), Config3

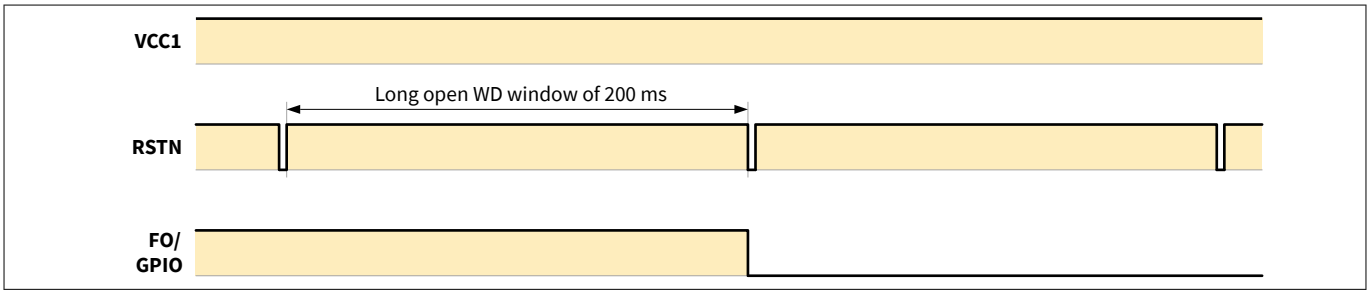

Figure 10 SBC Restart Mode entry due to WD failure and FO activation after 2nd WD trigger failure

1.3.2.4 Watchdog trigger failure (CFG_STATE=0, CFG=0), Config4

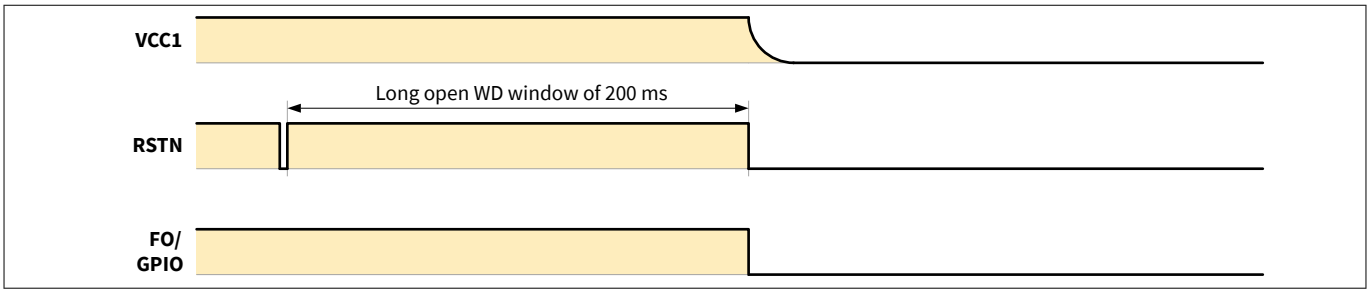

Figure 11 SBC Fail-Safe Mode entry and FOx activation after 2nd WD trigger failure

1.3.3 Behavior in case of VCC1 overvoltage

The behavior in case of VCC1 overvoltage differs from the response on watchdog trigger failure (see ***Table 2*** on page 4).

Strategy of VCC1 overvoltage signalization:

- Level 1: SPI flag (VCC1_OV) activation only.
- Level 2: SPI flag (VCC1_OV) + Restart Mode entry (FO activation).
- Level 3: SPI flag (VCC1_OV) + SBC Fail-Safe Mode entry (FO activation).

Additional selection via SPI bit VCC1_OV_RST in register M_S_CTRL (default value after POR/Soft Reset/ Restart = 0):

- If VCC1_OV_RST = 0 (default), a VCC1 overvoltage condition is only flagged with the SPI status bit VCC1_OV (SUP_STAT_2).
- If VCC1_OV_RST = 1, a VCC1 overvoltage condition sets the VCC1_OV bit and in addition, depending on the hardware configuration, below listed action is triggered:
  - If CFG0_STATE = 1, the SBC Restart Mode is entered in case of VCC1_OV.
    The fail output (FO/GPIO) is activated if configured as fail output. VCC1_OV_RST is cleared when the SBC enters the Restart Mode.
  - If CFG0_STATE = 0, the SBC Fail-Safe Mode is entered in case of VCC1_OV.
    The fail output (FO/GPIO) is activated if configured as fail output. A wake event is needed to exit the SBC Fail-Safe Mode. VCC1_OV_RST is cleared when the SBC enters the Restart Mode.

1.3.3.1 VCC1 overvoltage (CFG0_STATE=1, CFG=0/1), Config1/3

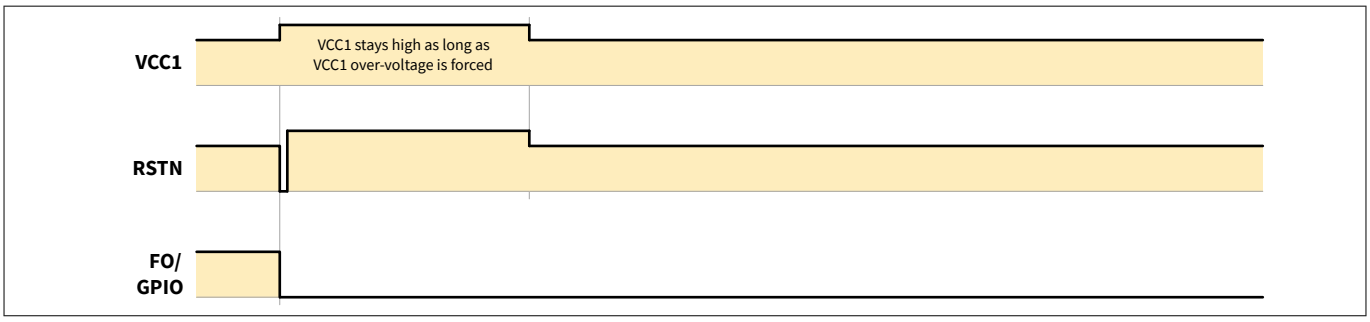

Figure 12 SBC Restart Mode entry due to VCC1 overvoltage

1.3.3.2 VCC1 overvoltage (CFG0_STATE=0, CFG=0/1), Config2/4

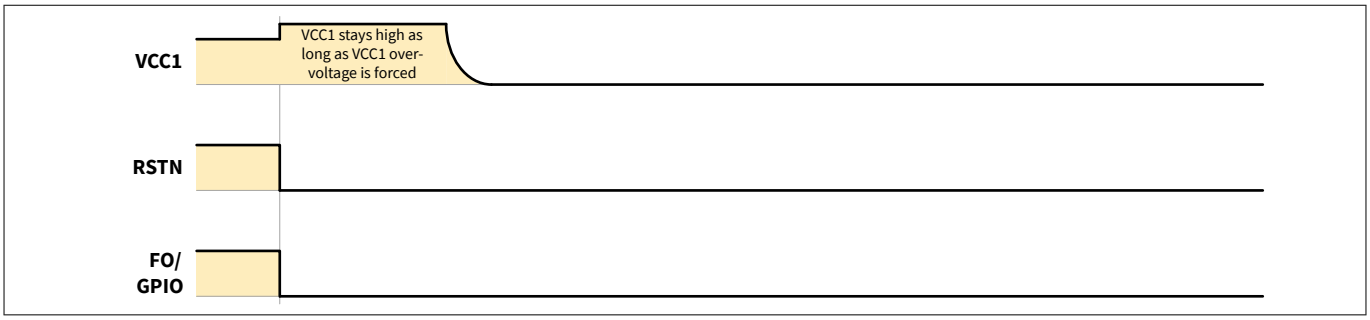

Figure 13 Fail-Safe mode entry due to VCC1 OV

1.3.3.3 VCC1 overvoltage and CFG=0 configuration

If the device has been triggered by a VCC1 overvoltage event in the CFG=0 configuration, it exits the SBC Restart Mode after a delay time, t_{RD1}, of typ. 10 ms. This time can be reduced to typ. 2 ms (t_{RD2}).

At the same time, VCC1_OV_RST is automatically cleared. The device stays in SBC Normal Mode, even if the overvoltage condition is still present. Though, the VCC1_OV bit remains set and must be cleared actively.

The SBC enters the Restart Mode again, only if the VCC1_OV_RST bit is set again.

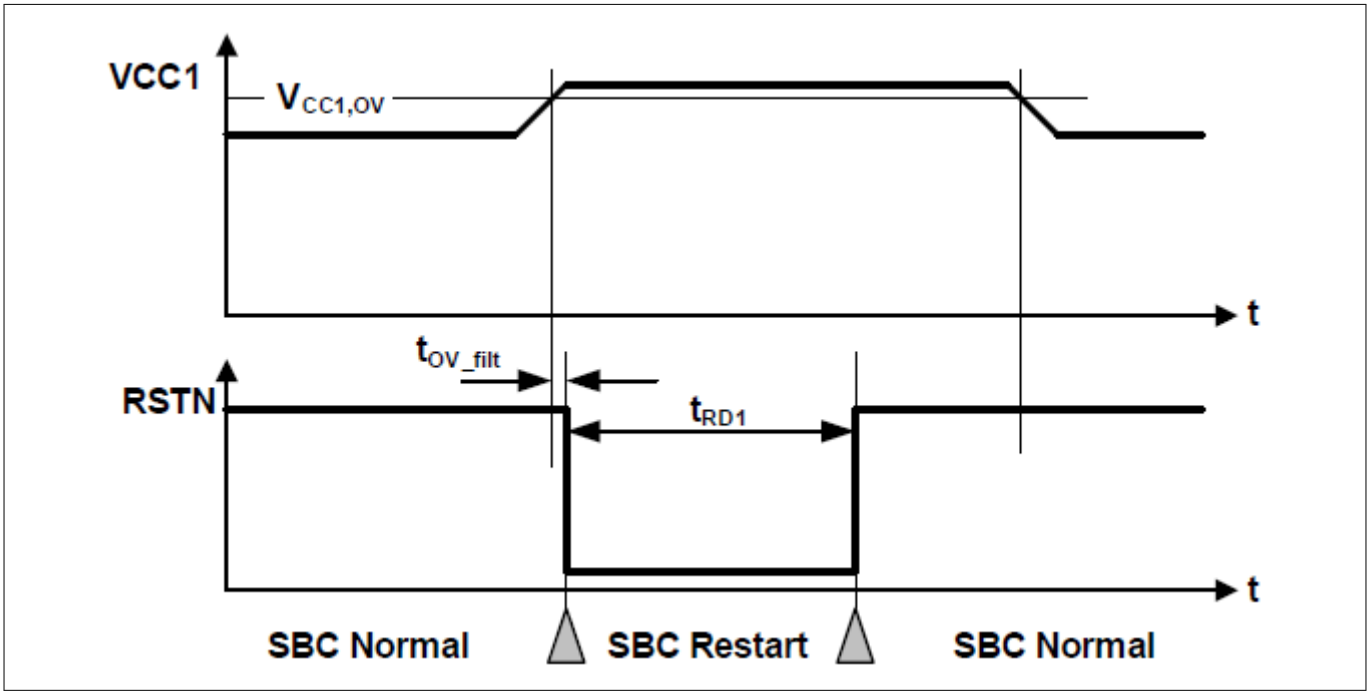

Figure 14 VCC1 Overvoltage Timing Diagram

This behavior differs from the undervoltage response, as shown below.

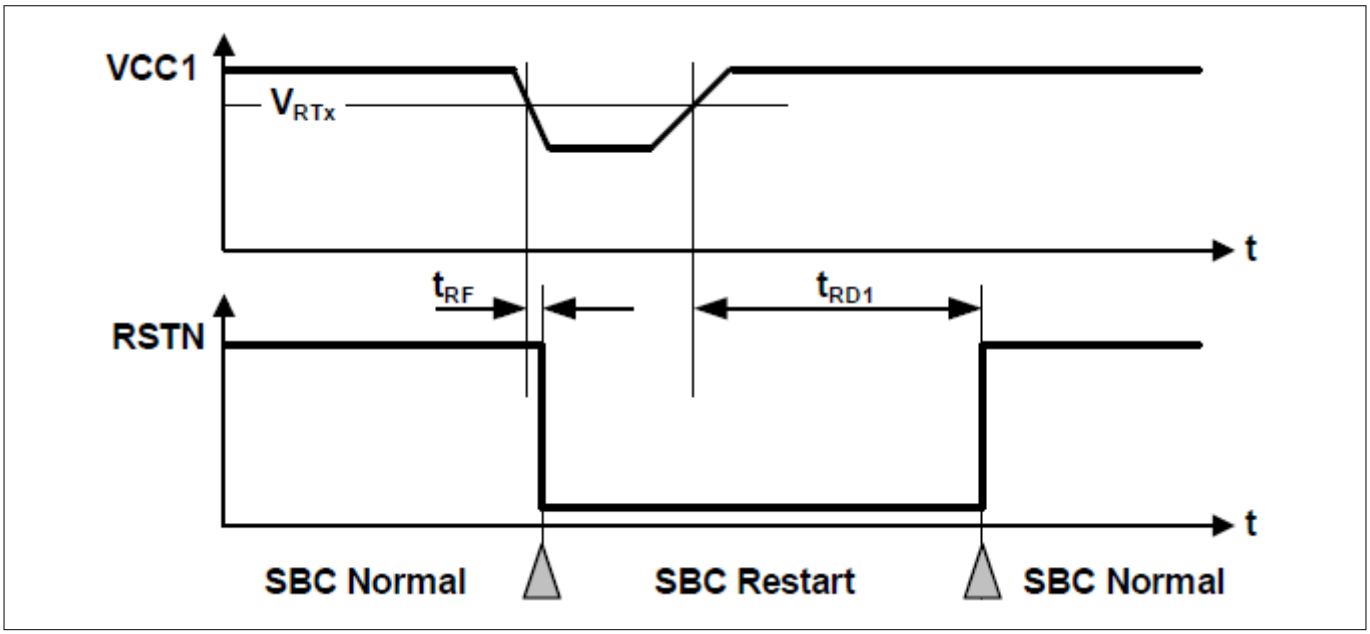

Figure 15 **VCC1 Undervoltage Timing Diagram**

1.4 Layout and BOM guidelines

1.4.1 Grounding concept and general layout recommendations

The power system of the TLE94x1 is separated into three supply domains for the main power stage (VCC1), the second power stage (VCC2), and the other internal control circuitry and for the CAN cell (VCAN). Also, the supply is separated with two VS pins, one for the main power (Pin 15) and one for internal circuitry (Pin 16) including the second power stage. There are three corresponding ground domains (Pins 11, 21 and 22). The concept is visualized in ***Figure 16***.

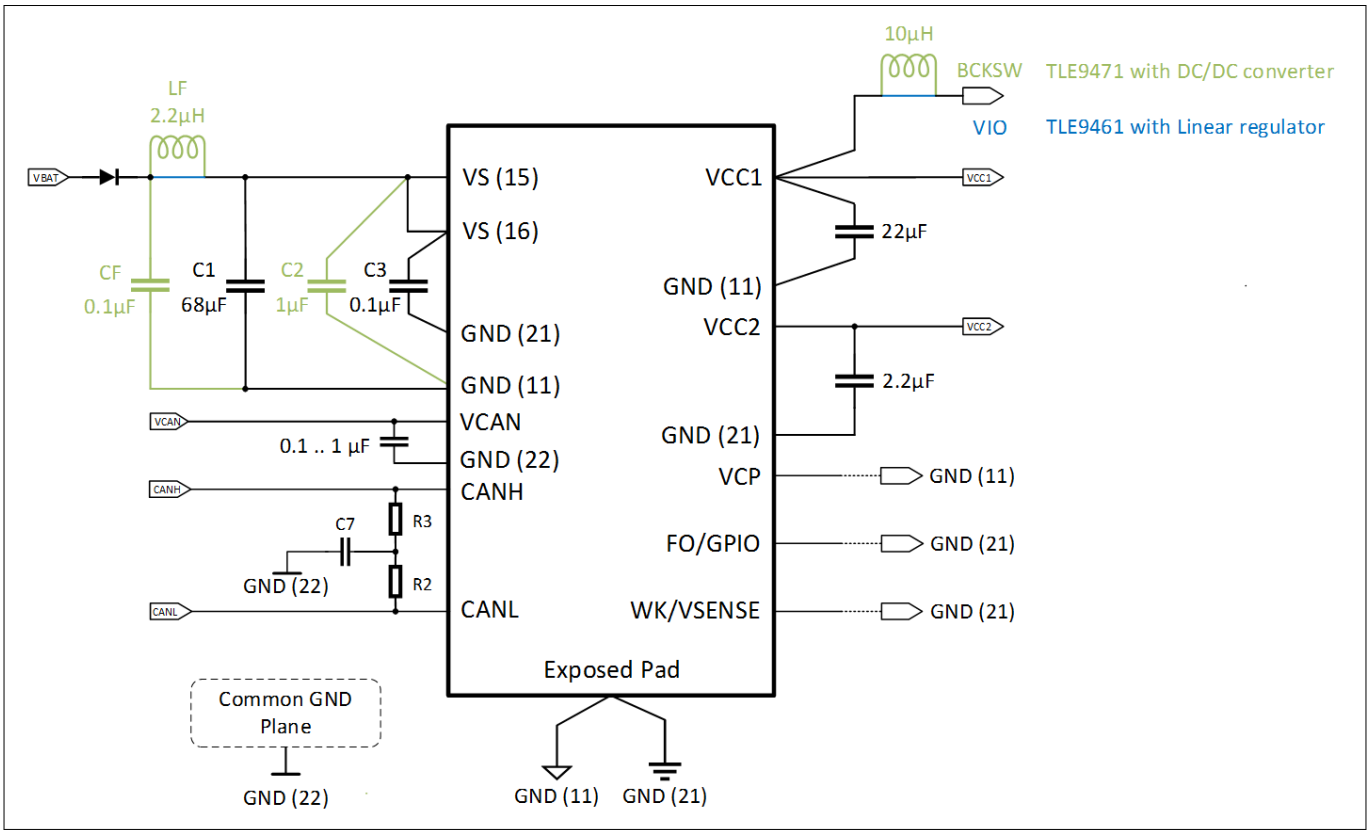

Figure 16 Grounding concept of TLE94x1 (only relevant pins are shown)

Finally, all ground (GND) domains should be connected with each other at the PCB (as star ground connection). An easy and recommended way to do so, is to connect power ground pins (11, 21) to the Exposed Pad landing pattern. The CAN power should be separated, and is connected to the common GND plane nearby.

The bypass capacitors C2 and C3 are used to dissipate higher frequency shares and cross-talk. To keep full filter capability, they should be placed close to the respective pin.

1.4.2 EMC considerations

- All connections are preferably short for a low impedance.
- Place capacitors at VS, VCAN, VCC1 and VCC2 as close as possible to these pins and the belonging ground.
- Bypass capacitors (e.g. C2, C3) connected close to the pins lower the reactance and limit electromagnetic emissions.
- All ground (GND) pins of the SBC should be connected together at the PCB (as star ground connection).
- Route CAN bus lines separated or even shielded.
- Place a bypass capacitor between VCAN and CAN GND (100 nF classical CAN, 1 µF CAN FD).

- Place SBC and microcontroller next to each other, as close as possible (focus on digital I/O).

1.4.3 Thermal considerations

- For improved thermal performance, a 4-layer PCB is recommended.
- The copper thickness and connection of high current nodes should be wide and thick (e.g. 35/70 µm).
- Thermal vias are recommended (as many as possible, preferably under the hot spots like Exposed Pads).
- Consider cooling areas as follows:
  - Connect all GND layers with thermal vias and use them for cooling (connect to Exposed Pad and common ground).
  - Form a quadratic copper area on the bottom side of the SBC with ≥ 300 mm^2.
  - Form a cooling area for the external high-side power transistor, if used (Note: connect to V_S).
- Avoid placing the SBC at the edge of the PCB.

1.4.4 ESD considerations

- All ground (GND) pins of the SBC should be connected together at the PCB (as star ground connection).
- Route CAN bus lines separated or even shielded.
- Place SBC and microcontroller next to each other, as close as possible (focus on digital I/O).
- Pins that are directly connected to VBAT (e.g. VSENSE) should get a serial resistor and bypass capacitor to limit ESD pulse effects.

1.5 BOM considerations

1.5.1 VS, VCC1, VCC2

VS is the supply voltage of the SBC. Both VS pins must be connected to the same input voltage source, which is typically the battery. Though they should be separately connected to the IC as shown in ***Figure 16*** on page 18.

The bulk capacitor C2 is used to reduce the source impedance and should be 68 µF. To get best EMC performance, it is recommended to use one or more bypass capacitors (C3) close to the VS pin (TLE9471x). Leadless ceramic capacitors with low ESR/ESL are recommended.

VCC1 is the output of the linear voltage regulator (TLE9461x) and of the switched mode converter (TLE9471x). The output capacitor is needed to guarantee a stable operation and to buffer transient load events. For stability, at least 1 µF is recommended. Connecting the output capacitor close to the pin and short to GND ensures best accuracy and lowest radiation.

	TLE9461x	**TLE9471x**
C_{OUT}	typ. 2.2 µF, connect directly at the VCC1 pin typ. 2.2 µF, connect directly at the VCC2 pin	typ. 22 µF, connect directly at the VCC1 pin typ. 2.2 µF, connect directly at the VCC2 pin
VIO	connect short to the VCC1 pin (at C_{OUT})	-
BCKSW	-	connect inductor between BCKSW and VCC1 with short and wide wires (inductor peak current)

1.5.2 Charge Pump Output (VCP)

The Lite SBC devices include a charge pump. It supports, at the VCP pin, the control of VBAT connected N-MOSFETS with an appropriate gate voltage >> VS.

Such a transistor can be used for a reverse current protection (e.g. low drop reverse-polarity protection) as well as for a battery connected external power switch, controlled by the SBC (e.g. to switch off in power save mode).

1.5.2.1 Reverse-Polarity Protection

The reverse polarity protection using an N-channel MOSFET is most efficient, but requires an appropriate gate voltage. Such voltage is provided by the Lite SBC. A series resistor of 1 kΩ next to the VCP pin limits the gate charge current of the external MOSFET.

The circuit for a reverse-battery protection is shown in the Application Diagrams (Chapter 14.1, Figure 50, large dashed box) of the datasheet. In case of a dynamic reverse battery connection, the bipolar transistor clamps the MOSFET (T2) gate to GND (former VBAT), closing the channel.

1.5.2.2 External High-Side Power Switch

The VCP pin voltage allows to drive an n-channel MOSFET that is connected to the battery (High-side), if the charge pump is enabled (CP_EN; default = Off after start-up/re-start). The charge pump state can be locked and reset (CFG_LOCK_0) in SBC Normal Mode.

The Application Diagram (Chapter 14.1, Figure 50) of the datasheet shows such MOSFET switch (T1), controlled by VCP. R_1 limits the dynamic gate charge current.

1.5.3 VSENSE

If the WK/VSENSE pin is used as VSENSE, a high-voltage monitoring (e.g. VBAT) can be directly done. The VSENSE pin must be protected against VBAT (un-buffered) pulses. For ESD protection reasons, it is recommended to put a 10 kΩ series resistor and a bypass capacitor of 10 nF close to the VSENSE pin. A reverse current protection (diode) must be added in case of a direct V_{BAT} connection.

2 Power dissipation and thermal measurements

2.1 Junction temperature measurement

2.1.1 Background

The maximum junction temperature of the device is an important parameter that needs to be determined in order to follow the maximum operating temperature condition as well as handling the operation beyond (up to thermal shutdown).

However, the device junction temperature cannot be measured directly, since the device is covered by a package. The junction temperature can be estimated, measuring the device temperature on top of the package, and using the thermal correlation factor Ψ_{JT}.

2.1.2 Boundary conditions for Ψ_{JT} value calculation

The factor Ψ_{JT} correlates the device junction temperature with that on top of the package. This value depends on the environmental conditions (e.g. air flow and board structure) and the thickness of the package. For the identification of the actual Ψ_{JT} value, the following conditions (according to JESD51) have been used:

- PCB designs with 15 thermal vias each (see figure below).
- Cooling area on bottom of PCB (300 mm^2).
- Ambient temperature: 25 °C and 85 °C.

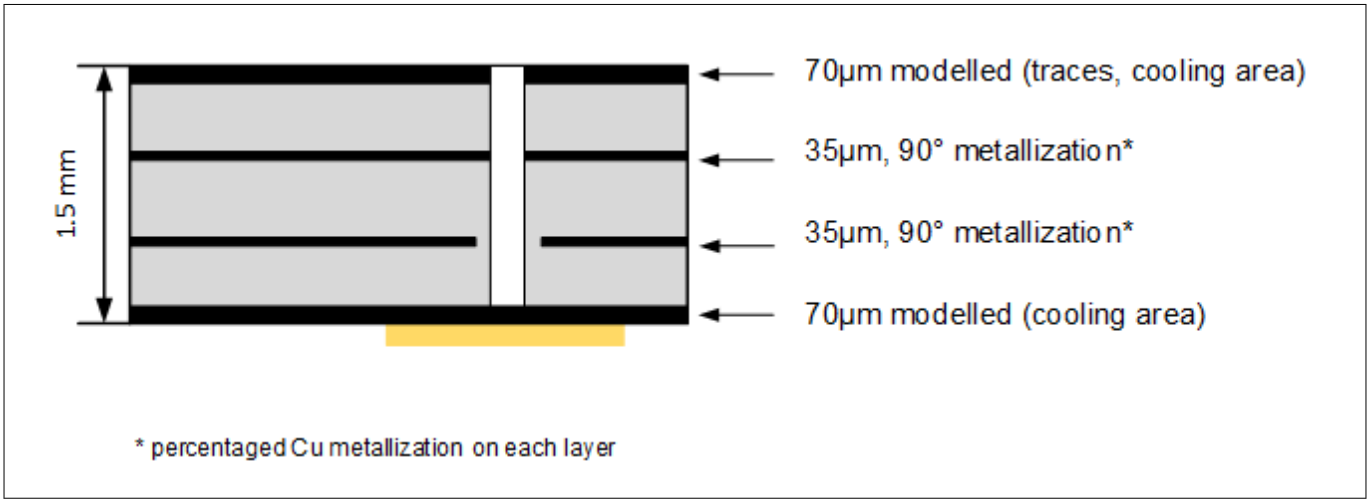

Figure 17 PCB cross section (JEDEC 2s2p) with cooling area

Table 4 Typical power dissipation (TA = 25 °C)

Condition (VCC1) / VCC2 = 5 V (100 mA)	Total Power Dissipation, P_{Diss} (W)	
	TLE9461x	TLE9471x
VCC1 = 5 V/3.3 V (150 mA)	1.8 / 2.05 W	0.94 / 1 W
VCC1 = 5 V/3.3 V (500 mA)	-	1.63 / 1.6 W

The power dissipation for other output currents and temperatures can be easily calculated with the Power Dissipation Tool, which can be found on www.infineon.com/SBC.

2.1.3 Results

The following table provides the results of the thermal measurements.

Table 5 $\Psi_{JT}/R_{\Theta JA}$ calculated with free air convection

PCB structure	T_A [°C]	25	85
2s2p	$R_{\Theta JA}$ [K/W]	37	36
	Ψ_{JT} [K/W]	4.4	5

2.1.4 Calculation of the device junction temperature (T_J)

The Ψ_{JT} values have been determined under natural convection conditions. Since it is calculated as

$$\Psi_{JT} = \frac{T_J - T_{Top}}{P_{Diss}},$$

the device junction temperature (T_J) can be estimated by rearranging the equation accordingly:

$$T_J = \left(\Psi_{JT} \cdot P_{Diss}\right) + T_{Top}$$

Example calculation

- Conditions
  - T_{Top} = 110 °C (temperature measured on top of the package)
  - T_A = 85 °C (use ***Table 5*** on page 22)
  - PCB type: 2s2p
  - Cooling Area = 300 mm²
  - P_{Diss} = see ***Table 4*** on page 22 for maximum values (VCC1 = 3.3 V)
- Calculation using TLE9461 with 150 mA:
  - T_J = (Ψ_{JT} * P_{Diss}) + 110 °C = (5 K/W * 2.05 W) + 110 °C = 120 °C
- Calculation using TLE9471 with 150 mA:
  - T_J = (Ψ_{JT} * P_{Diss}) + 110 °C = (5 K/W * 1 W) + 110 °C = 115 °C
- Calculation using TLE9471 with 500 mA:
  - T_J = (Ψ_{JT} * P_{Diss}) + 110 °C = (5 K/W * 1.6 W) + 110 °C = 118 °C

The DCDC converter enables a lower operating junction temperature at the same output power.

Calculating the maximum allowable power dissipation in order to stay within the maximum operating temperature can be done using the $R_{\theta JA}$ values of ***Table 5*** on page 22:

$$P_{dmax} = \frac{T_{Jmax} - T_A}{R_{\Theta JA}} = \frac{150°C - 85°C}{36K/W} = 1.8W$$

3 CAN partial networking hints - SWK configuration & activation

3.1 Background

CAN Partial Networking (PN) allows to reduce the current consumption of the CAN network significantly by putting selected nodes into a sleep mode, and waking them up only if needed. The Lite SBC family offers devices with CAN PN according to ISO11898-2:2016. The respective feature is named Selective Wake (SWK).

In the following sections, all configuration and activation tasks, needed to properly use this feature, are described.

3.2 SWK configuration and activation sequence

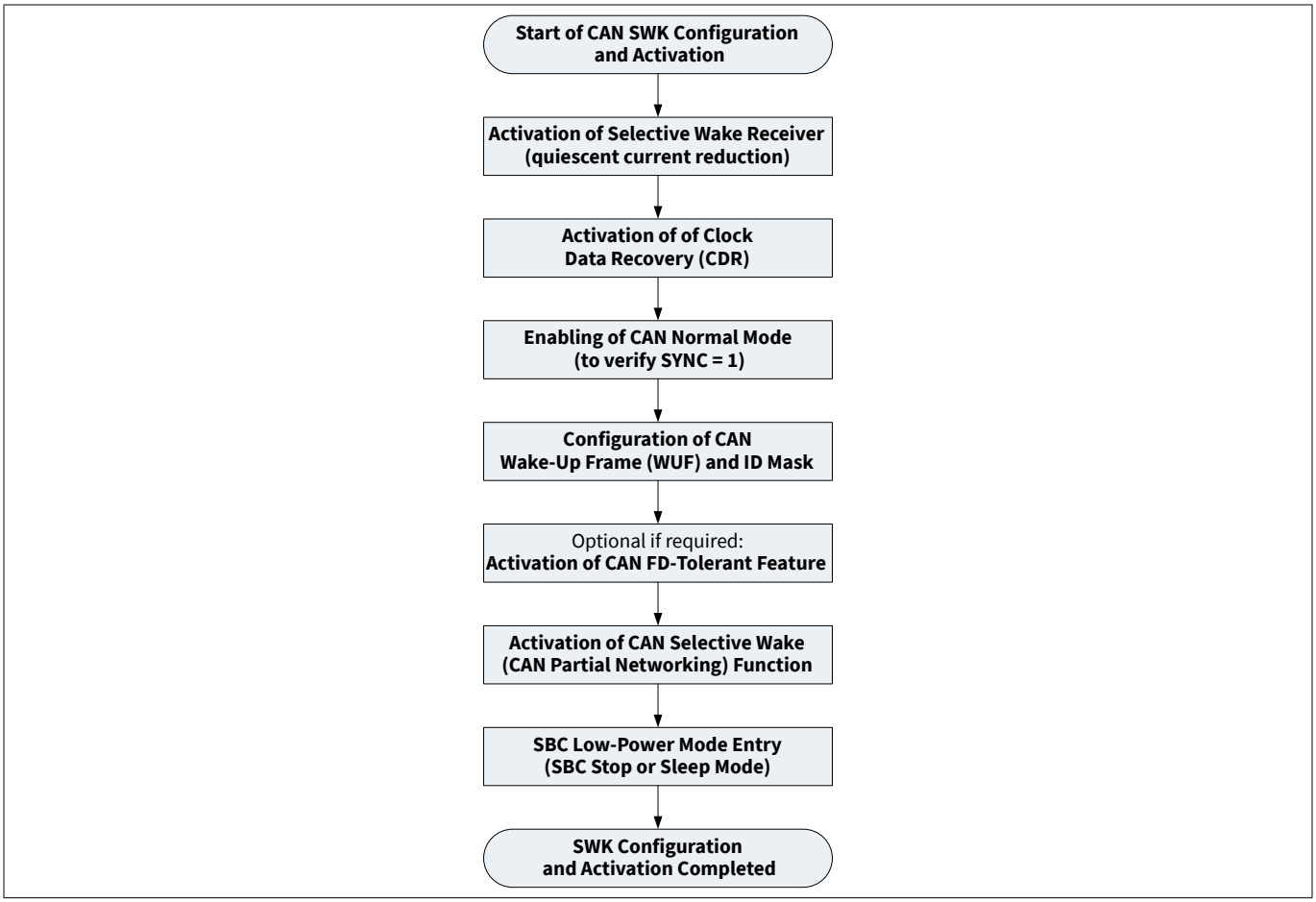

Figure 18 Overall SWK configuration & activation sequence

CAN partial networking hints - SWK configuration & activation

For a detailed explanation of the different sequence steps, see below:

- Activation of Selective Wake Receiver, see ***Chapter 3.3*** on page 25.
- Activation of Clock Data Recovery (CDR), see ***Chapter 3.4*** on page 26.
- Configuration of CAN Wake-Up Frame (WUF), see ***Chapter 3.5*** on page 27.
- Activation of CAN FD tolerant feature, see ***Chapter 3.6*** on page 28.
- Activation of CAN Selective Wake function, see ***Chapter 3.7*** on page 29.
- SBC Low-Power Mode entry, see ***Chapter 3.8*** on page 30.

3.3 Activation of the Selective Wake Receiver

The activation of the Selective Wake Receiver reduces the quiescent current to about 360 µA. Once partial networking is deactivated, resuming regular CAN communication, it is recommended to activate the Normal Mode Receiver again.

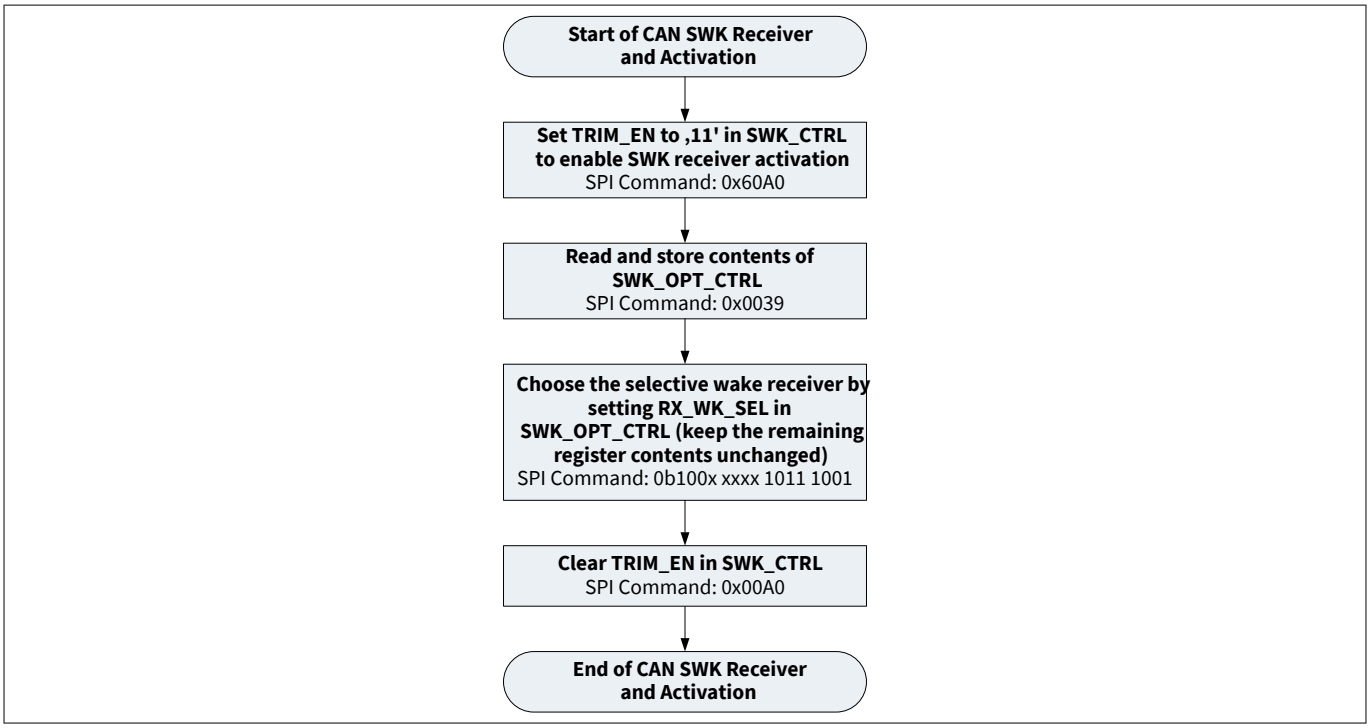

Figure 19 Activation of the Selective Wake Receiver

3.4 Activation of the Clock Data Recovery (CDR)

It is strongly recommended to enable the Clock Data Recovery (CDR) to compensate for drift effects (lifetime, temperature).

The CDR settings of the registers SWK_CDR_CTRL2, SWK_BTL0_CTRL1_CTRL, SWK_CDR_LIMIT_High_CTRL, SWK_CDR_LIMIT_LOW_CTRL need to be chosen depending on the CAN baud rate. Please also refer to *Recommended CDR Settings for Different Baud Rates* in the datasheet.

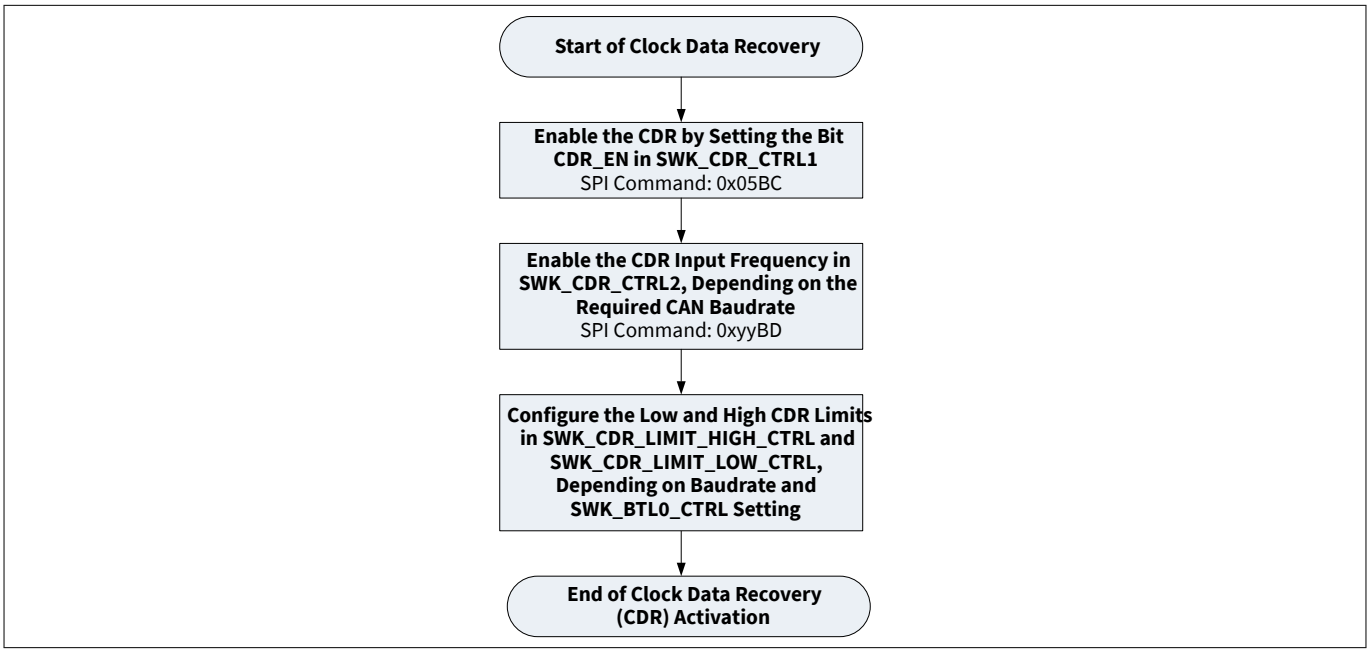

Figure 20 Activation of the Clock Data Recovery (CDR)

3.5 Configuration of the CAN Wake-Up Frame (WUF) and ID mask

The ID configuration depends on standard or extended frame format. In both cases, the configuration is done from the end of the registers, e.g. in SWK_ID3_CTRL and SWK_ID2_CTRL.

The DLC content must match exactly the number of data bytes.

It is not possible to mask the IDE bit (Identifier Extension bit).

The data bytes start from SWK_DATA7_CTRL, e.g., if two data bytes are sent, they have to be configured in SWK_DATA7_CTRL and SWK_DATA6_CTRL.

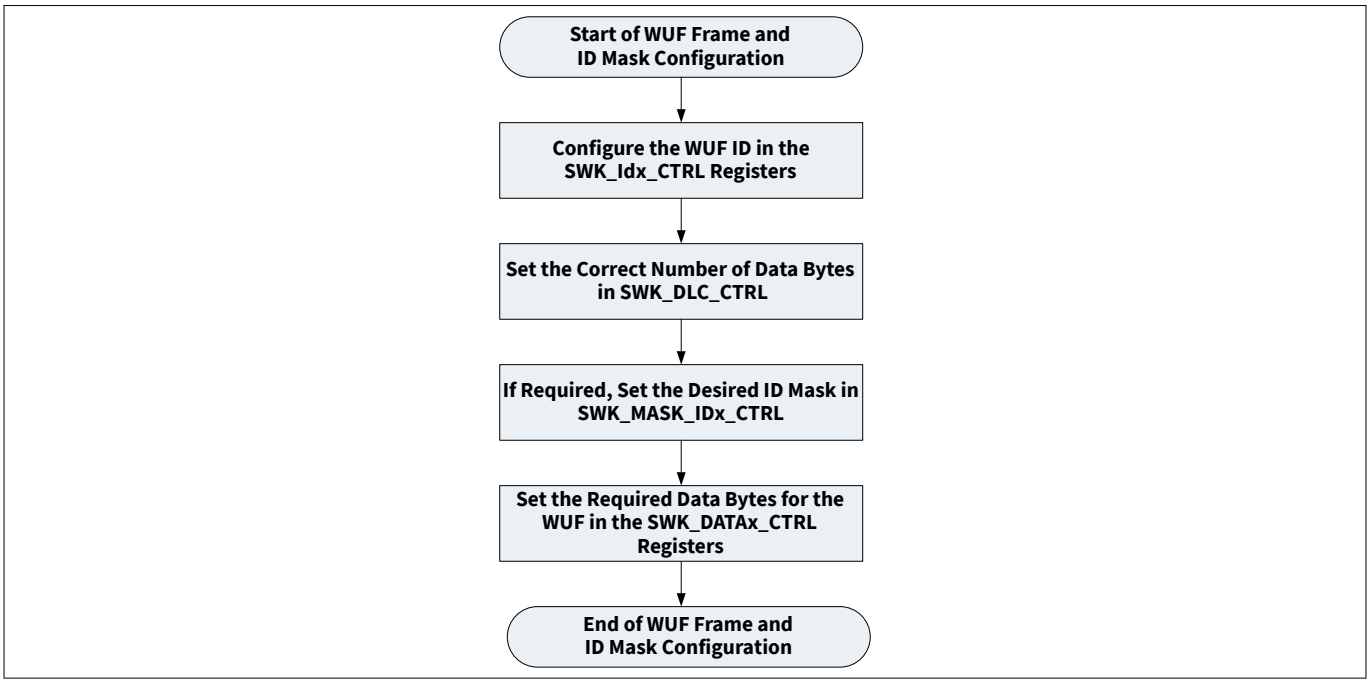

Figure 21 Configuration of the CAN Wake-Up Frame (WUF) and ID mask

3.6 Activation of the CAN FD tolerant feature (optional)

This is an optional feature and should only be used if the CAN FD tolerance is needed for the respective ECU (mixed classical and CAN FD networks).

The recommended settings apply for an arbitration rate of 500 kBit/s and a 2 MBit/s CAN FD communication.

For more information, please refer to chapter 5.6.7 of the datasheet, and to the SPI register SWK_CAN_FD_CTRL.

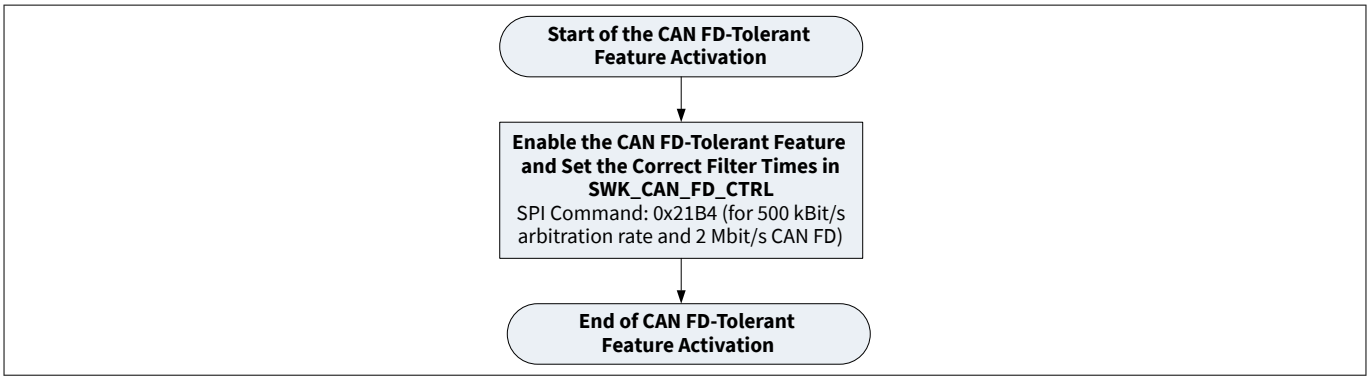

Figure 22 Activation of the CAN FD tolerant feature

SWK_CAN_FD_CTRL

CAN FD Configuration Control Register (Address 011 0100_B)

POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $00xx\ xxxx_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	DIS_ERR_CNT	RX_FILT_BYP	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN
r	r	rwh	rw	rw	rw	rw	rw

Figure 23 SWK_CAN_FD_CTRL register

3.7 Activation of the CAN Selective Wake (SWK) function

The synchronization of the protocol handler must be ensured for the Selective Wake operation, to ensure a wake-up via WUF.

The CFG_VAL bit is cleared by the SBC in case the SWK configuration is changed, or in case of a configuration error.

SWK_STAT content must be: SWK_SET = 1, SYNC = 1, WUP = 0, WUF = 0.

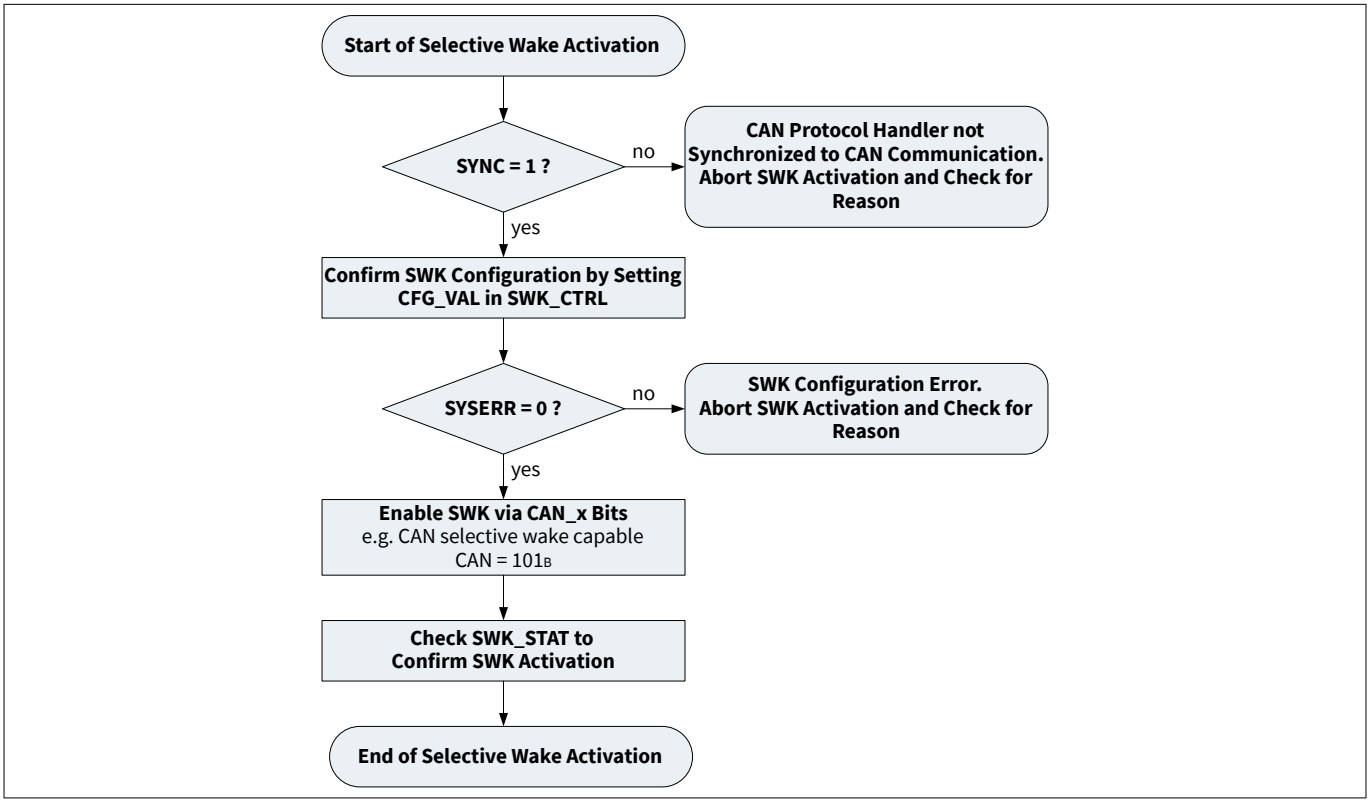

Figure 24 Activation of the CAN Selective Wake (SWK = CAN partial networking) function

3.8 SBC Low-Power Mode (SBC Stop or Sleep Mode) entry

Right after enabling SWK, this sequence should be executed.

Before entering SBC Sleep Mode, it is mandatory to check pending wake events and to clear the wake status register.

Wake events lead to disabling the SWK function.

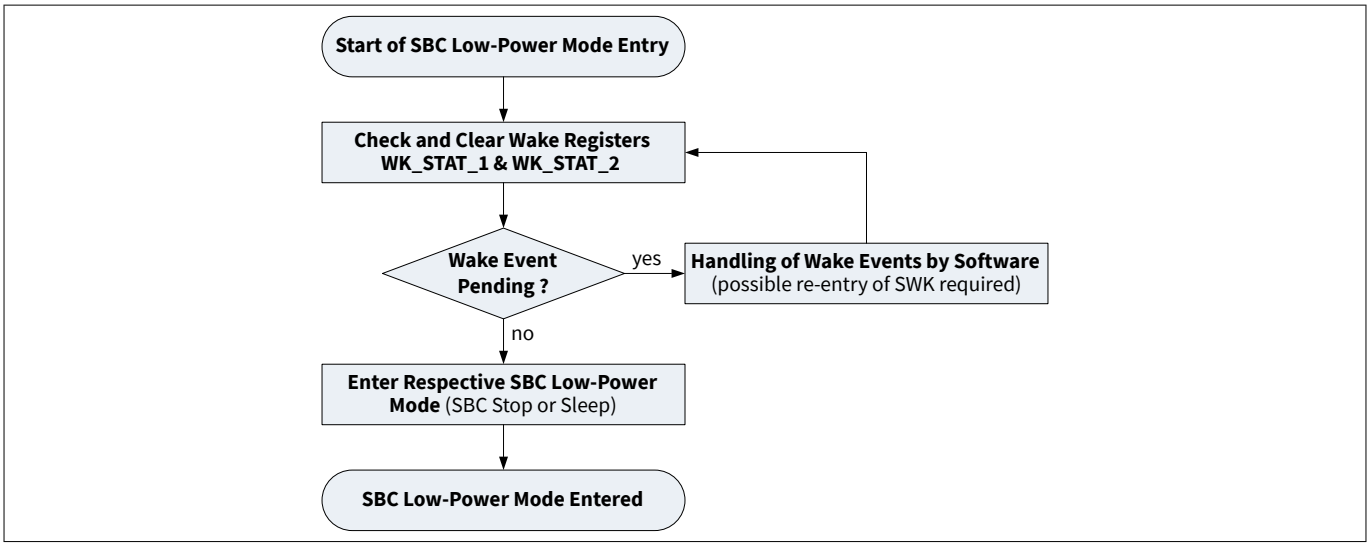

Figure 25 SBC Low-Power Mode entry

4 SPI interface

4.1 Lite System Basis Chip (Lite SBC) family

The Lite SBC family features an in-depth diagnosis and failure signalization in the SPI registers (status registers). These diagnosis and failure bits are intended to support a system and failure diagnosis of the ECU, which is typically required by the system and by functional safety.

The diagnosis functions are in general required by OEMs, but vary in detail, depending on the partitioning and implementation. There are also pre-warning bits (e.g. thermal pre-warning or VCC1 under-voltage pre-warning) which can be used to react early enough to perform emergency savings, to disregard incorrect measurements, or to shut down functions, avoiding a thermal shutdown.

4.2 SPI configuration

4.2.1 Timing

The SPI command is executed, at the latest, 6 µs after the CSN is set to HIGH. In general, care must be taken about the minimum CSN High time, and the minimum time between two SPI commands, which is 3 µs (see P_16.7.23 and 24 in the datasheet).

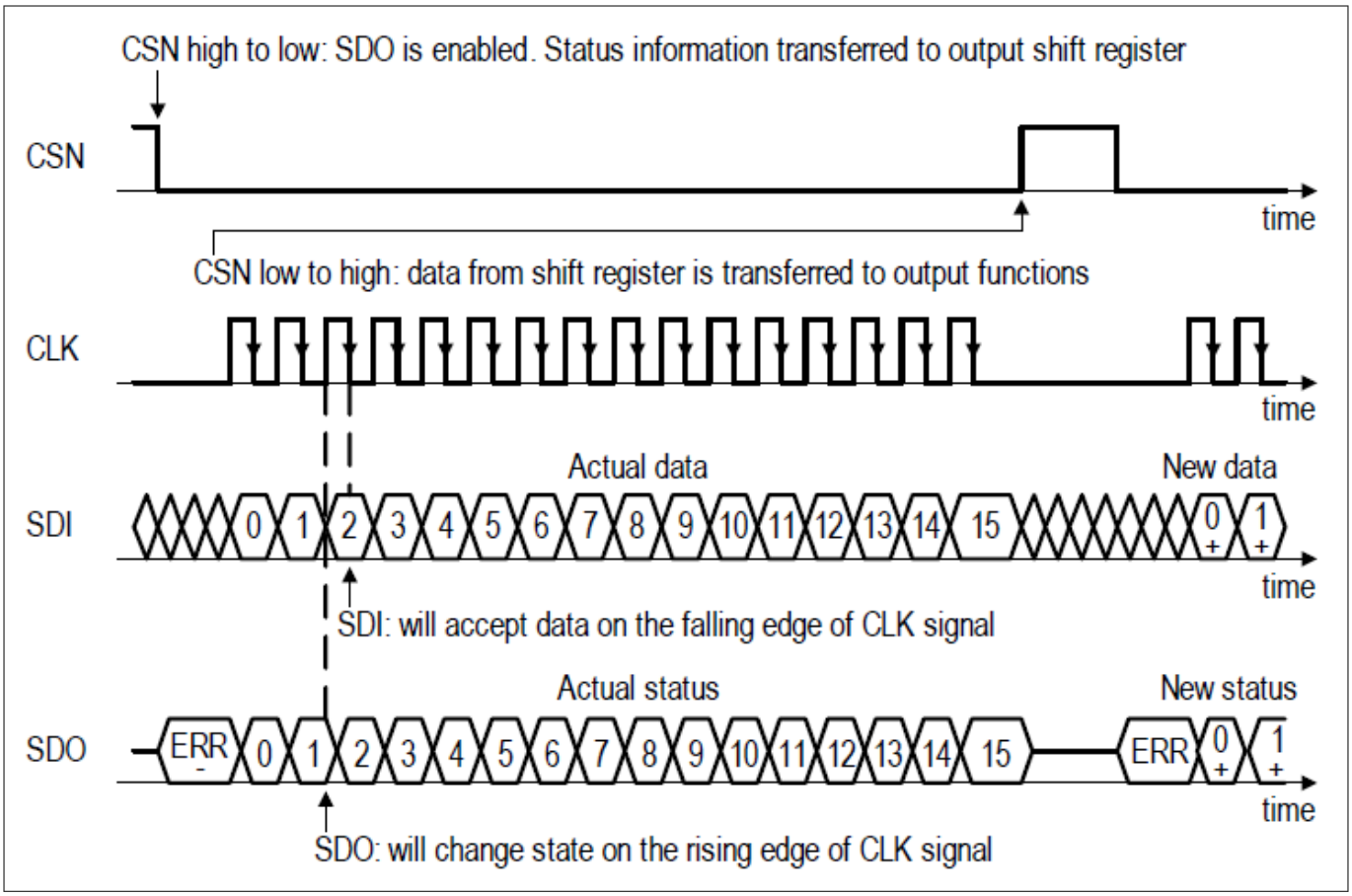

Figure 26 SPI timing diagram

The data is sampled with the falling edge of the clock, therefore, the clock polarity from the microcontroller usually must be set to inverted phase.

4.2.2 Status information field

The status information field immediately shows whether there was a change in status flags (avoids unnecessary polling). The bit in the status information field is set, if any bit in the respective register is set.

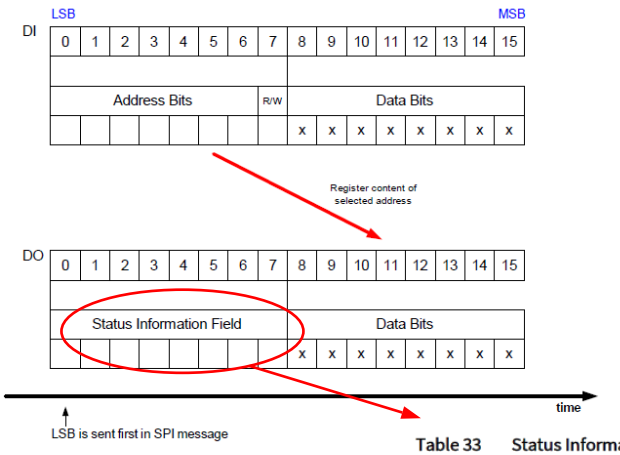

Table 33 Status Information Field

Bit in Status Information Field	Corresponding Address Bit	Status Register Description
0	100 0001	SUP_STAT_0 - Supply Status: POR, VCC2 fail, VCC1 fail
1	100 0010	THERM_STAT - Thermal Protection Status
2	100 0011	DEV_STAT- Device Status: Mode before wake-up-up/failure, WD Fail, SPI Fail, Failure
3	100 0100	BUS_STAT - Bus Failure Status: CAN;
4	100 0110 100 0111	WK_STAT_0, WK_STAT_1 - Wake Source Status; Status bit is a combinational OR of both registers
5	100 0000	SUP_STAT_1: VS_UV, VCC1_WARN/OV
6	101 0100	GPIO_OC_STAT: GPIO over current
7	101 0101	GPIO_OL_STAT: GPIO open load

Figure 27 SPI Interface – status information field

4.2.3 Register mapping structure

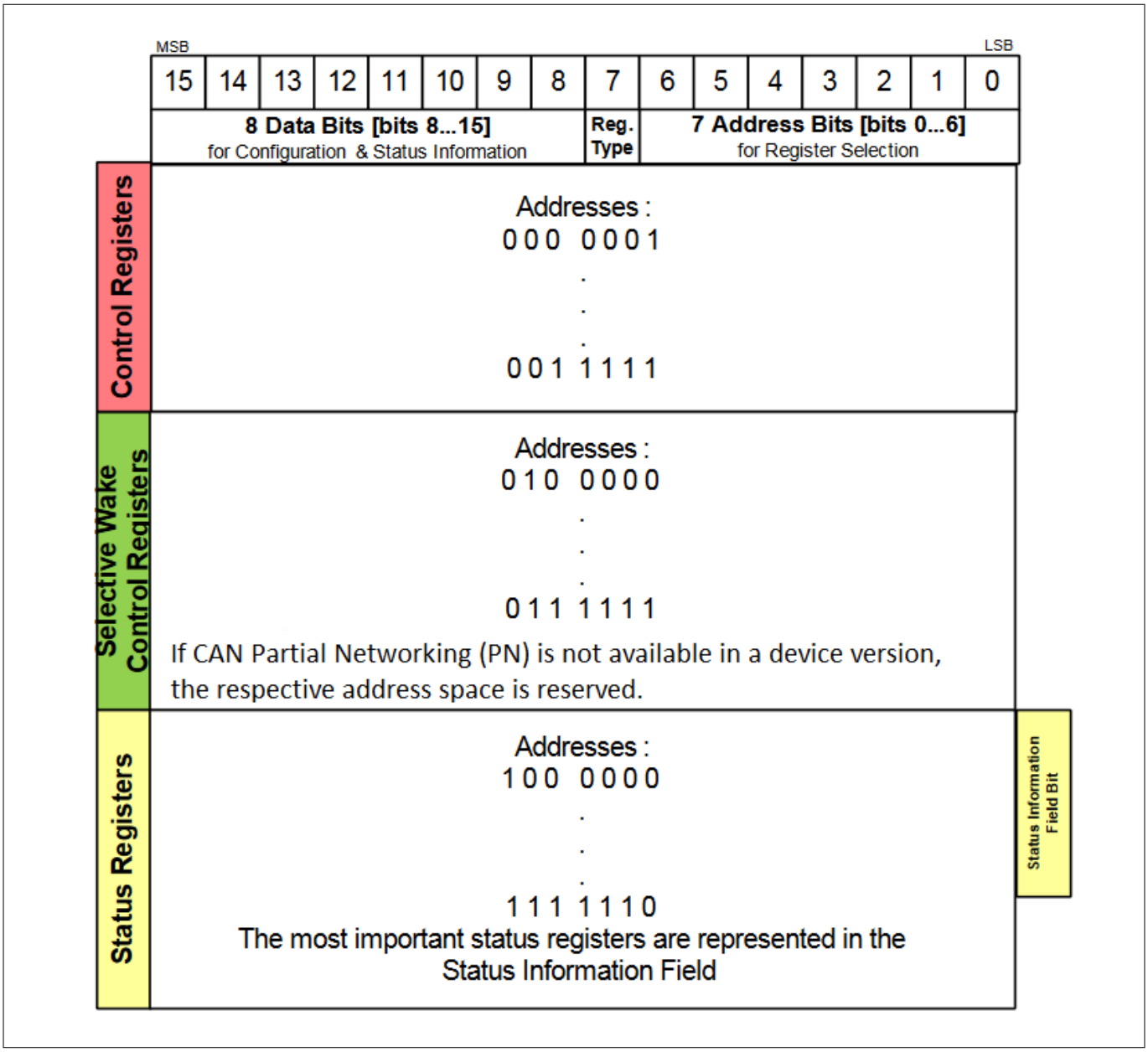

Figure 28 SPI Register Mapping Overview

The register mapping includes:

- Control registers to configure all SBC contents in SBC Normal Mode.
- SYS_CTRL is a freely usable 8-bit RAM register – not changed by SBC.
- Selective wake registers only visible in -3ES variants.
- Status registers for wake & failure signalization and diagnosis (keep content until actively cleared).

4.3 SPI diagnosis

4.3.1 Prewarning examples

- Thermal prewarning

TPW	0	rc	**Thermal Pre Warning** 0B , No Thermal Pre warning 1B , Thermal Pre warning detected

  - Provides early warning that the SBC is close to the critical junction temperature.
- VCC1 undervoltage prewarning

VCC1_ WARN	0	rc	**VCC1 Undervoltage Prewarning ($V_{PW,f}$)** 0B , No VCC1 undervoltage prewarning 1B , VCC1 undervoltage prewarning detected

  - Provides early warning in case the VCC1 UV threshold is set to a lower level, and the VCC1 voltage is not sufficient anymore.
  - Possible actions: Emergency saving of RAM data, refusing ADC measurements, disabling communication.

4.3.2 Determining source of restart/reset

Description
Power-On Reset Detection 0_B , No POR 1_B , POR occurred
Reserved, always reads as 0
VCC2 Over Temperature Detection 0_B , No over temperature 1_B , VCC2 over temperature detected
VCC2 Under Voltage Detection ($V_{CC2,UV,f}$) 0_B , No VCC2 Under voltage 1_B , VCC2 under voltage detected
VCC1 Short to GND Detection (<Vrtx for t>2ms after switch On) 0_B , No short 1_B , VCC1 short to GND detected
Reserved, always reads as 0
VCC1 UV-Detection (due to Vrtx reset) 0_B , No VCC1_UV detection 1_B , VCC1 UV-Fail detected

Wake-up via CAN Bus 0_B , No Wake-up 1_B , Wake-up
Wake-up via TimerX 0_B , No Wake-up 1_B , Wake-up
Reserved, always reads as 0
Wake-up via WK 0_B , No Wake-up 1_B , Wake-up

TSD2 Thermal Shut-Down Safe State Detection 0_B , No TSD2 safe state detected 1_B , TSD2 safe state detected: >16 consecutive TSD2 events occurred, next TSD2 waiting time is 60s
TSD2 Thermal Shut-Down Detection 0_B , No TSD2 event 1_B , TSD2 OT detected - leading to SBC Fail-Safe Mode
TSD1 Thermal Shut-Down Detection 0_B , No TSD1 fail 1_B , TSD1 OT detected (affected module is disabled)
Thermal Pre Warning 0_B , No Thermal Pre warning 1_B , Thermal Pre warning detected

Device Status before Restart Mode 00_B , Cleared (Register must be actively cleared) 01_B , Restart due to failure (WD fail, TSD2, VCC1_UV, trial to access SLEEP MODE without any wake source activated); also after a wake-up from Fail-Safe Mode 10_B , Sleep Mode 11_B , Reserved
Reserved, always reads as 0
Number of WD-Failure Events (1/2 WD failures depending on CFG1) 00_B , No WD Fail 01_B , 1x WD Fail, FO activation - Config 2 selected 10_B , 2x WD Fail, FO activation - Config 1 / 3 / 4 selected 11_B , Reserved (never reached)
SPI Fail Information 0_B , No SPI fail 1_B , Invalid SPI command detected
Activation of Fail Output FO 0_B , No Failure 1_B , Failure occurred

Figure 29 Status registers signalize source of wake-up and failure events

5 Reset behavior during power-up/down

5.1 Possible VCC1 undervoltage reset toggling due to dynamic load changes

If V_S is close to the VCC1 undervoltage threshold (VRTx), a dynamic variation of the load current (VCC1 and/or VCC2) can generate a reset toggling.

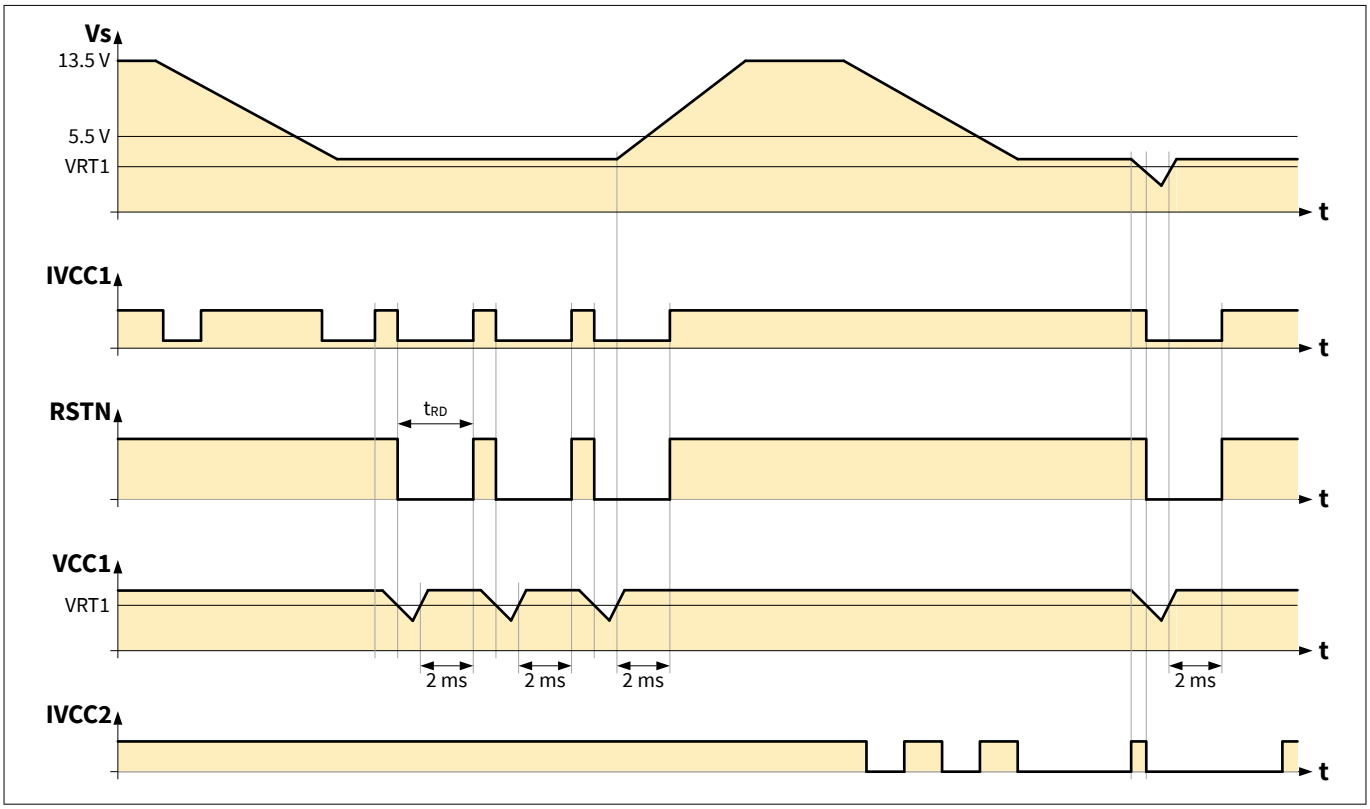

Figure 30 Simplified timing diagram of reset behavior at low supply voltage

- If V_S is close to the VCC1 undervoltage threshold level, the voltage regulator already operates in the linear region ($V_{drop} = R_{on} * I_{load}$).
- A VCC1 undervoltage reset forces the microcontroller into reset state as well, and the load current on VCC1 drops immediately.
- Therefore, VCC1 increases and could rise again above the undervoltage threshold (and the SBC reset is released).
- The startup of the microcontroller applies the load again, and V_S triggers the undervoltage level again.
- The behavior can repeat (toggling) as long as V_S stays at an appropriate level.
- Also a load step on VCC2, influencing the V_S level, could cause the same behavior of VCC1 undervoltage reset toggling.

5.2 Use case LV124-E07

4.7.2 Test

Table 17: Test Parameter E-07: Slow ramp-down and ramp-up of power supply voltage

Operating modes of the DUT	**Test 1:** KL 30 ON and KL 15 ON **Test 2:** KL 30 ON
Initial voltage	U_{Bmax}
Rate of voltage ramp-down/ramp-up	0.5 V/min
Hold time at U_{Bmax}	Until error memory completely read out
Minimum voltage	0 V
Final voltage	U_{Bmax}
Number of cycles	1 cycle in operating mode II.c 1 cycle in operating mode II.a
Number of DUT	minimum 6

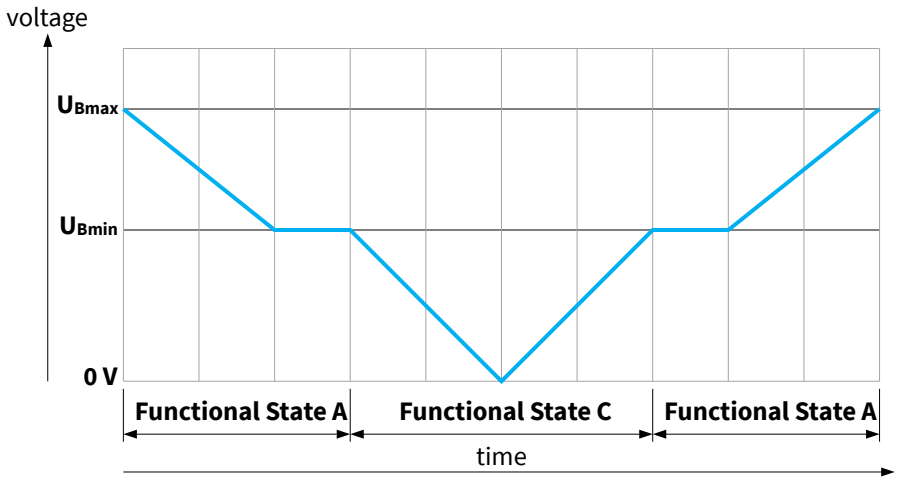

Figure 31 Voltage ramp for testing low supply voltage according to LV124

5.3 VCC1 undervoltage reset toggling at low V_S, expected system behavior

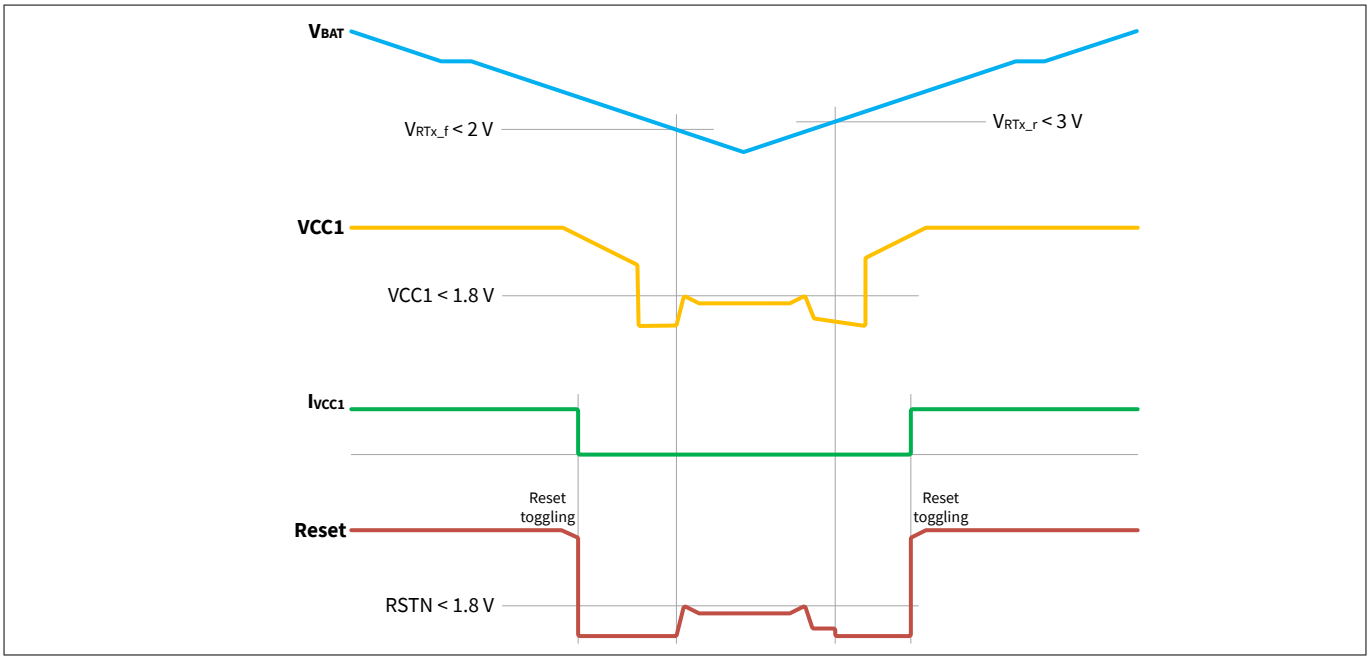

Figure 32 Expected system behaviour at low supply voltages according to LV124

6 Pin FMEA

6.1 Abstract

Note: The following information shall be considered as a basis for an FMEA on application level. It is not a description or warranty of a certain functionality, condition, or quality of the device.

The section shows the results of considerations taken during the pin FMEA. In addition, the effect of the potential failure on the Fail Output (FO) function is stated.

The devices of the Lite SBC family covered by this Pin FMEA are listed below:

- TLE9461x
- TLE9471x

Note: The NC pin can be ignored in the FMEA (internally not bonded).

6.2 Introduction

6.2.1 General information about FMEA

A failure modes and effects analysis (FMEA) is a procedure in operations management for the analysis of potential

failure modes within a system, for classification by severity or determination of the effect of failures on the system.

Failure modes are any errors or defects in a process, design, or item, especially those that affect the customer, and can be potential or actual. Effects analysis refers to studying the consequences of those failures.

6.2.2 Implementation

In an FMEA, failures are usually prioritized according to how serious their consequences are, how frequently they occur and how easily they can be detected. The purpose of the FMEA is to take actions to eliminate or reduce failures, starting with the highest-priority ones. It may be used to evaluate risk management priorities for mitigating known threat vulnerabilities.

This document is intended to provide a basis for an application-level FMEA at the customer side. A quantification on the severity, occurrence and detection levels is not given and needs to be done by the customer for each application individually.

6.3 Classification of Failure Effects

Table 6 Classes of Failure Effects

Class	Failure Effects
A	Damage to device affects application functionality
B	No damage to device, but thermal damage must be considered
C	No damage to device, but can affect application functionality
D	No damage to device, and no affect to application functionality

6.4 Pin FMEA Table

Table 7 Potential Failure Mode and Effects Analysis

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FO/GPIO) function	Class
1	VCAN	Pin open	No CAN functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to TXDCAN	No CAN functionality	FO unchanged	C
2	TXDCAN	Pin open	No CAN functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to RXDCAN	No CAN functionality	FO unchanged	C
3	RXDCAN	Pin open	No CAN functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to CLK	No CAN/SPI functionality	FO unchanged	C
4	CLK	Pin open	No SPI functionality	FO activated after WDT failure	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to SDI	No SPI functionality	FO activated after WDT failure	C
5	SDI	Pin open	No SPI functionality	FO activated after WDT failure	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to SDO	No SPI functionality	FO activated after WDT failure	C
6	SDO	Pin open	Partial SPI functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to CSN	No SPI functionality	FO unchanged	C
7	CSN	Pin open	No SPI functionality	FO activated after WDT failure	C
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to INTN	Corrupted SPI functionality	FO activated after WDT failure	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FO/GPIO) function	Class
8	INTN	Pin open	No interrupt	FO unchanged	C
		Pin shorted to GND	Continuous interrupt		
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to RSTN	Corrupted interrupt/reset	FO unchanged	C
9	RSTN	Pin open	No reset	FO unchanged	C
		Pin shorted to GND	Continuous reset		
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to TEST	Possible increased current consumption; possible SBC Development Mode entry	FO unchanged	B
10	TEST	Pin open	No SBC Development Mode possible	FO unchanged	D
		Pin shorted to GND			
		Pin shorted to VS	Chip destruction	Not functional	A
11	GND	Pin open	Functionality not ensured	FO unchanged	C
		Pin shorted to VS	No chip functionality, full recovery if short is removed	Not functional	B
		Pin shorted to VCC1	Buck/LDO, short circuit detection leads to Fail-Safe-Mode	FO activated	C
12	VIO (TLE9461x)	Pin open	No VCC1 supply to application	FO unchanged	C
		Pin shorted to GND	No VCC1 supply to application; short circuit detection leads to Fail-Safe-Mode	FO activated	
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to VCC1	Normal operation	FO unchanged	D
12	VCC1 (TLE9471x)	Pin open	No voltage feedback for regulation	FO unchanged	C
		Pin shorted to GND	No VCC1 supply to application; Fail-Safe	FO activated	
		Pin shorted to VS	Chip destruction	Not functional	A
		Pin shorted to BCKSW			

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FO/GPIO) function	Class
13	VCC1 (TLE9461x)	Pin open	No VCC1 functionality, WD failure	FO unchanged	C
		Pin shorted to GND	No VCC1 supply to application; short circuit detection leads to Fail-Safe-Mode	FO activated	
		Pin shorted to VS	Chip destruction	Not functional	A
13	BCKSW (TLE9471x)	Pin open	No VCC1 supply to application	FO unchanged	C
		Pin shorted to GND	No VCC1 supply to application; short circuit detection leads to Fail-Safe-Mode	FO activated	
		Pin shorted to VS	Chip destruction	Not functional	A
14	NC	Pin open	No effect	FO unchanged	D
		Pin shorted to GND			
		Pin shorted to VS	No effect (if floating)		
15	VS	Pin open	No device function; full recovery if short is removed	Not functional	B
		Pin shorted to GND			
		Pin shorted to VS (16)	Normal operation	FO unchanged	D
16	VS	Pin open	No device function; full recovery if short is removed	Not functional	C
		Pin shorted to GND			
		Pin shorted to VCP	No charge-pump functionality	FO unchanged	
17	VCP	Pin open	No charge-pump functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS			
		Pin shorted to WK/ VSENSE	Potential charge-pump failure		
18	WK/ VSENSE	Pin open	No WK/VSENSE functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS			
		Pin shorted to FO/ GPIO	No WK/VSENSE, no FO/GPIO functionality		
19	FO/GPIO	Pin open	No FO/GPIO functionality	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS			
		Pin shorted to VCC2			

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FO/GPIO) function	Class
20	VCC2	Pin open	No VCC2 supply to application	FO unchanged	C
		Pin shorted to GND	No VCC2 supply to application; current limit situation	FO unchanged	B
		Pin shorted to VS	No VCC2 supply to application; overvoltage situation	FO unchanged	C
21	GND	Pin open	Functionality not ensured	FO unchanged	C
		Pin shorted to VS	No SBC function	Not functional	
22	GND	Pin open	CAN functionality not ensured	FO unchanged	C
		Pin shorted to VS	No SBC function	Not functional	
		Pin shorted to CANH	No CAN functionality	FO unchanged	
23	CANH	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND			
		Pin shorted to VS	CAN communication disturbed; increased EME		
		Pin shorted to CANL	No CAN communication possible		
24	CANL	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN communication disturbed; increased EME		
		Pin shorted to VS	No CAN communication possible		

Revision History

Revision	Date	Changes
1.0	2018-09-28	Initial release

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