ITS4200S-ME-O

Smart High-Side NMOS-Power Switch

Data Sheet

Rev 1.0, 2012-09-01

Standard Power

1 Overview

SOT-223-4

Features

- CMOS compatible input
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized Electromagnetic Compatibility
- Overload protection
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of Vbb protection
- Electrostatic Discharge Protection (ESD)
- Green Product (RoHS compliant)

ITS4200S-ME-O is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications.

Description

The ITS4200S-ME-O is a protected single channel Smart High-Side NMOS-Power Switch in a SOT-223-4 package with charge pump and CMOS compatible input. The device is monolithically integrated in Smart technology.

Product Summary

Overvoltage protection V_{SAZmin}= 47V
Operating voltage range: 11V < V_S< 45V
On-state resistance R_{DSON} = typ 150mΩ
Nominal load current I_{LNOM}= 0.7A
Operating Temperature range: Tj = -40°C to 125°C
Standby Current: I_{SSTB} = 50µA

Application

- All types of resistive, inductive and capacitive loads
- Power switch for 12V and 24V DC applications with CMOS compatible control interface
- Driver for electromagnetic relays
- Power managment for high-side-switching with low current consumption in OFF-mode

Type	Package	Marking
ITS4200S-ME-O	SOT-223-4	I200SO

2 Block Diagram and Terms

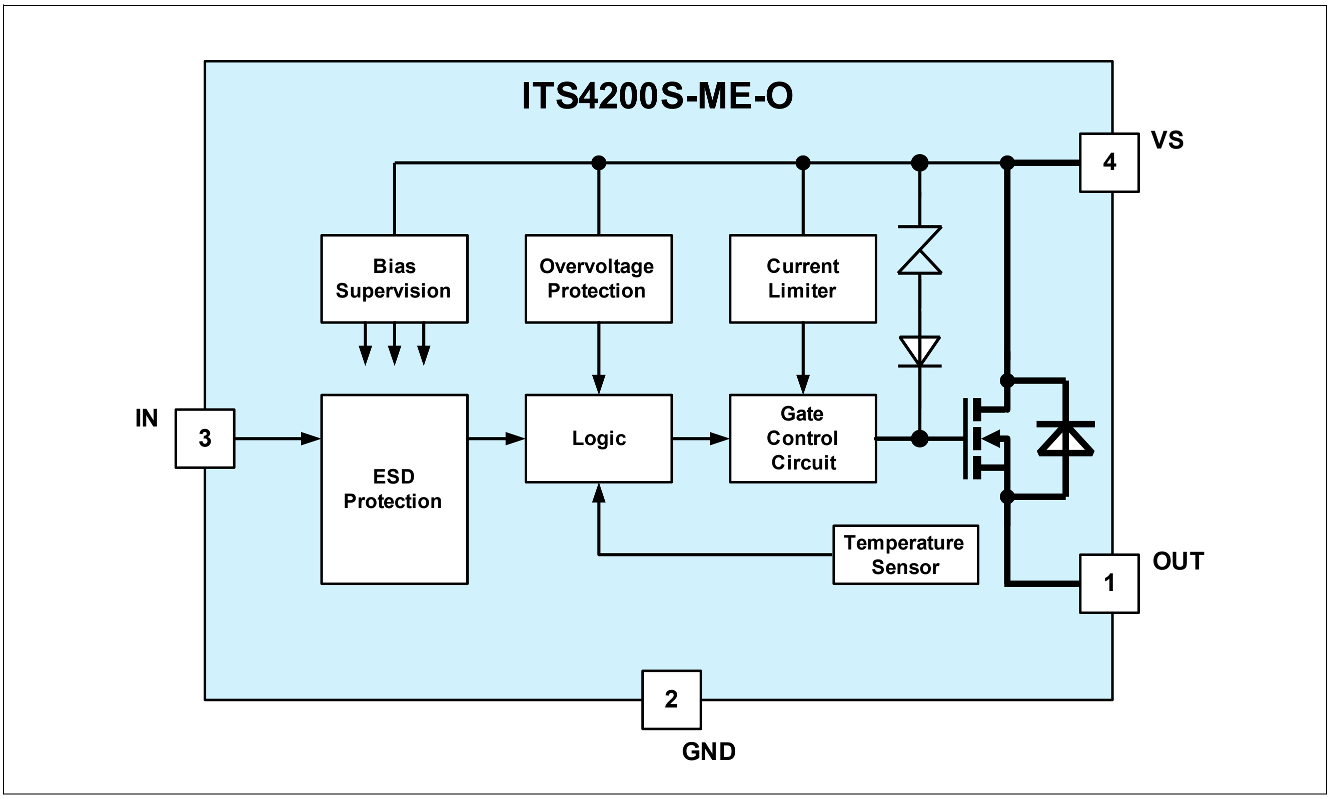


Figure 1 Block diagram

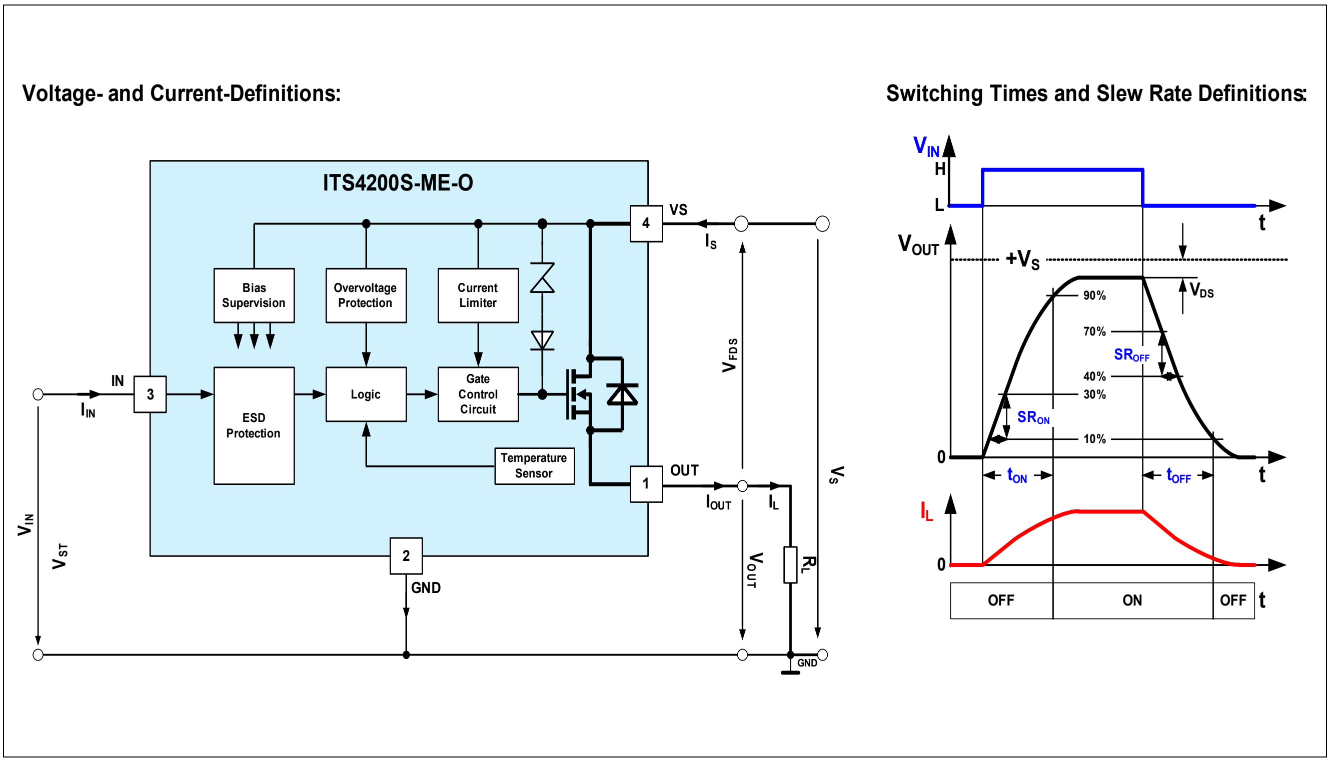


Figure 2 Terms - parameter definition

3 Pin Configuration

3.1 Pin Assignment

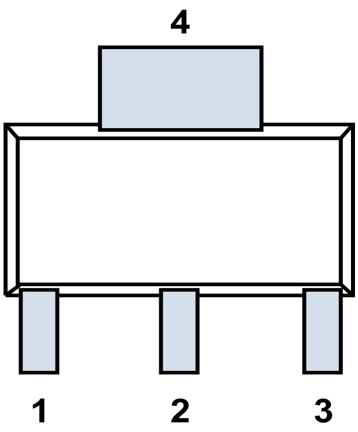


Figure 3 Pin configuration top view, SOT-223-4

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	OUT	Output to the load
2	GND	Logic ground
3	IN	Input, controles the power switch; the powerswitch is ON when high
4	VS	Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance)

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute maximum ratings at [2]Tj = 25°C unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage VS							
Voltage	V_S	–	–	48	V		4.1.1
Ground Current IGND							
Reverse Ground Current	V_S	- 0.5	–	–	A		4.1.2
Output stage OUT							
Output Current; (Short circuit current see electrical characteristics)	I_{OUT}	-1		Self limited	A		4.1.3
Input IN							
Voltage	V_{IN}	-10	–	V_S	V		4.1.4
Current	I_{IN}	-5	–	5	mA		4.1.5
Temperatures							
Junction Temperature	T_j	-40	–	125	°C		4.1.6
Storage Temperature	T_{stg}	-55	–	125	°C		4.1.7
Power dissipation							
Ta = 25 °C[1]	P_{tot}	–	–	1.4	W		4.1.8
Inductive load switch-off energy dissipation							
Tj = 125 °C; V_S=13.5V; IL= 0.5A[2]	E_{AS}	–	–	700	mJ	single pulse	4.1.9
ESD Susceptibility							
ESD susceptibility (input pin)	V_{ESD}	-1	–	1	kV	HBM[3]	4.1.10
ESD susceptibility (all other pins)	V_{ESD}	-5	–	5	kV	HBM[3]	4.1.11

1) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70mm thick) copper area for Vbb connection. PCB is vertical without blown air
2) Not subject to production test, specified by design
3) ESD susceptibility HBM according to EIA/JESD 22-A 114.

Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	V_S	11	–	45	V	V_S increasing	4.2.1
Continuous Input Voltage	V_{IN}	-3	–	V_S	V		4.2.2

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

This thermal data was generated in accordance to JEDEC JESD51 standards.

More information on www.jedec.org

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance - Junction to pin5	$R_{thj\text{-}pin5}$	–	41.8	–	K/W		4.3.1
Thermal Resistance - Junction to Ambient - 1s0p, minimal footprint	R_{thJA_1s0p}	–	155.5	–	K/W	2)	4.3.2
Thermal Resistance - Junction to Ambient - 1s0p, 300mm²	$R_{thJA\_1s0p\_300mm}$	–	76.1	–	K/W	3)	4.3.3
Thermal Resistance - Junction to Ambient - 1s0p, 600mm²	$R_{thJA\_1s0p\_600mm}$	–	67.1	–	K/W	4)	4.3.4
Thermal Resistance - Junction to Ambient - 2s2p	R_{thJA_2s2p}	–	93.6	–	K/W	5)	4.3.5
Thermal Resistance - Junction to Ambient with thermal vias - 2s2p	R_{thJA_2s2p}	–	50.0	–	K/W	6)	4.3.6

1) Not subject to production test, specified by design
2) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.
3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm^2; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.
4) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm^2; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.
5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).
6) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu. The diameter of the two vias are equal 0.3mm and have a plating of 25um with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.

5 Electrical Characteristics

Table 4 **V_S = 15V to 30V; Tj = -40°C to 125°C; all voltages with respect to ground. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at V_S = 13.5V, Tj = 25°C**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Powerstage							
NMOS ON Resistance	R_{DSON}		150	200	mΩ	I_{OUT}= 0.5A; T_j = 25°C; V_{IN}= 5V	5.0.1
NMOS ON Resistance	R_{DSON}		270	320	mΩ	I_{OUT}= 0.5A; T_j = 125°C; V_{IN}= 5V	5.0.2
Nominal Load Current; device on PCB [1]	I_{LNOM}	0.7			A	T_{pin5} = 85°C	5.0.3
Timings of Power Stages[2]							
Turn ON Time(to 90% of V_{out}); L to H transition of V_{IN}	t_{ON}		50	100	µs	V_S=15V; R_L = 47Ω	5.0.4
Turn OFF Time (to 10% of V_{out}); H to L transition of V_{IN}	t_{OFF}		75	150	µs	V_S=15V; R_L = 47Ω	5.0.5
ON-Slew Rate (10 to 30% of V_{out}); L to H transition of V_{IN}	SR_{ON}		1	2	V /µs	V_S=13.5V; R_L = 47Ω	5.0.6
OFF-Slew Rate; dV_{OUT} / dt_{ON} (70 to 40% of V_{out}); H to L transition of V_{IN}	SR_{OFF}		1	2	V /µs	V_S=13.5V; R_L = 47Ω	5.0.7
Under voltage lockout (charge pump start-stop-restart)							
Supply undervoltage; charge pump stop voltage	V_{SUV}	7.0		10.5	V	V_S decreasing	5.0.8
Supply startup voltage; Charge pump restart voltage	V_{SSU}			11	V	V_S increasing	5.0.9
Current consumption							
Operating current	I_{GND}		1.0	1.6	mA	V_{IN}= 5V	5.0.10
Standby current	I_{SSTB}		10	25	µA	V_{IN}= 0V; V_{OUT}= 0V -40°C < T_j < 85°C	5.0.11
Standby current	I_{SSTB}			50	µA	V_{IN}= 0V; V_{OUT}= 0V T_j = 125°C	5.0.12
Output leakage current	I_{OUTLK}		3.5	10	µA	V_{IN}= 0V; V_{OUT}= 0V	5.0.13
Protection functions [3]							
Initial peak short circuit current limit	I_{LSCP}			2.1	A	T_j = -40°C; V_S = 20V; V_{IN} = 5.0V; t_m =150µs	5.0.14
Initial peak short circuit current limit	I_{LSCP}		1.4		A	T_j = 25°C; V_S = 20V; V_{IN} = 5.0V; t_m =150µs	5.0.15
Initial peak short circuit current limit	I_{LSCP}	0.7			A	T_j =125°C; V_S = 20V; V_{IN} = 5.0V; t_m =150µs	5.0.16
Repetitive short circuit current limit T_j = T_{jTrip} ; see timing diagrams	I_{LSCR}		1.1		A	V_{IN} = 5.0V	5.0.17

Table 4 V_S = 15V to 30V; Tj = -40°C to 125°C; all voltages with respect to ground. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at V_S = 13.5V, Tj = 25°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output clamp at $V_{OUT} = V_S - V_{DSCL}$ (inductive load switch off)	V_{DSCL}	62	68		V	I_S = 4mA	5.0.18
Overvoltage protection $V_{OUT} = V_S - V_{ONCL}$	V_{SAZ}	47			V	I_S = 4mA	5.0.19
Thermal overload trip temperature	T_{jTrip}	135			°C		5.0.20
Thermal hysteresis	T_{HYS}		10		K		5.0.21
Reverse Battery[4)]							
Continuous reverse battery voltage	V_{SREV}	- 45			V		5.0.22
Forward voltage of the drain-source reverse diode	V_{FDS}		0.6	1.2	V	I_{FDS} = 1A; V_{IN}= 0V	5.0.23
Input interface; pin IN							
Input turn-ON threshold voltage	V_{INON}	3.0			V		5.0.24
Input turn-OFF threshold voltage	V_{INOFF}			1.8	V		5.0.25
Input threshold hysteresis	V_{INHYS}		0.2		V		5.0.26
Off state input current	I_{INOFF}	20			µA	V_{IN} < 1.8V	5.0.27
On state input current	I_{INON}	1		110	µA	$V_{IN} = V_S$ < 15V	5.0.28
Input resistance	R_{IN}	1.5	3.5	5.0	kΩ		5.0.29
Input Switch ON Delay Time	t_{dON}	150	350		µs		5.0.30

1) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm² (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position without blown air.

2) Timing values only with high slewrate input signal; otherwise slower.

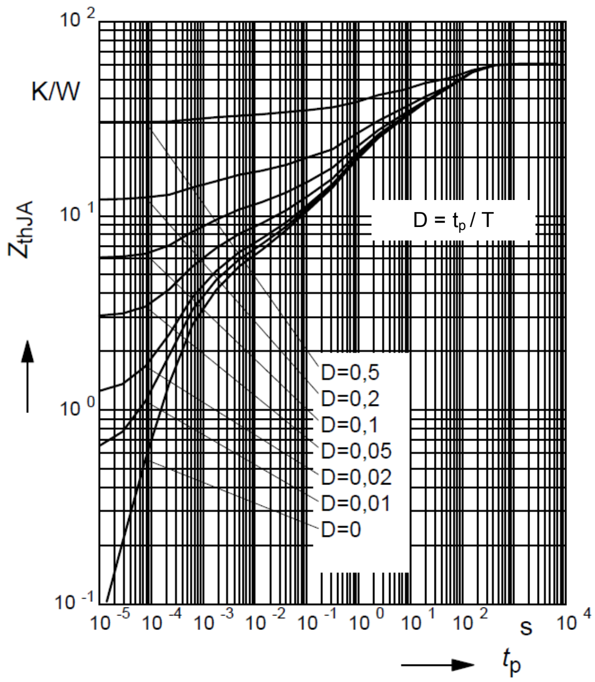
3) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4) Requires a 150W resistor in GND connection. The reverse load current trough the intrinsic drain-source diode of the power-MOS has to be limited by the connected load. Power dissipation is higher compared to normal operation due to the votage drop across the drain-source diode. The temperature protection is not functional during reverse current operation! Input current has to be limited (see max ratings).

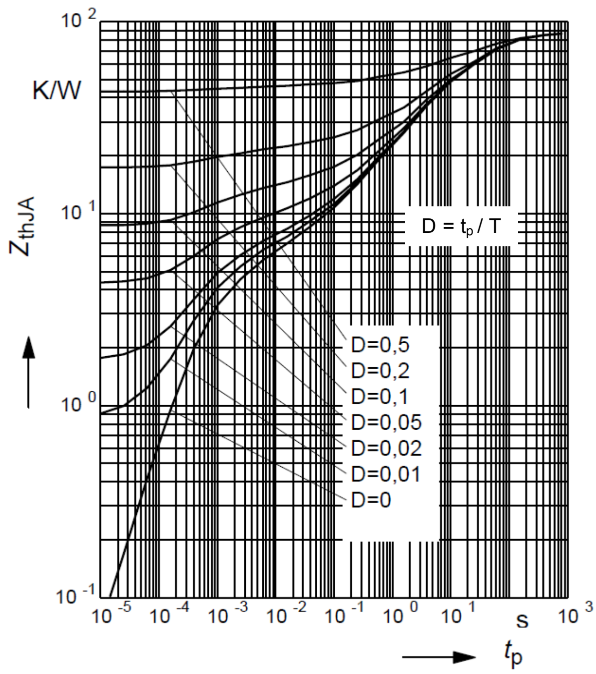
6 Typical Performance Graphs

Typical Performance Characteristics

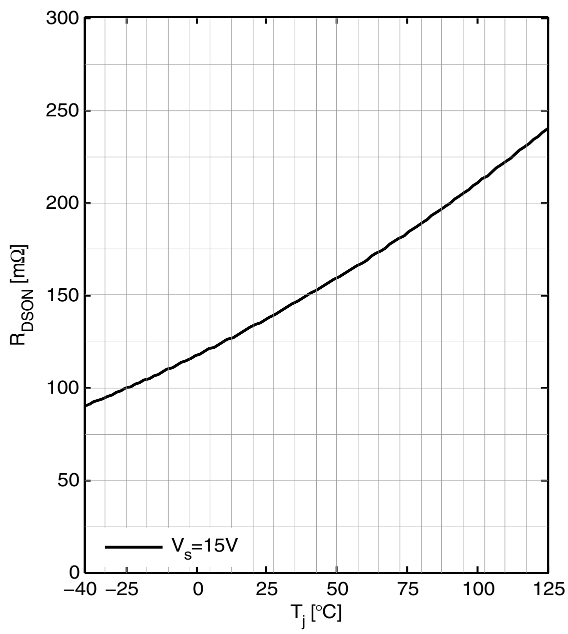
Transient Thermal Impedance Z_{thJA} versus Pulse Time t_p @ 6cm² heatsink area



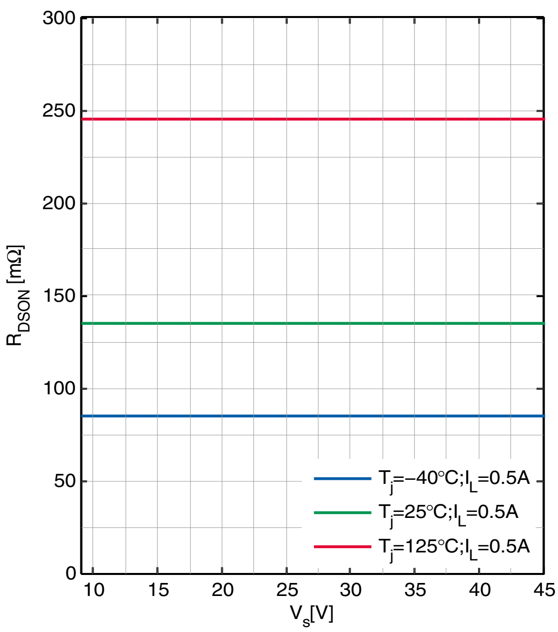
Transient Thermal Impedance Z_{thJA} versus Pulse Time t_p @ min footprint



On-Resistance R_{DSON} versus Junction Temperature T_j

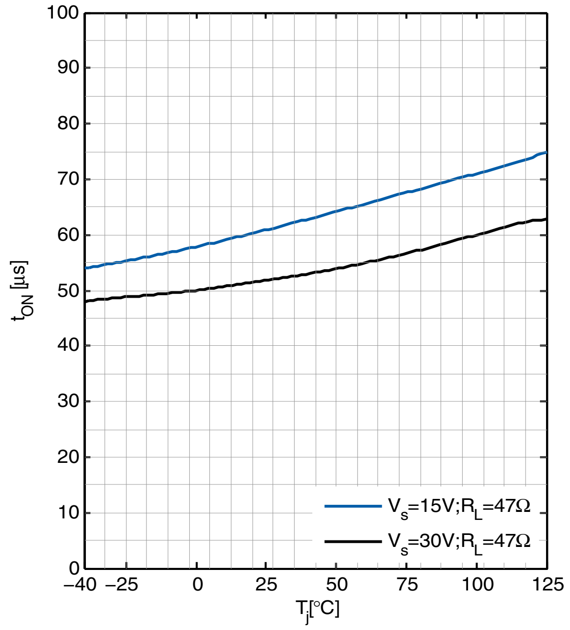


On-Resistance R_{DSON} versus Supply Voltage V_S

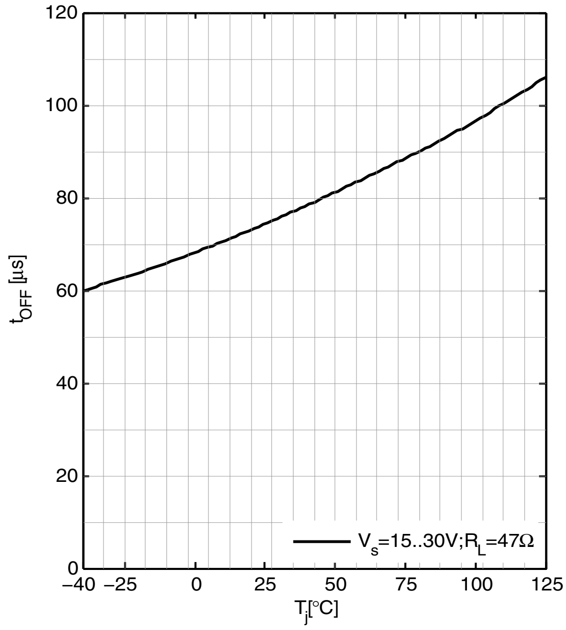


Typical Performance Characteristics

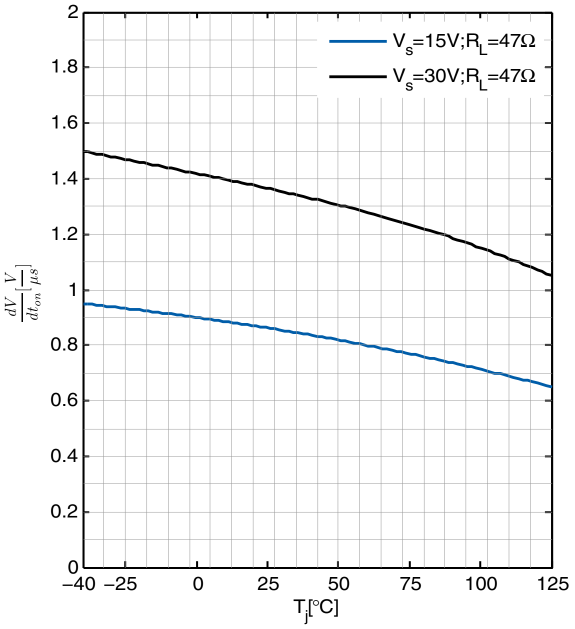
Switch ON Time t_{ON} versus Junction Temperature T_j



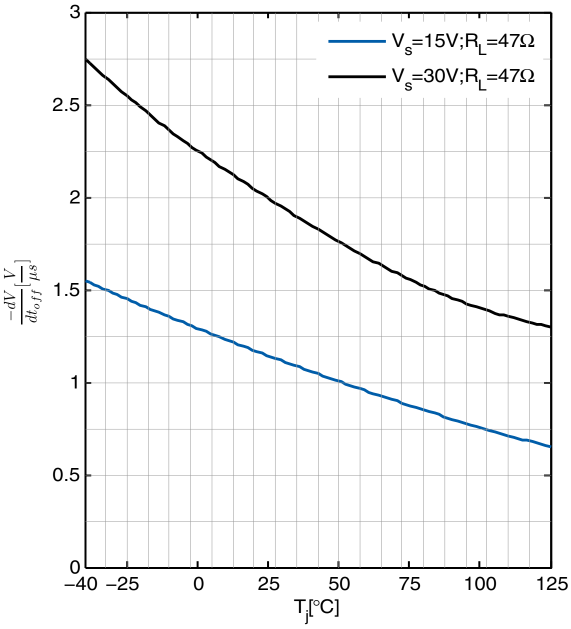
Switch OFF Time t_{OFF} versus Junction Temperature T_j



ON Slewrate SR_{ON} versus Junction Temperature T_j

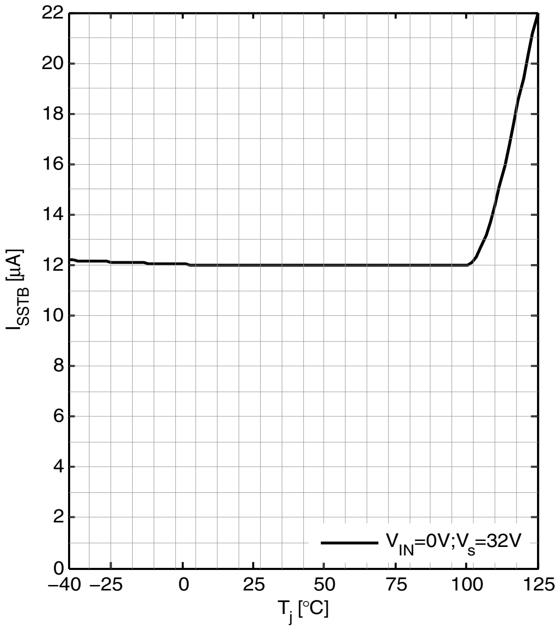


OFF Slewrate SR_{OFF} versus Junction Temperature T_j

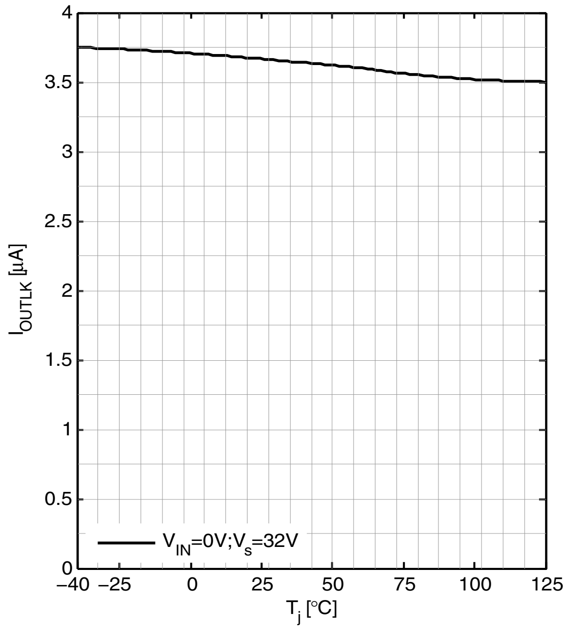


Typical Performance Characteristics

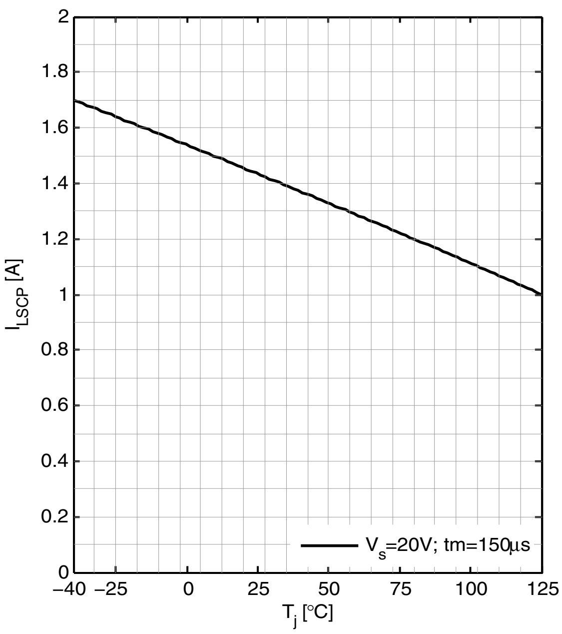
Standby Current I_{SSTB} versus Junction Temperature T_j



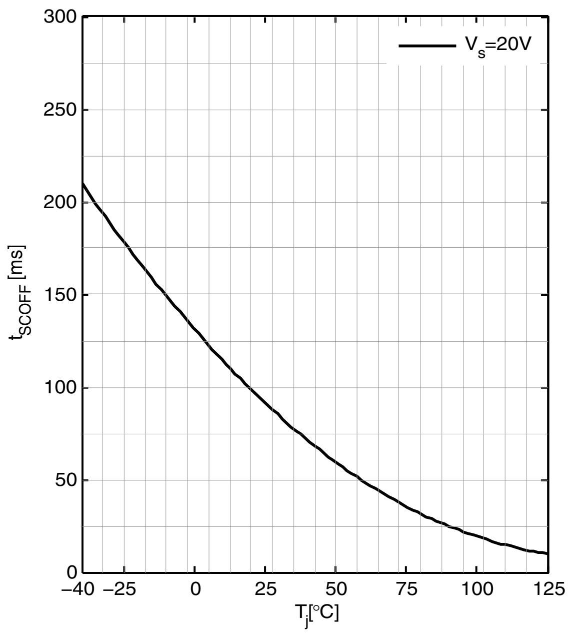
Output Leakage current I_{OUTLK} versus Junction Temperature T_j



Initial Peak Short Circuit Current Limt I_{LSCP} versus Junction TemperatureTj

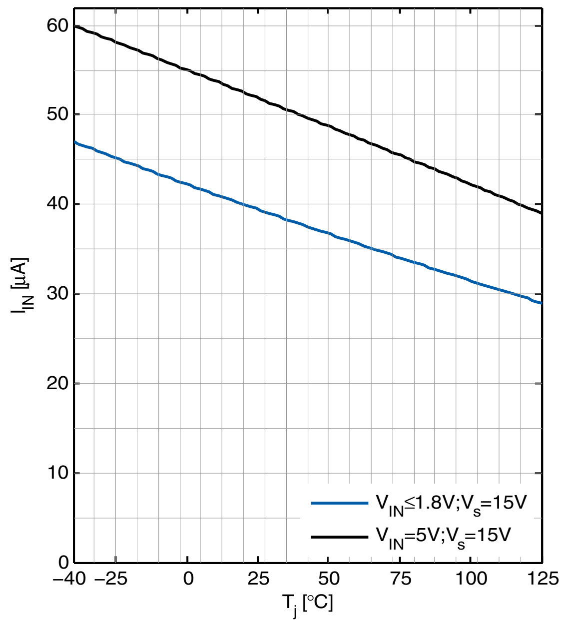


Initial Short Circuit Shutdown time t_{SCOFF} versus Junction Temperature T_j

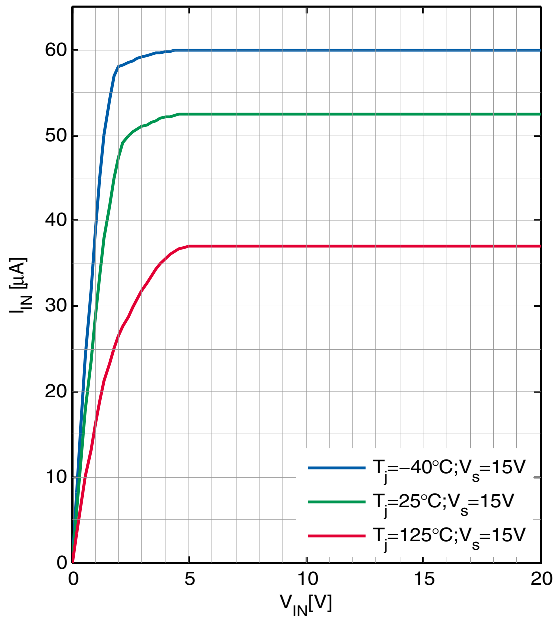


Typical Performance Characteristics

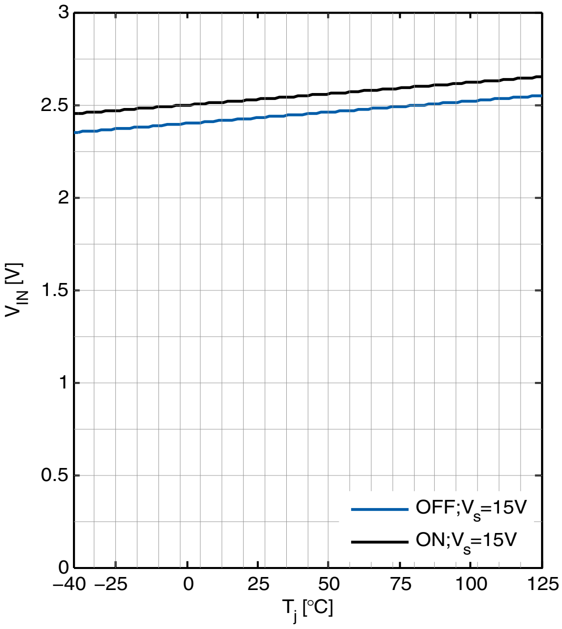
Input Current Consumption I_{IN} versus Junction Temperature T_j



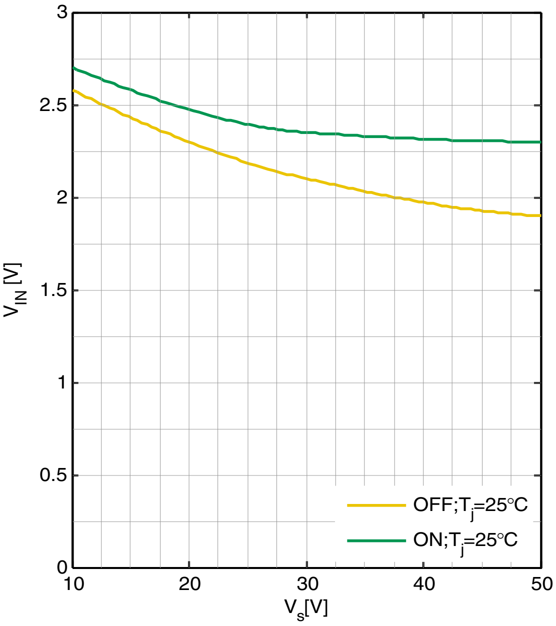
Input Current Consumption I_{IN} versus Input voltage V_{IN}



Input Threshold voltage $V_{INH,L}$ versus Junction Temperature T_j

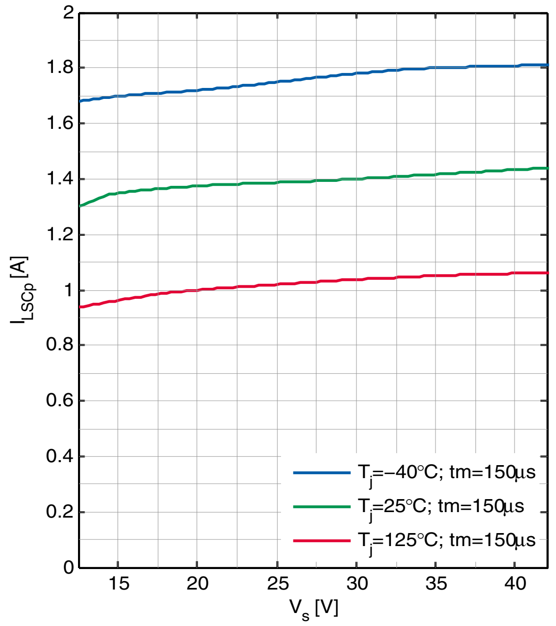


Input Threshold voltage $V_{INH,L}$ versusSupply Voltage V_S

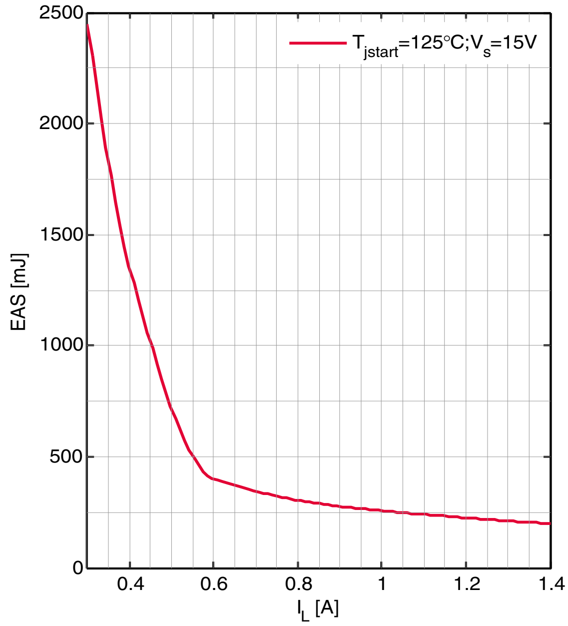


Typical Performance Characteristics

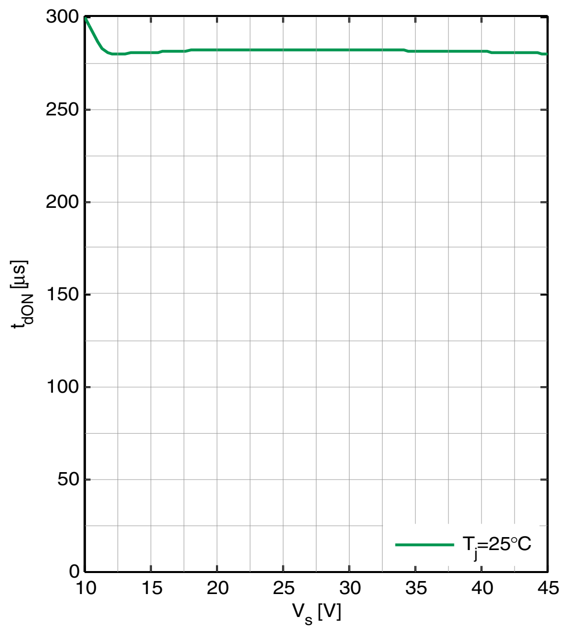
Initial Peak Short Circuit Current Limt I_{LSCP} versus Supply Voltage V_S



Max. allowable Inductive single pulse Switch-off Energy E_{AS} versus Load current I_L



Input Switch ON Delay Time t_{dON} versus Supply Voltage V_S



7 Application Information

7.1 Application Diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.

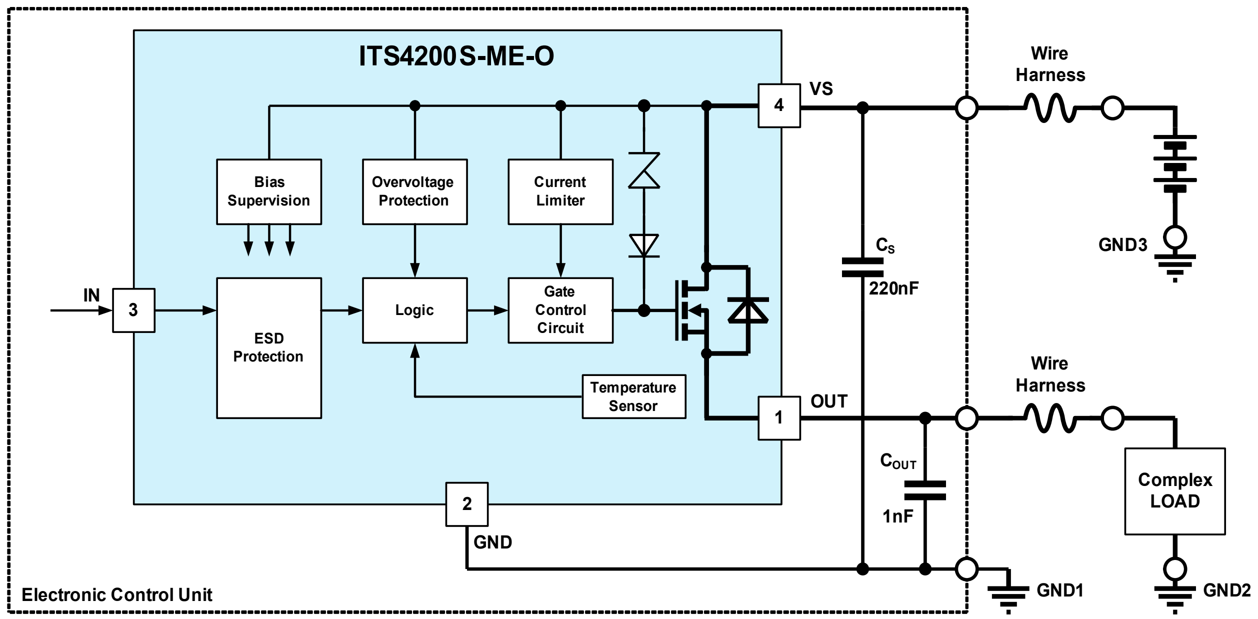


Figure 4 Application Diagram

The ITS4200S-ME-O can be connected directly to a supply network. It is recommended to place a ceramic capacitor (e.g. C_S = 220nF) between supply and GND to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS4200S-ME-O can be switched on and off with standard logic ground related logic signal at pin IN.

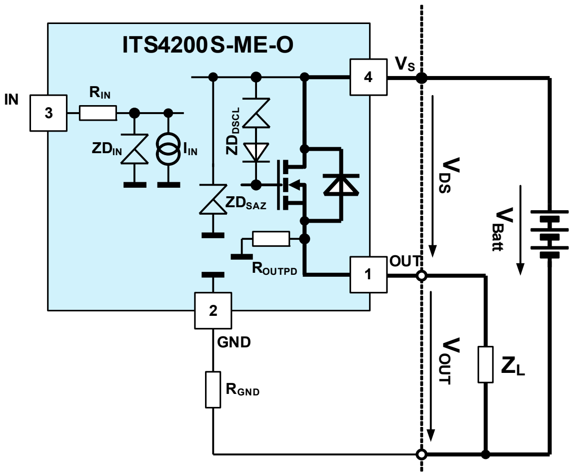
In standby mode (IN=L) the ITS4200S-ME-O is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transistion to minimize emissions. Only a small ceramic capacitor COUT=1nF is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behaviour of the **ITS4200S-ME-O** is shown. For further details please refer to application notes on the Infineon homepage.

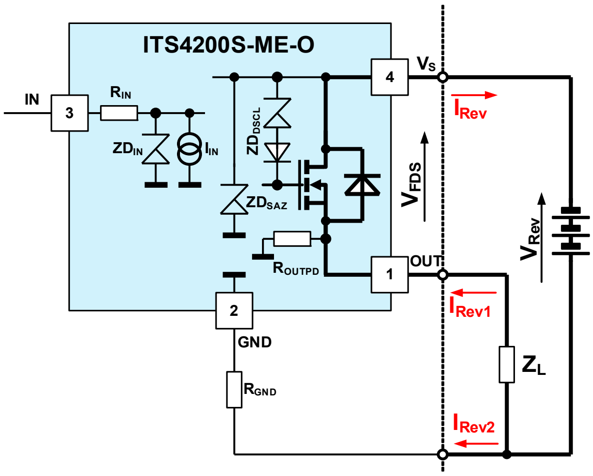
7.2 Special Feature Description

Supply over voltage:



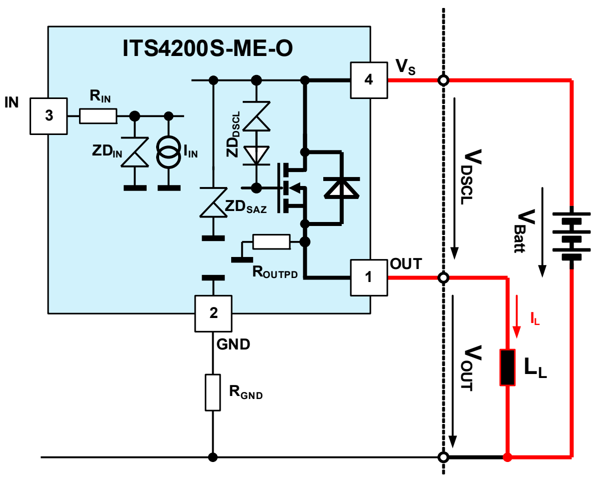
If over-voltage is applied to the V_S-Pin:
Voltage is limited to V_{ZDSAZ}; current can be calculated:
$\mathbf{I_{ZDSAZ} = (V_S - V_{ZDSAZ}) / R_{GND}}$
A typical value for RGND is 150Ω.
In case of ESD pulse on the input pin there is in both polarities a peak current $\mathbf{I_{INpeak} \sim V_{ESD} / R_{IN}}$

Supply reverse voltage:



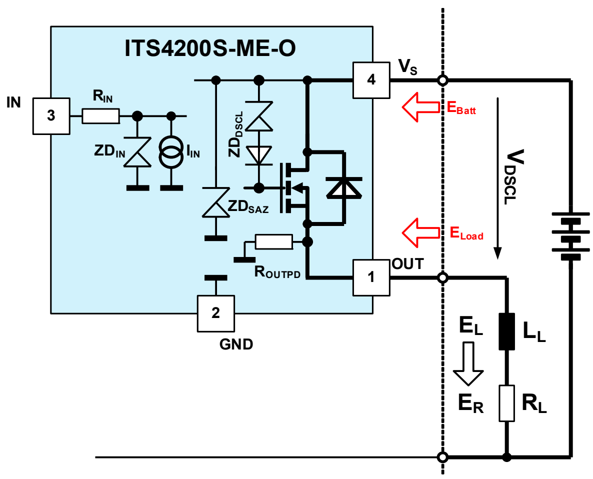
If reverse voltage is applied to the device:
1.) Current via load resistance RL:
$\mathbf{I_{Rev1} = (V_{Rev} - V_{FDS}) / R_L}$
2.) Current via Input pin IN and dignostic pin ST:
$\mathbf{I_{Rev2} = I_{ST} + I_{IN} \sim (V_{Rev} - V_{CC})/R_{IN} + (V_{Rev} - V_{CC})/R_{ST1,2}}$
Current I_{ST} must be limited with the extrernal series resistor R_{STS}. Both currents will sum up to:
$\mathbf{I_{Rev} = I_{Rev1} + I_{Rev2}}$

Drain-Source power stage clamper V_{DSCL}:



When an inductive load is switched off a current path must be established until the current is sloped down to zero (all energy removed from the inductive load). For that purpose the series combination Z_{DSCL} is connected between Gate and Drain of the power DMOS acting as an active clamp.
When the device is switched off, the voltage at OUT turns negative until V_{DSCL} is reached.
The voltage on the inductive load is the difference between V_{DSCL} and V_S.

Energy calculation:



Energy stored in the load inductance is given by:
$E_L = I_L^2 * L/2$
While demagnetizing the load inductance the energy dissipated by the Power-DMOS is:
$\mathbf{E_{AS} = E_S + E_L - E_R}$

With an approximate solution for $R_L = 0\Omega$:
$\mathbf{E_{AS} = ½ * L * I_L^2 * \{(1 - V_S / (V_S - V_{DSCL})}$

Figure 5 Special feature description

7.3 Typical Application Waveforms

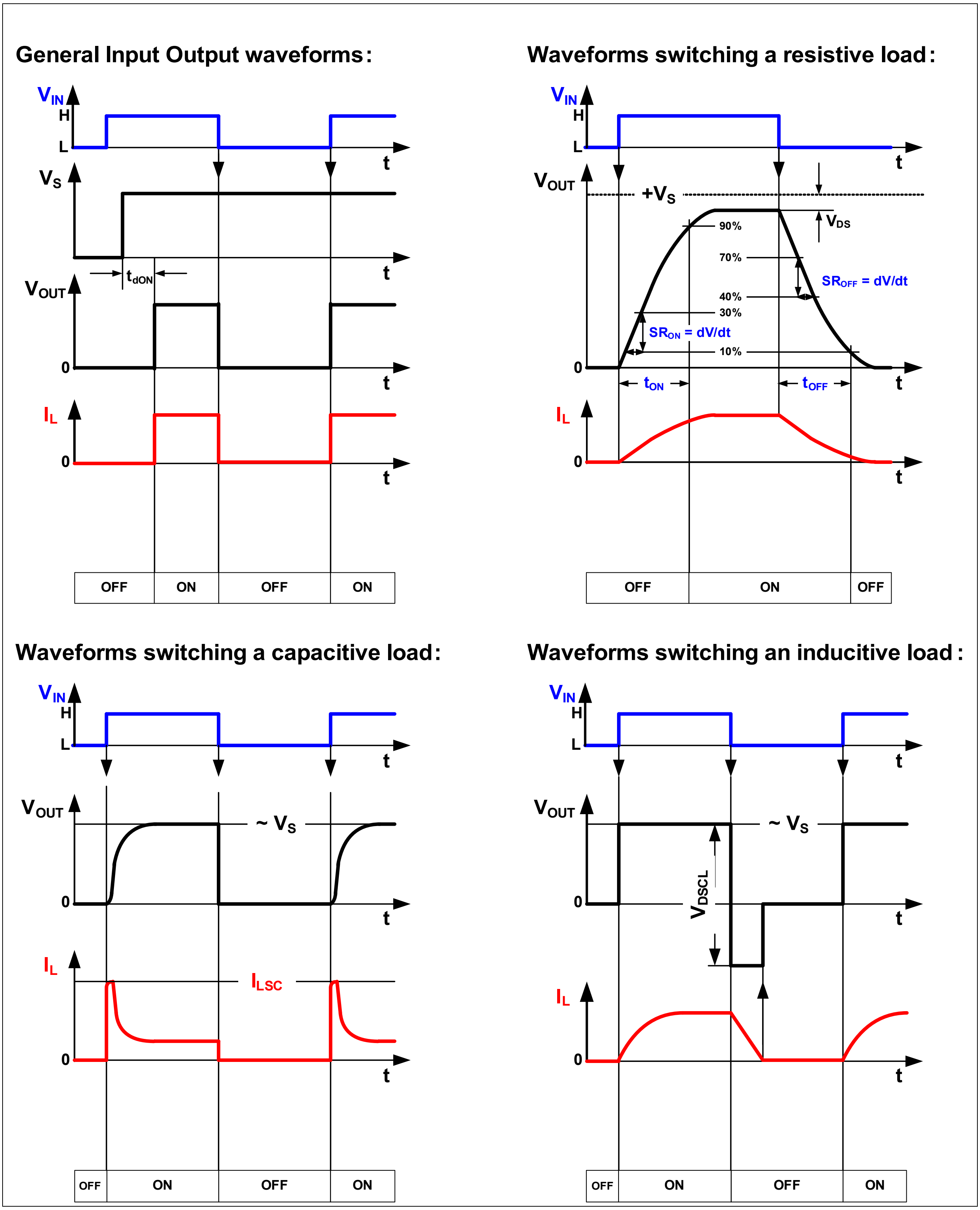


Figure 6 Typical application waveforms of the ITS4200S-ME-O

7.4 Protection Behavior

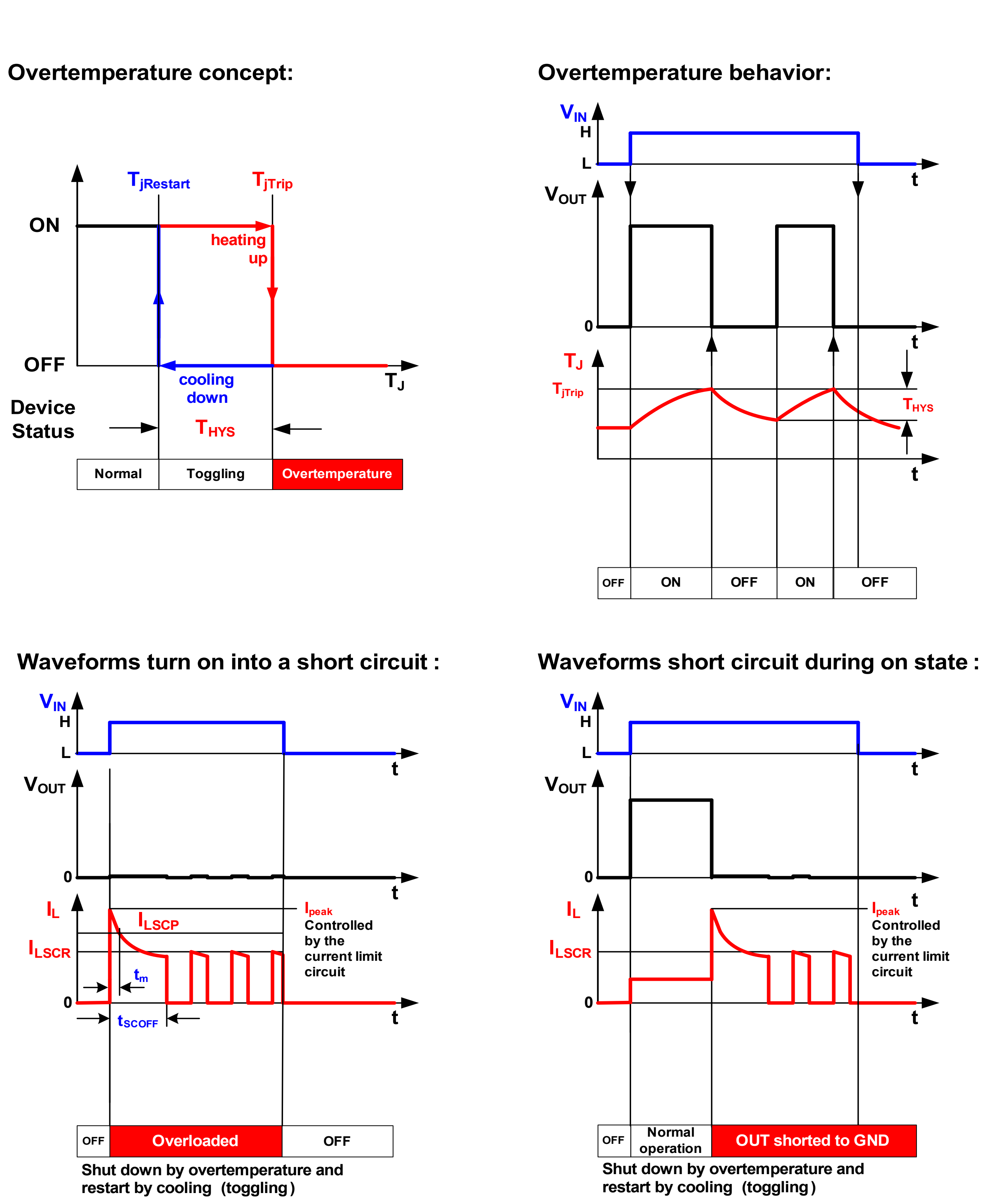


Figure 7 Protective behaviour of the ITS4200S-ME-O

8 Package outlines and footprint

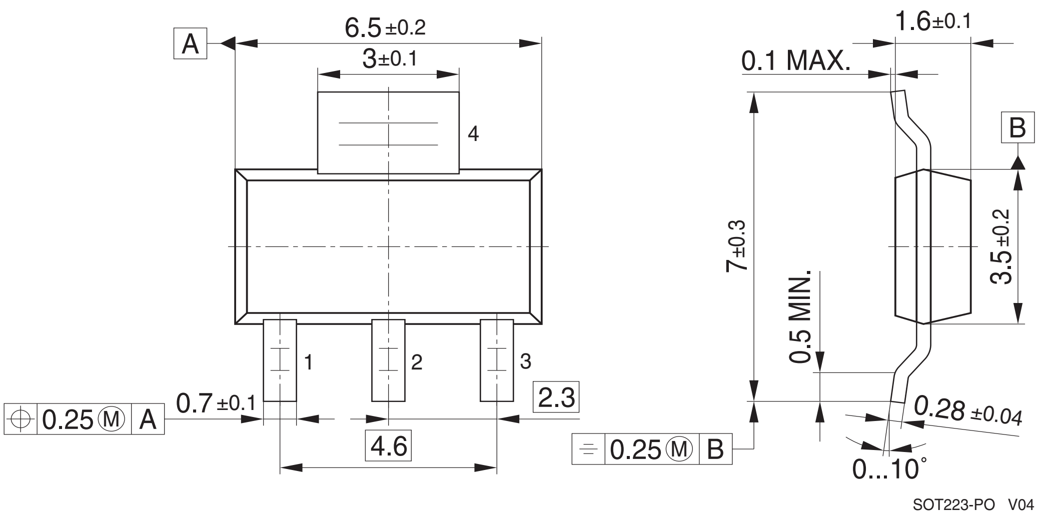


Figure 8 SOT-223-4 (Plastic Dual Small Outline Package, RoHS-Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020

9 Revision History

Revision	Date	Changes
V 1.0	12-09-01	Datasheet release

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