

## High Performance Position Servo Control IC



### Description

IRMCF143 is a high performance Flash based motion control IC designed primarily for position servo applications based on an incremental encoder. IRMCF143 is designed to achieve low cost yet high performance control solutions for advanced inverterized servo motor control. IRMCF143 contains two computation engines. One is the Flexible Motion Control Engine (MCE™) for sinusoidal Field Oriented Control (FOC) of servo motors; the other is an 8-bit high-speed microcontroller (8051). Both computation engines are integrated into one monolithic chip. The MCE™ contains a collection of control elements implemented in a dedicated computation engine such as Proportional plus Integral, Vector rotator, Angle estimator, Multiply/Divide, and Low loss SVPWM. The user can program a motion control algorithm by connecting these control elements using a graphic compiler. A unique analog/digital circuit and algorithm to fully support two leg shunt current sensing is also provided. The 8051 microcontroller performs 2-cycle instruction execution (15MIPS at 30MHz 8051CLK). The MCE and 8051 microcontroller are connected via dual port RAM for signal monitoring and command input. An advanced graphic compiler for the MCE™ is seamlessly integrated into the MATLAB/Simulink environment, while third party JTAG-based emulator tools are supported for 8051 software development. IRMCF143 comes in a 64 pin QFP package.

### Features

- MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal FOC control
- Built-in hardware peripheral for two shunt current feedback reconstruction and analog circuits
- Supports incremental encoder with Hall effect position sensor initialization
- 24bit position counter
- Position capture and compare
- Pulse + Direction input
- Brake control with gatekill input
- Loss minimization Space Vector PWM
- Three-channel analog outputs (PWM)
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Serial communication interface (UART)
- I2C/SPI serial interface
- Three general purpose timers, one capture timer
- Watchdog timer with independent internal clock
- Internal 64 Kbyte flash memory
- 3.3V single supply

### Product Summary

|                                              |                            |
|----------------------------------------------|----------------------------|
| Maximum clock input ( $f_{\text{crystal}}$ ) | 60MHz                      |
| Maximum Internal clock (SYSCLK)              | 120MHz                     |
| Maximum 8051 clock (8051CLK)                 | 30MHz                      |
| FOC computation time                         | 35 $\mu\text{sec}$ @100MHz |
| MCE™ computation data range                  | 16 bit signed              |
| 8051 Program Flash                           | 52KB                       |
| 8051/MCE Data RAM                            | 4KB                        |
| MCE Program RAM                              | 12KB                       |
| GateKill latency (digital filtered)          | 2 $\mu\text{sec}$          |
| PWM carrier frequency                        | 20 bits/ SYSCLK            |
| A/D input channels                           | 8                          |
| A/D converter resolution                     | 12 bits                    |
| A/D converter conversion speed               | 2 $\mu\text{sec}$          |
| Analog output (PWM) resolution               | 8 bits                     |
| UART baud rate (typ)                         | 57.6K bps                  |
| Encoder interface                            | 6                          |
| Number of digital I/O (max)                  | 22                         |
| Package (lead free)                          | QFP64                      |

### Ordering Information

| Orderable Part Number | Package Type | Standard Pack |          |
|-----------------------|--------------|---------------|----------|
|                       |              | Form          | Quantity |
| IRMCF143TR            | LQFP64       | Tape and Reel | 1500     |
| IRMCF143TY            | LQFP64       | Tray          | 1600     |

## Table of Contents

|           |                                                        |           |
|-----------|--------------------------------------------------------|-----------|
| <b>1</b>  | <b>Overview .....</b>                                  | <b>5</b>  |
| <b>2</b>  | <b>Pinout .....</b>                                    | <b>6</b>  |
| <b>3</b>  | <b>IRMCF143 Block Diagram and Main Functions .....</b> | <b>7</b>  |
| <b>4</b>  | <b>Application connection and Pin function .....</b>   | <b>8</b>  |
| 4.1       | 8051 Peripheral Interface Group .....                  | 9         |
| 4.2       | Motion Peripheral Interface Group .....                | 10        |
| 4.3       | Analog Interface Group .....                           | 10        |
| 4.4       | Power Interface Group .....                            | 11        |
| 4.5       | Test Interface Group .....                             | 11        |
| <b>5</b>  | <b>DC Characteristics .....</b>                        | <b>11</b> |
| 5.1       | Absolute Maximum Ratings .....                         | 12        |
| 5.2       | System Clock Frequency and Power Consumption .....     | 12        |
| 5.3       | Digital I/O DC Characteristics .....                   | 13        |
| 5.4       | PLL and Oscillator DC characteristics .....            | 14        |
| 5.5       | Analog I/O DC Characteristics .....                    | 14        |
| 5.6       | Under Voltage Lockout DC characteristics .....         | 15        |
| 5.7       | Itrip comparator DC characteristics .....              | 15        |
| 5.8       | CMEXT and AREF Characteristics .....                   | 15        |
| <b>6</b>  | <b>AC Characteristics .....</b>                        | <b>16</b> |
| 6.1       | Digital PLL AC Characteristics .....                   | 16        |
| 6.2       | Analog to Digital Converter AC Characteristics .....   | 17        |
| 6.3       | Op amp AC Characteristics .....                        | 18        |
| 6.4       | SYNC to SVPWM and A/D Conversion AC Timing .....       | 19        |
| 6.5       | GATEKILL to SVPWM AC Timing .....                      | 20        |
| 6.6       | Itrip AC Timing .....                                  | 20        |
| 6.7       | Interrupt AC Timing .....                              | 21        |
| 6.8       | I <sup>2</sup> C AC Timing .....                       | 22        |
| 6.9       | SPI AC Timing .....                                    | 23        |
|           | SPI Write AC timing .....                              | 23        |
|           | SPI Read AC Timing .....                               | 24        |
| 6.10      | UART AC Timing .....                                   | 25        |
| 6.11      | CAPTURE Input AC Timing .....                          | 26        |
| 6.12      | JTAG AC Timing .....                                   | 27        |
| <b>7</b>  | <b>I/O Structure .....</b>                             | <b>28</b> |
| <b>8</b>  | <b>Pin List .....</b>                                  | <b>31</b> |
| <b>9</b>  | <b>Package Dimensions .....</b>                        | <b>33</b> |
| <b>10</b> | <b>Part Marking Information .....</b>                  | <b>34</b> |
| <b>11</b> | <b>Qualification Information .....</b>                 | <b>34</b> |

## List of Tables

|           |                                                 |    |
|-----------|-------------------------------------------------|----|
| Table 1.  | Absolute Maximum Ratings.....                   | 12 |
| Table 2.  | System Clock Frequency.....                     | 12 |
| Table 3.  | Digital I/O DC Characteristics.....             | 13 |
| Table 4.  | PLL DC Characteristics .....                    | 14 |
| Table 5.  | Analog I/O DC Characteristics.....              | 14 |
| Table 6.  | UVcc DC Characteristics .....                   | 15 |
| Table 7.  | Itrip DC Characteristics.....                   | 15 |
| Table 8.  | CMEXT and AREF DC Characteristics .....         | 15 |
| Table 9.  | PLL AC Characteristics.....                     | 16 |
| Table 10. | A/D Converter AC Characteristics .....          | 17 |
| Table 11. | Current Sensing OP Amp AC Characteristics ..... | 18 |
| Table 12. | SYNC AC Characteristics .....                   | 19 |
| Table 13. | GATEKILL to SVPWM AC Timing .....               | 20 |
| Table 14. | Itrip AC Timing .....                           | 20 |
| Table 15. | Interrupt AC Timing.....                        | 21 |
| Table 16. | I <sup>2</sup> C AC Timing .....                | 22 |
| Table 17. | SPI Write AC Timing.....                        | 23 |
| Table 18. | SPI Read AC Timing.....                         | 24 |
| Table 19. | UART AC Timing .....                            | 25 |
| Table 20. | CAPTURE AC Timing.....                          | 26 |
| Table 21. | JTAG AC Timing.....                             | 27 |
| Table 22. | Pin List .....                                  | 32 |

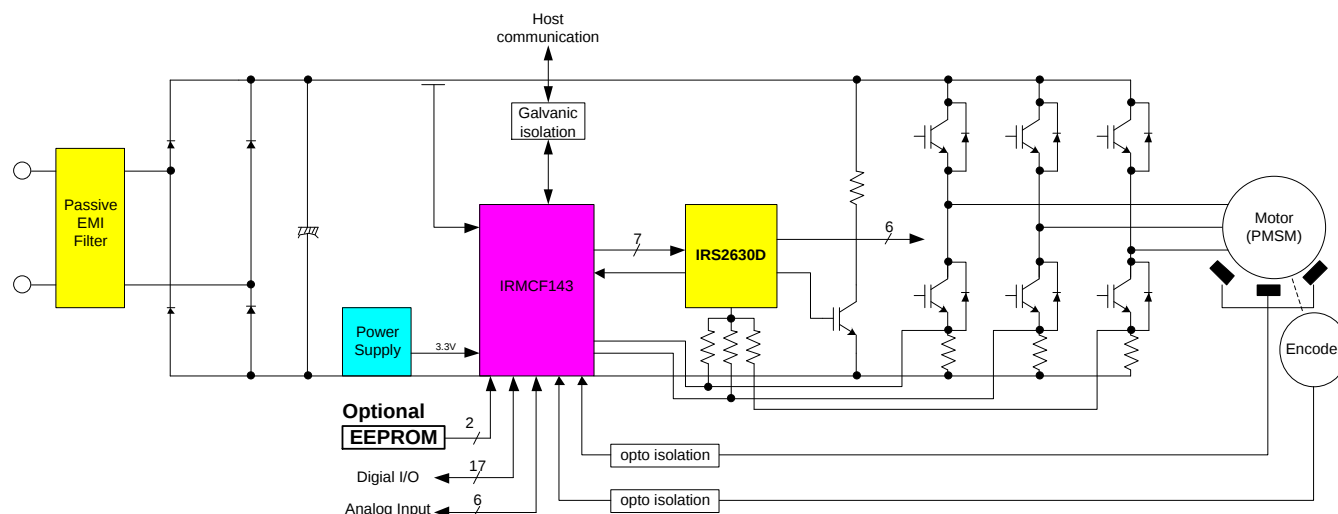
## List of Figures

|                                                                             |    |
|-----------------------------------------------------------------------------|----|
| Figure 1. Typical Application Block Diagram Using IRMCF143 .....            | 5  |
| Figure 2. Pinout of IRMCF143 .....                                          | 6  |
| Figure 3. IRMCF143 Block Diagram.....                                       | 7  |
| Figure 4. IRMCF143 Application Diagram.....                                 | 8  |
| Figure 5. Crystal circuit example .....                                     | 16 |
| Figure 6. Voltage droop and S/H hold time .....                             | 17 |
| Figure 7. Op amp output capacitor .....                                     | 18 |
| Figure 8. SYNC timing .....                                                 | 19 |
| Figure 9. Gatekill timing.....                                              | 20 |
| Figure 10. ITRIP timing.....                                                | 20 |
| Figure 11. Interrupt timing .....                                           | 21 |
| Figure 12. I <sup>2</sup> C Timing .....                                    | 22 |
| Figure 13. SPI write timing .....                                           | 23 |
| Figure 14. SPI read timing.....                                             | 24 |
| Figure 15. UART timing .....                                                | 25 |
| Figure 16. CAPTURE timing.....                                              | 26 |
| Figure 17. JTAG timing.....                                                 | 27 |
| Figure 18. PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH/BRAKE output .....           | 28 |
| Figure 19. All digital I/O except PWM output.....                           | 28 |
| Figure 20. RESET, GATEKILL I/O .....                                        | 28 |
| Figure 21. Analog input .....                                               | 29 |
| Figure 22. Analog operational amplifier output and AREF I/O structure ..... | 29 |
| Figure 23. VSS,AVSS pin I/O structure .....                                 | 29 |
| Figure 24. VDD1,VDDCAP pin I/O structure .....                              | 30 |
| Figure 25. XTAL0/XTAL1 pins structure.....                                  | 30 |

## 1 Overview

IRMCF143 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverter controlled position servo motor control applications. Unlike a traditional microcontroller or DSP, the IRMCK401 provides a built-in encoder interface and associated Field Oriented Control algorithm using the unique Flexible Motion Control Engine (MCETM) for a permanent magnet motor. It contains a flexible 24bit position counter, and separate position capture/compare unit to facilitate indexing function. The MCETM consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCK401 also employs additional PWM unit to control a brake IGBT. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using the IRMCF143.

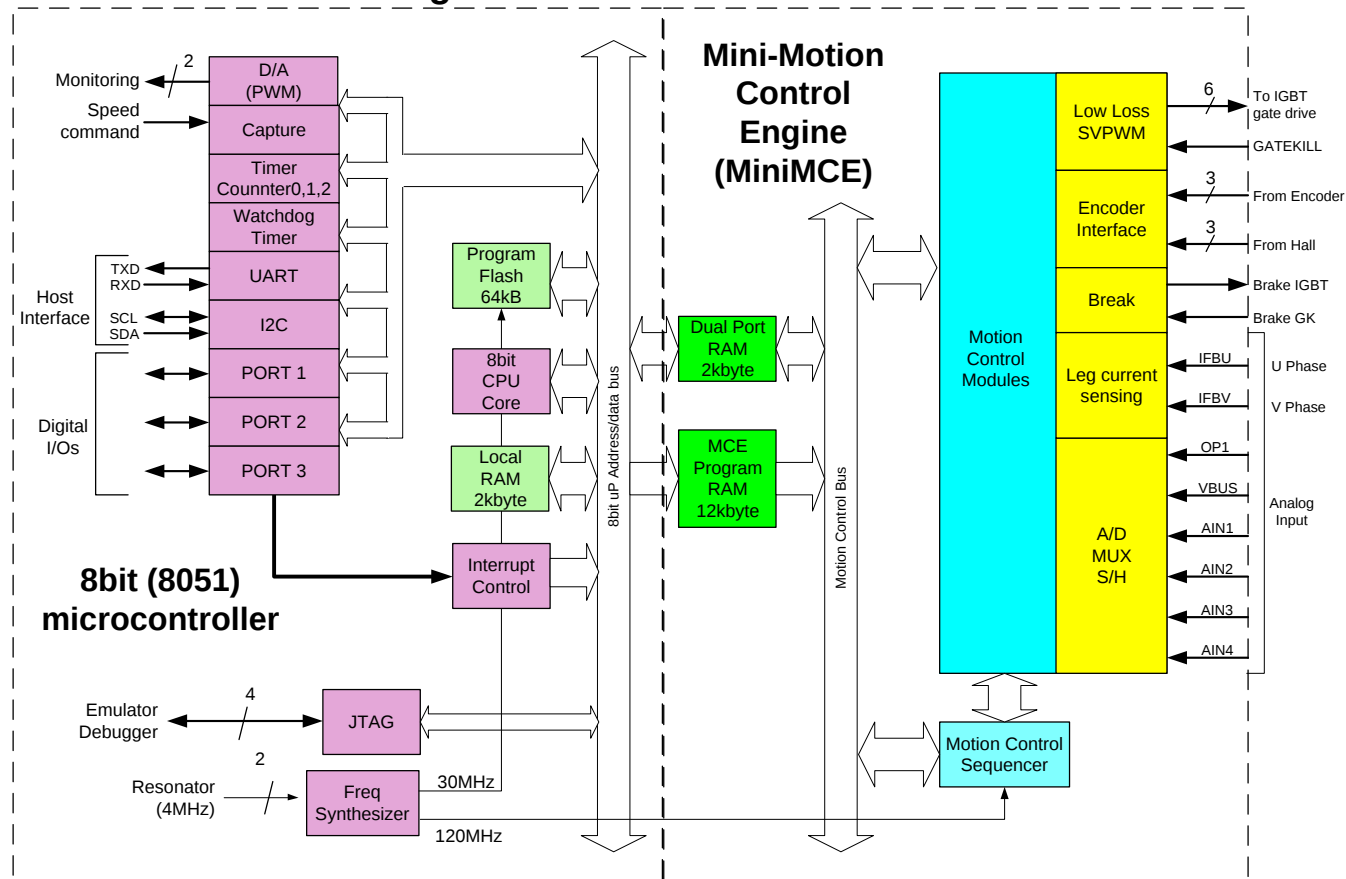
IRMCF143 contains 64K bytes of Flash program memory and comes in a 64-pin QFP package.



**Figure 1. Typical Application Block Diagram Using IRMCF143**



### 3 IRMCF143 Block Diagram and Main Functions



**Figure 3. IRMCF143 Block Diagram**

IRMCF143 contains the following functions for AC motor control applications:

#### Motion Control Engine (MCE™)

- FOC (complete Field Oriented Control)
- Proportional plus Integral block
- Low pass filter
- Differentiator and lag (high pass filter)
- Ramp
- Limit
- Angle estimate (sensorless control)
- Inverse Clark transformation
- Vector rotator
- Bit latch
- Peak detect
- Transition
- Multiply-divide (signed and unsigned)
- Adder
- Divide (signed and unsigned)
- Subtractor
- Comparator
- Counter
- Accumulator
- Switch
- Shift
- ATAN (arc tangent)
- Function block (any curve fitting, nonlinear function)
- 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
- MCE™ program memory and dual port RAM (6K byte)
- MCE™ control sequence

## 8051 microcontroller

- Two 16 bit timer/counters
- One 16 bit periodic timer
- One 16 bit watchdog timer
- One 16 bit capture timer
- Up to 24 discrete digital I/Os
- 8-channel 12 bit A/D (0 – 1.2V input)
  - Three buffered channels, two use for current sensing
  - Five unbuffered channels
- JTAG port (4 pins)
- Up to three channels of analog output (8 bit PWM)
- UART
- I<sup>2</sup>C/SPI port
- 64K byte Flash memory
- 2K byte data RAM

## 4 Application connection and Pin function

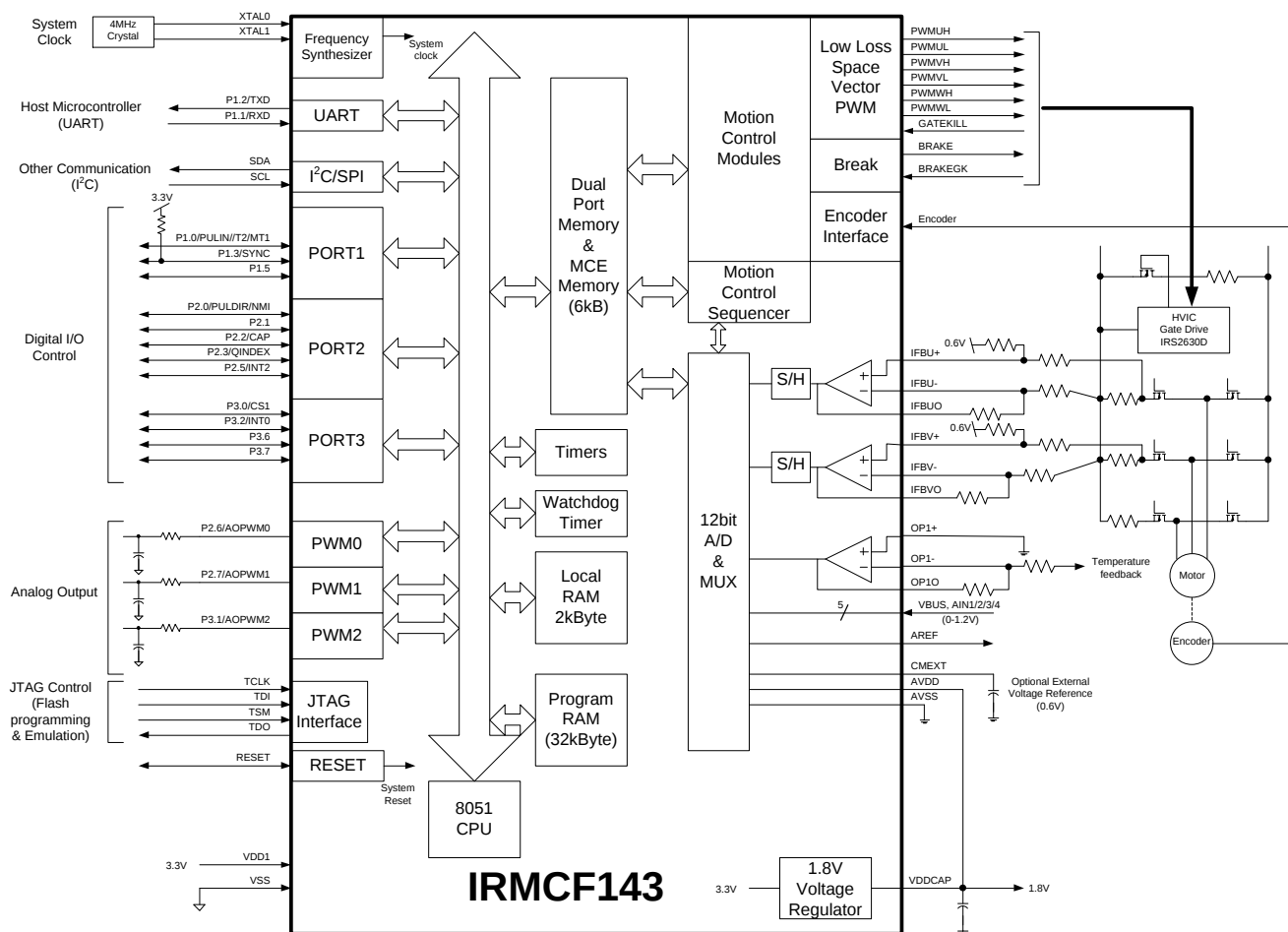


Figure 4. IRMCF143 Application Diagram

## 4.1 8051 Peripheral Interface Group

### UART Interface

|          |                                     |
|----------|-------------------------------------|
| P1.2/TXD | Output, Transmit data from IRMCF143 |
| P1.1/RXD | Input, Receive data to IRMCF143     |

### Discrete I/O Interface

|                   |                                                                                                                              |
|-------------------|------------------------------------------------------------------------------------------------------------------------------|
| P1.0/PULSE/T2/MT1 | Input/output port 1.0, can be configured as Timer/Counter 2 input or MCE pin timer 1 output, allocated by MCE as Pulse Input |
| P1.1/RXD          | Input/output port 1.1, can be configured as RXD input                                                                        |
| P1.2/TXD          | Input/output port 1.2, can be configured as TXD output                                                                       |
| P1.3/SYNC/SCK     | Input/output port 1.3, can be configured as SYNC output or SPI clock output                                                  |
| P1.4/ENC-A        | Input/output port 1.4, allocated by MCE as Encoder-A input                                                                   |
| P1.5              | Input/output port 1.5                                                                                                        |
| P1.6/ENC-B        | Input/output port 1.6, allocated by MCE as Encoder-B input                                                                   |
| P1.7/ENC-Z        | Input/output port 1.7, allocated by MCE as Encoder-Z input                                                                   |
| P2.0/DIR/NMI      | Input/output port 2.0, can be configured as non-maskable interrupt input, allocated by MCE as Direction Input                |
| P2.1              | Input/output port 2.1                                                                                                        |
| P2.2/CAP          | Input/output port 2.2, can be configured as capture timer input                                                              |
| P2.3/MATCH        | Input/output port 2.3, can be configured as MATCH output                                                                     |
| P2.5/INT2         | Input/output port 2.5, can be configured as INT2 input                                                                       |
| P2.6/AO0          | Input/output port 2.6, can be configured as AO0 output                                                                       |
| P2.7/AO1/MT2      | Input/output port 2.7, can be configured as AO1 output or MCE pin timer 2 output                                             |
| P3.0/CS1          | Input/output port 3.0, can be configured as SPI chip select 1                                                                |
| P3.1/AO2/MT3      | Input/output port 3.1, can be configured as AO2 output or MCE pin timer 3 output                                             |
| P3.2/INT0         | Input/output port 3.2, can be configured as INT0 input                                                                       |
| P3.3/HALL-3/INT1  | Input/output port 3.3, can be configured as INT1 input, allocated by MCE as Hall-3 input                                     |
| P3.4/HALL-1/T0    | Input/output port 3.4, can be configured as Timer 0 input, allocated by MCE as Hall-1 input                                  |
| P3.5/HALL-2/T1    | Input/output port 3.5, can be configured as Timer 1 input, allocated by MCE as Hall-2 input                                  |
| P3.6              | Input/output port 3.6                                                                                                        |
| P3.7              | Input/output port 3.7                                                                                                        |
| P5.1/TDI          | Input port 5.1, configured as JTAG port by default                                                                           |
| P5.2/TMS          | Input port 5.2, configured as JTAG port by default                                                                           |

### Analog Output Interface

|          |                                                                                           |
|----------|-------------------------------------------------------------------------------------------|
| P2.6/AO0 | Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency |
| P2.7/AO1 | Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency |
| P3.1/AO2 | Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency |

### Crystal Interface

|       |                              |
|-------|------------------------------|
| XTAL0 | Input, connected to crystal  |
| XTAL1 | Output, connected to crystal |

### Reset Interface

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| RESET | Input and Output, system reset, doesn't require external RC time constant |
|-------|---------------------------------------------------------------------------|

### I<sup>2</sup>C Interface

|           |                                                               |
|-----------|---------------------------------------------------------------|
| SCL/SO-SI | Output, I <sup>2</sup> C clock output, or SPI data            |
| SDA/CS0   | Input/output, I <sup>2</sup> C Data line or SPI chip select 0 |

**I<sup>2</sup>C/SPI Interface**

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| SCL/SO-SI     | Output, I <sup>2</sup> C clock output, or SPI data                          |
| SDA/CS0       | Input/output, I <sup>2</sup> C data line or SPI chip select 0               |
| P1.3/SYNC/SCK | Input/output port 1.3, can be configured as SYNC output or SPI clock output |
| P3.0/CS1      | Input/output port 3.0, can be configured as SPI chip select 1               |

**4.2 Motion Peripheral Interface Group**
**PWM**

|       |                                                                                                                        |
|-------|------------------------------------------------------------------------------------------------------------------------|
| PWMUH | Output, PWM phase U high side gate signal, internally pulled down by 58k $\Omega$ , configured high true at a power up |
| PWMUL | Output, PWM phase U low side gate signal, internally pulled down by 58k $\Omega$ , configured high true at a power up  |
| PWMVH | Output, PWM phase V high side gate signal, internally pulled down by 58k $\Omega$ , configured high true at a power up |
| PWMVL | Output, PWM phase V low side gate signal, internally pulled down by 58k $\Omega$ , configured high true at a power up  |
| PWMWH | Output, PWM phase W high side gate signal, internally pulled down by 58k $\Omega$ , configured high true at a power up |
| PWMWL | Output, PWM phase W low side gate signal, internally pulled down by 58k $\Omega$ , configured high true at a power up  |
| BRAKE | Output, BRAKE output signal, internally pulled up by 70k $\Omega$ , configured low true at a power up                  |

**Fault**

|          |                                                                                                          |
|----------|----------------------------------------------------------------------------------------------------------|
| GATEKILL | Input, upon assertion this negates all six PWM signals, active low, internally pulled up by 70k $\Omega$ |
| BRAKEGK  | Input, upon assertion, this negates BRAKE signal, active low, internally pulled up by 70k $\Omega$       |

**4.3 Analog Interface Group**

|        |                                                                                                                       |
|--------|-----------------------------------------------------------------------------------------------------------------------|
| AVSS   | Analog power return, (analog internal 1.8V power is shared with VDDCAP)                                               |
| AREF   | 0.6V buffered output                                                                                                  |
| CMEXT  | Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected.                                           |
| OP1+   | Input, Operational amplifier positive input for application sensing                                                   |
| OP1-   | Input, Operational amplifier negative input for application sensing                                                   |
| OP1O   | Output, Operational amplifier output for application sensing                                                          |
| IFBU+  | Input, Operational amplifier positive input for U phase current sensing                                               |
| IFBU-  | Input, Operational amplifier negative input for U phase current sensing                                               |
| IFBUO  | Output, Operational amplifier output for U phase current sensing                                                      |
| IFBV+  | Input, Operational amplifier positive input for V phase current sensing                                               |
| IFBV-  | Input, Operational amplifier negative input for V phase current sensing                                               |
| IFBVO  | Output, Operational amplifier output for V phase current sensing                                                      |
| VDCBUS | Input, Analog input channel (0 – 1.2V), allocated for DC bus voltage input                                            |
| AIN1   | Input, Analog input channel 1 (0 – 1.2V), allocated by MCE as speed input, needs to be pulled down to AVSS if unused  |
| AIN2   | Input, Analog input channel 2 (0 – 1.2V), allocated by MCE as torque input, needs to be pulled down to AVSS if unused |

|      |                                                                                     |
|------|-------------------------------------------------------------------------------------|
| AIN3 | Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused |
| AIN4 | Input, Analog input channel 4 (0 – 1.2V), needs to be pulled down to AVSS if unused |

#### 4.4 Power Interface Group

|        |                                                                                                                                                                                                                                                    |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD1   | Digital power (3.3V)                                                                                                                                                                                                                               |
| VDDCAP | Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally<br><b>Note:</b> The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin. |
| VSS    | Digital common                                                                                                                                                                                                                                     |

#### 4.5 Test Interface Group

|          |                                            |
|----------|--------------------------------------------|
| P5.2/TMS | JTAG test mode input or input digital port |
| TDO      | JTAG data output                           |
| P5.1/TDI | JTAG data input, or input digital port     |
| TCK      | JTAG test clock                            |

#### 4.6 Incremental Encoder/Hall sensor Group

|                  |                             |
|------------------|-----------------------------|
| P1.4/ENC-A       | Incremental Encoder A input |
| P1.6/ENC-B       | Incremental Encoder B input |
| P1.7/ENC-Z       | Incremental Encoder Z input |
| P3.3/HALL-3/INT1 | Hall sensor 3 input         |
| P3.4/HALL-1/T0   | Hall sensor 1 input         |
| P3.5/HALL-2/T1   | Hall sensor 2 input         |

## 5 DC Characteristics

### 5.1 Absolute Maximum Ratings

| Symbol    | Parameter             | Min    | Typ | Max    | Condition       |
|-----------|-----------------------|--------|-----|--------|-----------------|
| $V_{DD1}$ | Supply Voltage        | -0.3 V | -   | 3.6 V  | Respect to VSS  |
| $V_{IA}$  | Analog Input Voltage  | -0.3 V | -   | 1.98 V | Respect to AVSS |
| $V_{ID}$  | Digital Input Voltage | -0.3 V | -   | 6.0 V  | Respect to VSS  |
| $T_A$     | Ambient Temperature   | -40 °C | -   | 85 °C  |                 |
| $T_S$     | Storage Temperature   | -65 °C | -   | 150 °C |                 |

**Table 1. Absolute Maximum Ratings**

**Caution:** Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

### 5.2 System Clock Frequency and Power Consumption

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ .  $V_{DD1}=3.3\text{V}$ , Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol | Parameter         | Min | Typ               | Max | Unit |
|--------|-------------------|-----|-------------------|-----|------|
| SYCLK  | System Clock      | 32  | -                 | 120 | MHz  |
| $P_D$  | Power consumption |     | 100 <sup>1)</sup> | -   | mW   |

**Table 2. System Clock Frequency**

Note 1) The value is based on the condition of MCE clock=100MHz, 8051 clock 20MHz with a actual motor running by a typical MCE application program and 8051 code.

### 5.3 Digital I/O DC Characteristics

| Symbol          | Parameter                 | Min     | Typ         | Max             | Condition               |
|-----------------|---------------------------|---------|-------------|-----------------|-------------------------|
| $V_{DD1}$       | Supply Voltage            | 3.0 V   | 3.3 V       | 3.6 V           | Recommended             |
| $V_{IL}$        | Input Low Voltage         | -0.3 V  | -           | 0.8 V           | Recommended             |
| $V_{IH}$        | Input High Voltage        | 2.0 V   |             | 3.6 V           | Recommended             |
| $C_{IN}$        | Input capacitance         | -       | 3.6 pF      | -               | (1)                     |
| $I_L$           | Input leakage current     |         | $\pm 10$ nA | $\pm 1$ $\mu$ A | $V_O = 3.3$ V or 0 V    |
| $I_{OL1}^{(2)}$ | Low level output current  | 8.9 mA  | 13.2 mA     | 15.2 mA         | $V_{OL} = 0.4$ V<br>(1) |
| $I_{OH1}^{(2)}$ | High level output current | 12.4 mA | 24.8 mA     | 38 mA           | $V_{OH} = 2.4$ V<br>(1) |
| $I_{OL2}^{(3)}$ | Low level output current  | 17.9 mA | 26.3 mA     | 33.4 mA         | $V_{OL} = 0.4$ V<br>(1) |
| $I_{OH2}^{(3)}$ | High level output current | 24.6 mA | 49.5 mA     | 81 mA           | $V_{OH} = 2.4$ V<br>(1) |

**Table 3. Digital I/O DC Characteristics**

Note:

- (1) Data guaranteed by design.
- (2) Applied to SCL/SO-SI, SDA/CS0 pins.
- (3) Applied to all digital I/O pins except SCL/SO-SI and SDA/CS0 pins.

## 5.4 PLL and Oscillator DC characteristics

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ ,  $V_{DD1} = 3.3\text{V}$ , Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol              | Parameter                                  | Min                   | Typ | Max                   | Condition                           |
|---------------------|--------------------------------------------|-----------------------|-----|-----------------------|-------------------------------------|
| $V_{IL\text{ OSC}}$ | Oscillator (XTAL0,1)<br>Input Low Voltage  | 0                     | -   | $0.2 \cdot V_{DDCAP}$ | $V_{DDCAP}$ = voltage at VDDCAP pin |
| $V_{IH\text{ OSC}}$ | Oscillator (XTAL0,1)<br>Input High Voltage | $0.8 \cdot V_{DDCAP}$ | -   | $V_{DDCAP}$           | $V_{DDCAP}$ = voltage at VDDCAP pin |

**Table 4 PLL DC Characteristics**

## 5.5 Analog I/O DC Characteristics

- OP amps for application sensing (OP1+, OP1-, OP1O, OP2+, OP2-, OP2O, OP3+, OP3-, OP3O)

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ ,  $V_{DD1} = 3.3\text{V}$ , Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                        | Min                  | Typ               | Max           | Condition                             |
|----------------|----------------------------------|----------------------|-------------------|---------------|---------------------------------------|
| $V_{OFFSET}$   | Input Offset Voltage             | -                    | -                 | 26 mV         | $V_{AVDD} = 1.8\text{ V}$             |
| $V_I$          | Input Voltage Range              | 0 V                  |                   | 1.2 V         | Recommended                           |
| $V_{OUTSW}$    | OP amp output<br>operating range | 50 mV <sup>(1)</sup> | -                 | 1.2 V         | $V_{AVDD} = 1.8\text{ V}$             |
| $C_{IN}$       | Input capacitance                | -                    | 3.6 pF            | -             | (1)                                   |
| $R_{FDBK}$     | OP amp feedback<br>resistor      | 5 k $\Omega$         | -                 | 20 k $\Omega$ | Requested<br>between IFBO and<br>IFB- |
| OP $G_{AINCL}$ | Operating Close loop<br>Gain     | 80 db                | -                 | -             | (1)                                   |
| CMRR           | Common Mode<br>Rejection Ratio   | -                    | 80 db             | -             | (1)                                   |
| $I_{SRC}$      | Op amp output source<br>current  | -                    | 1 mA              | -             | $V_{OUT} = 0.6\text{ V}$<br>(1)       |
| $I_{SNK}$      | Op amp output sink<br>current    | -                    | 100 $\mu\text{A}$ | -             | $V_{OUT} = 0.6\text{ V}$<br>(1)       |

**Table 5. Analog I/O DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.6 Under Voltage Lockout DC characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter                     | Min    | Typ    | Max    | Condition |
|------------|-------------------------------|--------|--------|--------|-----------|
| $UV_{CC+}$ | UVcc positive going Threshold | 2.78 V | 3.04 V | 3.23 V | (1)       |
| $UV_{CC-}$ | UVcc negative going Threshold | 2.78 V | 2.97 V | 3.23 V |           |
| $UV_{CCH}$ | UVcc Hysteresys               | -      | 73 mV  | -      | (1)       |

**Table 6. UVcc DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.7 Itrip comparator DC characteristics

Unless specified,  $V_{DD1}=3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$ .

| Symbol      | Parameter                      | Min | Typ   | Max | Condition                |
|-------------|--------------------------------|-----|-------|-----|--------------------------|
| $I_{trip+}$ | Itrip positive going Threshold | -   | 1.22V | -   | $V_{DD1} = 3.3\text{ V}$ |
| $I_{trip-}$ | Itrip negative going Threshold | -   | 1.10V | -   | $V_{DD1} = 3.3\text{ V}$ |
| $I_{tripH}$ | Itrip Hysteresys               | -   | 120mV | -   |                          |

**Table 7. Itrip DC Characteristics**

## 5.8 CMEXT and AREF Characteristics

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ . Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol       | Parameter                        | Min    | Typ    | Max    | Condition                 |
|--------------|----------------------------------|--------|--------|--------|---------------------------|
| $V_{CM}$     | CMEXT voltage                    | 495 mV | 600 mV | 700 mV | $V_{VDD1} = 3.3\text{ V}$ |
| $V_{AREF}$   | Buffer Output Voltage            | 495 mV | 600 mV | 700 mV | $V_{VDD1} = 3.3\text{ V}$ |
| $\Delta V_o$ | Load regulation ( $V_{DC}-0.6$ ) | -      | 1 mV   | -      | (1)                       |
| PSRR         | Power Supply Rejection Ratio     | -      | 75 db  | -      | (1)                       |

**Table 8. CMEXT and AREF DC Characteristics**

Note:

(1) Data guaranteed by design.

## 6 AC Characteristics

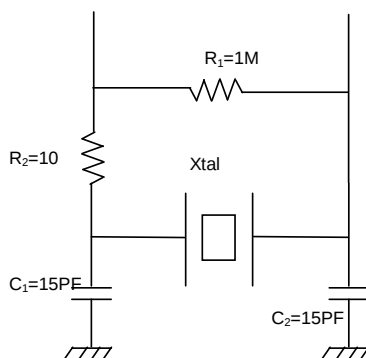
### 6.1 Digital PLL AC Characteristics

| Symbol      | Parameter                   | Min                  | Typ      | Max           | Condition                            |
|-------------|-----------------------------|----------------------|----------|---------------|--------------------------------------|
| $F_{CLKIN}$ | Crystal input frequency     | 3.2 MHz              | 4 MHz    | 60 MHz        | <sup>(1)</sup><br>(see figure below) |
| $F_{PLL}$   | Internal clock frequency    | 32 MHz               | 50 MHz   | 128 MHz       | <sup>(1)</sup>                       |
| $F_{LWPP}$  | Sleep mode output frequency | $F_{CLKIN} \div 256$ | -        | -             | <sup>(1)</sup>                       |
| $J_S$       | Short time jitter           | -                    | 200 psec | -             | <sup>(1)</sup>                       |
| $D$         | Duty cycle                  | -                    | 50 %     | -             | <sup>(1)</sup>                       |
| $T_{LOCK}$  | PLL lock time               | -                    | -        | 500 $\mu$ sec | <sup>(1)</sup>                       |

**Table 9. PLL AC Characteristics**

Note:

(1) Data guaranteed by design.



**Figure 5. Crystal circuit example**

## 6.2 Analog to Digital Converter AC Characteristics

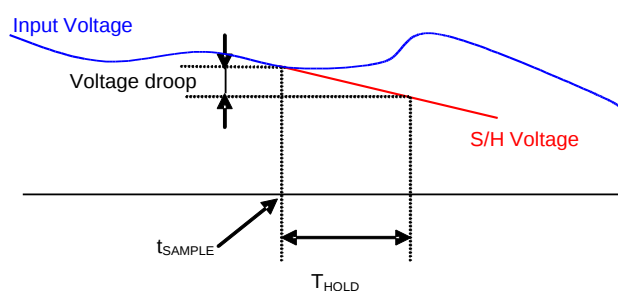
Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol            | Parameter                     | Min | Typ | Max                  | Condition                                         |
|-------------------|-------------------------------|-----|-----|----------------------|---------------------------------------------------|
| $T_{\text{CONV}}$ | Conversion time               | -   | -   | 2.05 $\mu\text{sec}$ | (1)                                               |
| $T_{\text{HOLD}}$ | Sample/Hold maximum hold time | -   | -   | 10 $\mu\text{sec}$   | Voltage droop $\leq 15$ LSB<br>(see figure below) |

**Table 10 . A/D Converter AC Characteristics**

Note:

(1) Data guaranteed by design.



**Figure 6. Voltage droop and S/H hold time**

### 6.3 Op amp AC Characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

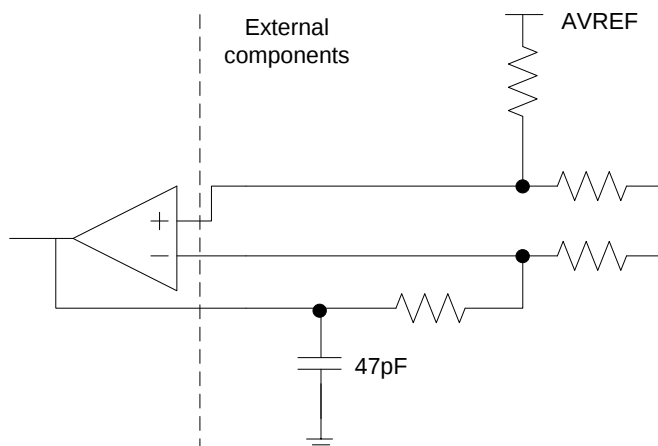
| Symbol     | Parameter          | Min | Typ                   | Max | Condition                                                     |
|------------|--------------------|-----|-----------------------|-----|---------------------------------------------------------------|
| $OP_{SR}$  | OP amp slew rate   | -   | 10 V/ $\mu\text{sec}$ | -   | $V_{DD1} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup> |
| $OP_{IMP}$ | OP input impedance | -   | $10^8\ \Omega$        | -   | <sup>(1)</sup> <sup>(2)</sup>                                 |
| $T_{SET}$  | Settling time      | -   | 400 ns                | -   | $V_{DD1} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup> |

**Table 11 Current Sensing OP Amp AC Characteristics**

Note:

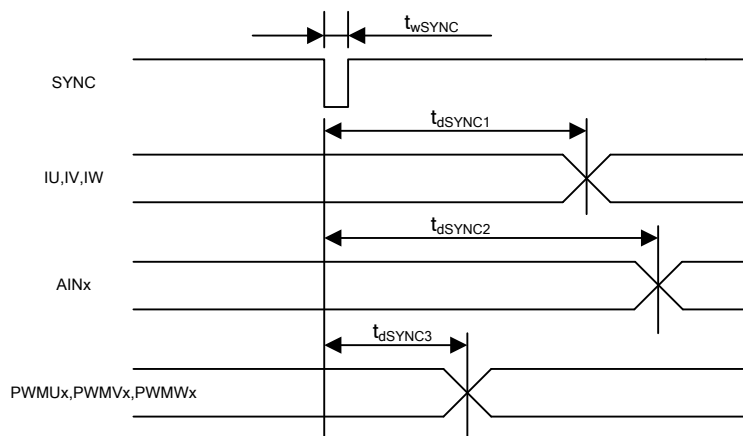
(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 7.



**Figure 7. Op amp output capacitor**

## 6.4 SYNC to SVPWM and A/D Conversion AC Timing



**Figure 8. SYNC timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

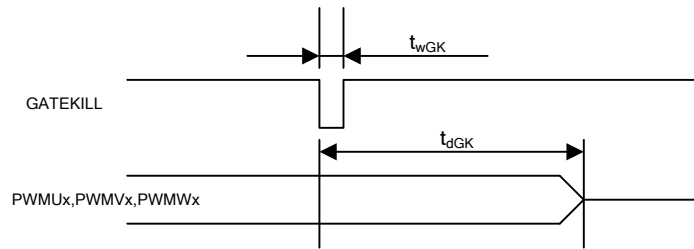
| Symbol              | Parameter                                      | Min | Typ | Max | Unit                  |
|---------------------|------------------------------------------------|-----|-----|-----|-----------------------|
| $t_{w\text{SYNC}}$  | SYNC pulse width                               | -   | 32  | -   | SYSCLK                |
| $t_{d\text{SYNC1}}$ | SYNC to current feedback conversion time       | -   | -   | 100 | SYSCLK                |
| $t_{d\text{SYNC2}}$ | SYNC to AIN0-AIN4 analog input conversion time | -   | -   | 200 | SYSCLK <sup>(1)</sup> |
| $t_{d\text{SYNC3}}$ | SYNC to PWM output delay time                  | -   | -   | 2   | SYSCLK                |

**Table 12. SYNC AC Characteristics**

Note:

(1) AIN3, AIN4 and OP1O channels are converted once every 3 SYNC events

## 6.5 GATEKILL to SVPWM AC Timing



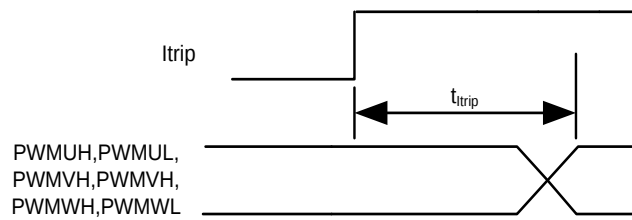
**Figure 9. Gatekill timing**

Unless specified, Ta = 25°C.

| Symbol    | Parameter                    | Min | Typ | Max | Unit  |
|-----------|------------------------------|-----|-----|-----|-------|
| $t_{wGK}$ | GATEKILL pulse width         | 32  | -   | -   | SYCLK |
| $t_{dGK}$ | GATEKILL to PWM output delay | -   | -   | 100 | SYCLK |

**Table 13. GATEKILL to SVPWM AC Timing**

## 6.6 Itrip AC Timing



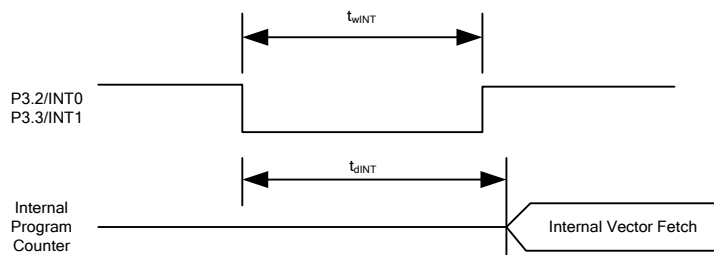
**Figure 10. ITRIP timing**

Unless specified, Ta = 25°C.

| Symbol      | Parameter               | Min | Typ | Max                 | Unit       |
|-------------|-------------------------|-----|-----|---------------------|------------|
| $t_{ITRIP}$ | Itrip propagation delay | -   | -   | 100(sysclk)+1.0usec | SYCLK+usec |

**Table 14. Itrip AC Timing**

## 6.7 Interrupt AC Timing



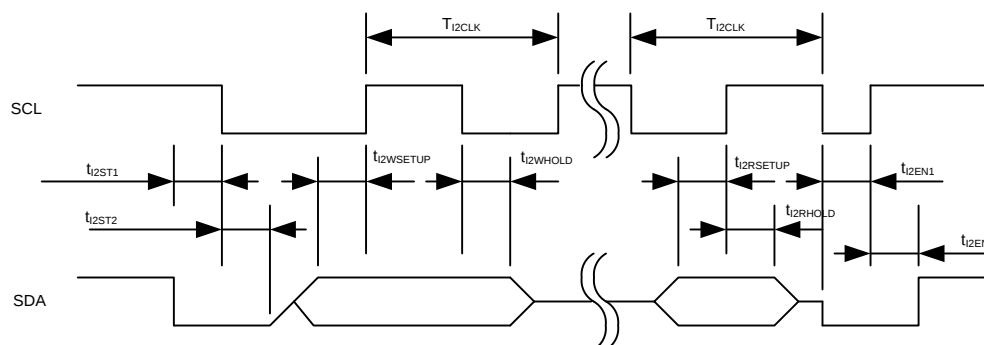
**Figure 11. Interrupt timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter                           | Min | Typ | Max | Unit   |
|------------|-------------------------------------|-----|-----|-----|--------|
| $t_{WINT}$ | INT0, INT1 Interrupt Assertion Time | 4   | -   | -   | SYSClk |
| $t_{dINT}$ | INT0, INT1 latency                  | -   | -   | 4   | SYSClk |

**Table 15. Interrupt AC Timing**

## 6.8 I<sup>2</sup>C AC Timing



**Figure 12. I<sup>2</sup>C Timing**

Unless specified, Ta = 25°C.

| Symbol                | Parameter                         | Min                                         | Typ | Max  | Unit               |
|-----------------------|-----------------------------------|---------------------------------------------|-----|------|--------------------|
| T <sub>I2CLK</sub>    | I <sup>2</sup> C clock period     | 10                                          | -   | 8192 | SYCLK              |
| t <sub>I2ST1</sub>    | I <sup>2</sup> C SDA start time   | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2ST2</sub>    | I <sup>2</sup> C SCL start time   | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2WSETUP</sub> | I <sup>2</sup> C write setup time | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2WHOLD</sub>  | I <sup>2</sup> C write hold time  | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2RSETUP</sub> | I <sup>2</sup> C read setup time  | I <sup>2</sup> C filter time <sup>(1)</sup> | -   | -    | SYCLK              |
| t <sub>I2RHOLD</sub>  | I <sup>2</sup> C read hold time   | 1                                           | -   | -    | SYCLK              |

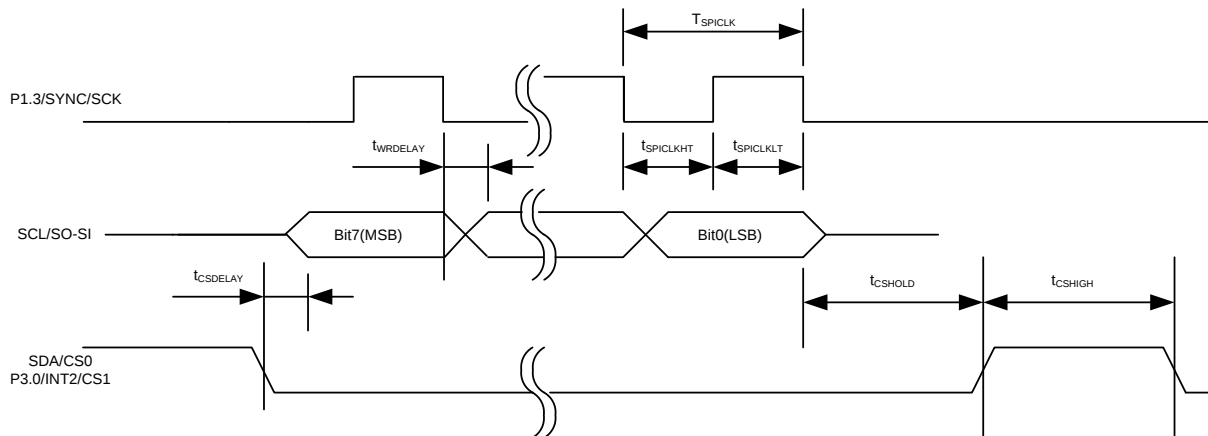
**Table 16. I<sup>2</sup>C AC Timing**

Note:

(1) I<sup>2</sup>C read setup time is determined by the programmable filter time applied to I<sup>2</sup>C communication.

## 6.9 SPI AC Timing

### SPI Write AC timing



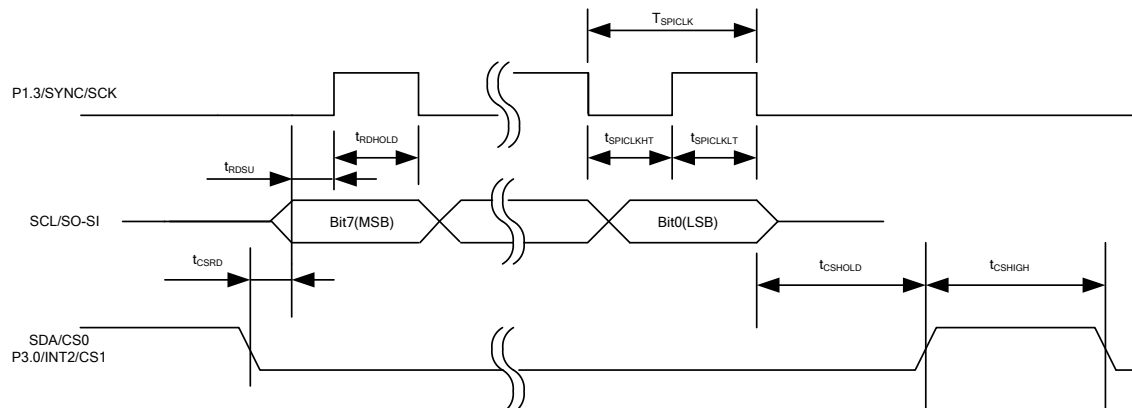
**Figure 13. SPI write timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                                          | Min | Typ | Max | Unit         |
|----------------|----------------------------------------------------|-----|-----|-----|--------------|
| $T_{SPICLK}$   | SPI clock period                                   | 4   | -   | -   | SYSClk       |
| $t_{SPICLKHT}$ | SPI clock high time                                | -   | 1/2 | -   | $T_{SPICLK}$ |
| $t_{SPICLKLT}$ | SPI clock low time                                 | -   | 1/2 | -   | $T_{SPICLK}$ |
| $t_{CSDelay}$  | CS to data delay time                              | -   | -   | 10  | nsec         |
| $t_{WRDELAY}$  | CLK falling edge to data delay time                | -   | -   | 10  | nsec         |
| $t_{CSHIGH}$   | CS high time between two consecutive byte transfer | 1   | -   | -   | $T_{SPICLK}$ |
| $t_{CSHOLD}$   | CS hold time                                       | -   | 1   | -   | $T_{SPICLK}$ |

**Table 17. SPI Write AC Timing**

## SPI Read AC Timing



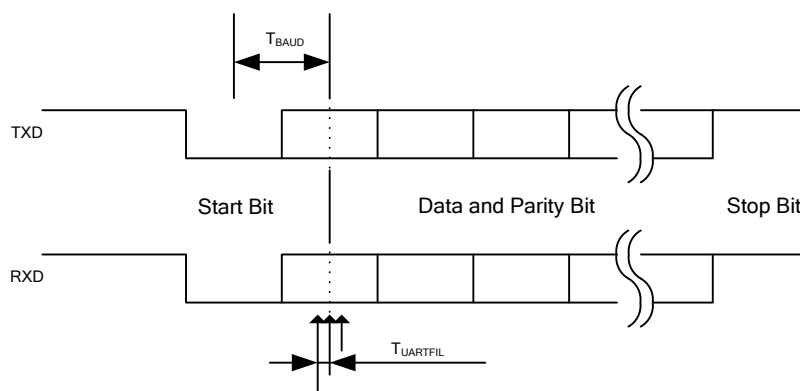
**Figure 14. SPI read timing**

Unless specified,  $T_a = 25^{\circ}\text{C}$ .

| Symbol                | Parameter                                          | Min | Typ | Max | Unit                |
|-----------------------|----------------------------------------------------|-----|-----|-----|---------------------|
| $T_{\text{SPICLK}}$   | SPI clock period                                   | 4   | -   | -   | SYSCCLK             |
| $t_{\text{SPICLKHT}}$ | SPI clock high time                                | -   | 1/2 | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{SPICLKLT}}$ | SPI clock low time                                 | -   | 1/2 | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{CSRD}}$     | CS to data delay time                              | -   | -   | 10  | nsec                |
| $t_{\text{RDSU}}$     | SPI read data setup time                           | 10  | -   | -   | nsec                |
| $t_{\text{RDHOLD}}$   | SPI read data hold time                            | 10  | -   | -   | nsec                |
| $t_{\text{CSHIGH}}$   | CS high time between two consecutive byte transfer | 1   | -   | -   | $T_{\text{SPICLK}}$ |
| $t_{\text{CSHOLD}}$   | CS hold time                                       | -   | 1   | -   | $T_{\text{SPICLK}}$ |

**Table 18. SPI Read AC Timing**

## 6.10 UART AC Timing



**Figure 15. UART timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

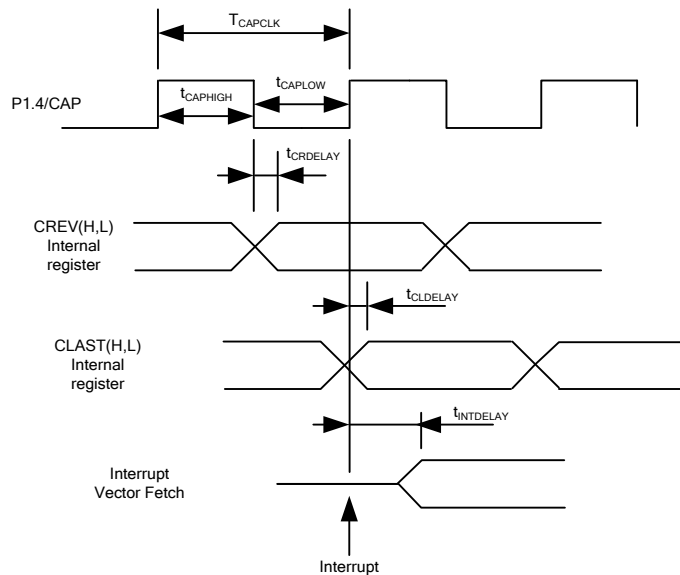
| Symbol        | Parameter                                  | Min | Typ   | Max | Unit       |
|---------------|--------------------------------------------|-----|-------|-----|------------|
| $T_{BAUD}$    | Baud Rate Period                           | -   | 57600 | -   | bit/sec    |
| $T_{UARTFIL}$ | UART sampling filter period <sup>(1)</sup> | -   | 1/16  | -   | $T_{BAUD}$ |

**Table 19. UART AC Timing**

Note:

- (1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of  $1/16 T_{BAUD}$ . If three sampled values do not agree, then UART noise error is generated.

## 6.11 CAPTURE Input AC Timing



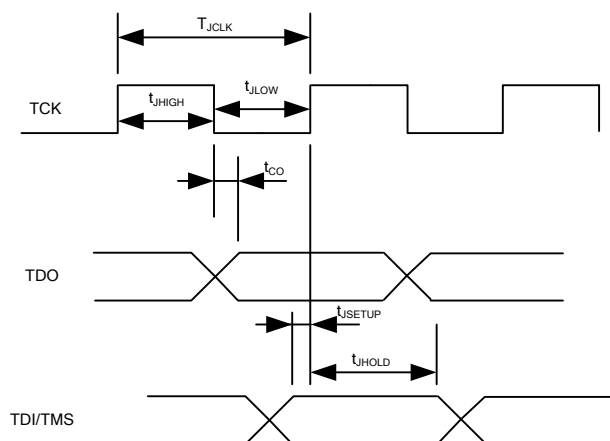
**Figure 16. CAPTURE timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                                           | Min | Typ | Max | Unit  |
|----------------|-----------------------------------------------------|-----|-----|-----|-------|
| $T_{CAPCLK}$   | CAPTURE input period                                | 8   | -   | -   | SYCLK |
| $t_{CAPHIGH}$  | CAPTURE input high time                             | 4   | -   | -   | SYCLK |
| $t_{CAPLOW}$   | CAPTURE input low time                              | 4   | -   | -   | SYCLK |
| $t_{CRDELAY}$  | CAPTURE falling edge to capture register latch time | -   | -   | 4   | SYCLK |
| $t_{CLDELAY}$  | CAPTURE rising edge to capture register latch time  | -   | -   | 4   | SYCLK |
| $t_{INTDELAY}$ | CAPTURE input interrupt latency time                | -   | -   | 4   | SYCLK |

**Table 20. CAPTURE AC Timing**

## 6.12 JTAG AC Timing



**Figure 17. JTAG timing**

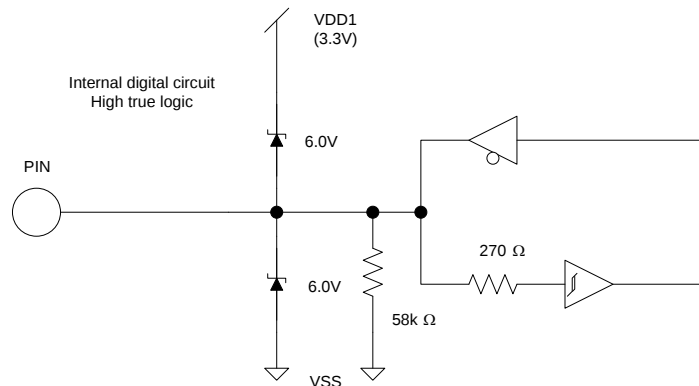
Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol       | Parameter                         | Min | Typ | Max | Unit |
|--------------|-----------------------------------|-----|-----|-----|------|
| $T_{JCLK}$   | TCK Period                        | -   | -   | 50  | MHz  |
| $t_{JHIGH}$  | TCK High Period                   | 10  | -   | -   | nsec |
| $t_{JLOW}$   | TCK Low Period                    | 10  | -   | -   | nsec |
| $t_{CO}$     | TCK to TDO propagation delay time | 0   | -   | 5   | nsec |
| $t_{JSETUP}$ | TDI/TMS setup time                | 4   | -   | -   | nsec |
| $t_{JHOLD}$  | TDI/TMS hold time                 | 0   | -   | -   | nsec |

**Table 21. JTAG AC Timing**

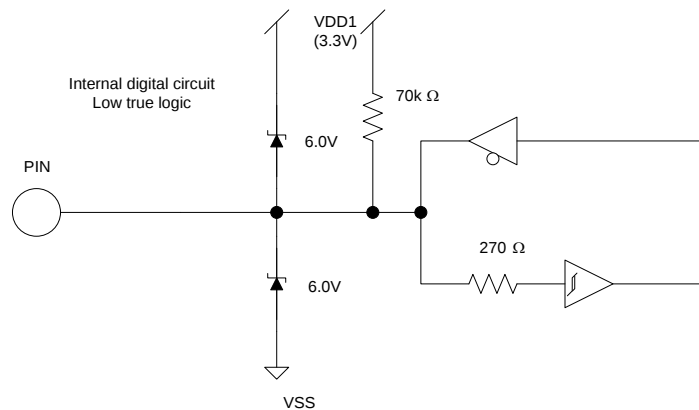
## 7 I/O Structure

The following figure shows the PWM output (PWMUH/PWMUL/PWMVH/PWMVL/PWMWH/PWMWL/BRAKE)



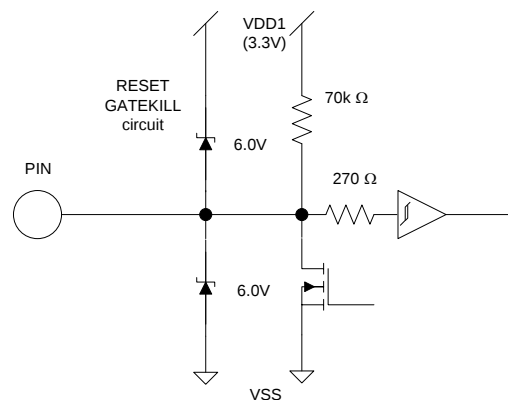
**Figure 18. PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH/BRAKE output**

The following figure shows the digital I/O structure except the PWM output



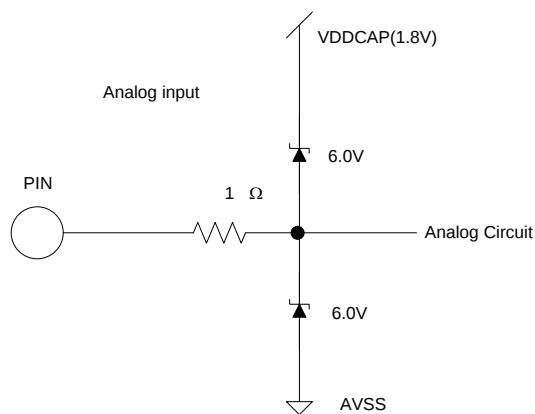
**Figure 19. All digital I/O except PWM/BRAKE output**

The following figure shows RESET and GATEKILL I/O structure.



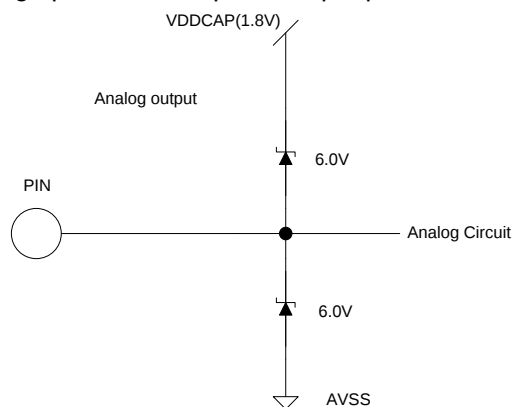
**Figure 20. RESET, GATEKILL I/O**

The following figure shows the analog input structure.



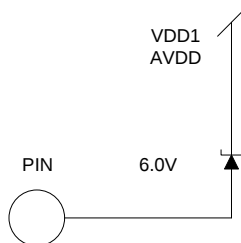
**Figure 21. Analog input**

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.



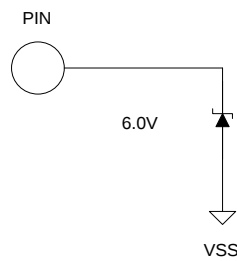
**Figure 22. Analog operational amplifier output and AREF I/O structure**

The following figure shows the VSS,AVSS pin I/O structure



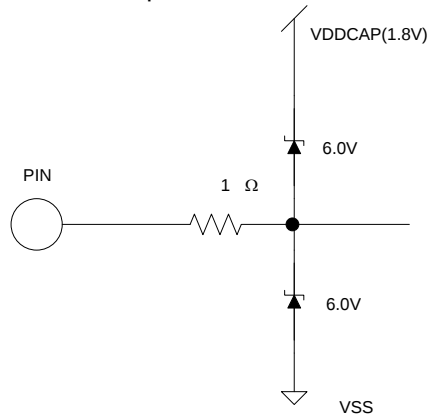
**Figure 23. VSS,AVSS pin I/O structure**

The following figure shows the VDD1,VDDCAP pin I/O structure



**Figure 24. VDD1,VDDCAP pin I/O structure**

The following figure shows the XTAL0 and XTAL1 pins structure



**Figure 25. XTAL0/XTAL1 pins structure**

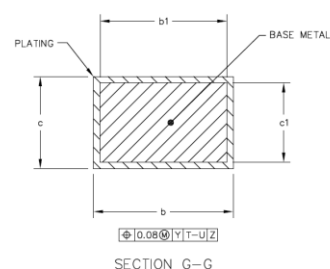
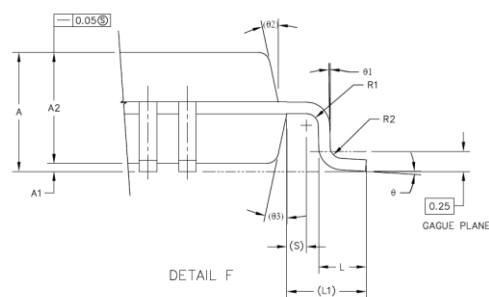
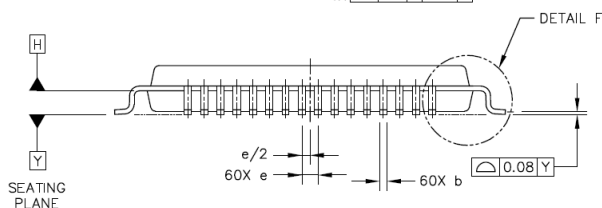
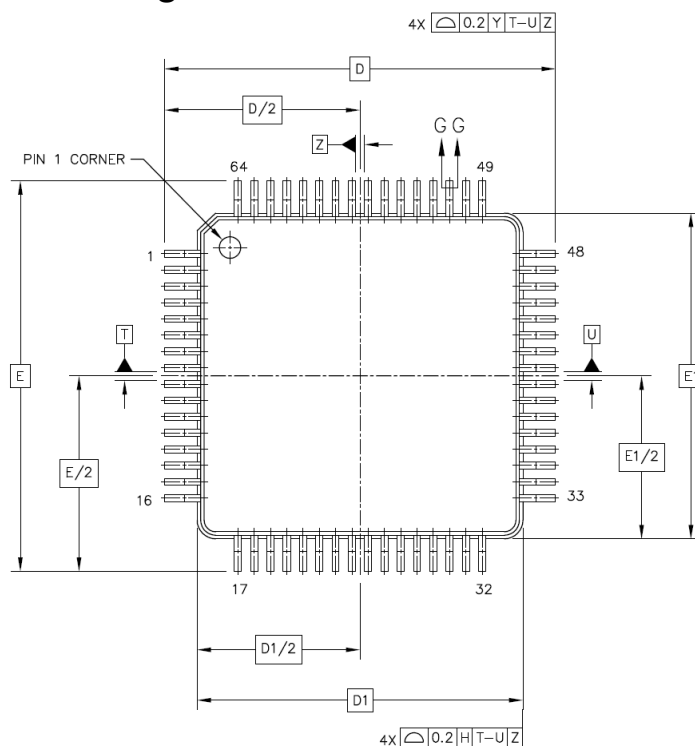
## 8 Pin List

| Pin Number | Pin Name          | Internal Pull-up / down | Pin Type | Description                                                                                                       |
|------------|-------------------|-------------------------|----------|-------------------------------------------------------------------------------------------------------------------|
| 1          | XTAL0             | --                      | I        | Crystal input                                                                                                     |
| 2          | XTAL1             | --                      | O        | Crystal output                                                                                                    |
| 3          | P1.0/PULSE/T2/MT1 | --                      | I/O      | Discrete programmable I/O or Pulse Input or Timer/Counter 2 input or MCE Pin Timer 1                              |
| 4          | SCL/SO-SI         | --                      | I/O      | I <sup>2</sup> C clock output (open drain, need pull up) or SPI data                                              |
| 5          | SDA/CS0           | --                      | I/O      | I <sup>2</sup> C data (open drain, need pull up) or SPI Chip Select 0                                             |
| 6          | P1.3/SYNC/SCK     | --                      | I/O      | Discrete programmable I/O or SYNC output or SPI clock output                                                      |
| 7          | P1.4/ENC-A        | --                      | I/O      | Discrete programmable I/O or Encoder A input                                                                      |
| 8          | P1.6/ENC-B        | --                      | I/O      | Discrete programmable I/O or Encoder B input                                                                      |
| 9          | P1.7/ENC-C        | --                      | I/O      | Discrete programmable I/O or Encoder C input                                                                      |
| 10         | VDD1              | --                      | P        | 3.3V digital power                                                                                                |
| 11         | VSS               | --                      | P        | Digital common                                                                                                    |
| 12         | VDDCAP            | --                      | P        | Internal 1.8V output, Capacitor(s) to be connected                                                                |
| 13         | P2.0/DIR/NMI      | --                      | I/O      | Discrete programmable I/O or DIR input or Non-maskable Interrupt input                                            |
| 14         | P3.2/INT0         | --                      | I/O      | Discrete programmable I/O or Interrupt 0 input                                                                    |
| 15         | P2.2/CAP          | --                      | I/O      | Discrete programmable I/O or Capture Timer input                                                                  |
| 16         | P2.3/MATCH        | --                      | I/O      | Discrete programmable I/O or MATCH output                                                                         |
| 17         | P2.5/INT2         | --                      | I/O      | Discrete programmable I/O or Interrupt 2 input                                                                    |
| 18         | P2.6/AO0          | --                      | I/O      | Discrete programmable I/O or PWM 0 digital output                                                                 |
| 19         | P2.7/AO1/MT2      | --                      | I/O      | Discrete programmable I/O or PWM 1 digital output or MCE pin timer 2 output                                       |
| 20         | OP1O              | --                      | O        | Op amp output for application sensing, 0-1.2V range                                                               |
| 21         | OP1-              | --                      | I        | Op amp negative input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused            |
| 22         | OP1+              | --                      | I        | Op amp positive input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused            |
| 23         | VDCBUS            | --                      | I        | Analog input channel (0 – 1.2V), allocated by MCE for DC bus voltage input                                        |
| 24         | AIN1              | --                      | I        | Analog input channel 1, 0-1.2V range, allocated by MCE as speed input, needs to be pulled down to AVSS if unused  |
| 25         | AIN2              | --                      | I        | Analog input channel 2, 0-1.2V range, allocated by MCE as torque input, needs to be pulled down to AVSS if unused |
| 26         | AIN3              | --                      | I        | Analog input channel 3, 0-1.2V range, needs to be pulled down to AVSS if unused                                   |
| 27         | AIN4              | --                      | I        | Analog input channel 4, 0-1.2V range, needs to be pulled down to AVSS if unused                                   |
| 28         | IFBU-             | --                      | I        | Op amp negative input for U phase current sensing, 0-1.2V range                                                   |
| 29         | IFBU+             | --                      | I        | Op amp positive input for U phase current sensing, 0-1.2V range                                                   |
| 30         | IFBUO             | --                      | O        | Op amp output for U phase current sensing, 0-1.2V range                                                           |

| Pin Number | Pin Name         | Internal Pull-up / down | Pin Type | Description                                                                 |
|------------|------------------|-------------------------|----------|-----------------------------------------------------------------------------|
| 31         | CMEXT            | --                      | O        | Unbuffered 0.6V output. Capacitor needs to be connected.                    |
| 32         | AREF             | --                      | O        | Analog reference voltage output (0.6V)                                      |
| 33         | IFBV-            | --                      | I        | Op amp negative input for V phase current sensing, 0-1.2V range             |
| 34         | IFBV+            | --                      | I        | Op amp positive input for V phase current sensing, 0-1.2V range             |
| 35         | IFBVO            | --                      | O        | Op amp output for V phase current sensing, 0-1.2V range                     |
| 36         | AVSS             | --                      | P        | Analog common                                                               |
| 37         | VDDCAP           | --                      | P        | Internal 1.8V output, Capacitor(s) to be connected                          |
| 38         | VDD1             | --                      | P        | 3.3V digital power                                                          |
| 39         | VSS              | --                      | P        | Digital common                                                              |
| 40         | P3.1/AO2/MT3     | --                      | I/O      | Discrete programmable I/O or PWM 2 digital output or MCE pin timer 3 output |
| 41         | PWMWL            | 58 kΩ Pull down         | O        | PWM gate drive for phase W low side, configurable either high or low true.  |
| 42         | PWMVL            | 58 kΩ Pull down         | O        | PWM gate drive for phase V low side, configurable either high or low true   |
| 43         | PWMUL            | 58 kΩ Pull down         | O        | PWM gate drive for phase U low side, configurable either high or low true   |
| 44         | PWMWH            | 58 kΩ Pull down         | O        | PWM gate drive for phase W high side, configurable either high or low true  |
| 45         | P3.7             | --                      | I/O      | Discrete programmable I/O                                                   |
| 46         | P2.1             | --                      | I/O      | Discrete programmable I/O                                                   |
| 47         | P3.6             | --                      | I/O      | Discrete programmable I/O                                                   |
| 48         | PWMVH            | 58 kΩ Pull down         | O        | PWM gate drive for phase V high side, configurable either high or low true  |
| 49         | PWMUH            | 58 kΩ Pull down         | O        | PWM gate drive for phase U high side, configurable either high or low true  |
| 50         | P1.5             | --                      | I/O      | Discrete programmable I/O.                                                  |
| 51         | BRAKE            | 70 kΩ Pull up           | O        | Brake output, configured low true at a power up                             |
| 52         | BRAKEGK          | 70 kΩ Pull up           | I        | Brake shutdown input, active low input.                                     |
| 53         | GATEKILL         | 70 kΩ Pull up           | I        | PWM shutdown input, configurable digital filter, active low input.          |
| 54         | P3.0/CS1         | 70 kΩ Pull up           | I/O      | Discrete programmable I/O or SPI Chip Select 1                              |
| 55         | TMS /P5.2        | --                      | I        | JTAG test mode select or digital input port                                 |
| 56         | TDO              | --                      | O        | JTAG test data output                                                       |
| 57         | TDI /P5.1        | --                      | I        | JTAG test data input or digital input port                                  |
| 58         | TCK              | --                      | I        | JTAG test clock                                                             |
| 59         | RESET            | --                      | I        | Reset, low true, Schmitt trigger input                                      |
| 60         | P1.1/RXD         | --                      | I/O      | UART receiver input or Discrete programmable I/O                            |
| 61         | P1.2/TXD         | --                      | I/O      | UART transmitter output or Discrete programmable I/O                        |
| 62         | HALL-1/P3.4/T0   | --                      | I/O      | Hall-1 input or discrete programmable I/O or Timer/Counter 0 input          |
| 63         | HALL-2/P3.5/T1   | --                      | I/O      | Hall-2 input or discrete programmable I/O or Timer/Counter 1 input          |
| 64         | HALL-3/P3.3/INT1 | --                      | I/O      | Hall-3 input or discrete programmable I/O or Interrupt 1 input              |

**Table 22. Pin List**

## 9 Package Dimensions

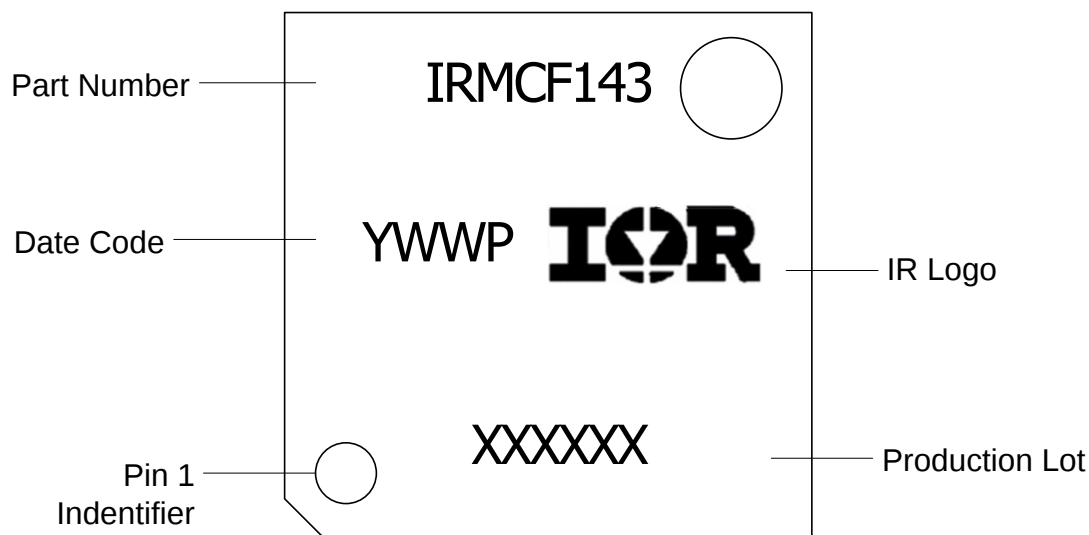


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
7. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

| DIM | MIN  | MAX  | DIM | MIN | MAX | DIM | MIN | MAX |
|-----|------|------|-----|-----|-----|-----|-----|-----|
| A   | ---  | 1.6  | L1  | 1   | REF |     |     |     |
| A1  | 0.05 | 0.15 | R1  | 0.1 | 0.2 |     |     |     |
| A2  | 1.35 | 1.45 | R2  | 0.1 | 0.2 |     |     |     |
| b   | 0.17 | 0.27 | S   | 0.2 | REF |     |     |     |
| b1  | 0.17 | 0.23 | θ   | 0°  | 7°  |     |     |     |
| c   | 0.09 | 0.2  | θ1  | 0°  | --- |     |     |     |
| c1  | 0.09 | 0.16 | θ2  | 12° | REF |     |     |     |
| D   | 12   | BSC  | θ3  | 12° | REF |     |     |     |
| D1  | 10   | BSC  |     |     |     |     |     |     |
| e   | 0.5  | BSC  |     |     |     |     |     |     |
| E   | 12   | BSC  |     |     |     |     |     |     |
| E1  | 10   | BSC  |     |     |     |     |     |     |
| L   | 0.45 | 0.75 |     |     |     |     |     |     |

## 10 Part Marking Information



## 11 Qualification Information

|                                   |                         |                                                       |
|-----------------------------------|-------------------------|-------------------------------------------------------|
| <b>Qualification Level</b>        |                         | Industrial <sup>††</sup><br>(per JEDEC JESD 47E)      |
| <b>Moisture Sensitivity Level</b> |                         | MSL3 <sup>†††</sup><br>(per IPC/JEDEC J-STD-020C)     |
| <b>ESD</b>                        | <b>Machine Model</b>    | Class B<br>(per JEDEC standard JESD22-A114D)          |
|                                   | <b>Human Body Model</b> | Class 2<br>(per EIA/JEDEC standard EIA/JESD22-A115-A) |
| <b>RoHS Compliant</b>             |                         | Yes                                                   |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Note:** Test condition for Temperature Cycling test is -40C to 125C.

## Revision History

International  
 Rectifier

Data and Specifications are subject to change without notice

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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