

Reference designs for IR3883

About this document

Scope and purpose

The IR3883 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 3mm X 3 mm Power QFN package. Key features offered by the IR3883 include selectable Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DE), Over Current Protection with three selectable levels, precision 0.5V reference voltage, Power Good, thermal protection, Enable input, input under-voltage lockout for proper start-up, internal LDO and pre-bias start-up. Output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous MOSFET for optimum cost and performance and the current limit is thermally compensated. This document contains the schematic, bill of materials, transient response and efficiency of several reference designs using IR3883. Test results are obtained using standard IRDC3883 evaluation board. Detailed application information for IR3883 is available in the IR3883 data sheet and IRDC3883 user guide.

Intended audience

This document is intended to provide a comprehensive design reference for different application configurations. Design engineers can easily create their designs with the provided Bill of Material, and understand the expected performance of IR3883.

Table of Contents

About this document	1
Table of Contents	1
1 IRDC3883 Schematic	2
2 Bill of materials	3
3 Reference design examples for 12V input	4
3.1 Bill of material	4
3.2 Transient load response	4
3.3 Typical efficiency and power loss curves	5
3.4 Load regulation	9
4 Reference design examples for 5V input	12
4.1 Bill of material	12
4.2 Transient load response	12
4.3 Typical efficiency and power loss curves	12
4.4 Load regulation	13
Revision History	16

IRDC3883 Schematic

1 IRDC3883 Schematic

Figure 1 shows the schematic of the IRDC3883 evaluation board with $V_{in} = 12\text{ V}$, $V_o = 3.3\text{ V}$, $I_{o\max} = 3\text{ A}$.

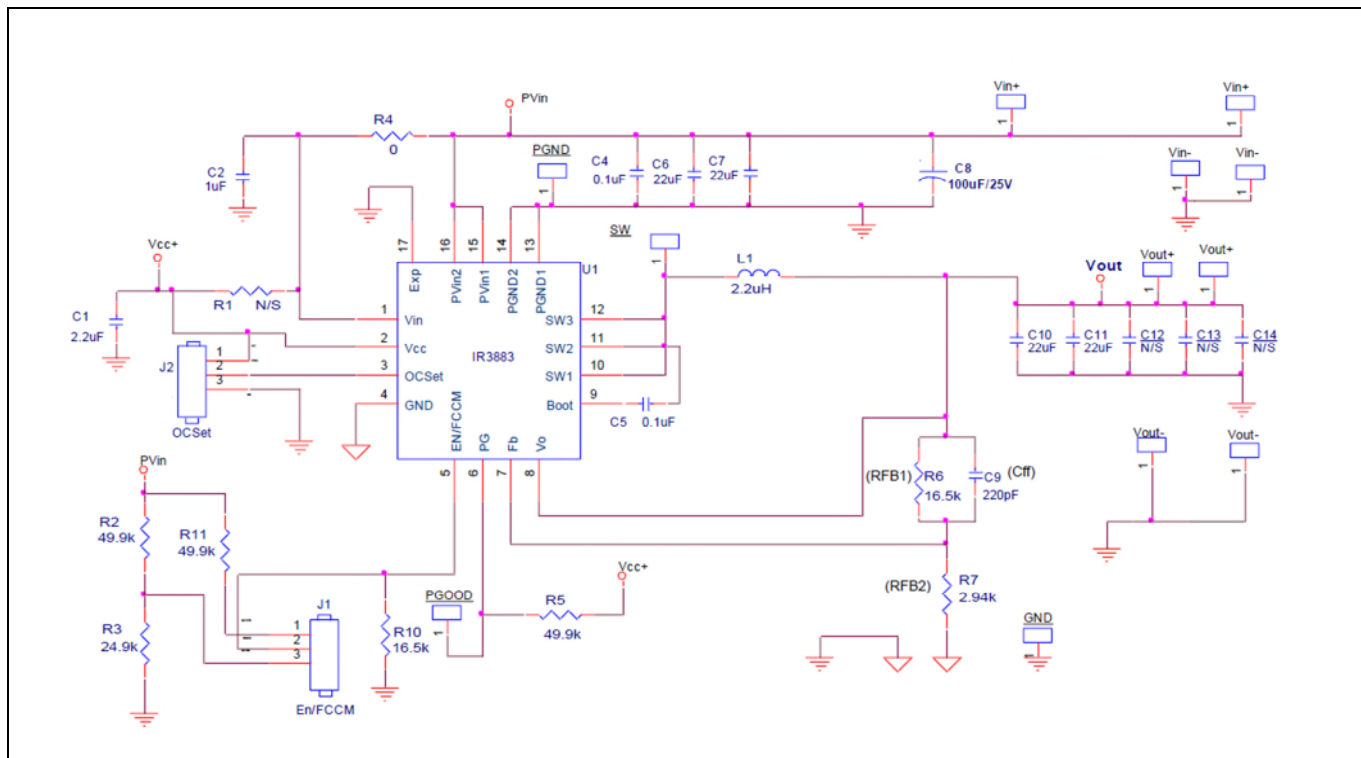


Figure 1 Schematic of the IRDC3883 evaluation board

Bill of materials

2 Bill of materials

Table 1 Bill of materials

Item	Quantity	Part Reference	Value	Description	Part Number	Manufacture
1	1	C1	2.2 μ F	2.2 μ F 16 V 10% X5R 0402	GRM155R61C225KE44D	Murata
2	1	C2	1 μ F	1 μ F 16 V 10% X5R 0402	GRM155R61C105KE01D	Murata
3	2	C4 C5	0.1 μ F	0.1 μ F 16 V 10% X7R 0402	GRM155R71C104KA88D	Murata
4	2	C6 C7	22 μ F	22 μ F 16 V 20% X5R 0805	C2012X5R1C226M125AC	TDK
5	2	C10 C11	22 μ F	22 μ F 6.3 V 20% X5R 0805	C2012X5R0J226M	TDK
6	1	C8 (Note)	100 μ F/25V	Alum 100 μ F 25 V 20% SMD	EEE-1EA101XP	Panasonic
7	3	R2 R5 R11	49.9 k Ω	49.9 kohm 1% 1/10 W 0402	ERJ-2RKF4992X	Panasonic
8	1	R3	24.9 k Ω	24.9 kohm 1% 1/10 W 0402	ERJ-2RKF2492X	Panasonic
9	1	R4	0	0.0 ohm jumper 1/10 W	ERJ-2GE0R00X	Panasonic
10	1	R10	16.5 k Ω	16.5 kohm 1% 1/10 W 0402	ERJ-2RKF1652X	Panasonic
11	1	U1	IR3883	3mmx3mm 3 A POL regulator	IR3883MTRPBF	Infineon
12	1	L	Refer to table 2 and table 3			
13	1	R6 (RFB1)				
14	1	R7 (RFB2)				
15	1	C9 (Cff)				
16	1	R1				
17	1	R4				

Note: C8 is used to damp the oscillations induced by parasitic inductance of long power cables.

Reference design examples for 12V input

3 Reference design examples for 12V input

Reference designs for $PV_{in} = V_{in} = 12\text{ V}$, $I_{omax} = 3\text{ A}$

3.1 Bill of material

Table 2 Bill of materials for $PV_{in} = V_{in} = 12\text{ V}$, $I_{omax} = 3\text{ A}$, internal LDO

V _o (V)	R4	R1	R6 (kΩ) (R _{FB1})	R7 (kΩ) (R _{FB2})	L1 (μH)	P/N	C9 (pF) (C _{ff})	C10, C11(μF) (C _{out})
1	0	N/S	16.5	16.5	1.0	XEL4030-102	100	2 x 22 μF 6.3 V X5R 20% 0805
1.2			16.5	11.8		DCR = 8.89 mΩ 4 mm x 4 mm x 3.1 mm		
1.8			16.5	6.34	1.5	XEL4030-152	220	
2.5			16.5	4.12	2.2	XAL5030-222		
3.3			16.5	2.94		DCR = 13.2 mΩ 5.28 mm x 5.48 mm x 3.1 mm		
5			16	1.78	3.3	XAL5030-332		
						DCR = 21.2 mΩ 5.28 mm x 5.48 mm x 3.1 mm		

3.2 Transient load response

Table 3 Transient load response for $PV_{in} = V_{in} = 12\text{ V}$, $V_{cc} = \text{internal LDO}$, $I_o = 0\text{ A} - 1\text{ A} @ 2.5\text{ A}/\mu\text{s}$

V_o (V)	Overshoot/Undershoot (mV) (I_o step = 1 A @ 2.5 A/ μ s)
1	29 mV/-14 mV
1.2	30 mV/-14 mV
1.8	40 mV/-26 mV
2.5	48 mV/-30 mV
3.3	57 mV/-39 mV
5	80 mV/-73 mV

Reference design examples for 12V input

3.3 Typical efficiency and power loss curves

$P_{V_{in}} = V_{in} = 12\text{ V}$, V_{cc} = internal LDO, $I_o = 0\text{ A} - 3\text{ A}$, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3883, the inductor losses and the losses of the input and output capacitors.

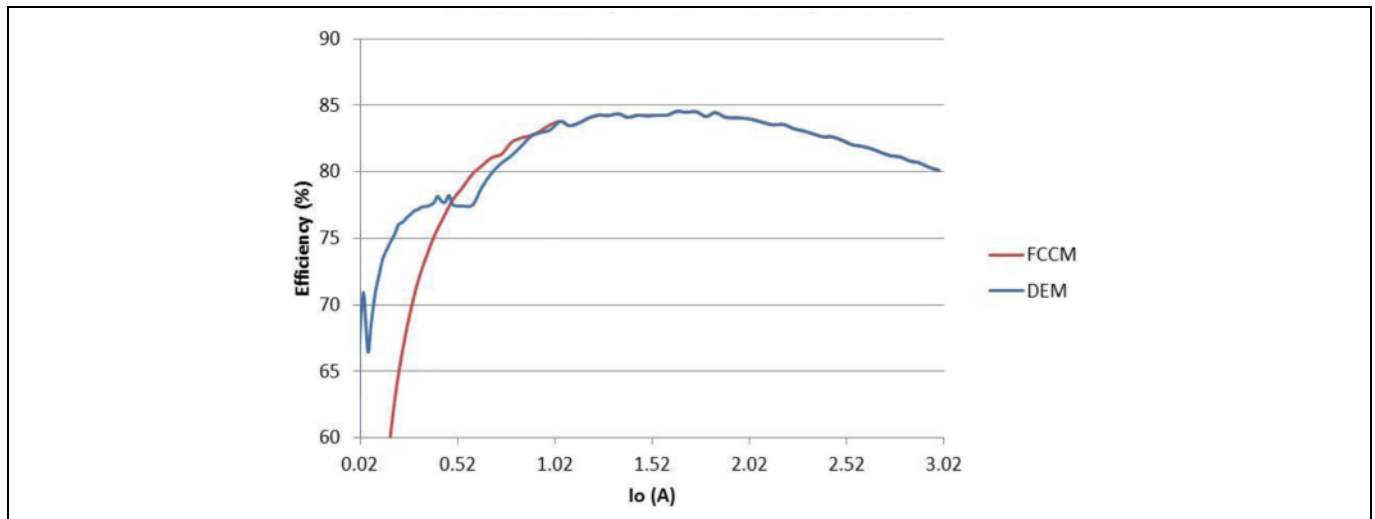


Figure 2 IR3883 efficiency @ $P_{V_{in}} = V_{in} = 12\text{ V}$, $V_o = 1.0\text{ V}$

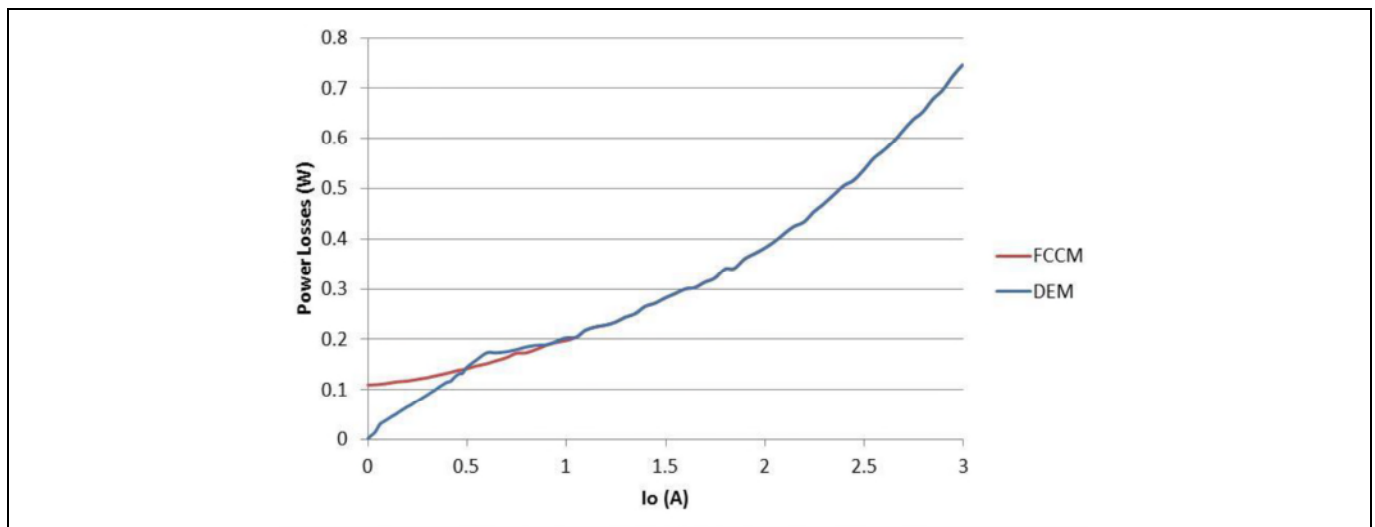


Figure 3 IR3883 power losses @ $P_{V_{in}} = V_{in} = 12\text{ V}$, $V_o = 1.0\text{ V}$

Reference design examples for 12V input

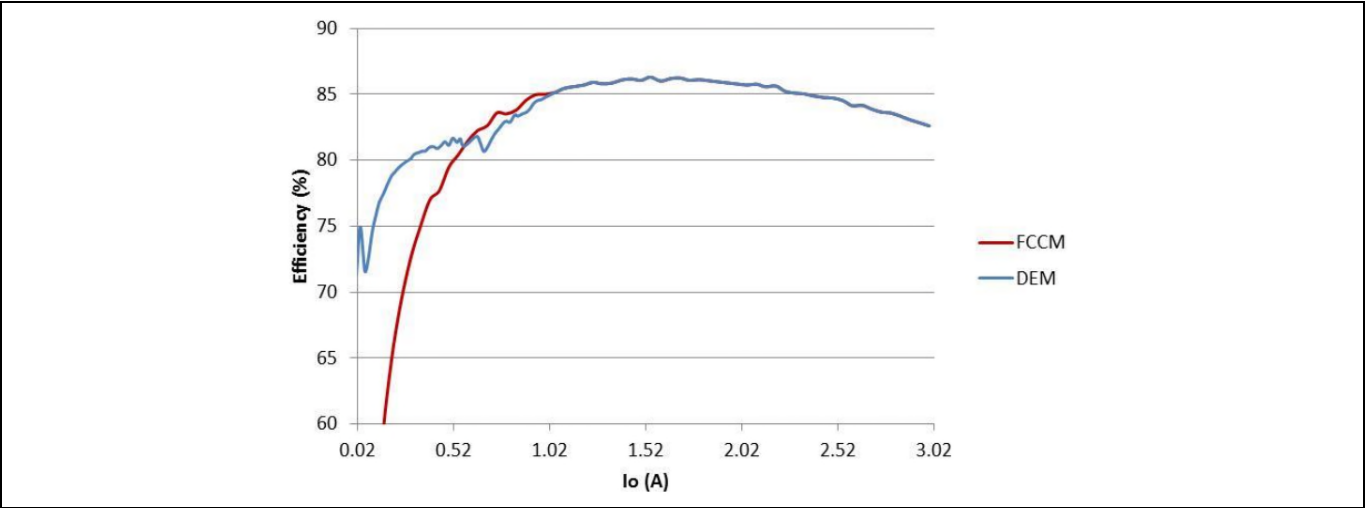


Figure 4 IR3883 efficiency @ $PV_{in} = V_{in} = 12V$, $V_o = 1.2 V$

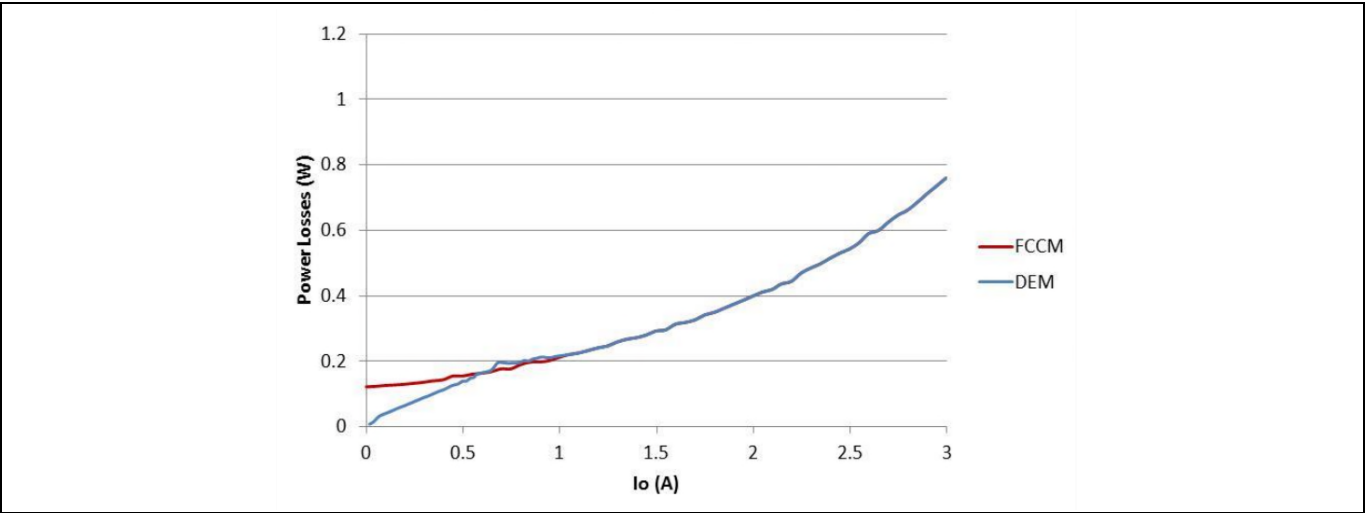


Figure 5 IR3883 power losses @ $PV_{in} = V_{in} = 12V$, $V_o = 1.2 V$

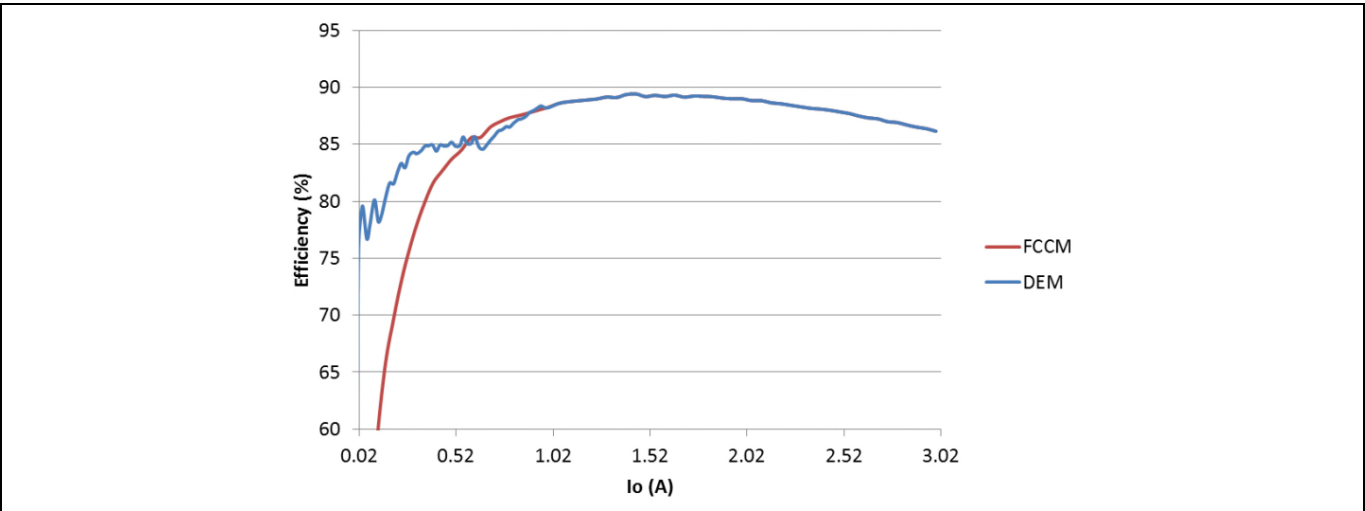


Figure 6 IR3883 efficiency @ $PV_{in} = V_{in} = 12V$, $V_o = 1.8 V$

Reference design examples for 12V input

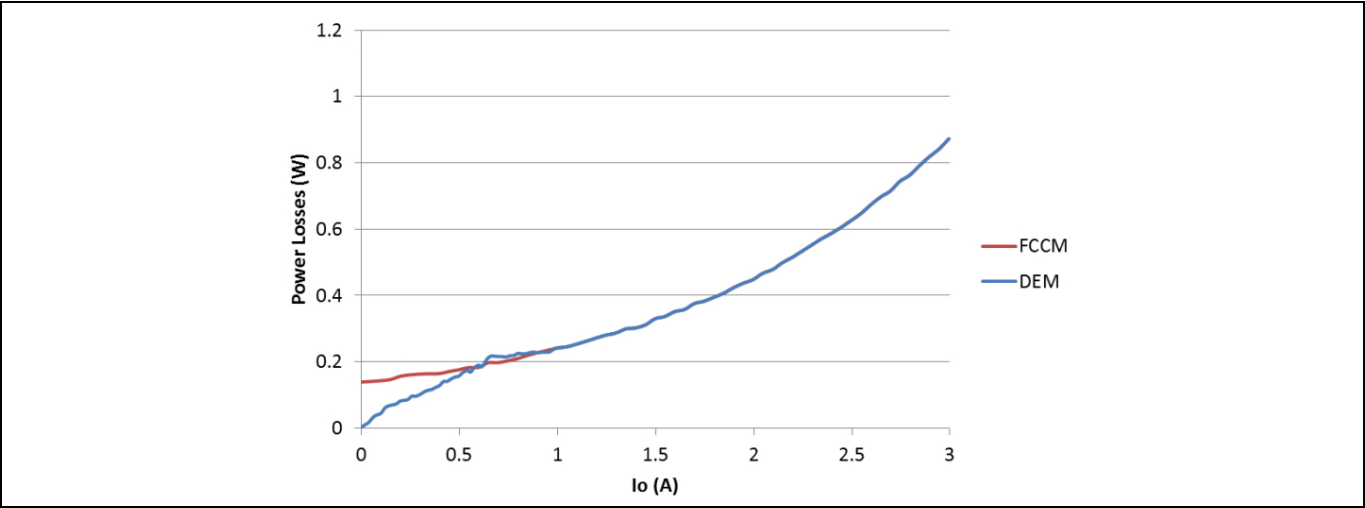


Figure 7 IR3883 power losses @ $PV_{in} = V_{in} = 12V$, $V_o = 1.8 V$

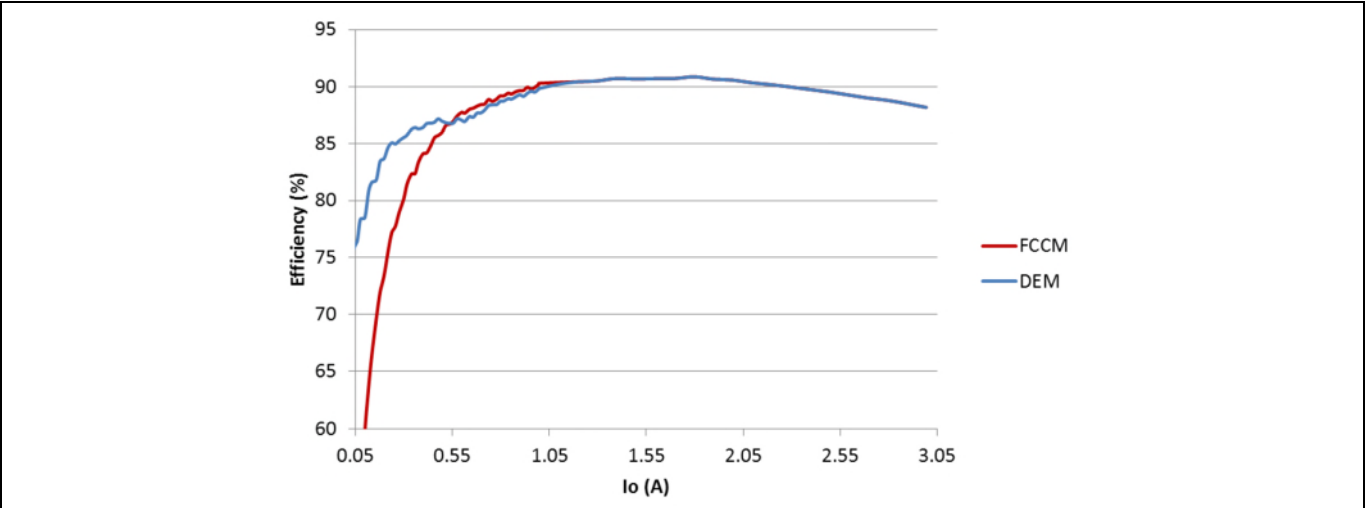


Figure 8 IR3883 efficiency @ $PV_{in} = V_{in} = 12V$, $V_o = 2.5 V$

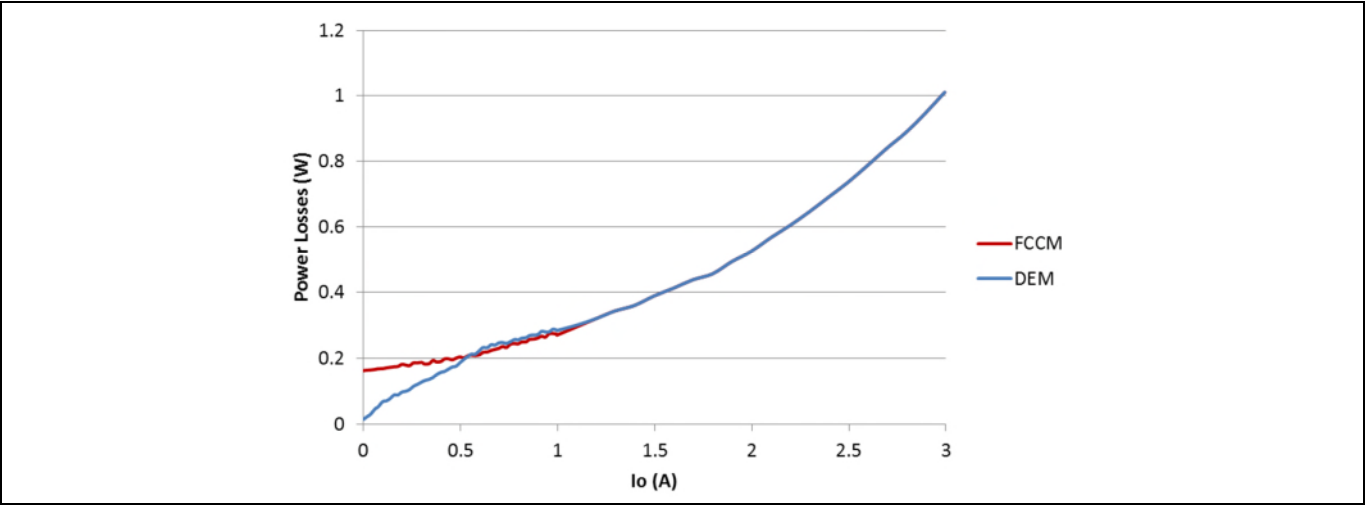


Figure 9 IR3883 power losses @ $PV_{in} = V_{in} = 12V$, $V_o = 2.5 V$

Reference design examples for 12V input

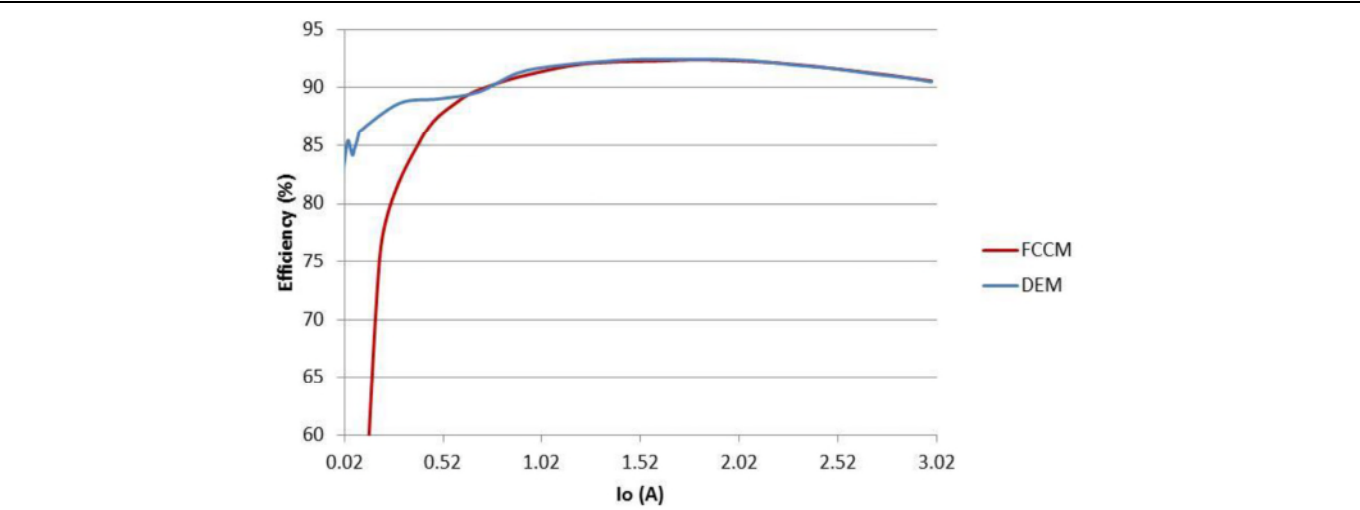


Figure 10 IR3883 efficiency @ $PV_{in} = V_{in} = 12V$, $V_o = 3.3 V$

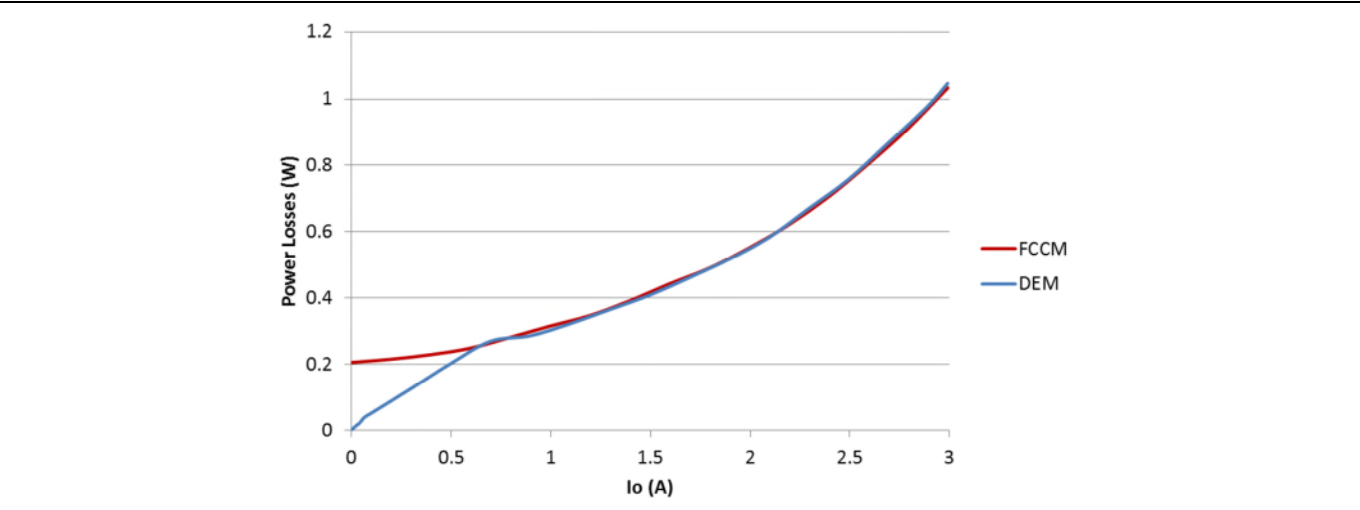


Figure 11 IR3883 power losses @ $PV_{in} = V_{in} = 12V$, $V_o = 3.3 V$

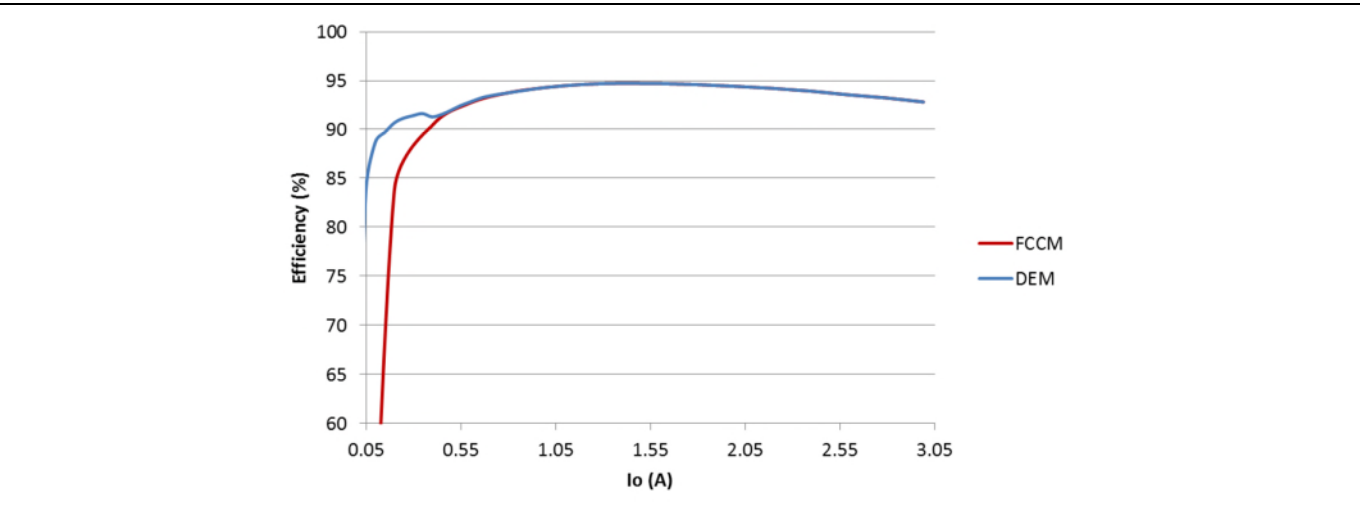
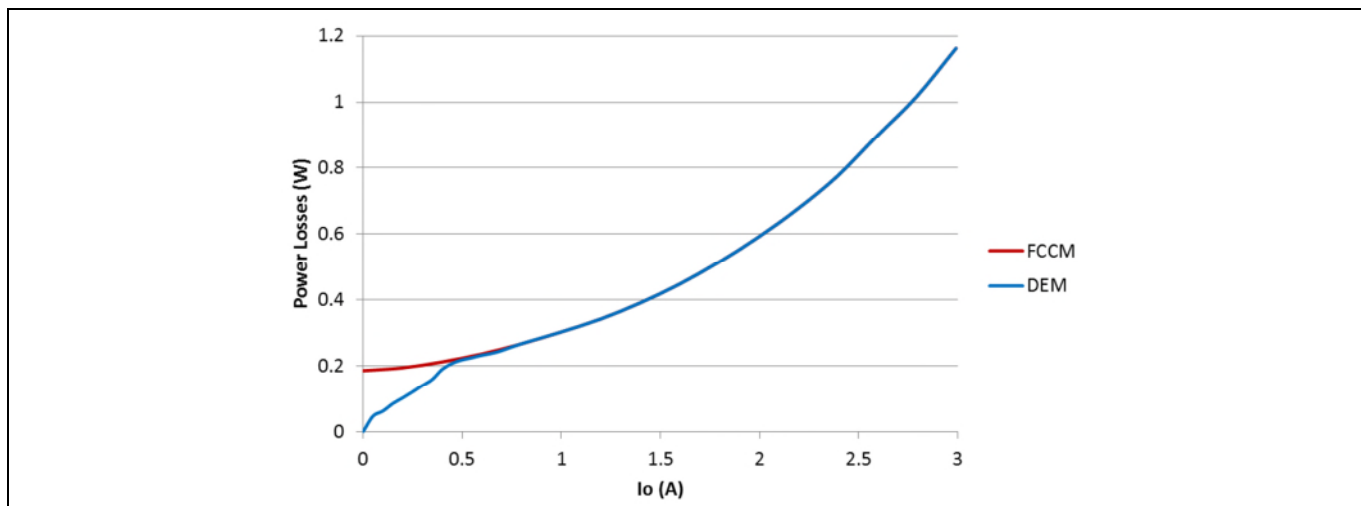


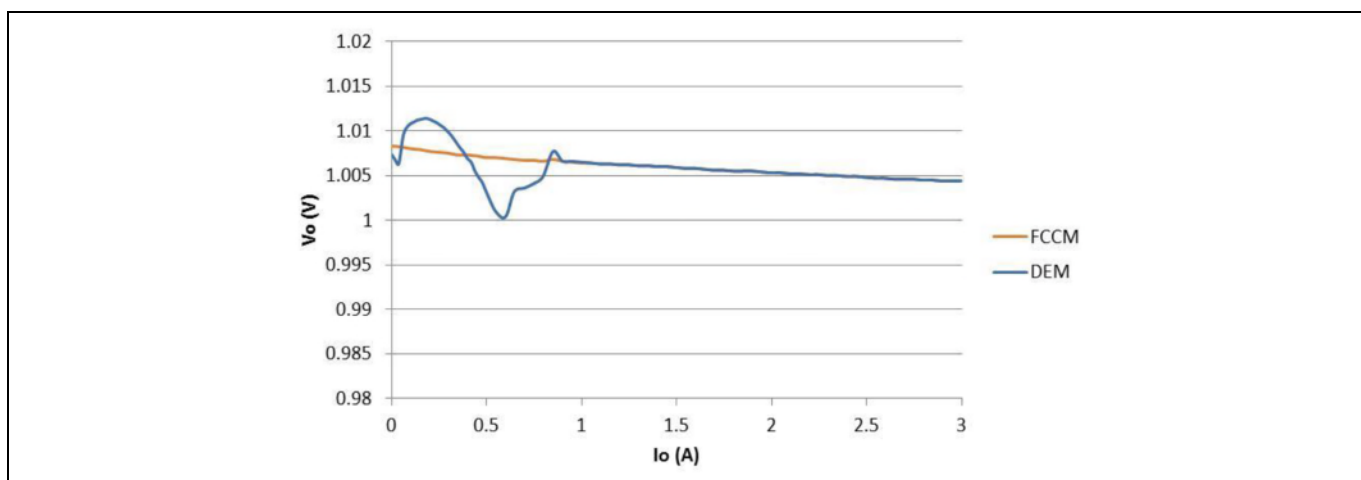
Figure 12 IR3883 efficiency @ $PV_{in} = V_{in} = 12V$, $V_o = 5 V$

Reference design examples for 12V input

Figure 13 IR3883 power losses @ $PV_{in} = V_{in} = 12V$, $V_o = 5V$

3.4 Load regulation

$PV_{in} = V_{in} = 12V$, $I_o = 0A-3A$, Room Temperature, No Air Flow.

Figure 14 IR3883 load regulation @ $PV_{in} = V_{in} = 12V$, $V_o = 1.0V$

Reference design examples for 12V input

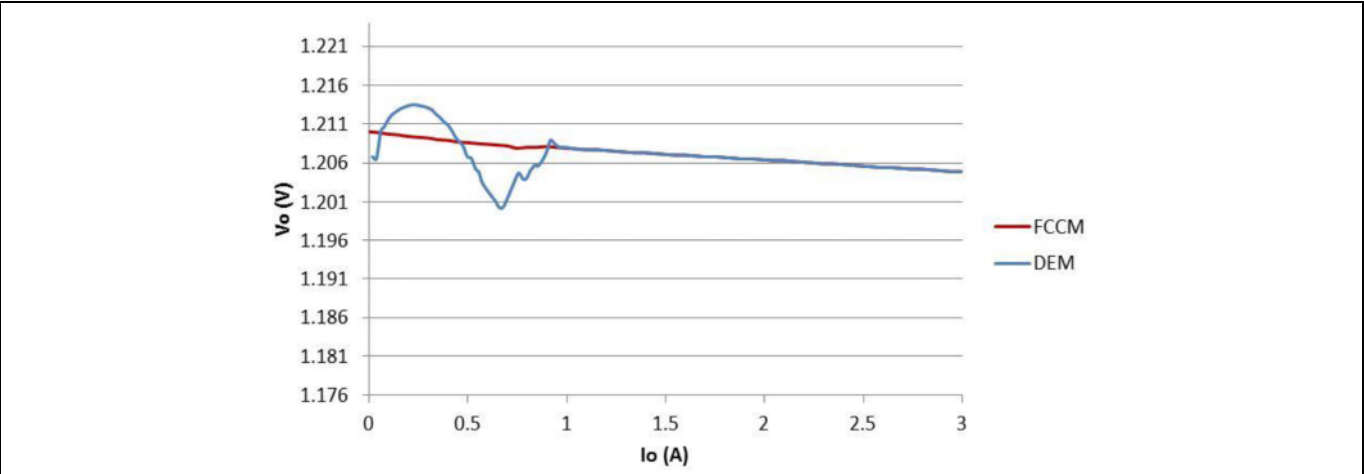


Figure 15 IR3883 load regulation @ $PV_{in} = V_{in} = 12\text{ V}$, $V_O = 1.2\text{ V}$

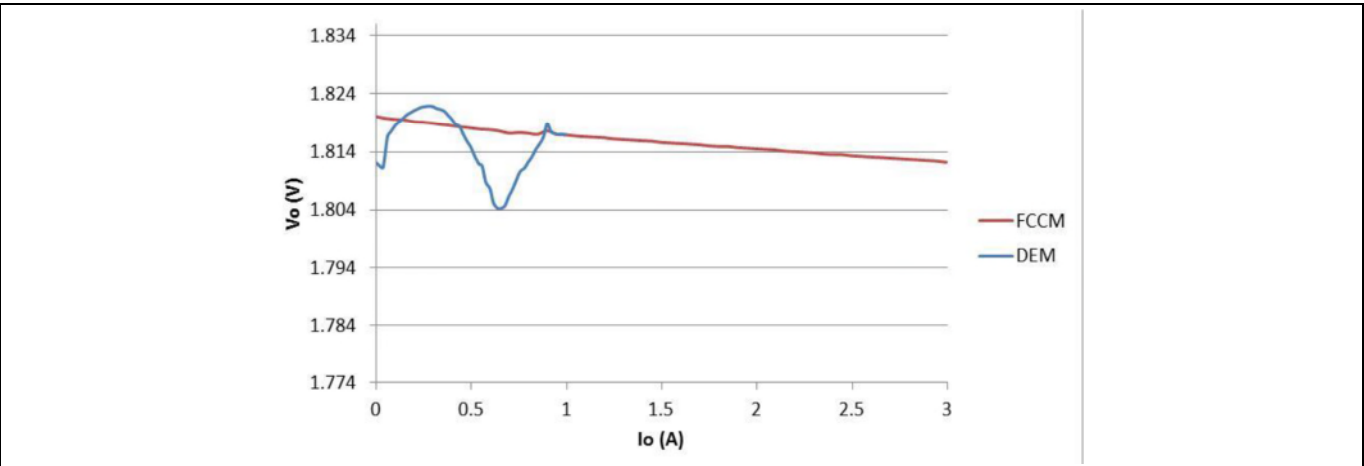


Figure 16 IR3883 load regulation @ $PV_{in} = V_{in} = 12\text{ V}$, $V_O = 1.8\text{ V}$

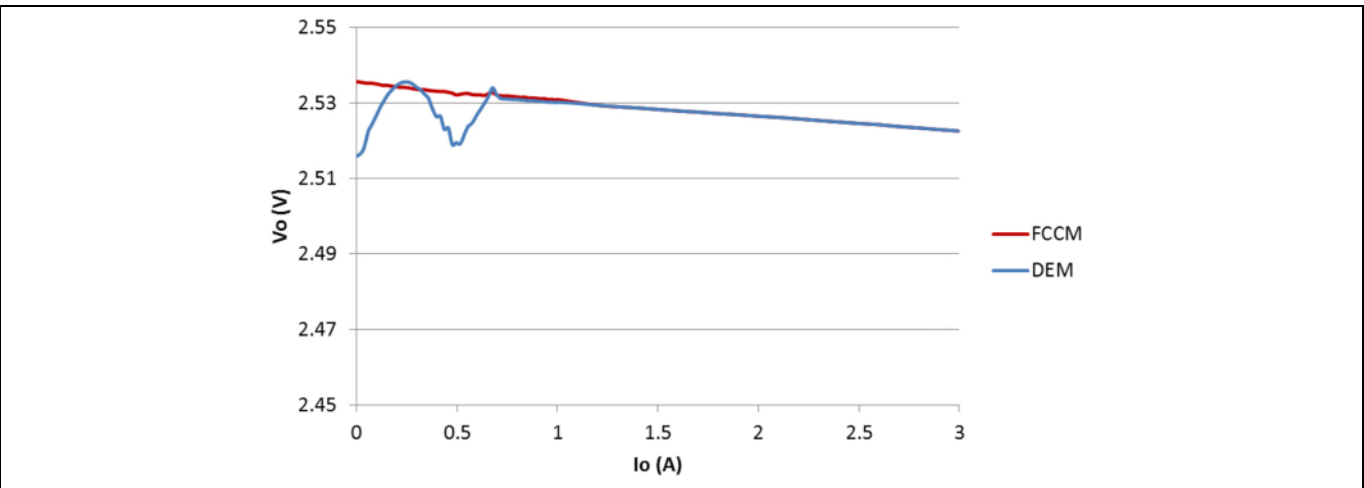


Figure 17 IR3883 load regulation @ $PV_{in} = V_{in} = 12\text{ V}$, $V_O = 2.5\text{ V}$

Reference design examples for 12V input

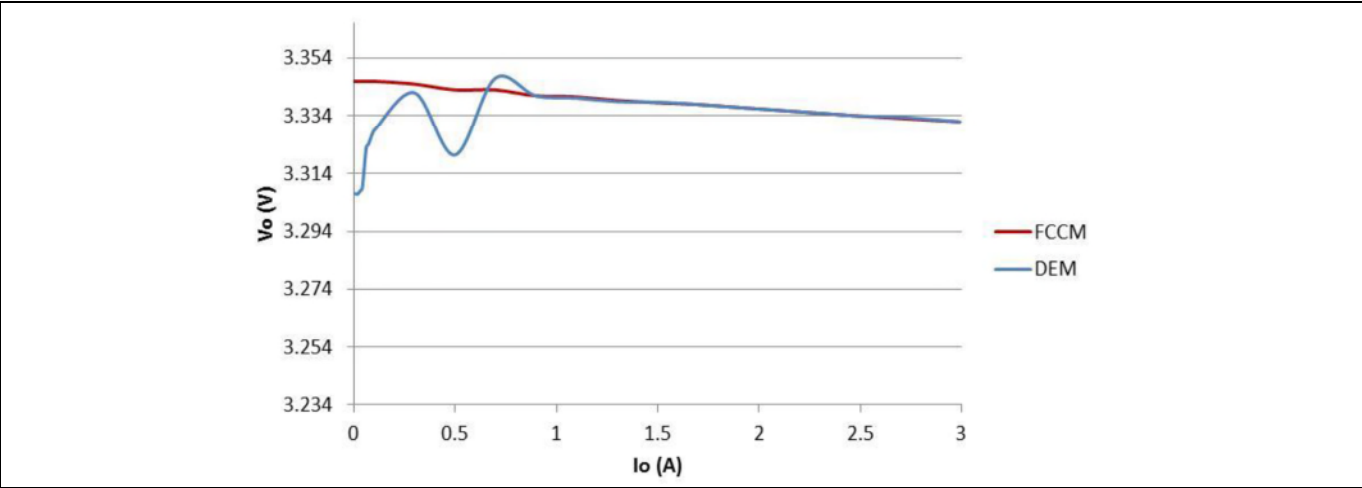


Figure 18 IR3883 load regulation @ $PV_{in} = V_{in} = 12\text{ V}$, $V_0 = 3.3\text{ V}$

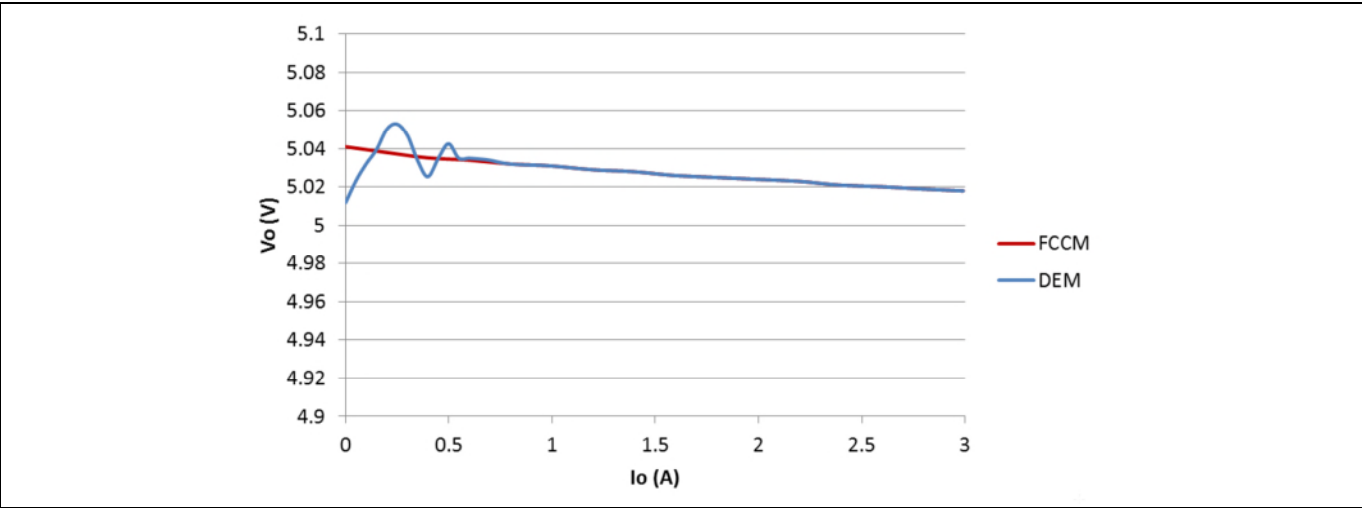


Figure 19 IR3883 load regulation @ $PV_{in} = V_{in} = 12\text{ V}$, $V_0 = 5\text{ V}$

4 Reference design examples for 5V input

Reference designs for $PV_{in} = V_{in} = V_{CC} = 5\text{ V}$, $I_{o\max} = 3\text{ A}$

4.1 Bill of material

Table 4 Bill of material for $PV_{in} = V_{in} = V_{CC} = 5\text{ V}$, $I_{o\max} = 3\text{ A}$

V _o (V)	R4	R1	R6 (kΩ) (R _{FB1})	R7 (kΩ) (R _{FB2})	L1 (μH)	P/N	C9 (pF) (C _{ff})	C10, C11(μF) (C _{out})
0.9	0	0	15	18.7	1	XEL4030-102 DCR = 8.89 mΩ 4 mm x 4 mm x 3.1 mm	100	2 x 22 μF 6.3 V X5R 20% 0805
1			16.5	16.5				
1.2			16.5	11.8			220	
1.8			16.5	6.34	1.5	XEL4030-152 DCR = 15.1 mΩ 4 mm x 4 mm x 3.1 mm		
2.5			16.5	4.12				

4.2 Transient load response

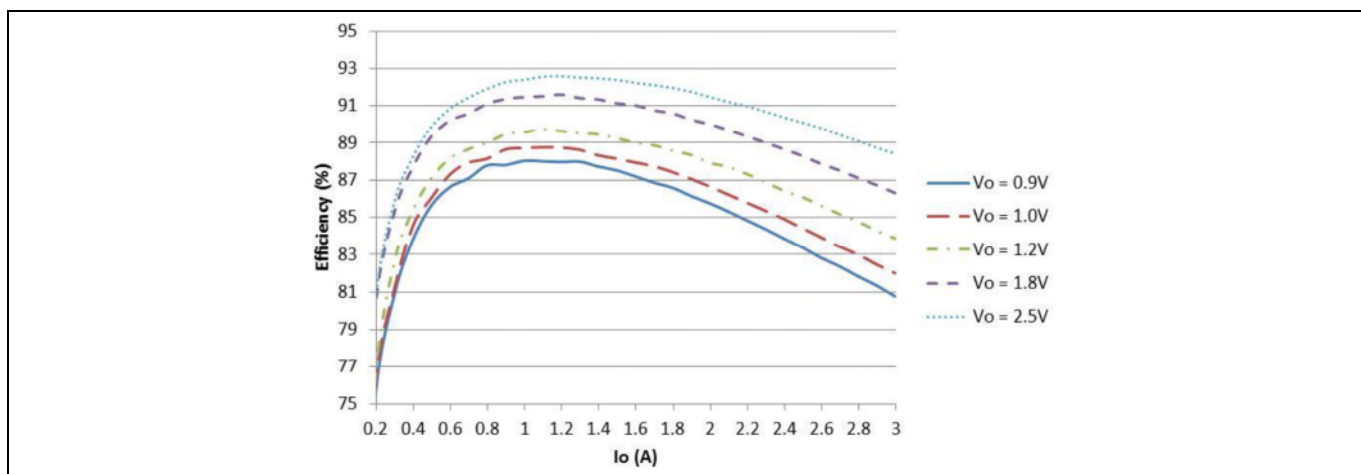
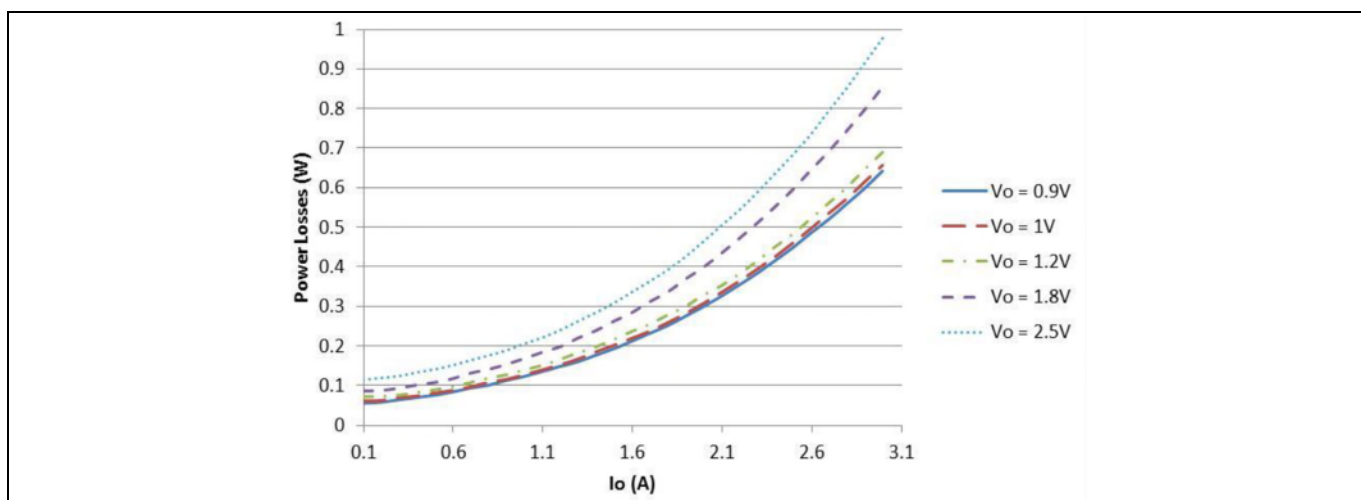
Table 5 $PV_{in} = V_{in} = V_{CC} = 5\text{ V}$, $I_o = 0\text{ A} - 1\text{ A @ } 2.5\text{ A}/\mu\text{s}$

V_o (V)	Overshoot/Undershoot (mV) (I_o step = 1 A @ 2.5 A/ μ s)
0.9	30 mV/-10 mV
1	32 mV/-12.4 mV
1.2	34 mV/-20 mV
1.8	40 mV/-28 mV
2.5	50 mV/-40 mV

4.3 Typical efficiency and power loss curves

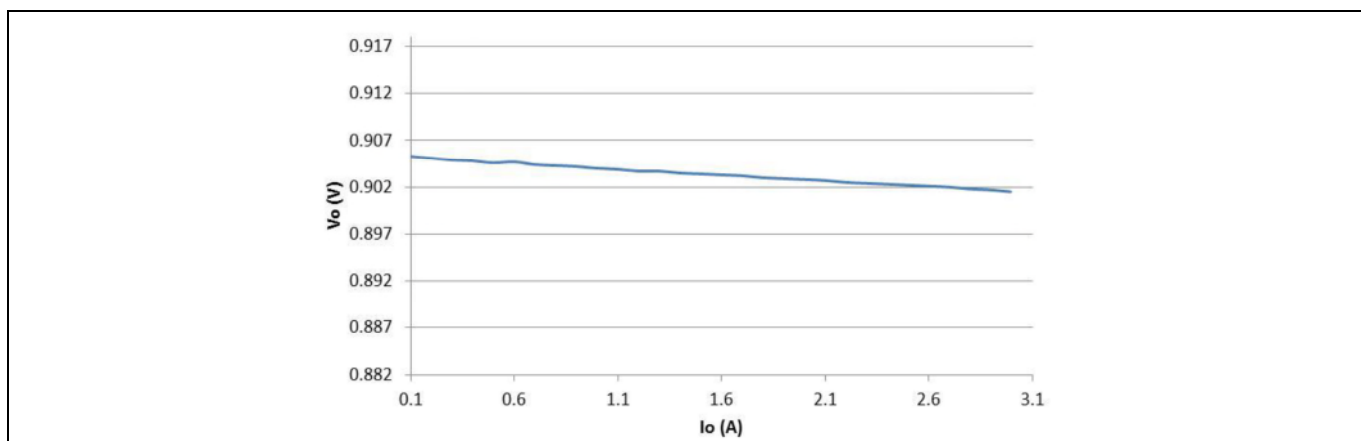
$PV_{in} = V_{in} = V_{CC} = 5\text{ V}$, $I_o = 0\text{ A} - 3\text{ A}$, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3883, the inductor losses and the losses of the input and output capacitors. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Reference design examples for 5V input

Figure 20 IR3883 efficiency @ $PV_{in} = V_{in} = V_{cc} = 5$ V and FCCMFigure 21 IR3883 power losses @ $PV_{in} = V_{in} = V_{cc} = 5$ V and FCCM

4.4 Load regulation

$PV_{in} = V_{in} = V_{cc} = 5$ V, $I_o = 0$ A-3 A, Room Temperature, No Air Flow.

Figure 22 IR3883 load regulation @ $PV_{in} = V_{in} = V_{cc} = 5$ V and FCCM, $V_o = 0.9$ V

Reference design examples for 5V input

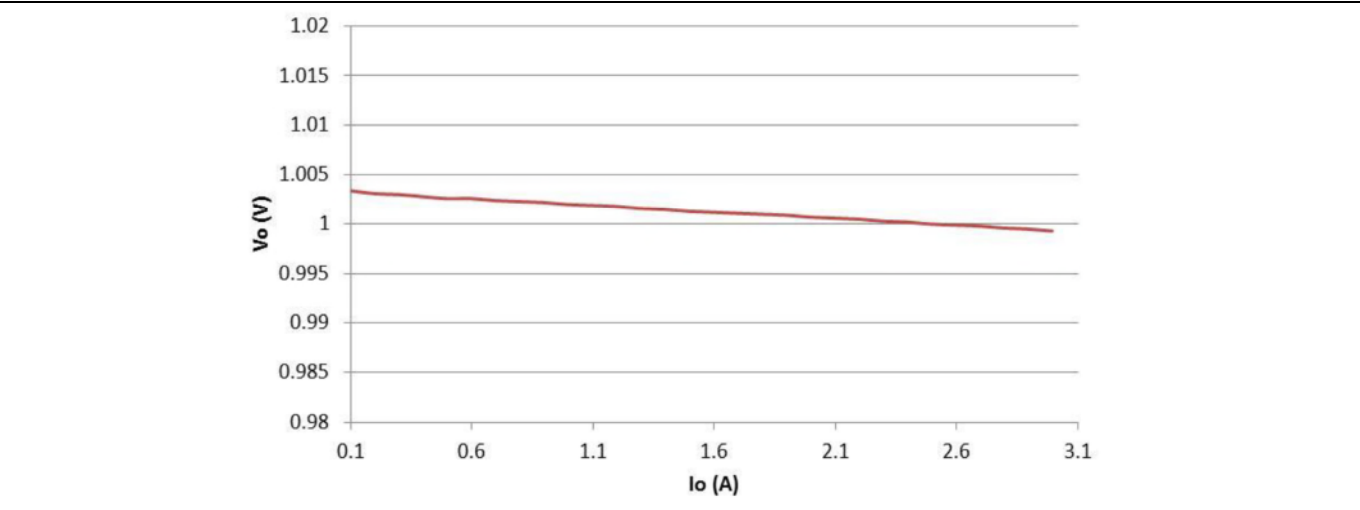


Figure 23 IR3883 load regulation @ $PV_{in} = V_{in} = V_{CC} = 5\text{ V}$ and FCCM, $V_o = 1.0\text{ V}$

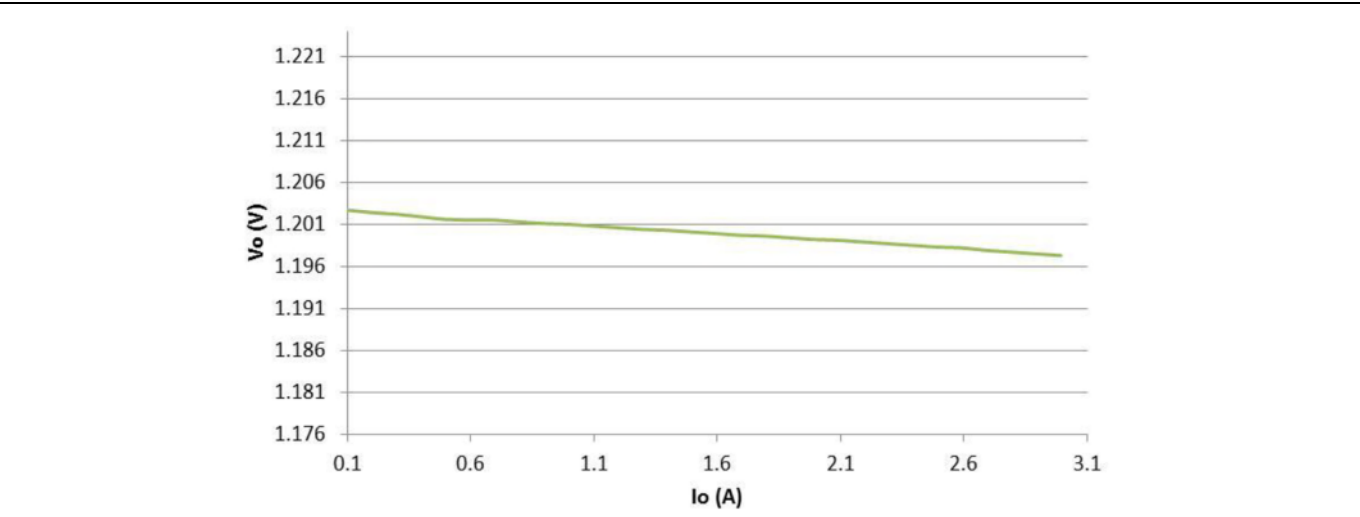


Figure 24 IR3883 load regulation @ $PV_{in} = V_{in} = V_{CC} = 5\text{ V}$ and FCCM, $V_o = 1.2\text{ V}$

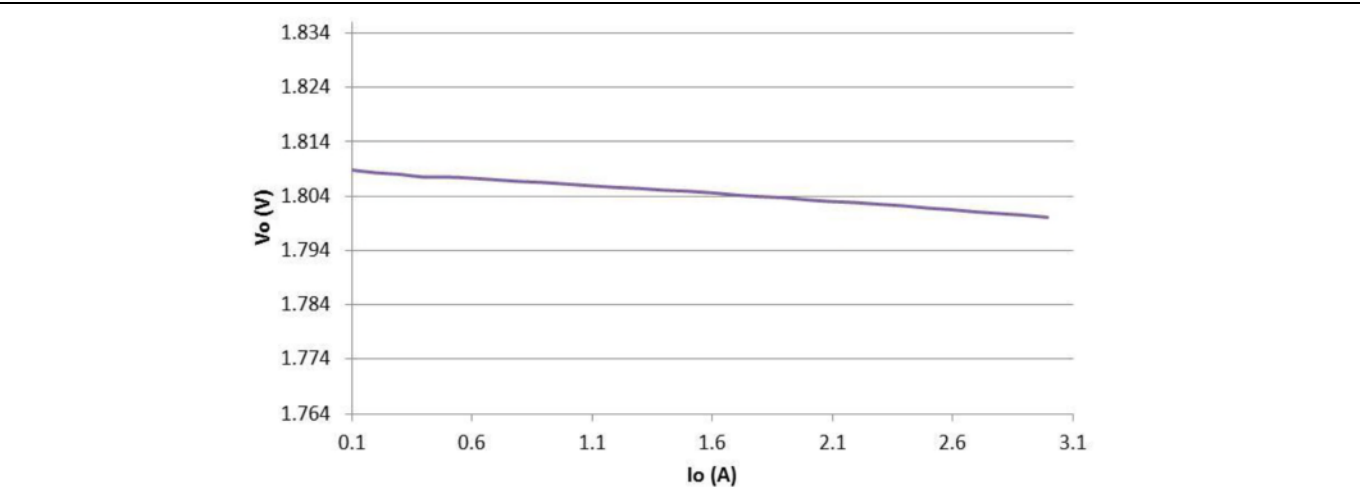


Figure 25 IR3883 load regulation @ $PV_{in} = V_{in} = V_{CC} = 5\text{ V}$ and FCCM, $V_o = 1.8\text{ V}$

Reference design examples for 5V input

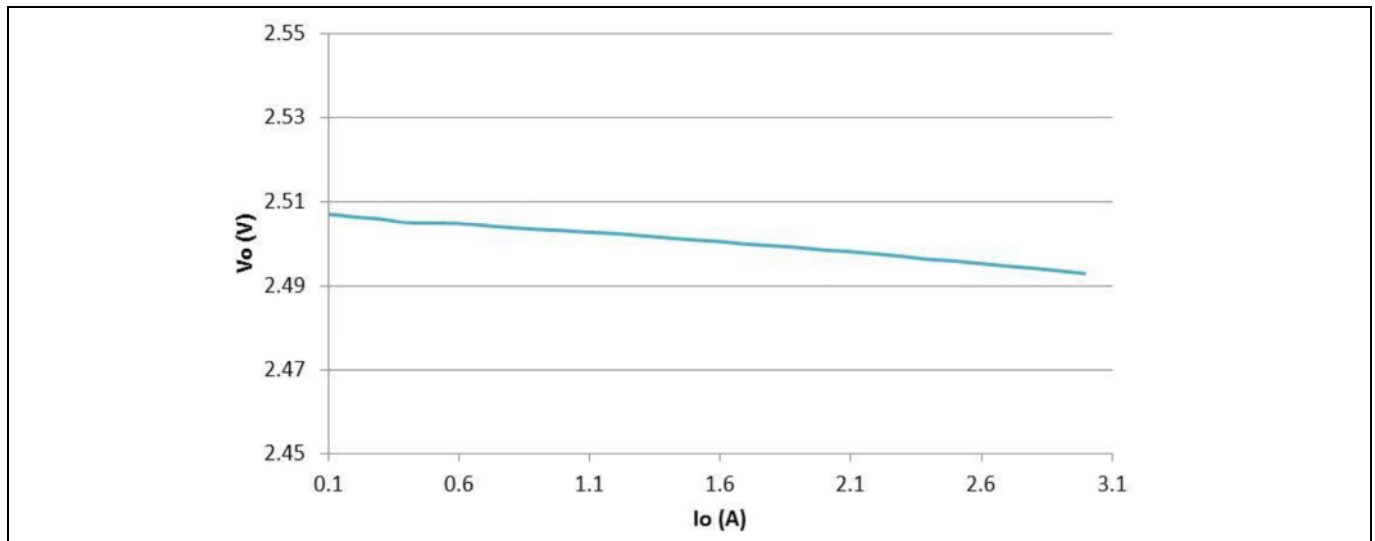


Figure 26 IR3883 load regulation @ $PV_{in} = V_{in} = V_{cc} = 5\text{ V}$ and FCCM, $V_o = 2.5\text{ V}$



Revision History

Revision History

Major changes since the last revision

Page or Reference	Description of change

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