International
IOR Rectifier
AN INFINEON TECHNOLOGIES COMPANY

IR7184SPBF

700V Half-Bridge Driver

Features

- Drives IGBT/MOSFET power devices
- Gate drive supplies up to 20V per channel
- Integrated deadtime protection
- Shoot-through (cross-conduction) protection
- Undervoltage lockout for V_{CC} and for V_{BS}
- 3.3V, 5V , 15V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Matched propagation delays
- -40°C to 125°C operating range
- RoHS compliant
- Lead-Free

Product Summary

V_{OFFSET}	≤ 700V
V_{OUT}	10V – 20V
I_{o+} & I_{o-} (typ.)	1.9A / 2.3A
t_{ON} & t_{OFF} (typ.)	680ns & 270ns
Deadtime (typ.)	400ns

Description

The IR7184S is a high voltage, high speed, power MOSFET and IGBT gate driver with high-side and low-side referenced output channel. This IC is designed to be used with low-cost bootstrap power supplies. Proprietary HVIC and latch immune CMOS technologies have been implemented in a rugged monolithic structure. The floating logic input is compatible with standard CMOS or LSTTL outputs (down to 3.3V logic). The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Shoot-through protection circuitry and a minimum deadtime circuitry have been integrated into this IC. Propagation delays are matched to simplify the HVIC's use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high-side configuration, which operate up to 700V.

Package Options

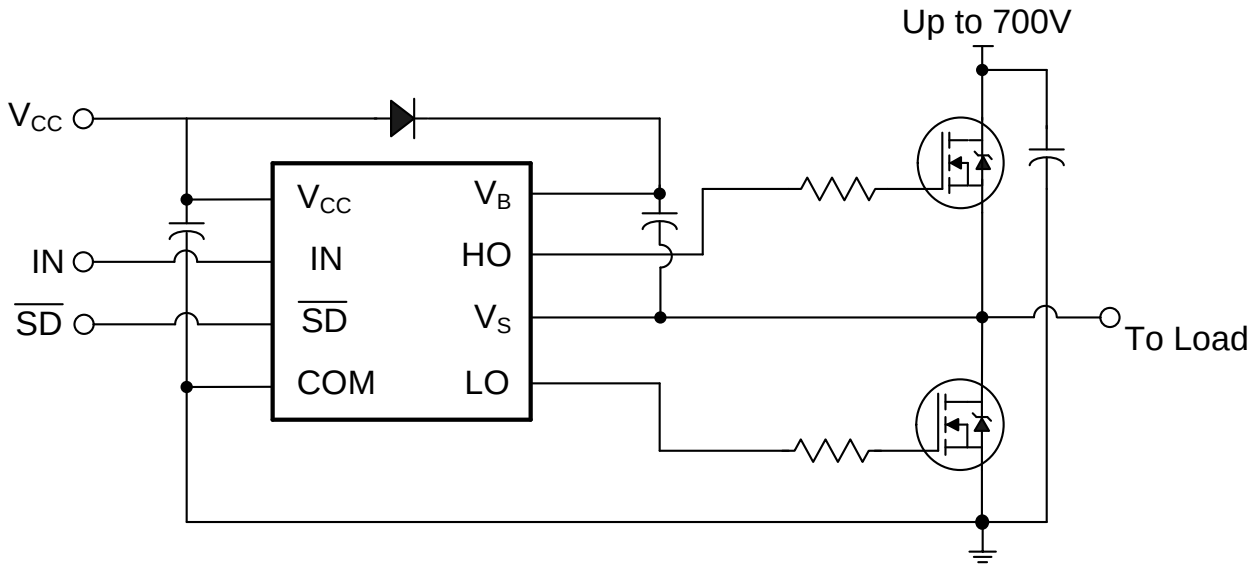
8-Lead SOIC

Typical Applications

- Appliance motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR7184SPBF	SO8N	Tube	95	IR7184SPBF
IR7184SPBF	SO8N	Tape and Reel	2500	IR7184STRPBF

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer tour Application Notes & DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Low side and logic fixed supply voltage	-0.3	25†	V
V_{IN}	Logic input voltage ($\overline{SD}$ & IN)	COM - 0.3	COM + 5.2	
V_B	High side floating absolute voltage	-0.3	725	
V_S	High side floating supply offset voltage	V_B- 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage	COM - 0.3	V_{CC} + 0.3	
COM	Power ground	V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^oC$	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	$^oC/W$
T_J	Junction temperature	—	150	^oC
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are tested at 25V.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15V.

Symbol	Definition	Min	Max	Units
V_{CC}	Low-side supply voltage	10	20	V
V_{IN}	IN, $\overline{SD}$ input voltage	0	5††	
V_B	High-side floating well supply voltage	V_S + 10	V_S + 20	
V_S	High-side floating well supply offset voltage†	COM - 5†	700	
V_{HO}	Floating gate drive output voltage	V_s	V_B	
V_{LO}	Low-side output voltage	COM	V_{CC}	
COM	Power ground	-5	5	
T_A	Ambient temperature	-40	125	^oC

† Logic operation for V_S of –8V to 600V. Logic state held for V_S of –5 V to $–V_{BS}$. Please refer to Design Tip DT97-3 for more details.

†† IN and /SD are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

(V_{CC} - COM) = (V_B - V_S) = 15V. T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

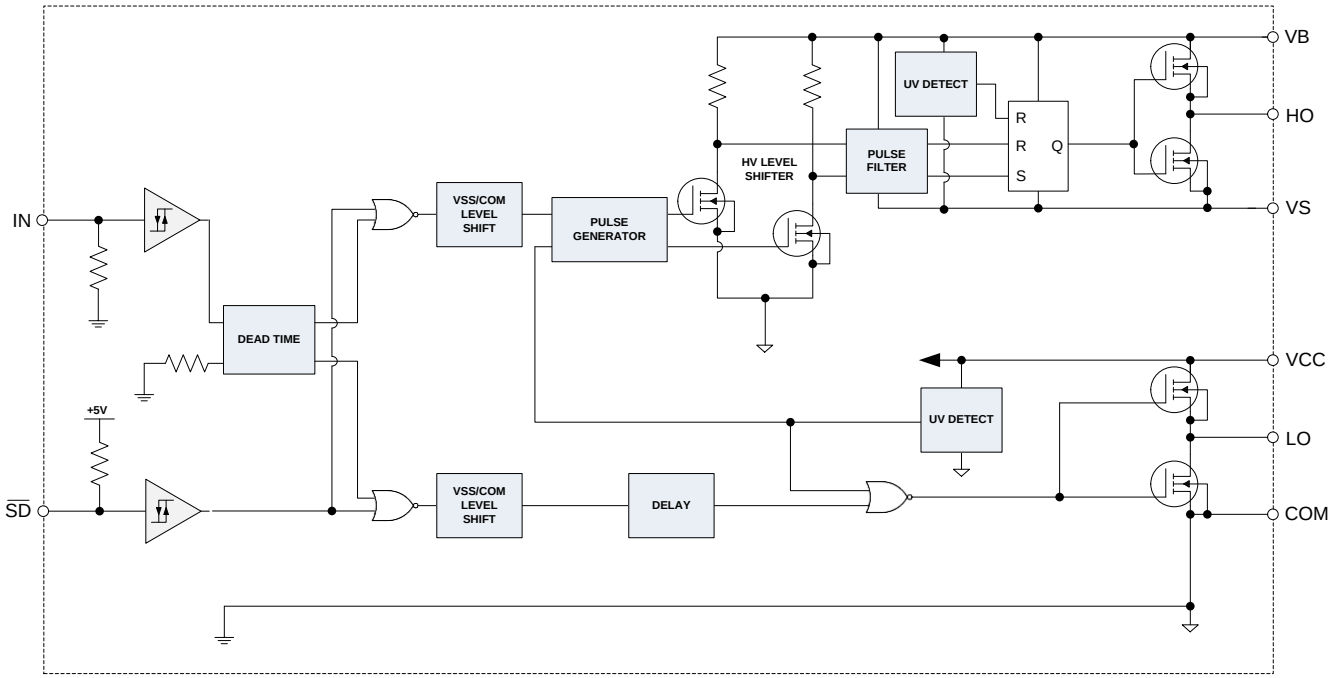
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.3	0.7	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8	8.9	9.8		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.3	0.7	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	µA	V_B = V_S = 700V
I_{QBS}	Quiescent V_{BS} supply current	—	60	150		V_{IN} = 0V, V_{IN} = 5V
I_{QCC}	Quiescent V_{CC} supply current	—	1000	1600		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	—	—	1.8	V	I_O = 0A
V_{OL}	Low level output voltage drop, V_O	—	—	0.3		
I_{o+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0V, PW ≤ 10µs
I_{o-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15V,, PW ≤ 10µs
V_{IH}	Logic “1” input voltage	2.7	—	—	V	
V_{IL}	Logic “0” input voltage	—	—	0.8		
$V_{SD,TH+}$	Logic “1” input voltage	2.7	—	—		
$V_{SD,\ TH-}$	Logic “0” input voltage	—	—	0.8		
I_{IN+}	Input bias current (HO = High)	—	25	60	µA	V_{IN} = 5V, V_{SD} = 0V
I_{IN-}	Input bias current (HO = Low)	—	—	1		V_{IN} = 0V , V_{SD} = 5V

Dynamic Electrical Characteristics

V_{CC}= V_B = 15V, V_S = COM, T_A = 25°C, and C_L = 1000pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	680	900	ns	V_S = 0V
t_{OFF}	Turn-off propagation delay	—	270	400		V_S = 0V or 700V
t_R	Turn-on rise time	—	40	60		V_S = 0V
t_F	Turn-off fall time	—	20	35		
MT_{ON}	Delay matching, HS & LS turn-on	—	0	90		
MT_{OFF}	Delay matching, HS & LS turn-off	—	0	50		
t_{SD}	Shut-down propagation delay	—	80	270		
DT	Deadtime	280	400	520		
MDT	Deadtime matching time	—	—	50		

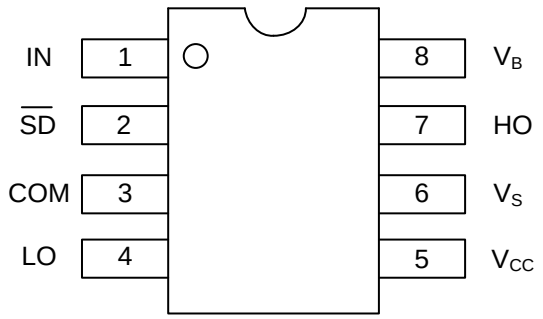
Functional Block Diagram



Lead Definitions

Symbol	Description
VCC	Low-side and logic supply voltage
VB	High-side gate drive floating supply
VS	High voltage floating supply return
IN	Logic inputs for high-side and low-side gate driver outputs
/SD	Logic inputs for shut-down
HO	High-side driver output
LO	Low-side driver output
COM	Low-side gate drive return

Lead Assignments



8-Lead SOIC

Application Information and Additional Details

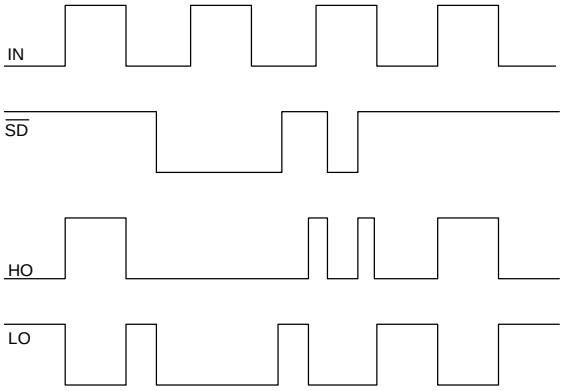


Figure 1. Input/Output Timing Diagram

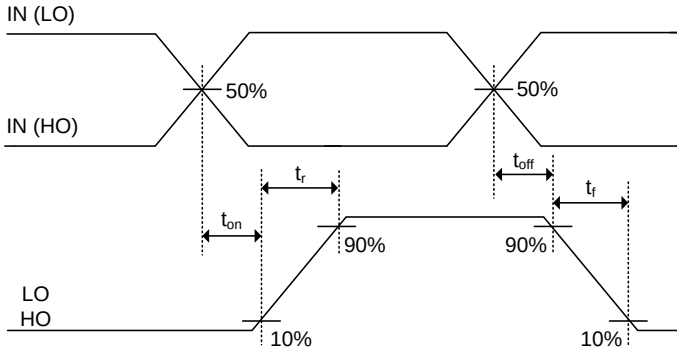


Figure 2. Switching Time Waveform Definitions

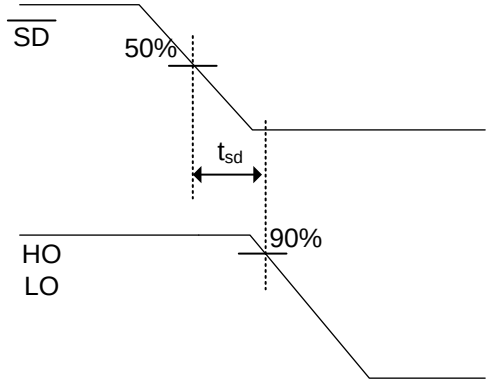


Figure 3. Shutdown Waveform Definitions

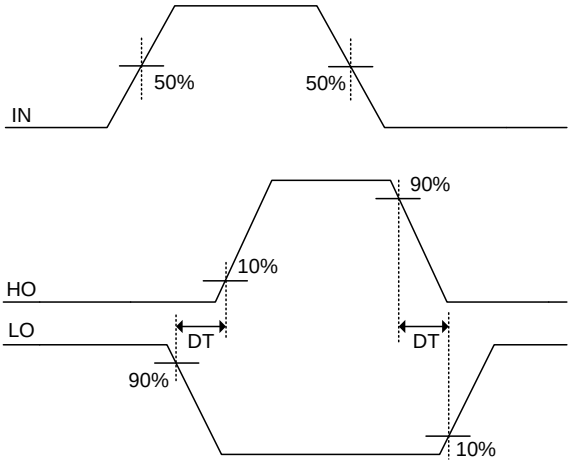


Figure 4. Deadtime Waveform Definitions

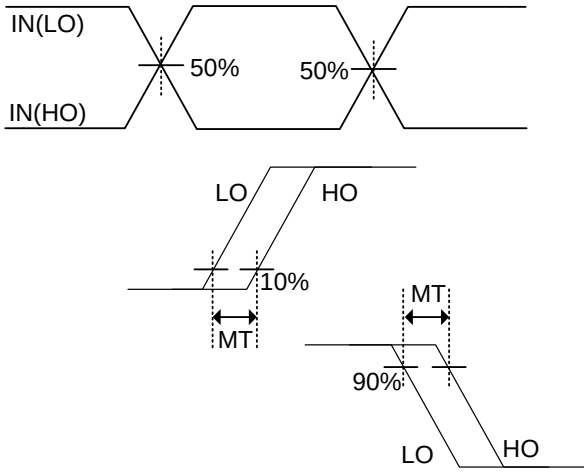
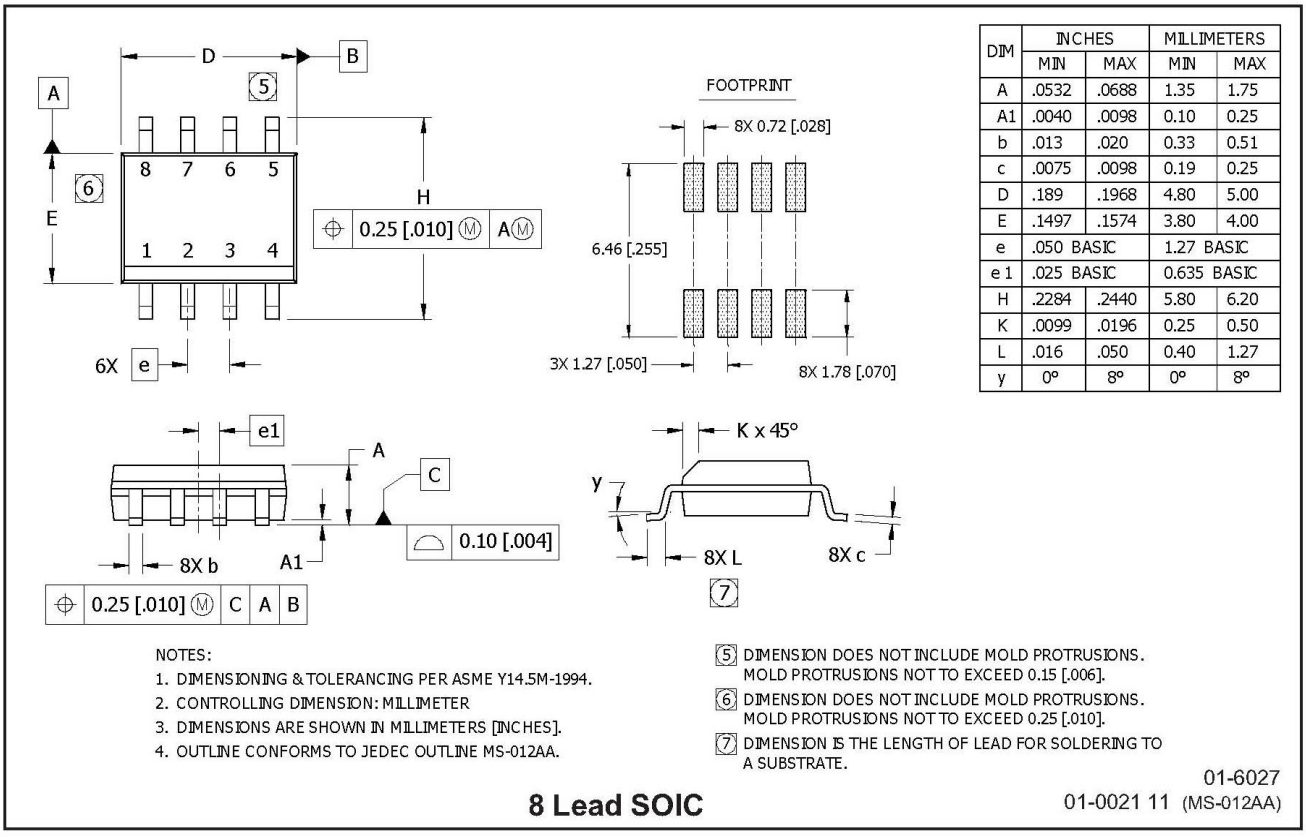


Figure 5. Delay Matching Waveform Definitions

Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

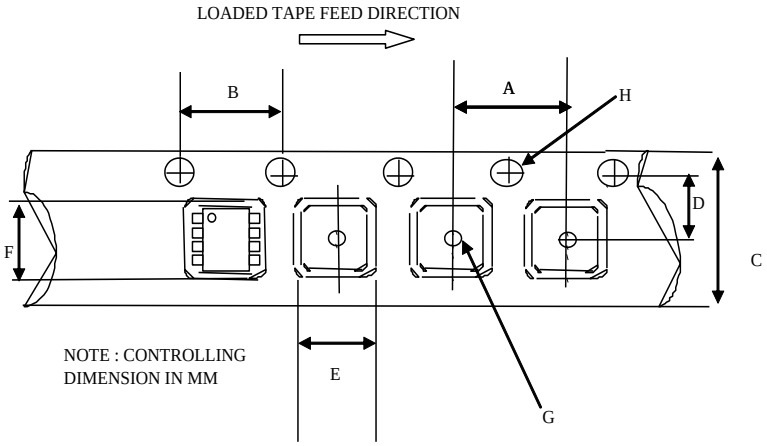
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

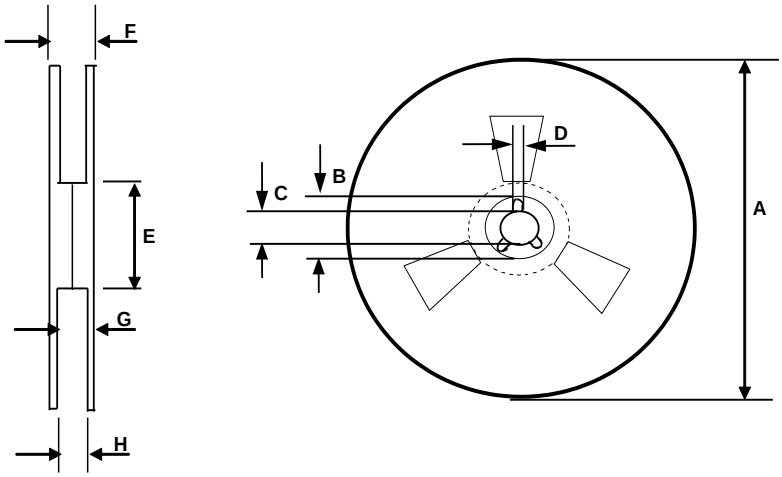
8 Lead SOIC

Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

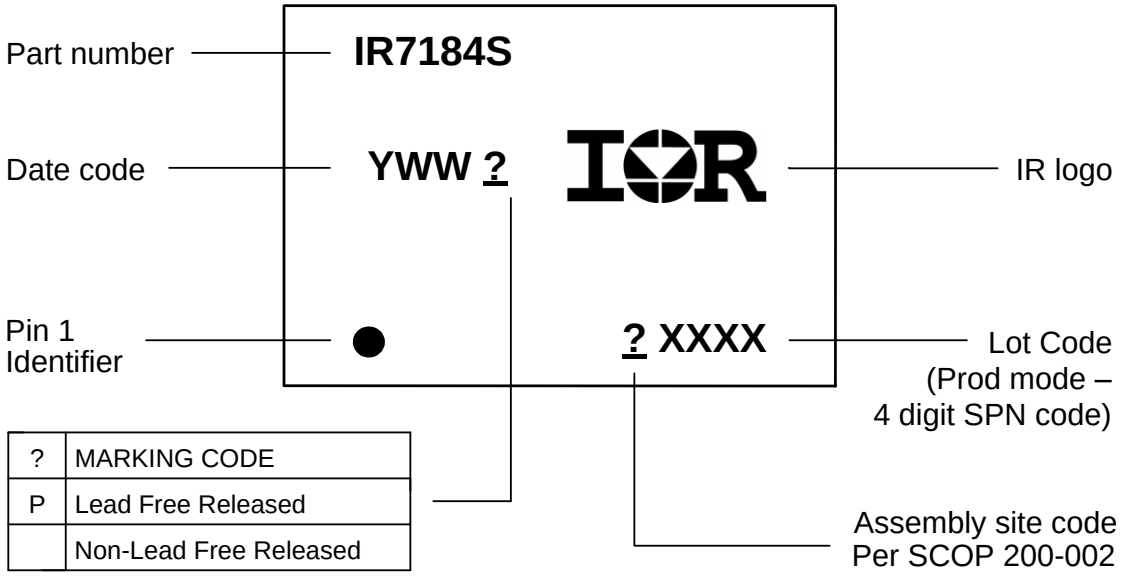
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		8 Lead SOIC	MSL2†††, 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 1B (per JEDEC standard JEDEC JS-001-2012)	
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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