

MOSFET

500V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

Adapter, Charger and Lighting

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	550	V
$R_{DS(on),max}$	3	Ω
I_D	2.6	A
$Q_{g,typ}$	4.3	nC
$I_{D,pulse}$	4.1	A
$E_{oss}@400V$	0.49	μJ

Type / Ordering Code	Package	Marking	Related Links
IPN50R3K0CE	PG-SOT223	50S3K0	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	2.6 1.6	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	4.1	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	18	mJ	$I_D = 0.5\text{A}$; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.03	mJ	$I_D = 0.5\text{A}$; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	0.5	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	5.0	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	0.8	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	4.1	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$
Maximum diode commutation speed ³⁾	di/dt	-	-	500	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJS}	-	-	25.4	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient for minimal footprint	R_{thJA}	-	-	160	$^\circ\text{C/W}$	minimal footprint
Thermal resistance, junction - ambient soldered on copper area	R_{thJA}	-	-	75	$^\circ\text{C/W}$	Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm ² (one layer 70 μm thick) copper area for drain connection and cooling. PCB is vertical without blown air.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	reflow MSL3

¹⁾ DPAK equivalent. Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClk} = 400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{GS(th)}$	2.50	3	3.50	V	$V_{DS}=V_{GS}$, $I_D=0.03mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=500V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=500V$, $V_{GS}=0V$, $T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.70	3.00	Ω	$V_{GS}=13V$, $I_D=0.4A$, $T_j=25^\circ C$ $V_{GS}=13V$, $I_D=0.4A$, $T_j=150^\circ C$
Gate resistance	R_G	-	6	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	84	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Output capacitance	C_{oss}	-	7	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	6	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	19	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	7.3	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=0.5A$, $R_G=5.3\Omega$
Rise time	t_r	-	5.8	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=0.5A$, $R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	23	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=0.5A$, $R_G=5.3\Omega$
Fall time	t_f	-	49	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=0.5A$, $R_G=5.3\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.5	-	nC	$V_{DD}=400V$, $I_D=0.5A$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	2.6	-	nC	$V_{DD}=400V$, $I_D=0.5A$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	4.3	-	nC	$V_{DD}=400V$, $I_D=0.5A$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=400V$, $I_D=0.5A$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.83	-	V	$V_{GS}=0V$, $I_F=0.5A$, $T_f=25^{\circ}C$
Reverse recovery time	t_{rr}	-	99	-	ns	$V_R=400V$, $I_F=0.5A$, $di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	0.3	-	μC	$V_R=400V$, $I_F=0.5A$, $di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	4.2	-	A	$V_R=400V$, $I_F=0.5A$, $di_F/dt=100A/\mu s$

4 Electrical characteristics diagrams

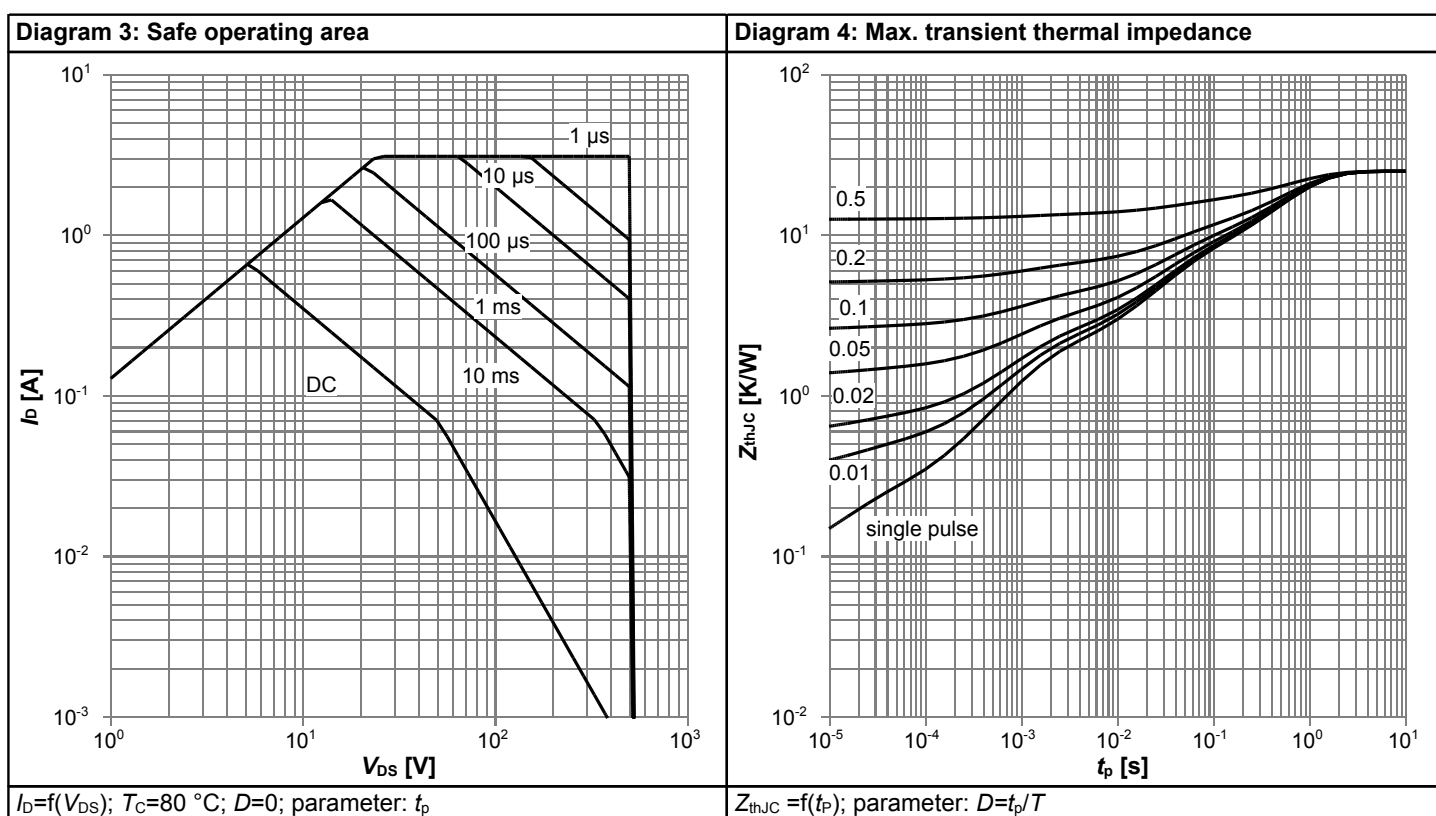
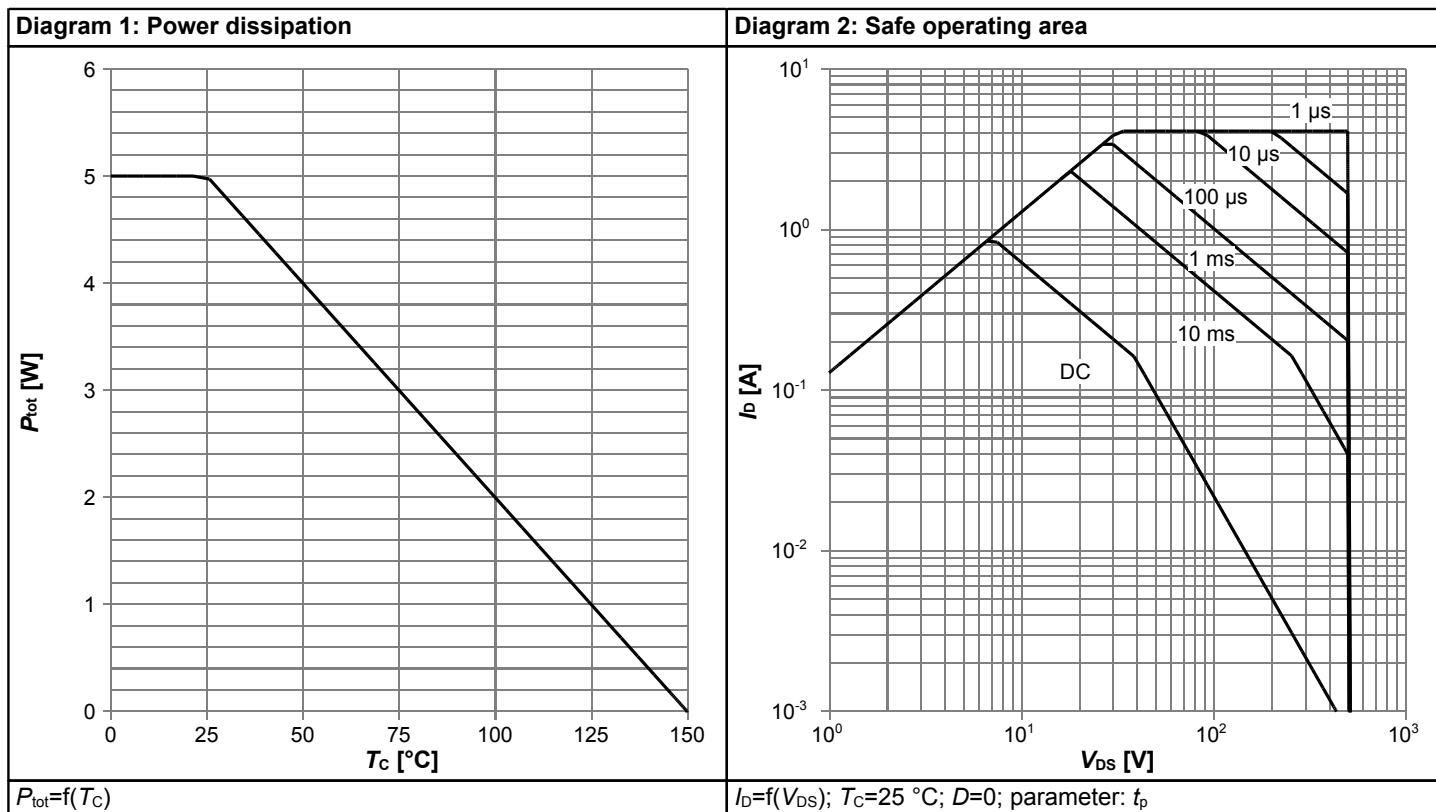
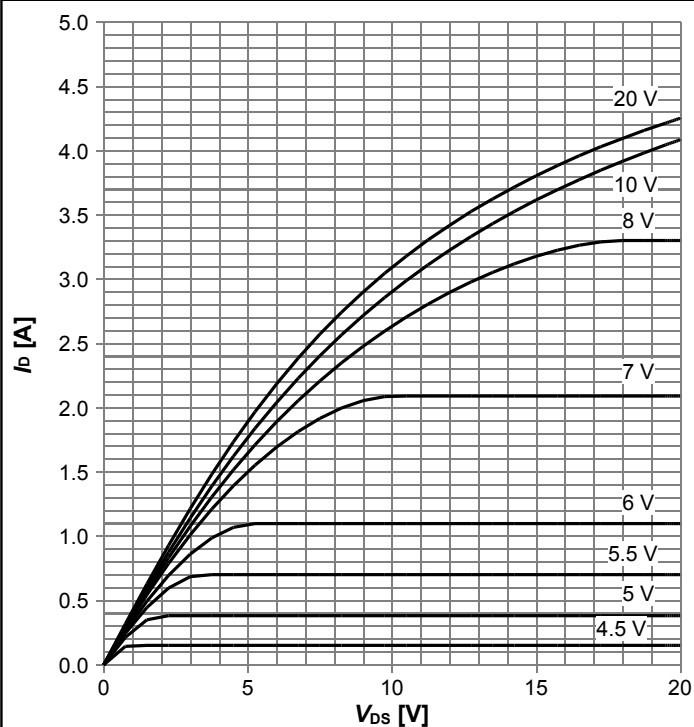
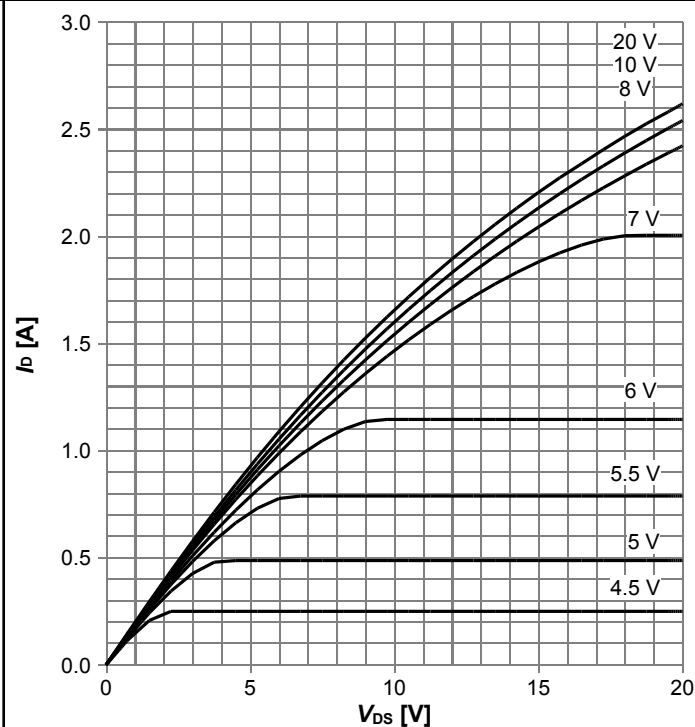


Diagram 5: Typ. output characteristics



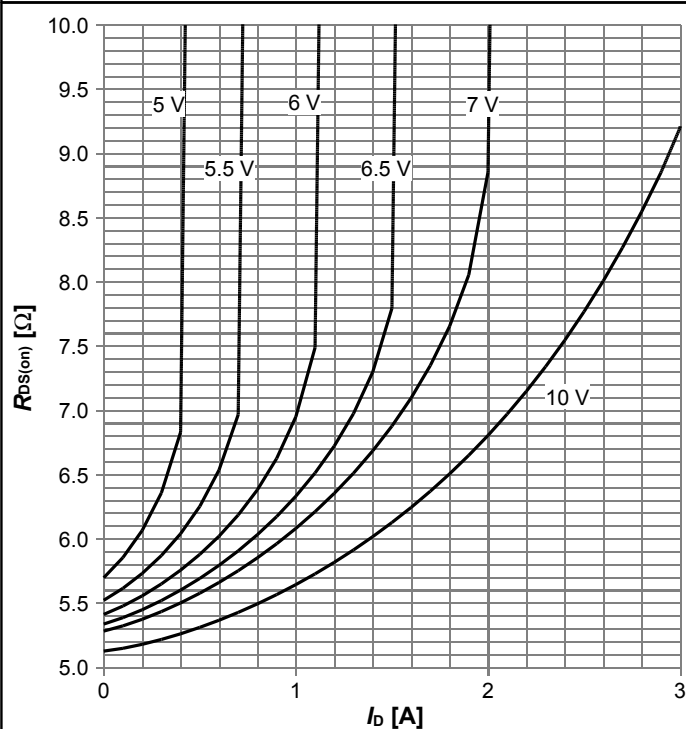
$I_D = f(V_{DS})$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



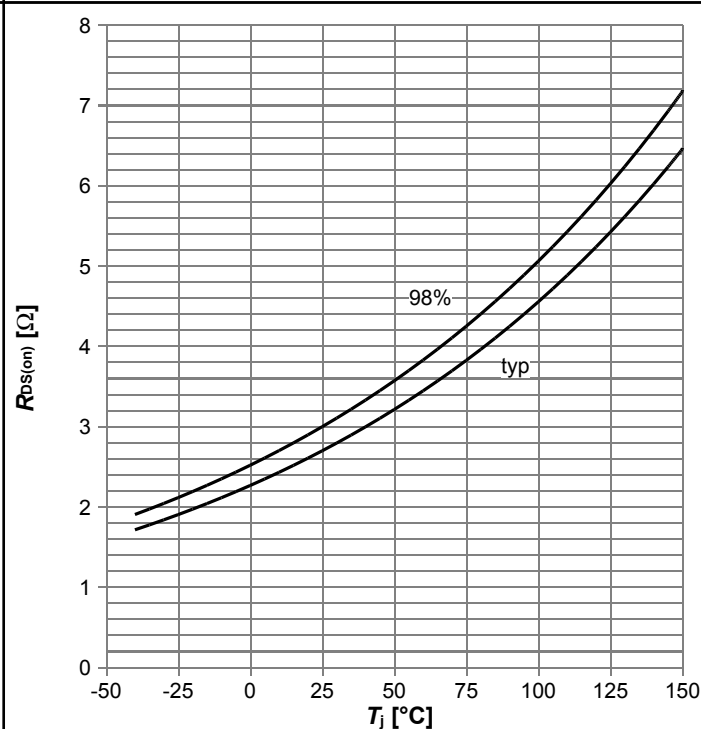
$I_D = f(V_{DS})$; $T_J = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



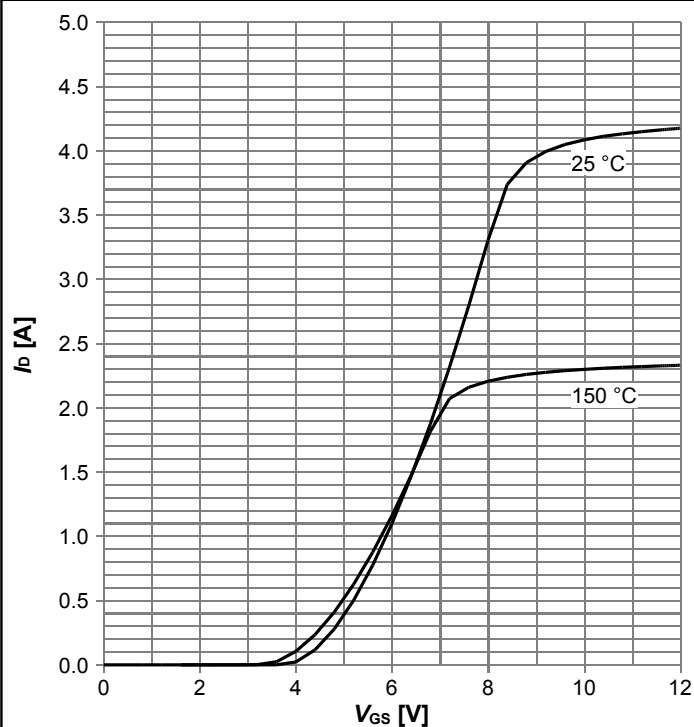
$R_{DS(on)} = f(I_D)$; $T_J = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



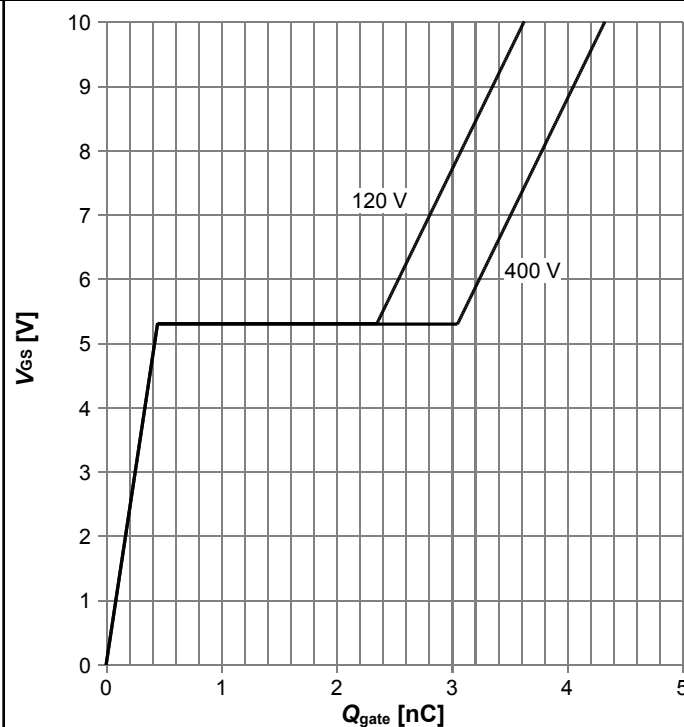
$R_{DS(on)} = f(T_J)$; $I_D = 0.4\text{ A}$; $V_{GS} = 13\text{ V}$

Diagram 9: Typ. transfer characteristics



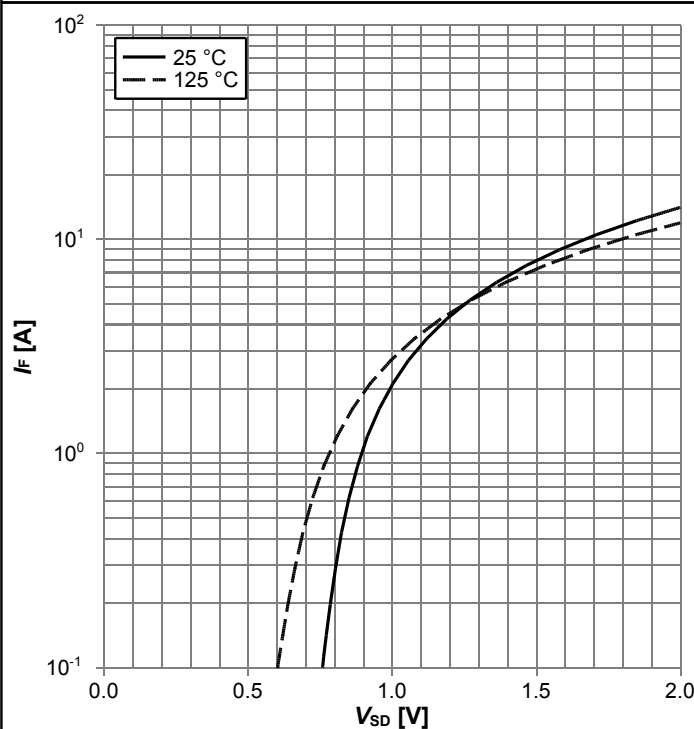
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



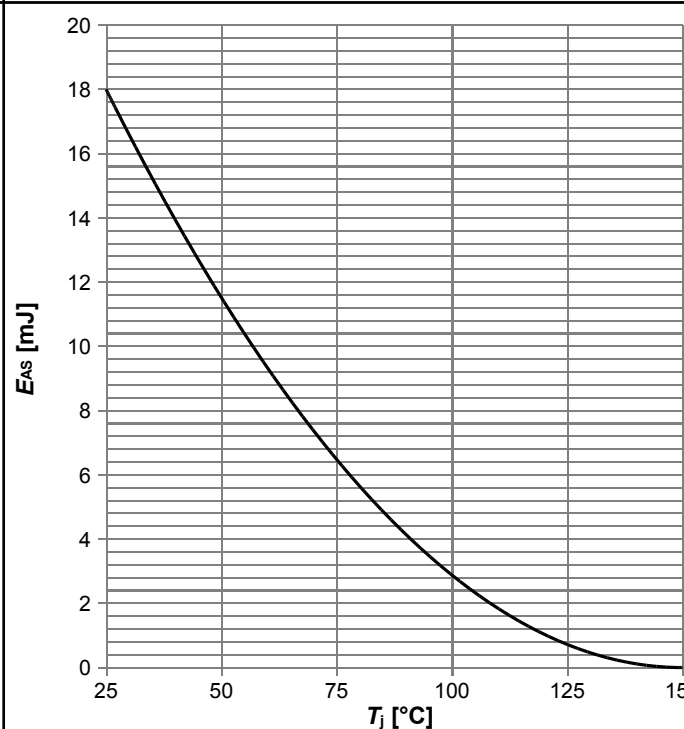
$V_{GS} = f(Q_{gate})$; $I_D = 0.5$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



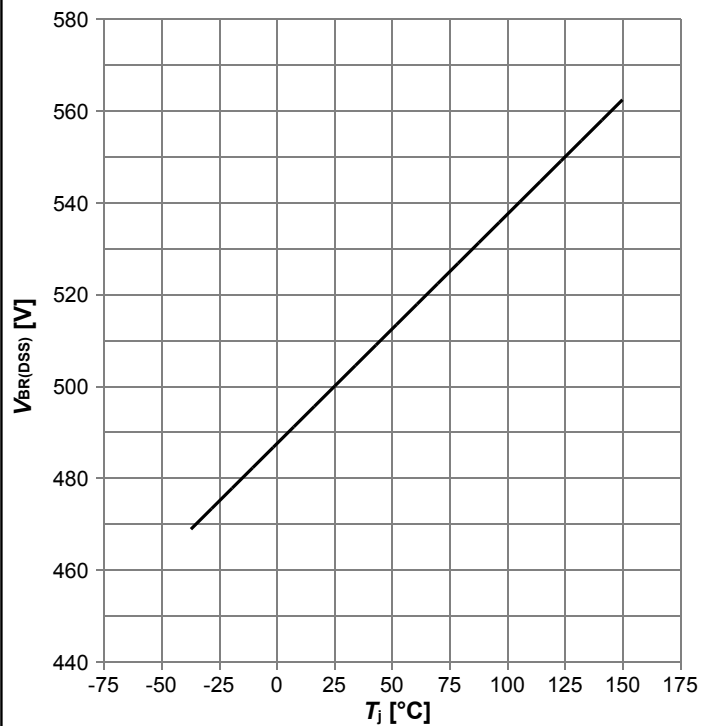
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



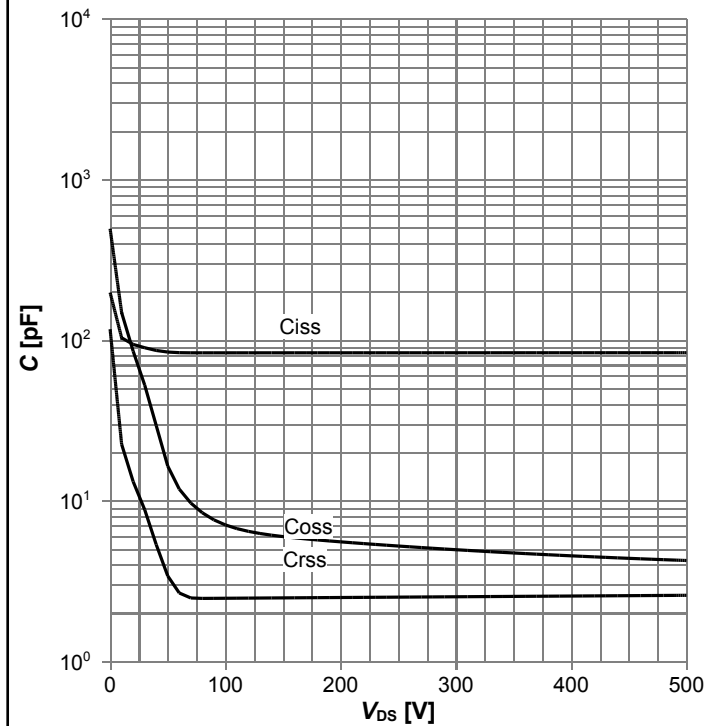
$E_{AS} = f(T_j)$; $I_D = 0.5$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



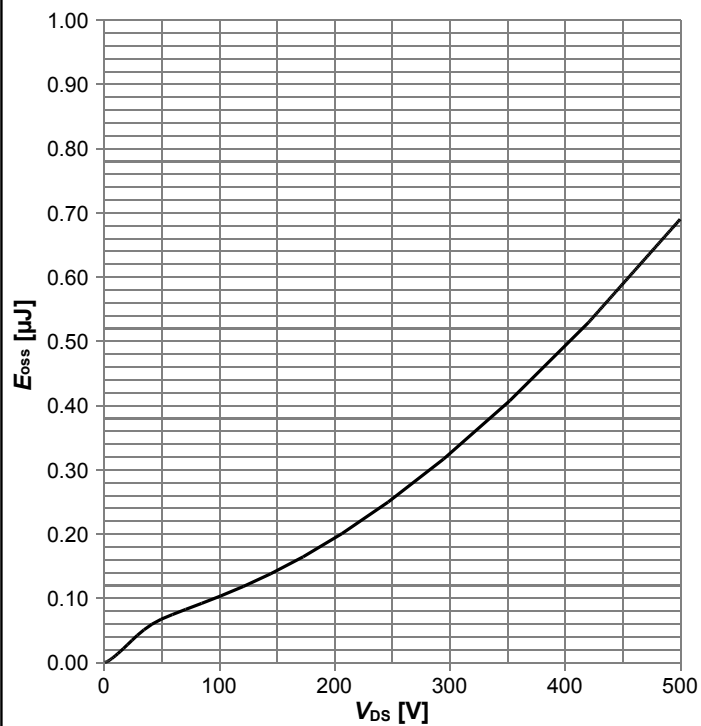
$V_{BR(DSS)} = f(T_J); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
 $R_{g1} = R_{g2}$	 $t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$

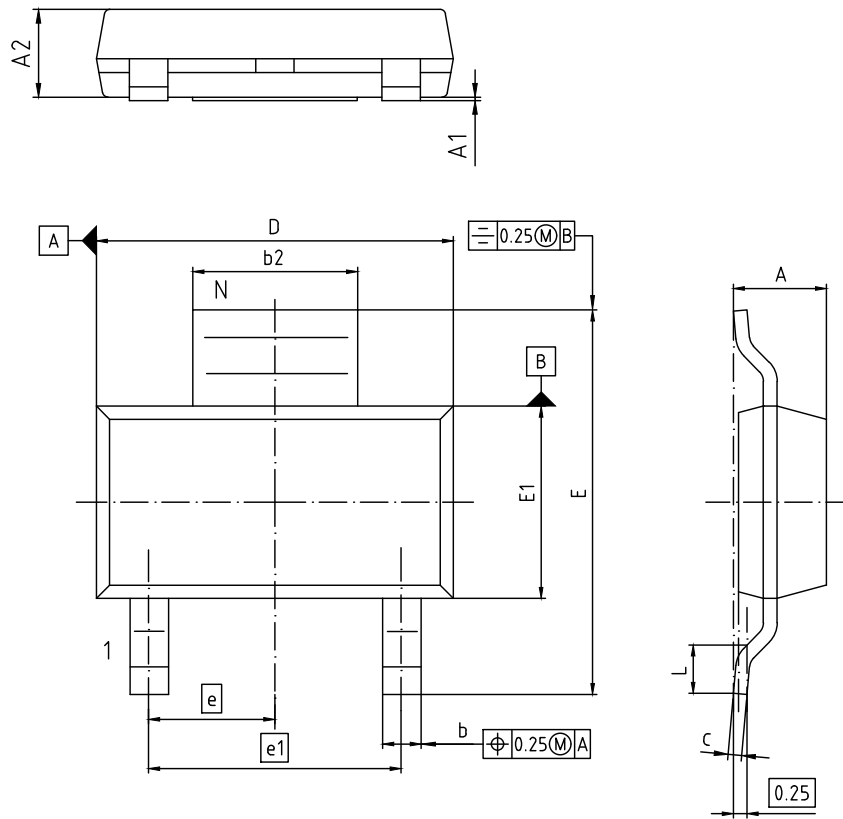
Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

DOCUMENT NO. Z8B00180553
SCALE 0 2.5 5mm
EUROPEAN PROJECTION
ISSUE DATE 24-02-2016
REVISION 01

Figure 1 Outline PG-SOT223, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPN50R3K0CE

Revision: 2016-06-13, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-04-29	Release of final version
2.1	2016-06-13	Updated ID ratings

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81726 München, Germany
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