

CoolMOS™ Power Transistor

Features

- Lowest figure of merit $R_{ON} \times Q_g$
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Pb-free lead plating; RoHS compliant, Halogen free
- Fully qualified according to JEDEC¹⁾ for Industrial Applications

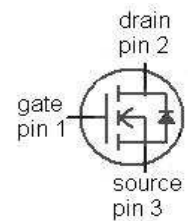
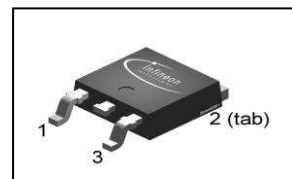
Product Summary

$V_{DS} @ T_{jmax}$	550	V
$R_{DS(on),max}$	0.399	Ω
$Q_{g,typ}$	17	nC

CoolMOS CP is designed for:

- Hard and softswitching SMPS topologies
- DCM PFC for Lamp Ballast
- PWM for Lamp Ballast & PDP and LCD TV

PG-TO252



Type	Package	Marking
IPD50R399CP	PG-TO252	5R399P

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	9	A
		$T_C=100\text{ °C}$	6	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	20	
Avalanche energy, single pulse	E_{AS}	$I_D=3.3\text{ A}$, $V_{DD}=50\text{ V}$	215	mJ
Avalanche energy, repetitive $t_{AR}^{2),3)}$	E_{AR}	$I_D=3.3\text{ A}$, $V_{DD}=50\text{ V}$	0.33	
Avalanche current, repetitive $t_{AR}^{2),3)}$	I_{AR}		3.3	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=0\ldots400\text{ V}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
		AC ($f>1\text{ Hz}$)	± 30	
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	83	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	°C

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	$T_C=25\text{ °C}$	4.9	A
Diode pulse current ²⁾	$I_{S,pulse}$		20	
Reverse diode dv/dt ⁴⁾	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.5	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, reflowsoldering	T_{solder}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=0.33\text{ mA}$	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=500\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=500\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	10	-	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$, $I_D=4.9\text{ A}$, $T_j=25\text{ °C}$	-	0.36	0.399	Ω
		$V_{GS}=10\text{ V}$, $I_D=4.9\text{ A}$, $T_j=150\text{ °C}$	-	0.90	-	
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	2.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V},$ $f=1\text{ MHz}$	-	890	-	pF
Output capacitance	C_{oss}		-	40	-	
Effective output capacitance, energy related ⁶⁾	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 400 V	-	38	-	
Effective output capacitance, time related ⁷⁾	$C_{o(tr)}$		-	81	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=400\text{ V},$ $V_{GS}=10\text{ V}, I_D=4.9\text{ A},$ $R_{G,ext}=35.1\ \Omega$	-	35	-	ns
Rise time	t_r		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	80	-	
Fall time	t_f		-	14	-	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD}=400\text{ V}, I_D=4.9\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	4	-	nC
Gate to drain charge	Q_{gd}		-	6	-	
Gate charge total	Q_g		-	17	23	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V

Reverse Diode

Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=4.9\text{ A},$ $T_j=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	$V_R=400\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	260	-	ns
Reverse recovery charge	Q_{rr}		-	1.9	-	μC
Peak reverse recovery current	I_{rrm}		-	12.2	-	A

¹⁾ J-STD20 and JESD22

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR} \cdot f$.

⁴⁾ $I_{SD} \leq I_D$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DClink}=400\text{ V}$, $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j,max}$, identical low and high side switch

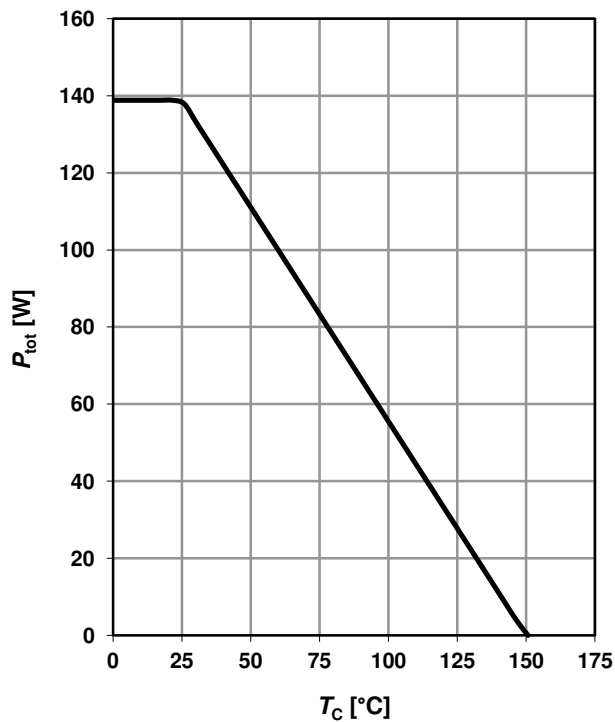
⁵⁾ Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70mm thick) copper area for drain connection. PCB without blown air.

⁶⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁷⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

1 Power dissipation

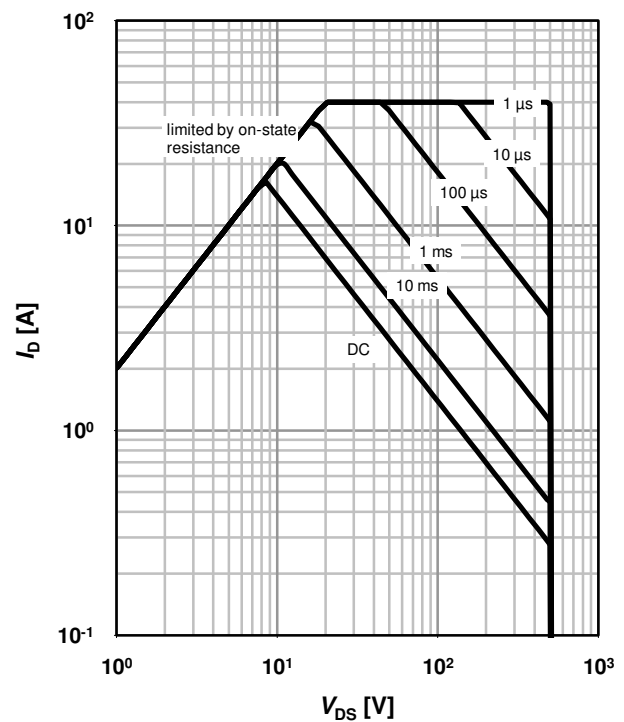
$$P_{\text{tot}} = f(T_C)$$



2 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

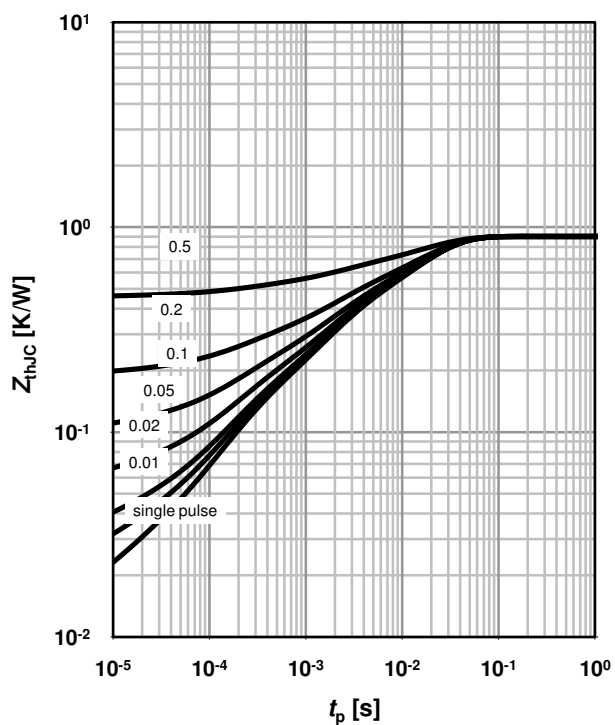
parameter: t_p



3 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

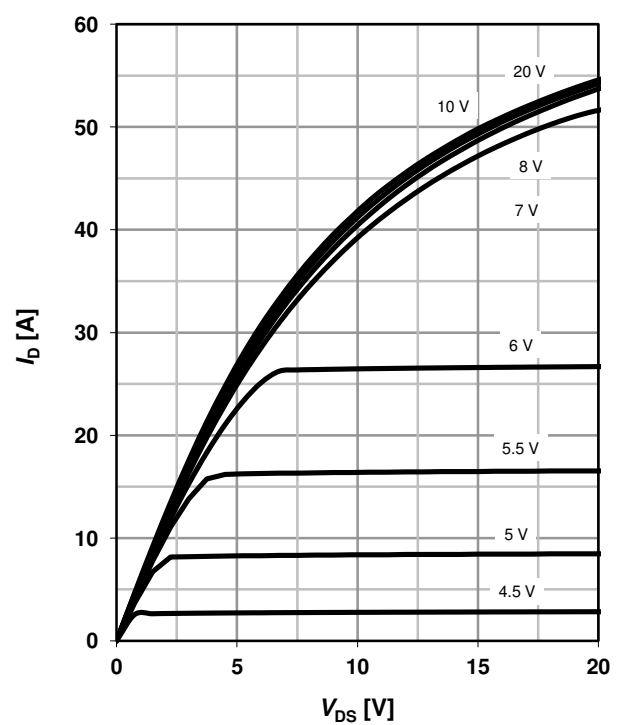
parameter: $D = t_p / T$



4 Typ. output characteristics

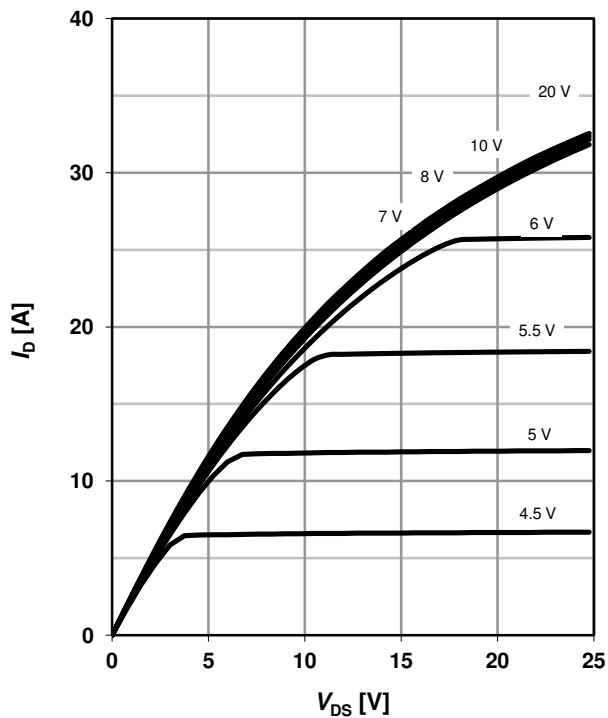
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: V_{GS}



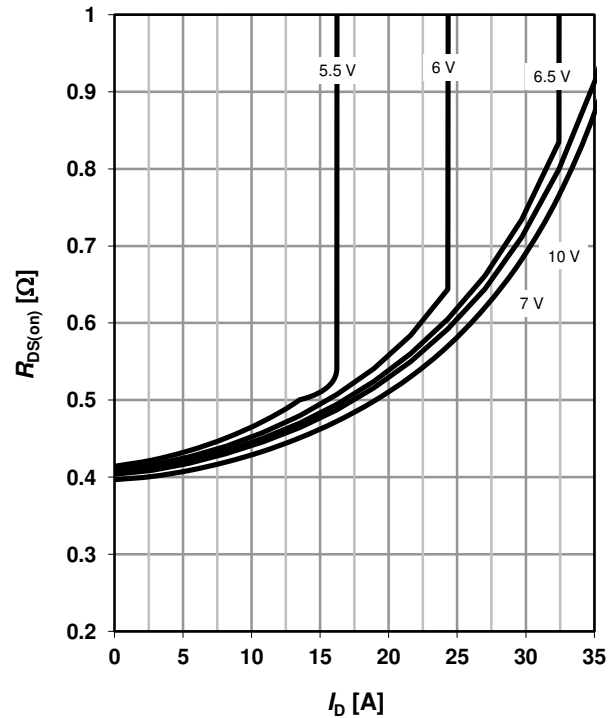
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 150^\circ\text{C}$

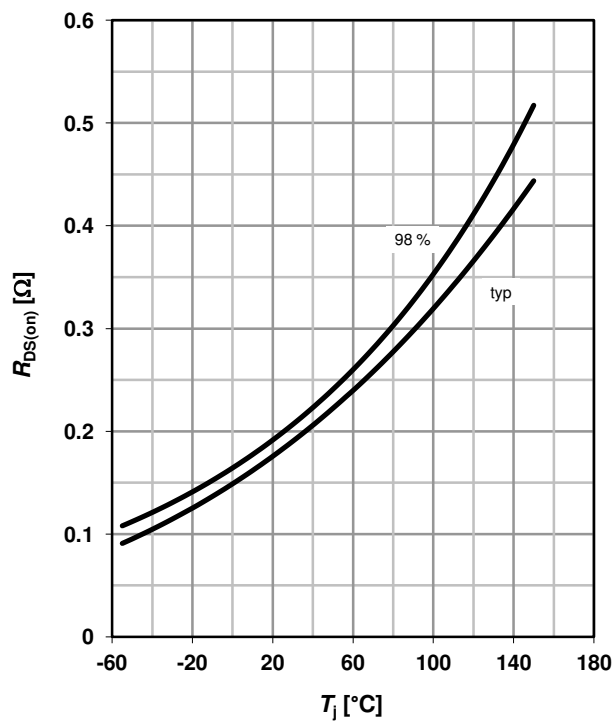
parameter: V_{GS}


6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 150^\circ\text{C}$

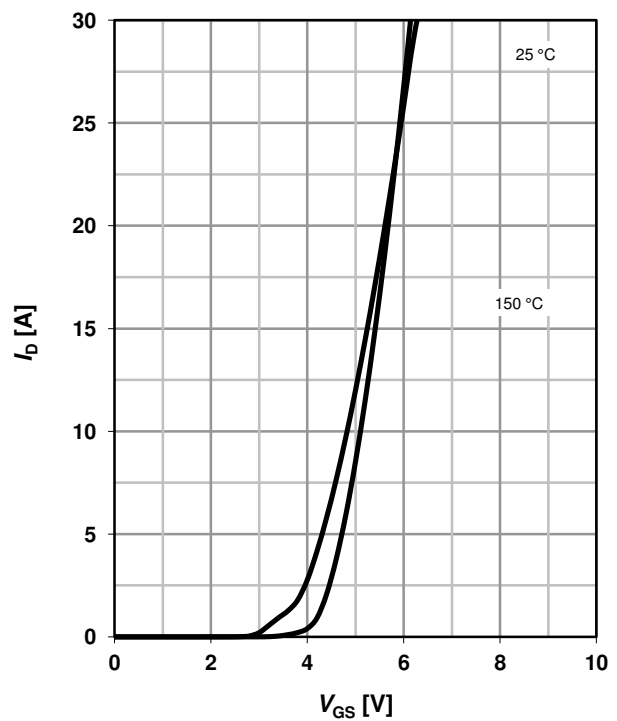
parameter: V_{GS}


7 Drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 4.9\text{ A}; V_{GS} = 10\text{ V}$


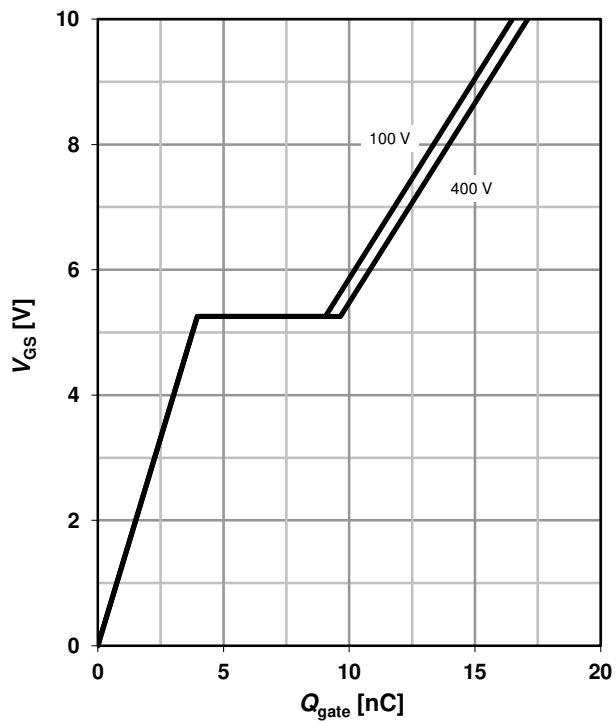
8 Typ. transfer characteristics

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)\text{max}}$

parameter: T_j


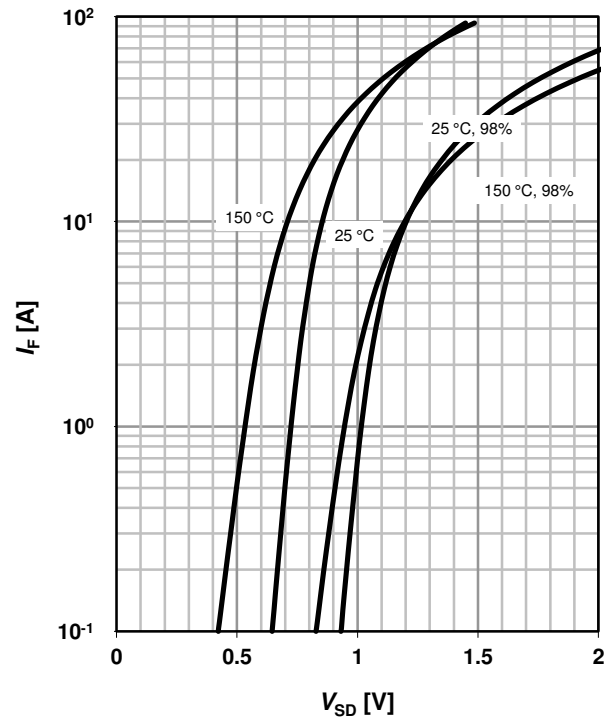
9 Typ. gate charge

 $V_{GS}=f(Q_{gate}); I_D=4.9\text{ A pulsed}$

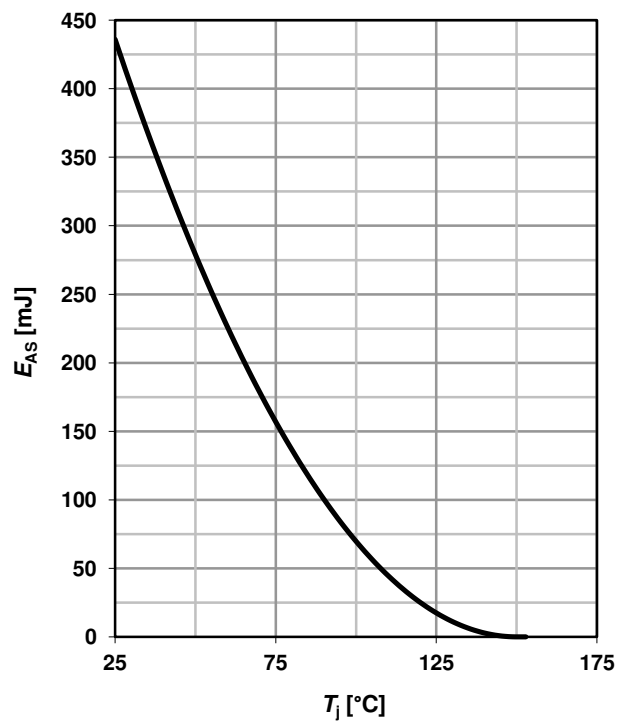
parameter: V_{DD}


10 Forward characteristics of reverse diode

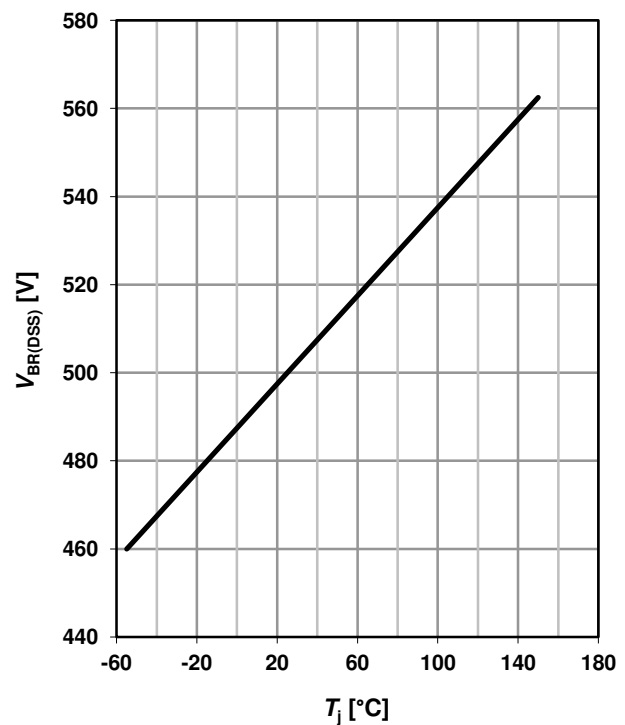
 $I_F=f(V_{SD})$

parameter: T_j


11 Avalanche energy

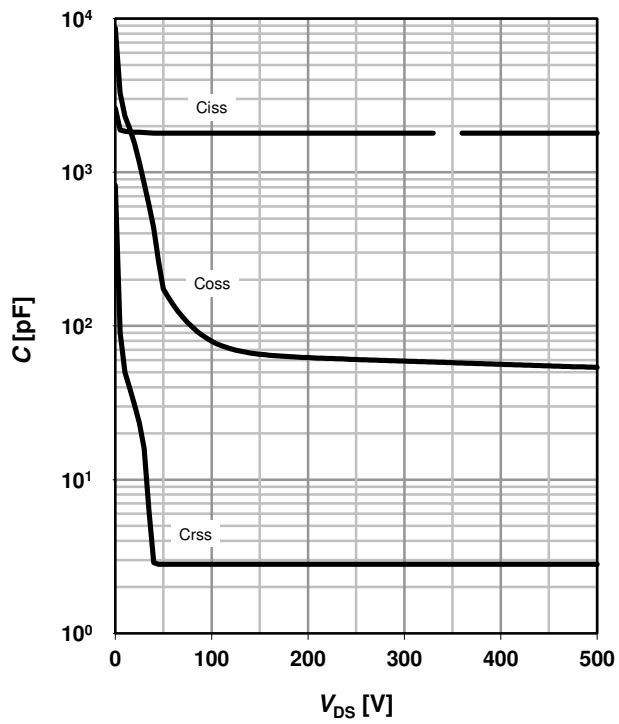
 $E_{AS}=f(T_j); I_D=3.3\text{ A}; V_{DD}=50\text{ V}$


12 Drain-source breakdown voltage

 $V_{BR(DSS)}=f(T_j); I_D=0.25\text{ mA}$


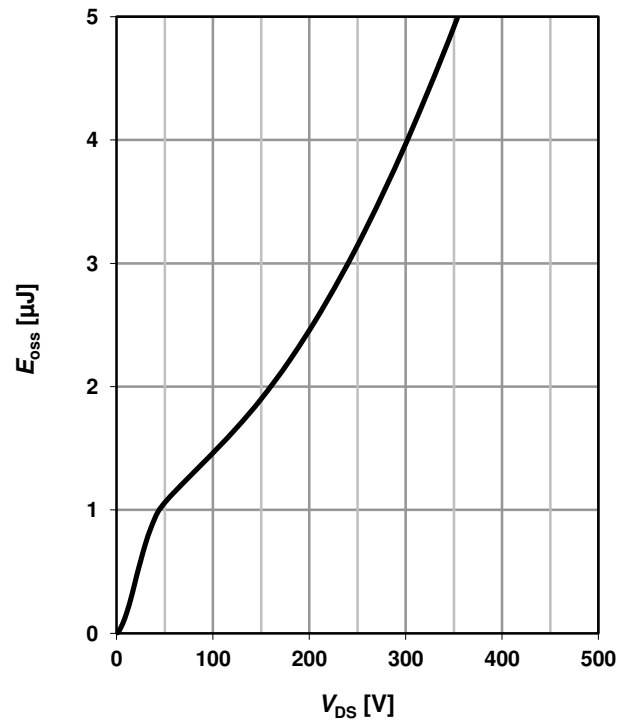
13 Typ. capacitances

$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

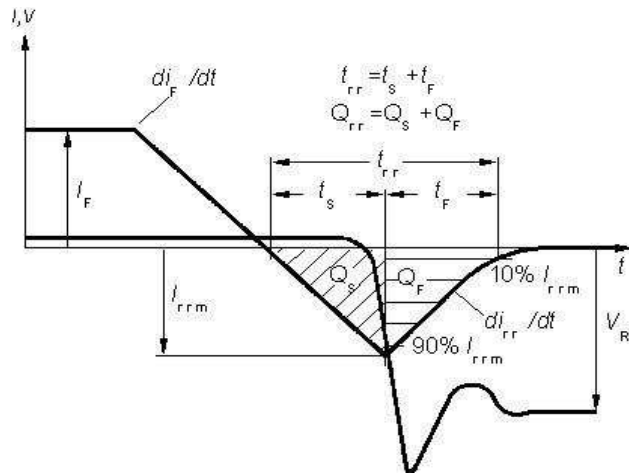


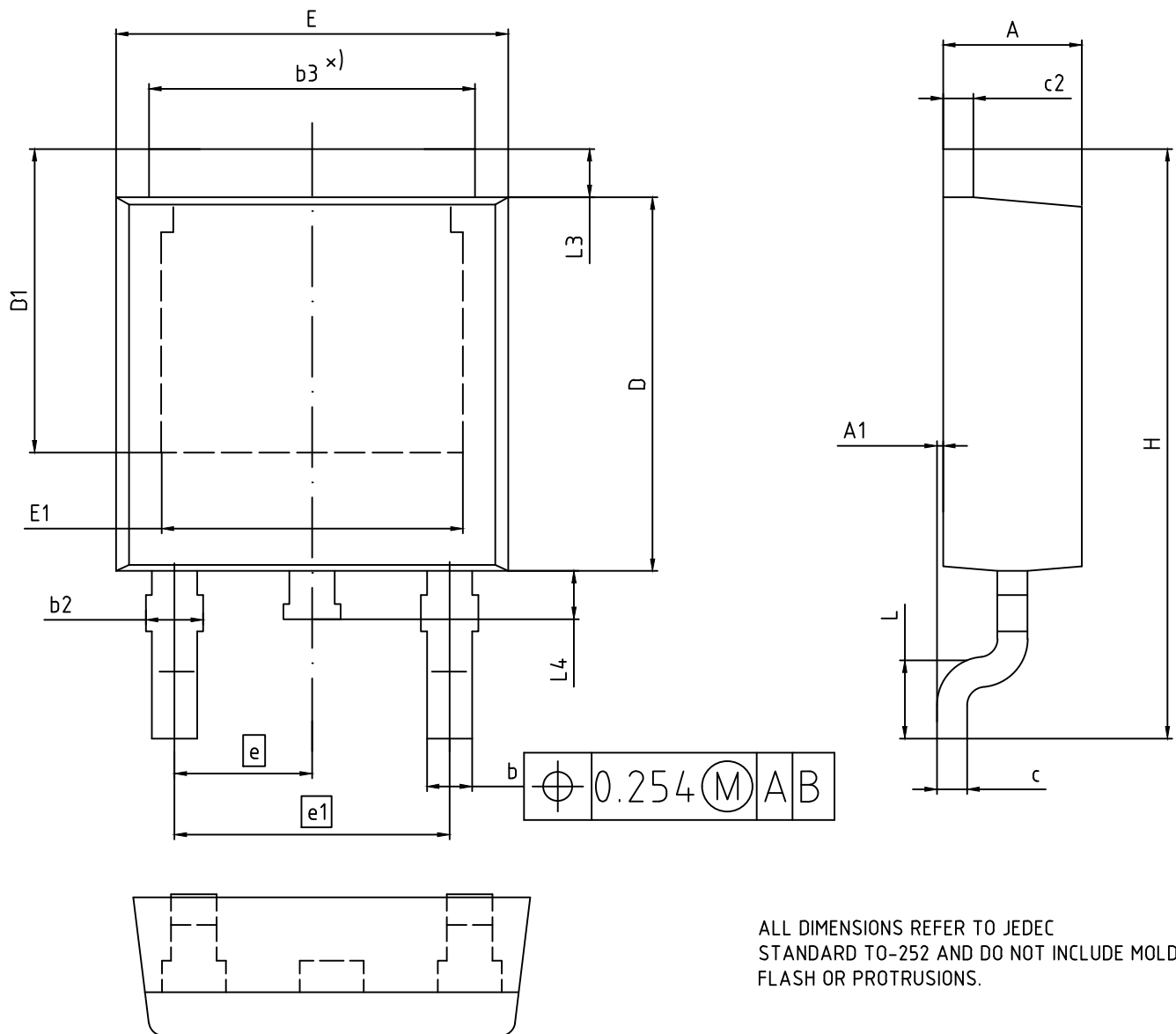
14 Typ. Coss stored energy

$E_{oss}=f(V_{DS})$



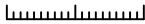
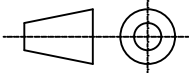
Definition of diode switching characteristics



PG-TO252-3-1/PG-TO252-3-11/PG-TO252-3-21: Outline


ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

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IPD50R399CP

Revision: 2020-05-26, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2020-05-26	Update package outline

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