

EVAL_AUDAMP24

IRS20957SPBF + IGT40R070D1 E8220 evaluation board

About this document

Scope and purpose

The EVAL_AUDAMP24 GaN e-mode High Electron Mobility Transistor (HEMT) evaluation board is a two-channel, 225 W/ch (4 Ω at ± 43 V) or 250 W/ch (8 Ω at ± 63 V) half-bridge class D audio power amplifier for Hi-Fi audio systems. This evaluation board demonstrates how to use the CoolGaN™ gallium nitride transistor, IRS20957S controller IC, implement protection circuits, and design an optimum PCB layout using the IGT40R070D1 E8220, CoolGaN™ gallium nitride transistor. The reference design provides all the required housekeeping power supplies for ease of use. The two-channel design is scalable for power and the number of channels.

Applications

- Hi-Fi amplifiers
- AV receivers
- Home theater systems
- Powered speakers
- Musical instrument amplifiers

Features

- Output power:
 - 225 W x 2 channels (1 percent THD+N, 4 Ω at ± 43 V)
 - 250 W x 2 channels (1 percent THD+N, 8 Ω at ± 63 V)
- Multiple protection features:
 - Over-Current Protection (OCP), high-side and low-side CoolGaN™ transistors
 - Over-Voltage Protection (OVP)
 - Under-Voltage Protection (UVP), high-side and low-side CoolGaN™ transistors
 - Over-Temperature Protection (OTP)
- PWM modulator:
 - Self-oscillating half-bridge topology with optional clock synchronization

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Specifications

1 Specifications

Table 1 General test conditions

| Condition | | Notes/conditions |
|----------------------------|--|-----------------------------|
| Supply voltages | $\pm 38\text{ V} \sim \pm 75\text{ V}$ | Bipolar power supply |
| Rated load impedance | 4 to 8 Ω | Resistive load |
| Self-oscillating frequency | 500 kHz | No input signal, adjustable |
| Voltage gain | 33 dB | |

Table 2 Electrical data

| Data | Typical | Notes/conditions |
|---|--|--|
| Infineon devices | IRS20957SPBF integrated class D IC IGT40R070D1 E8220 CoolGaN™ HEMTs | |
| Modulator | Self-oscillating, second-order sigma-delta modulation, analog input | |
| Output power CH1 to 2: (1 percent THD+N) | 225 W | 1 kHz, RL = 4 Ω |
| | 250 W | 1 kHz, RL = 8 Ω |
| Output power CH1 to 2: (10 percent THD+N) | 280 W | 1 kHz, RL = 4 Ω |
| | 310 W | 1 kHz, RL = 8 Ω |
| Rated load impedance | 4 to 8 Ω | Resistive load |
| Idling supply current | $\pm 67\text{ mA}$ | No input signal $\pm 43\text{ V}$ |
| | $\pm 85\text{ mA}$ | No input signal $\pm 63\text{ V}$ |
| Channel efficiency | 96 percent | Single-channel driven, 250 W, class D stage |

Table 3 Audio performance

| Audio performance | Volume control bypassed | Class D output | Notes/conditions |
|----------------------------|-------------------------|-------------------|---|
| Signal-to-noise Ratio(SNR) | 118 dB | 107 dB | Filter: A-weighting(12017), 20 kHz SPCL |
| Residual noise | 67 μV | 101 μV | Filter: A-weighting(12017), 20 kHz SPCL |

2 EVAL_AUDAMP24 overview

The EVAL_AUDAMP24 features a two-channels self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation, having a class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation enables the designer to apply sufficient error correction.



Figure 1 EVAL_AUDAMP24

The EVAL_AUDAMP24 self-oscillating topology consists of the following essential functional blocks:

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and CoolGaN™ HEMTs
- Output LPF

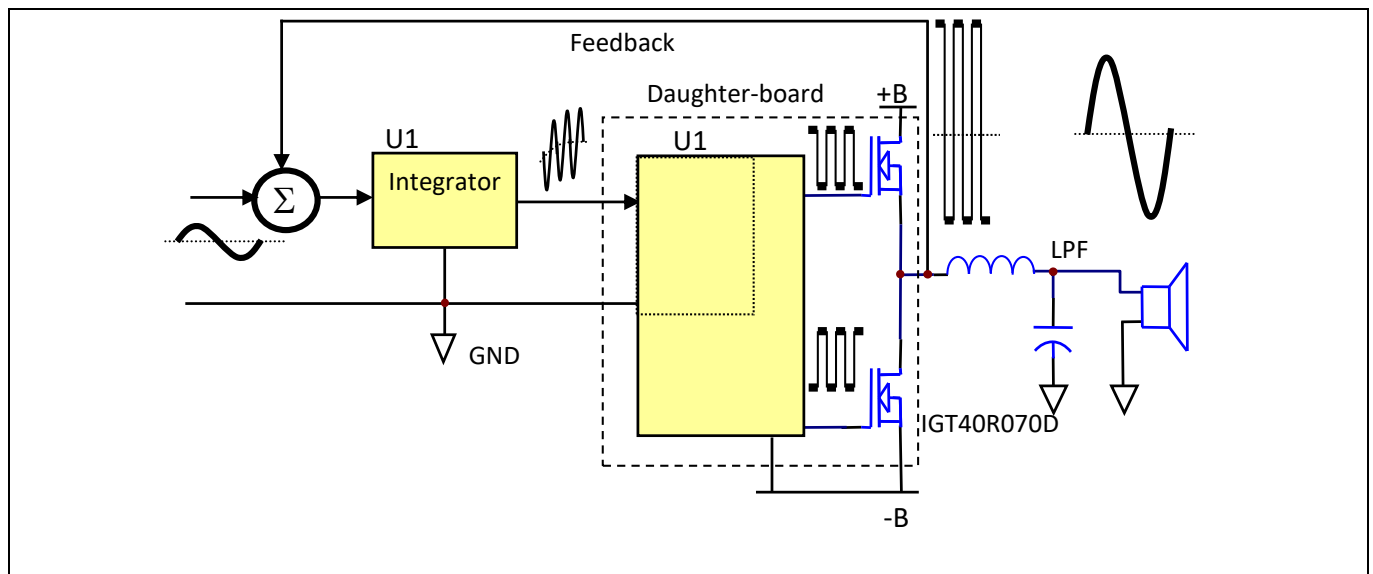
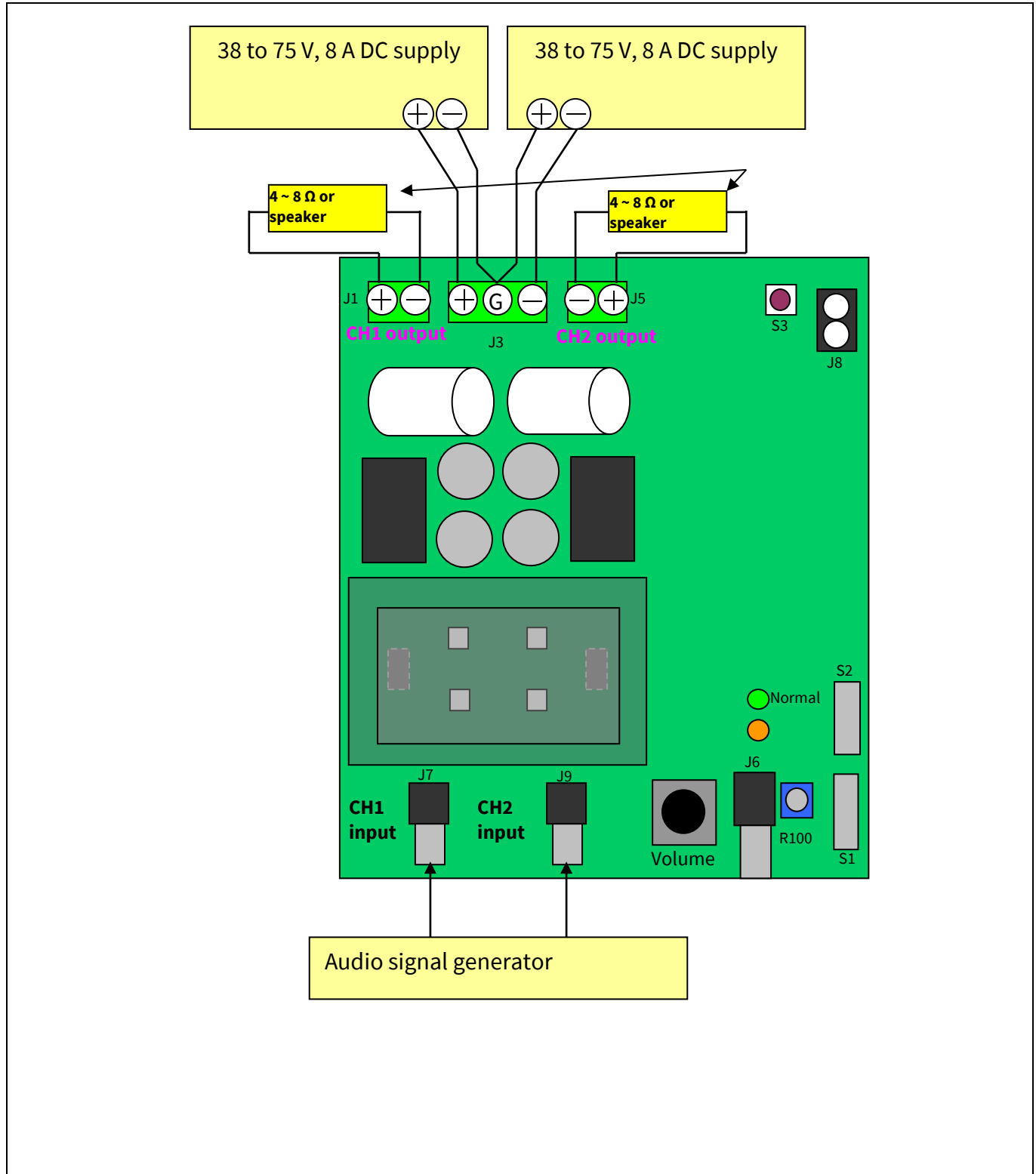


Figure 2 Simplified block diagram of class D amplifier

Setup guide

3 Setup guide

3.1 Typical connections

**Figure 3** Typical connections

Connector description

4 Connector description

Table 4 Connector description

| | | |
|---------|----|--------------------------------------|
| CH1 IN | J7 | Analog input for CH1 |
| CH2 IN | J9 | Analog input for CH2 |
| POWER | J3 | Positive and negative supply (+B/-B) |
| CH1 OUT | J1 | Output for CH1 |
| CH2 OUT | J5 | Output for CH2 |
| EXT CLK | J6 | External clock sync |
| DCP OUT | J8 | DC protection relay output |

5 Audio analyzer setup

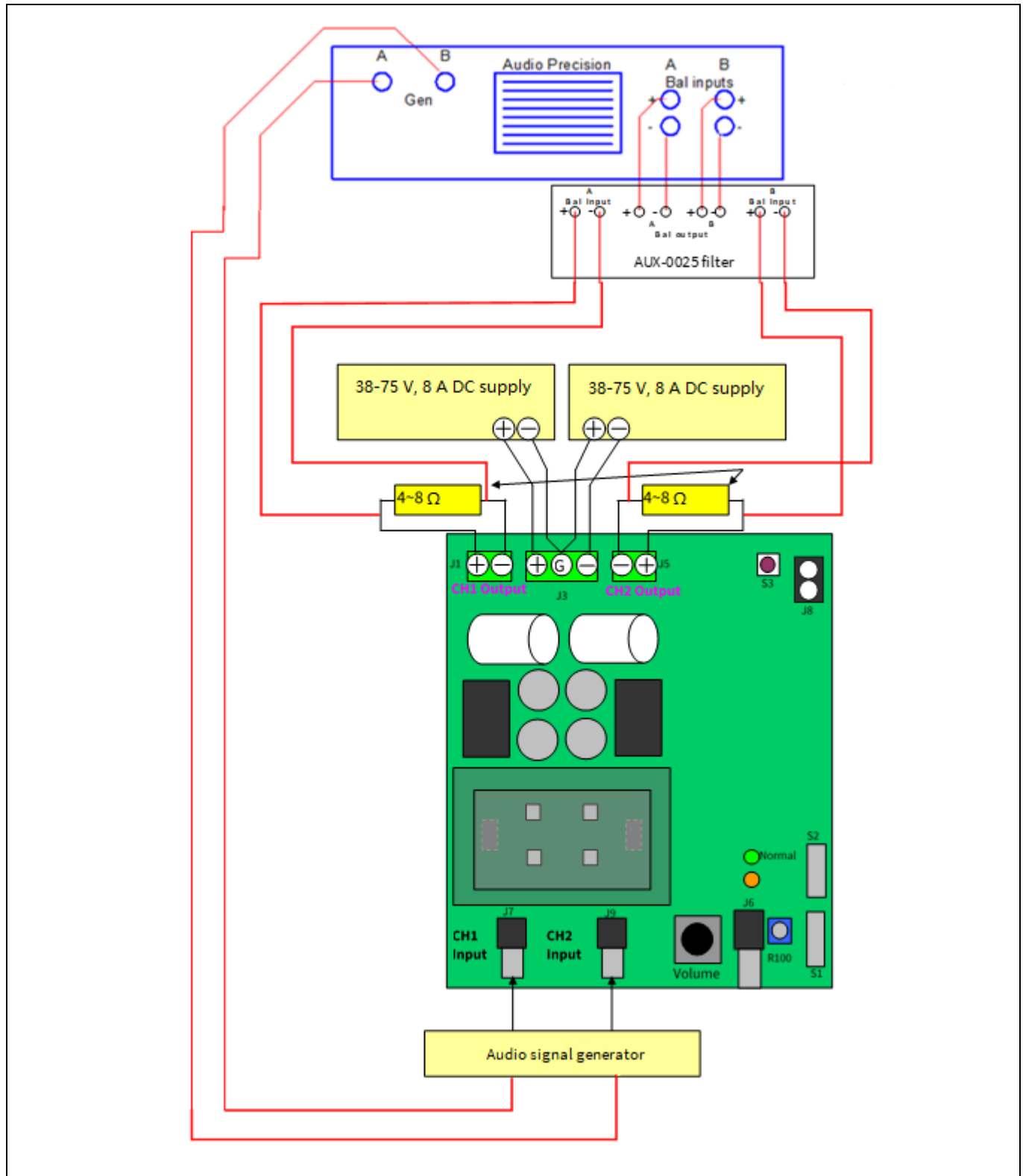


Figure 4 Audio analyzer connection

6 Operating the evaluation board

6.1 Test setup

1. Connect 4 or 8 Ω 250 W dummy loads to output connectors (J1 and J5 as shown in [Figure 3](#)) and parallel it with input of the Audio Precision (AP) analyzer.
2. Connect the Audio Signal Generator (ASG) to J7 and J9 for CH1 and CH2 respectively (AP).
3. Set up the dual power supply with voltages of ± 43 V or ± 63 V; set current limit to 8 A.
4. Turn-off the dual power supply before connecting to “on” of the Unit Under Test (UUT).
5. Set switch S1 to the middle position (self-oscillating).
6. Set volume level knob R130 fully counter-clockwise (minimum volume).
7. Connect the dual power supply to J3, as shown on [Figure 3](#) or [Figure 4](#).

6.2 Power-up sequence

8. Turn-on the dual power supply. The $\pm B$ supplies must be applied and removed at the same time.
9. Red LED (protection) should turn-on almost immediately and turn-off after about 3 s.
10. Green LED (normal) then turns on after the red LED is extinguished and should stay on.
11. Quiescent current for the positive supply should be 67 mA \pm 10 mA at ± 43 V, 84 mA \pm 10 mA at ± 63 V.
12. Quiescent current for the negative supply should be 62 mA \pm 10 mA at ± 43 V, 74 mA \pm 10 mA at ± 63 V.
13. Push S3 switch (trip and reset push-button) to restart the sequence of LED indicators, which should be the same as noted above in steps 9 to 10.

6.3 Audio functionality tests

1. With AP no filter (more than 500 kHz), monitor the channel's switching frequency on the AP's analog analyzer.
2. Set S1 to “self” (self-oscillating) position.
3. Adjust R49 and R74 on the board to change the self-oscillating frequency to 500 kHz \pm 15 kHz.
4. Set the AP's analog analyzer to 20 kHz AES17 filter.
5. Connect the audio signal from the AP to J7 and J9.
6. Apply 1 V_{RMS} at 1 kHz sinusoidal signal from the ASG.
7. Turn control volume up (R130 clockwise) to obtain an output reading of 225 W (4 Ω load) or 250 W (8 Ω load).
8. Sweep the audio signal voltage from 15 mV_{RMS} to 1.5 V_{RMS}.
9. Run the AP test as shown in Figures 5 to 13, below.

6.4 External clock function

1. With AP no filter (more than 500 kHz), monitor the channel's switching frequency on the AP's analog analyzer.
2. Set S1 to “self” (self-oscillating) position.
3. Adjust R49 and R74 on the board to change self-oscillating frequency to 20 to 30 percent higher than the desired external clock.
4. Set S1 to “Ext” (external clock) position in order to enable the onboard clock oscillator.
5. Connect the external clock signal generator output to J6.
6. Set the AP's analog analyzer to 20 kHz AES17 filter
7. Connect the audio signal from the AP to J7 and J9.
8. Sweep the audio signal voltage from 15 mV_{RMS} to 1.5 V_{RMS}.

6.5 Power-down sequence

14. Turn-off \pm power supply at the same time.
15. All LEDs turn-off when housekeeping power supplies are off.

7 Audio performance

7.1 Power vs. THD+N

Test conditions:

$V_{bus} = \pm 43 \text{ V}$

Input signal = 1 kHz

Load impedance = 4Ω

$F_{PWM} = 500 \text{ kHz}$

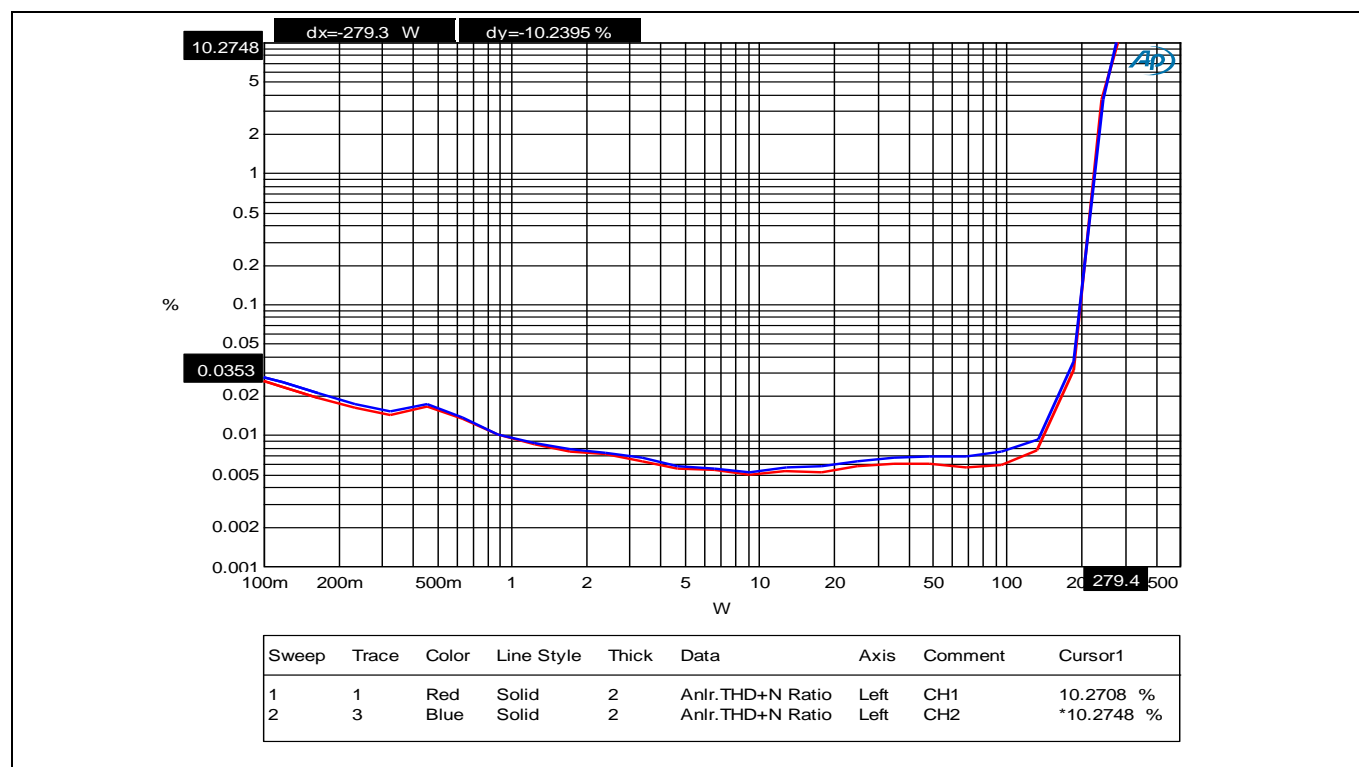


Figure 5 Power vs. THD+N 4Ω load

EVAL_AUDAMP24

IRS20957SPBF + IGT40R070D1 E8220 evaluation board

Audio performance

Test conditions:

$$V_{bus} = \pm 63 \text{ V}$$

Input signal = 1 kHz

Load impedance = 8Ω

$F_{PWM} = 500 \text{ kHz}$

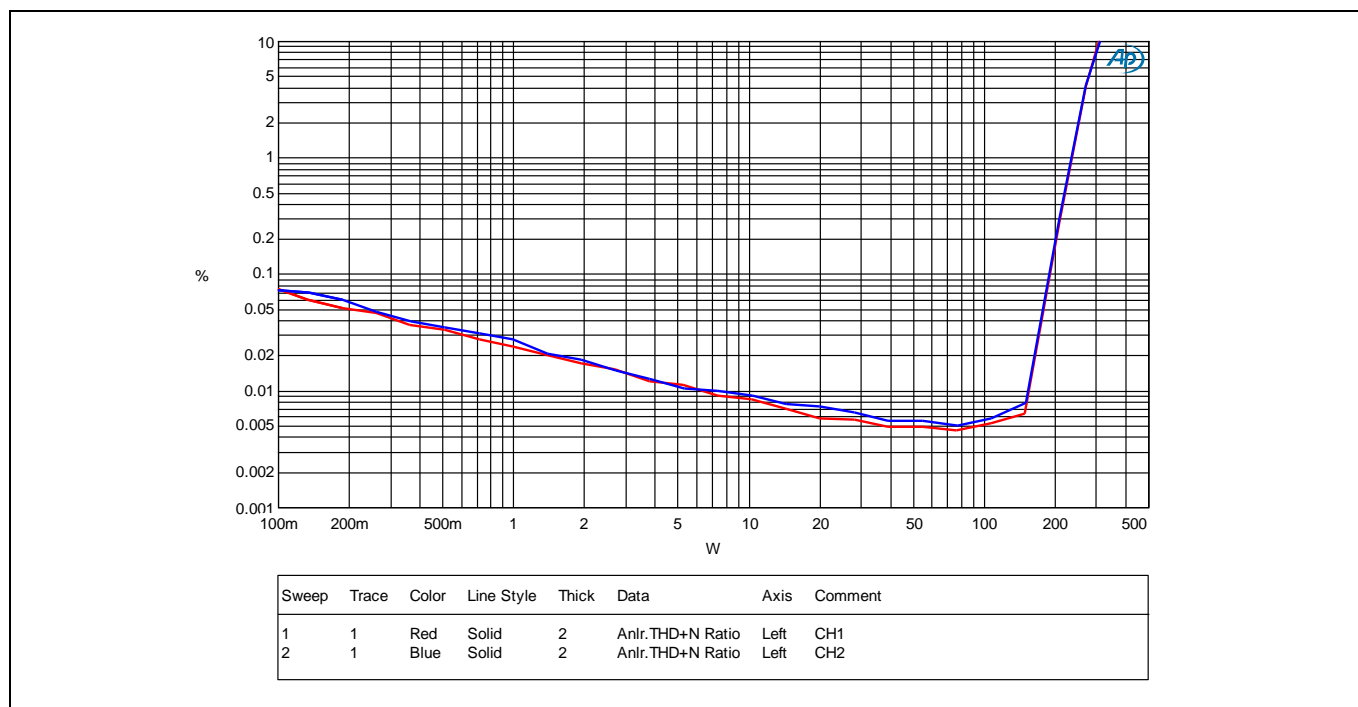


Figure 6 Power vs. THD+N 8Ω load

7.2 Frequency response

Test conditions:

$$V_{bus} = \pm 43 \text{ V}$$

Output power = 1 W

Load impedance = 4Ω

$F_{PWM} = 500 \text{ kHz}$

Audio performance

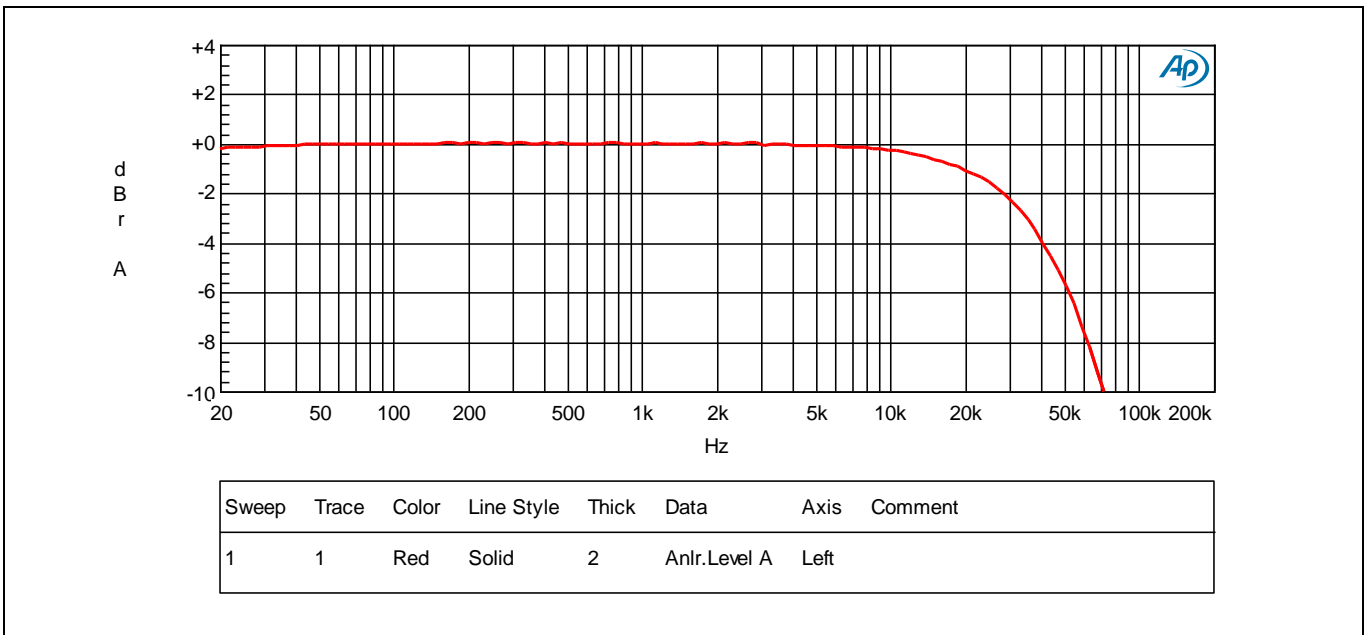


Figure 7 Frequency response 4 Ω load

Test conditions:

$V_{bus} = \pm 63 \text{ V}$

Output power = 1 W

Load impedance = 8 Ω

$F_{PWM} = 500 \text{ kHz}$

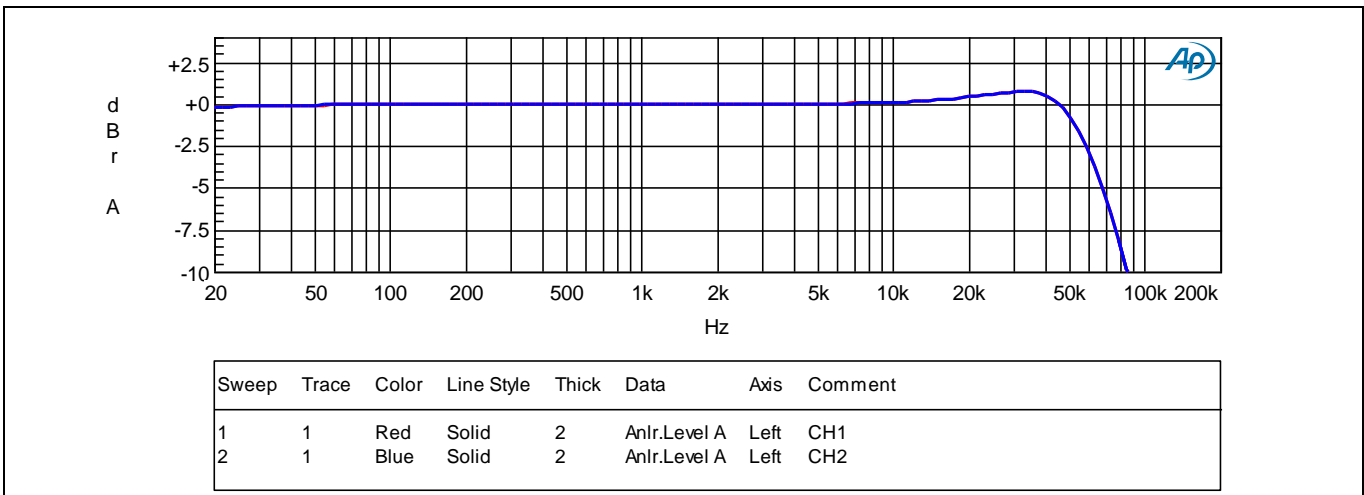


Figure 8 Frequency response 8 Ω load

EVAL_AUDAMP24

IRS20957SPBF + IGT40R070D1 E8220 evaluation board

Audio performance

7.3 Noise floor

Test conditions:

$V_{bus} = \pm 43 \text{ V}$

No input signal

Load impedance = 4Ω

$F_{PWM} = 500 \text{ kHz}$

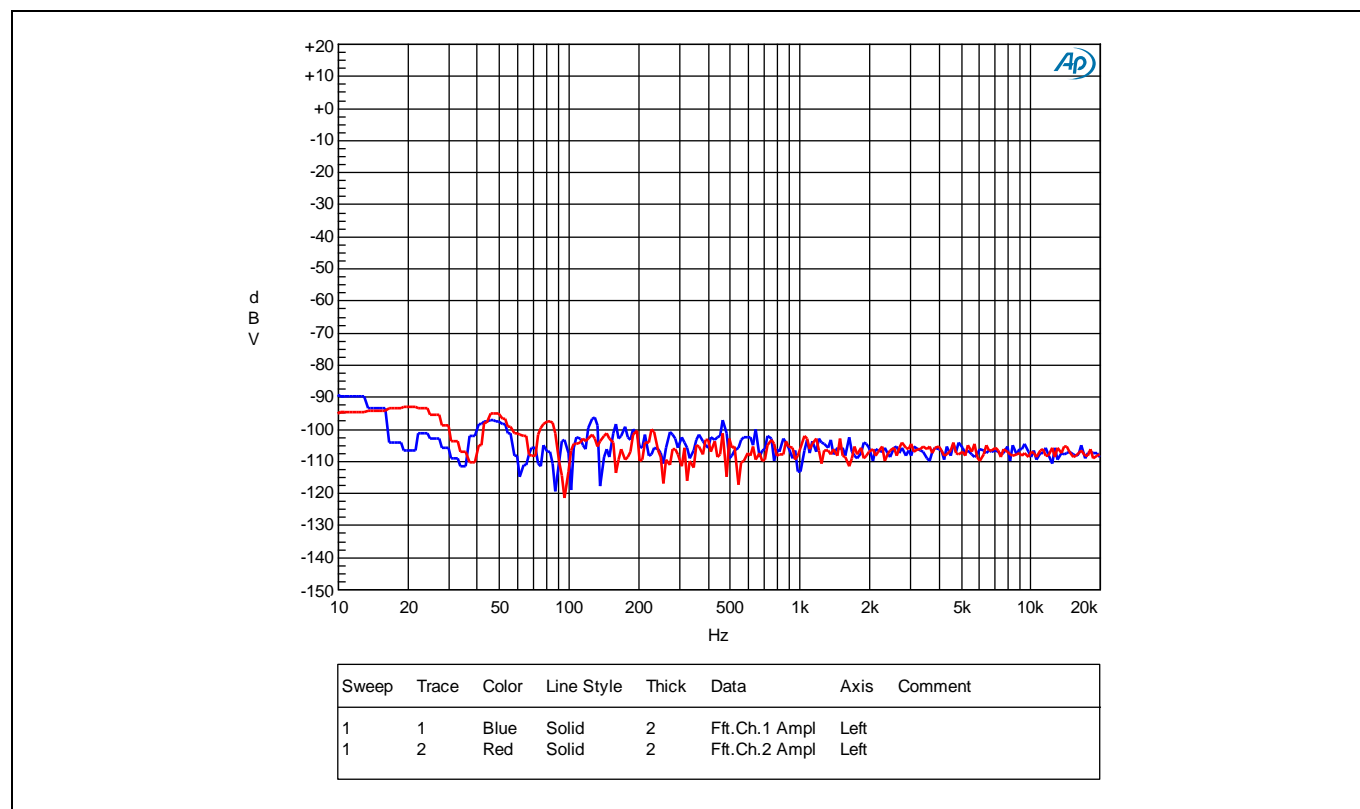


Figure 9 Noise floor 4Ω load

Test conditions:

$V_{bus} = \pm 63 \text{ V}$

No input signal

Load impedance = 8Ω

$F_{PWM} = 500 \text{ kHz}$

Audio performance

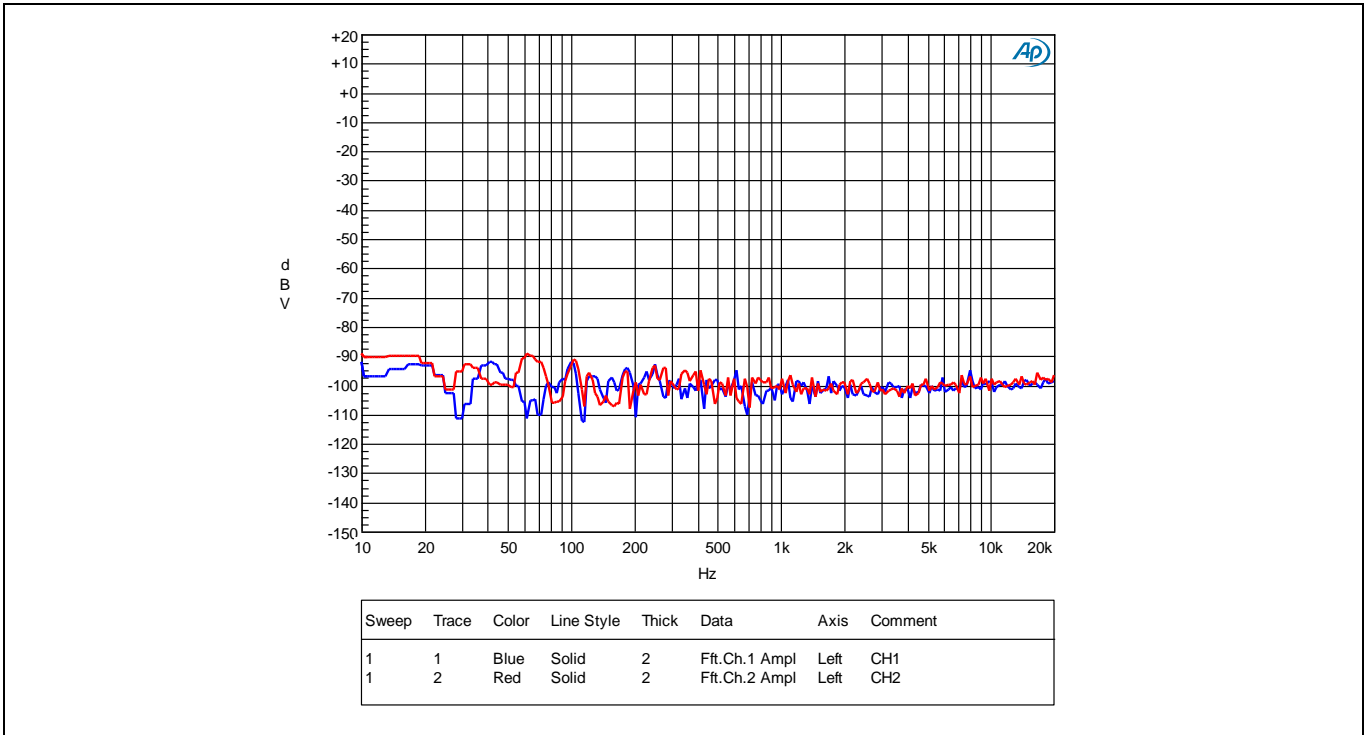


Figure 10 Noise floor 8 Ω load

7.4 Noise floor with 1 V_{RMS} output

Test conditions:

$$V_{bus} = \pm 43 \text{ V}$$

Output = 1 V_{RMS} at 1 kHz

Load impedance = 4 Ω

F_{PWM} = 500 kHz

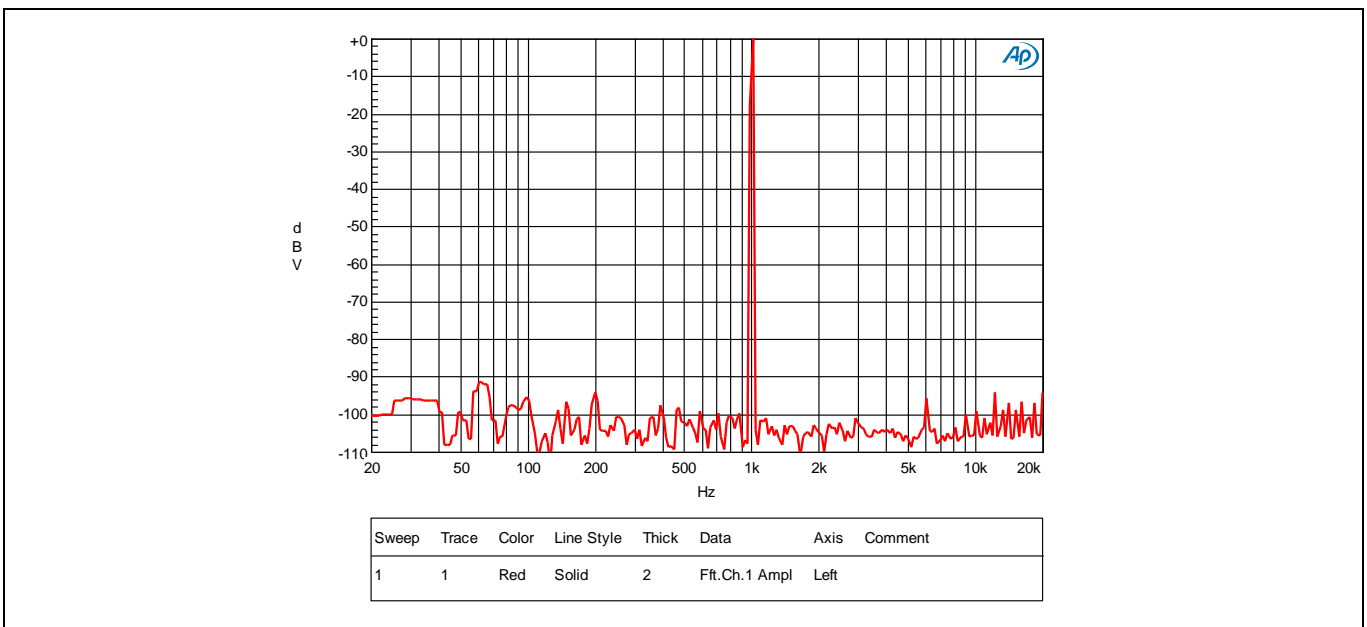


Figure 11 Noise floor with 1 V_{RMS} output 4 Ω load

EVAL_AUDAMP24

IRS20957SPBF + IGT40R070D1 E8220 evaluation board

Audio performance

Test conditions:

$V_{bus} = \pm 63\text{ V}$

Output = 1 V_{RMS} at 1 kHz

Load impedance = $8\ \Omega$

$F_{PWM} = 500\text{ kHz}$

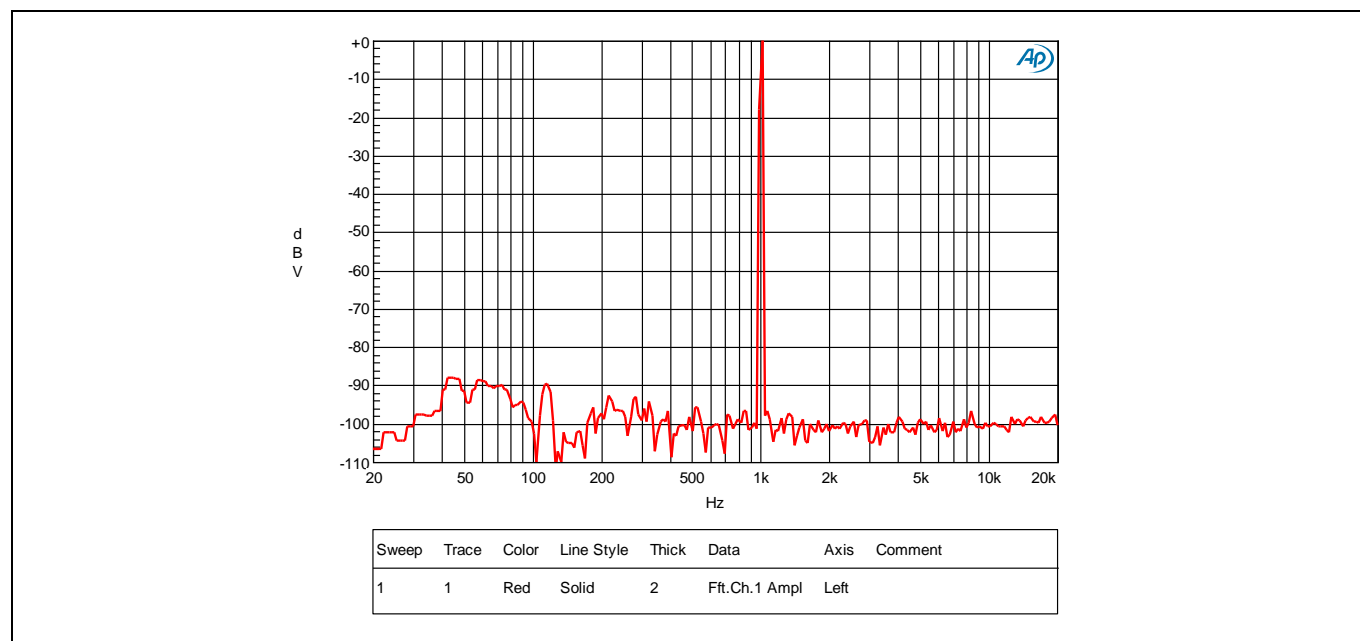


Figure 12 Noise floor with 1 V_{RMS} output $8\ \Omega$ load

8 Functional descriptions

8.1 Class D operation

Referring to CH1 as an example, the op-amp U6 forms a front-end second-order integrator with C38, C42 and R50 + R49P. This integrator receives a rectangular feedback waveform from the class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM signal, the input signal shifts the average value of this quadratic waveform (through gain relationship between R40, R154 and R38 + R39) so that the duty varies according to the instantaneous value of the analog input signal. The IRS20957SPBF input comparator processes the signal to create the required PWM signal. This PWM signal is internally level-shifted down to the negative supply rail where this signal is split into two signals, with opposite polarity and added dead-time, for high-side and low-side CoolGaN™ HEMT gate signals, respectively. The IRS20957SPBF drives two IGT40R070D1 E8220 CoolGaN™ HEMTs in the power stage to provide the amplified PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC Low-Pass Filter (LPF) formed by L4 and C34, which filters out the class D switching carrier signal.

8.2 CoolGaN™ gallium nitride HEMT

A gallium nitride (GaN) transistor is one of the HEMTs that enables superior performance, far exceeding the silicon MOSFET with its very low on-resistance, very high speed and clean switching capabilities.

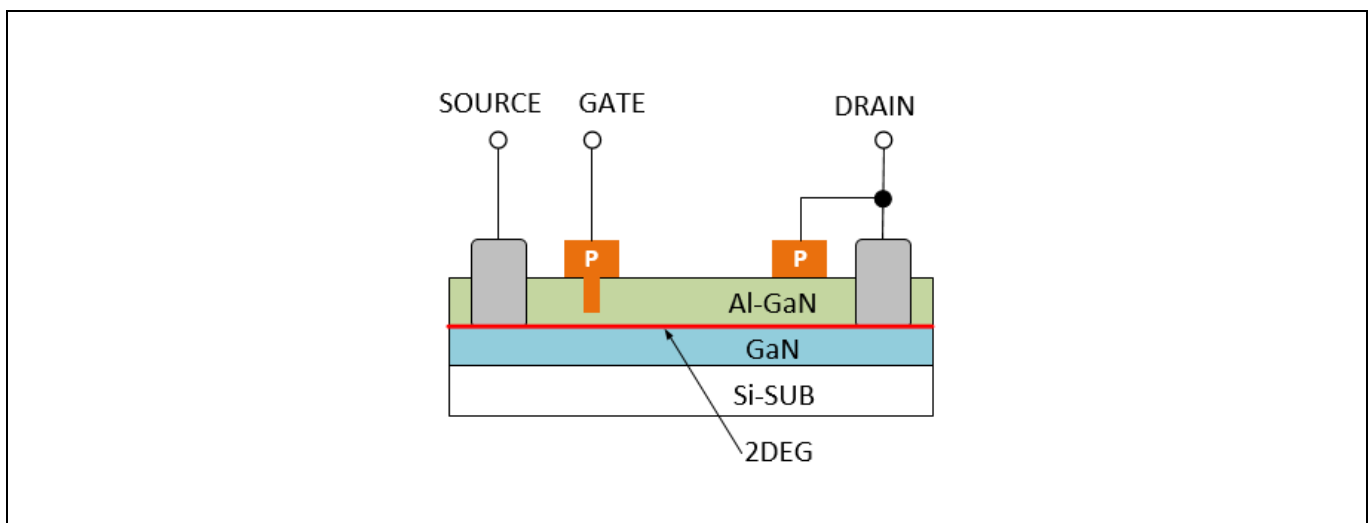


Figure 13 Internal structure of Infineon's CoolGaN™

The basic structure of a GaN FET is similar to a silicon MOSFET, with gate, source and drain terminals. The heart of the GaN switch is a lateral two-dimensional electron gas (2DEG) layer formed in the GaN layer. The 2DEG is a pool of free electrons formed by the hetero junction between Al-GaN and GaN, making a short-circuit between the source and drain in very low resistance. Adding a p-GaN gate on top of the Al-GaN layer makes the adjacent 2DEG depleted so the drain and source are not conducting with no gate bias applied ($V_{GS} = 0$ V). This enhancement mode gate works similarly to conventional silicon MOSFETs. When a positive bias voltage is applied to the gate, the depletion disappears and the 2DEG forms a low-resistance conducting channel.

The reverse conduction mode from source to drain is very necessary in a class D amplifier during blanking time so that the switching output voltage is kept within the power supply rails. The GaN switch is a bi-directional device in nature, so it realizes reverse current as one of the on-states. When the drain voltage becomes lower than the source, the drain starts acting as a source and turns on the device, allowing reverse current to flow. A silicon MOSFET is a uni-directional switch accompanied by an intrinsic PN junction body diode that provides a reverse current from source to drain when the device is off.

Functional descriptions

The absence of a body diode in the GaN FET is a notable feature because it eliminates the major source of switching noise previously caused by the PN junction body diode, and therefore the GaN FET realizes much cleaner switching even at high-voltage, high-current, high-speed switching operations.

A class D amplifier demands lower $R_{DS(ON)}$ and faster and cleaner switching transitions for higher power ratings that are transitional performance trade-offs in Si MOSFETs. Therefore, a class D amplifier can greatly benefit from a GaN-based FET.

Figure 14 is the class D switching stage using a GaN FET, Infineon IGT40R070D1 E8220. Using a GaN FET takes a different gate-drive scheme. A silicon MOSFET receives 0 V or 10 V gate voltage with respect to the source to turn the switch off and on. The gate injection type GaN transistor, such as Infineon's CoolGaN™, is controlled in a similar fashion but with different gate-drive voltage and some sustaining DC gate current. In this design example, an interfacing circuit (R25, R26, R29, C12 and D6 in the low-side gate drive and identical for the high-side) is inserted in the gate of the GaN FET. The output from the interface circuit swings between -1 V and +3 V instead of 0 V and 10 V from the IRS20957SPBF class D controller IC.

One unique requirement of the CoolGaN™ gate drive besides lower threshold voltage is that it requires a small amount of DC gate current to sustain the on-state. The R25 in the schematic provides the DC bias current path. R26 and C12 induce charge and discharge current to turn the device on and off. The diode between gate and source, D6, limits negative gate voltage at -1 V so the body diode equivalent action maintains drop voltage from source to drain. With this gate interface circuit, a gate-driver IC originally designed for a MOSFET can work with a GaN transistor, including V_{DS} based short-circuit protection.

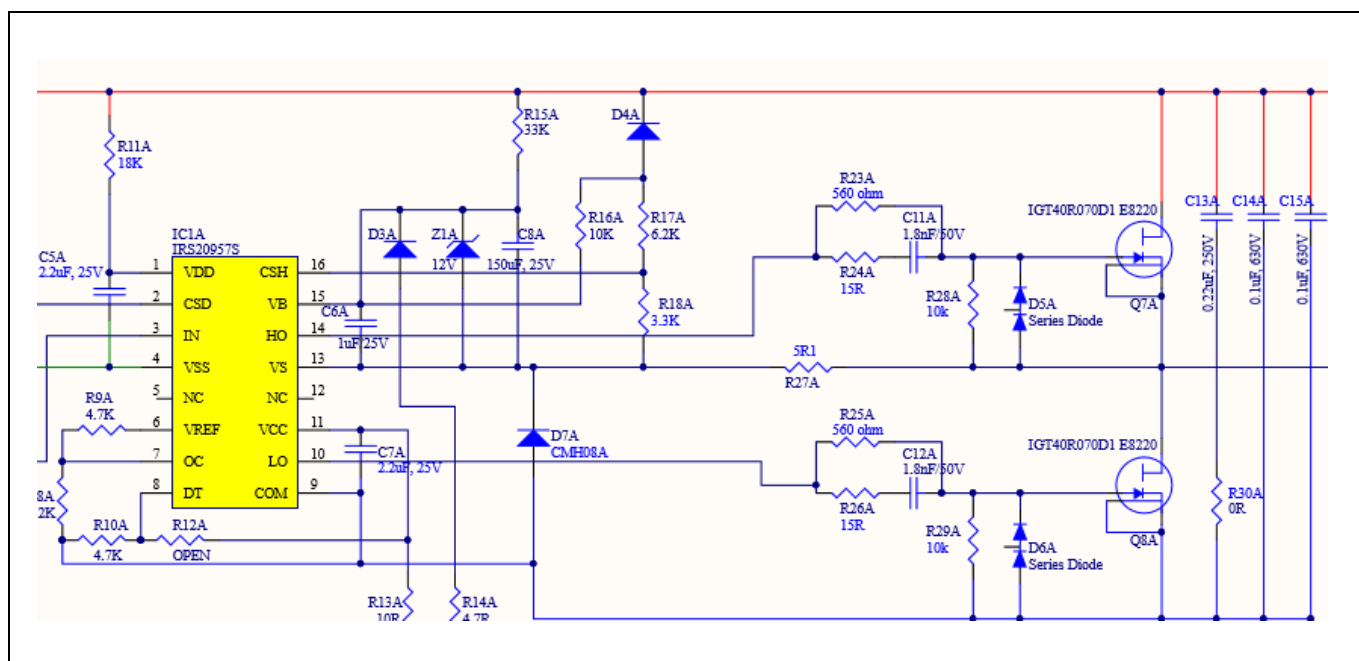


Figure 14 CoolGaN™ gate-drive interface circuit

Functional descriptions

8.3 Power supply

The EVAL_AUDAMP24 has all the necessary housekeeping power supplies onboard, and only requires a pair of symmetrical power supplies ranging from $\pm 38\text{ V}$ to $\pm 82\text{ V}$ (+B, GND, -B) for operation. The internally generated housekeeping power supplies include a $\pm 5\text{ V}$ supply for analog signal processing (preamp, etc.), while a $+12\text{ V}$ supply (V_{CC}), referenced to -B, is included to supply the class D gate-driver stage.

For the externally applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C45 ~ C48 on the motherboard, along with high-frequency bypass-capacitors C19 ~ C26 on the daughter board, address the high-frequency ripple current that results from switching action. In designs involving unregulated power supplies, the designer should place a set of bus capacitors, with enough capacitance to handle the audio-ripple current, externally. Overall regulation and output voltage ripple for the power supply design are not critical when using the EVAL_AUDAMP24 class D amplifier as the Power Supply Rejection Ratio (PSRR) of the EVAL_AUDAMP24 is excellent ([Figure 15](#)).

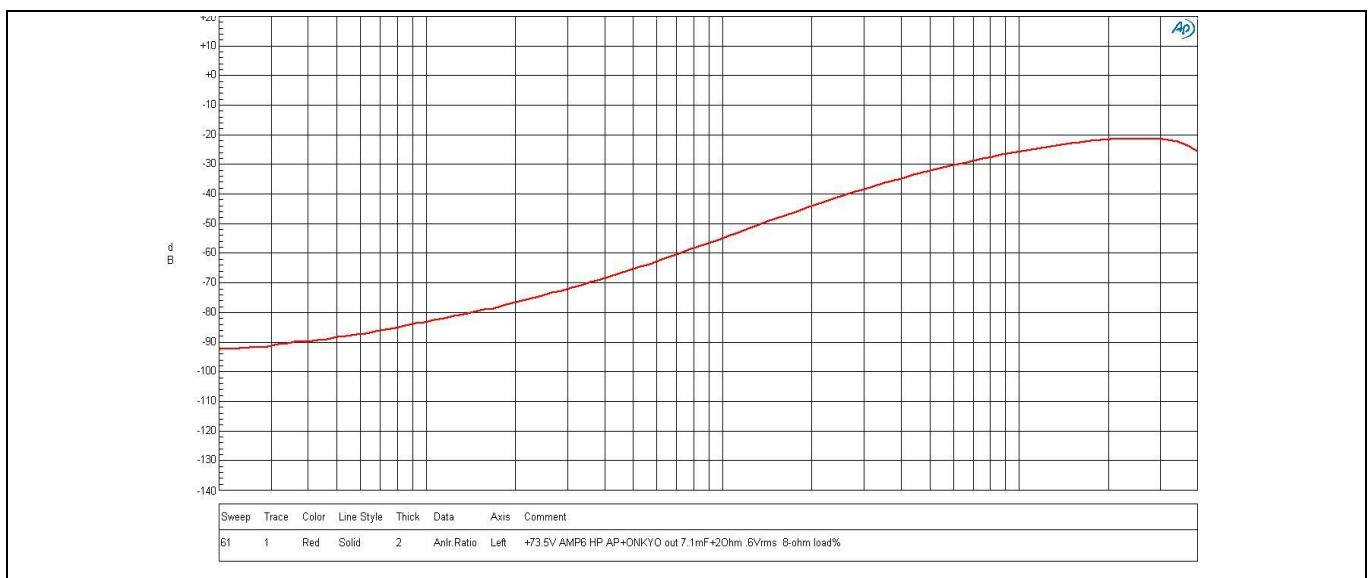


Figure 15 AMP24 PSRR

8.4 Bus pumping

Since the EVAL_AUDAMP24 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.

The following conditions worsen bus pumping:

- Lower frequencies (bus-pumping duration is longer per half cycle)
- Higher power output current (more energy transfers between supplies)
- Smaller bus capacitors (the same energy will cause a larger voltage increase)

The EVAL_AUDAMP24 has protection features that will shut down the switching operation if the bus voltage becomes too high (more than 82 V) or too low (less than 36 V). One of the easiest countermeasures is to drive both of the channels out of phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection is only done on the -B supply as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase).

Functional descriptions

8.5 Housekeeping power supply

The internally generated housekeeping power supplies include ± 5 V for analog signal processing, and +12 V supply (V_{CC}) referred to the negative supply rail -B for the CoolGaN™ gate drive. The gate-driver section of the IRS20957SPBF uses V_{CC} to drive gates of the CoolGaN™ s. V_{CC} is referenced to -B (negative power supply). D6, R4 and C15 form a bootstrap floating supply for the HO gate driver.

8.6 Input

A proper input signal is an analog signal ranging from 20 Hz to 20 kHz with up to 3 V_{RMS} amplitude with a source impedance of no more than 600 Ω . Input signal with frequencies from 30 kHz to 60 kHz may cause LC resonance in the output LPF, causing a large reactive current flowing through the switching stage, and the LC resonance can activate OCP.

The EVAL_AUDAMP24 has an RC network called a Zobel network (R45 and C36) to damp the resonance and prevent peaking frequency response with light loading impedance. (Figure 16), but is not thermally rated to handle continuous supersonic frequencies. These supersonic input frequencies should therefore be avoided. Separate mono RCA connectors provide input to each of the two channels. Although both channels share a common ground, it is necessary to connect each channel separately to limit noise and cross-talk between channels.

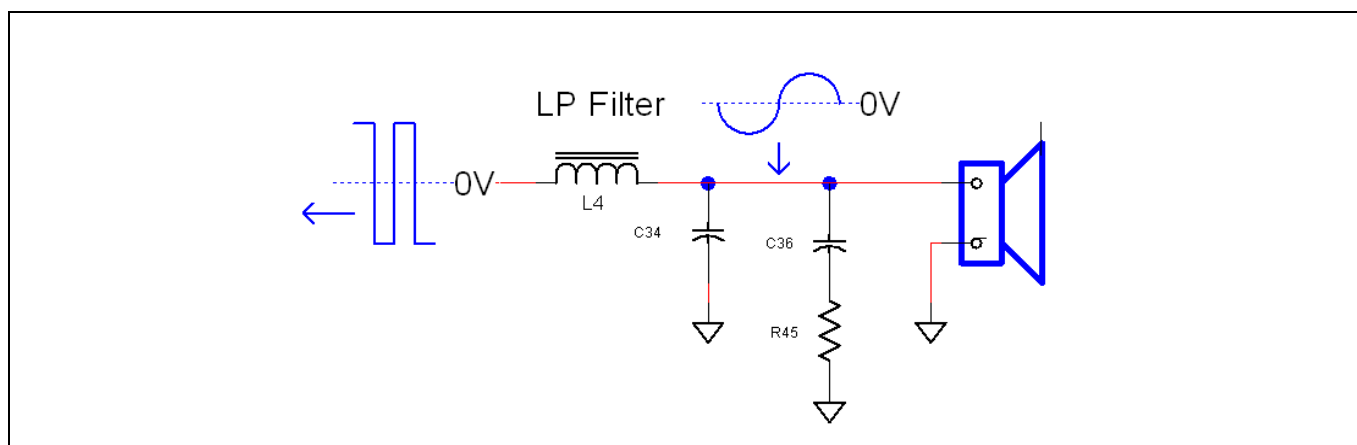


Figure 16 Output LPF and Zobel network

8.7 Output

Both outputs for the EVAL_AUDAMP24 are single-ended and therefore have terminals labeled (+) and (-) with the (-) terminal connected to power ground. Each channel is optimized for 4 Ω speaker load for a maximum output power of 225 W or 8 Ω speaker load for a maximum output power of 250 W.

8.8 Load impedance

Each channel is optimized for a 4 to 8 Ω speaker load in half-bridge.

8.9 Gain setting/volume control

The EVAL_AUDAMP24 has an internal volume control (potentiometer R130, labeled "VOLUME") for gain adjustment. Gain settings for both channels are tracked and controlled by the volume control IC (U_2) setting the gain from the microcontroller IC (U_3). The total gain is a product of the power-stage gain, which is constant (+33 dB), and the input-stage gain that is directly controlled by the volume adjustment. The volume range is about 100 dB with minimum volume setting to mute the system with an overall gain of less than -60 dB.

Functional descriptions

For best performance in testing, the internal volume control should be set to 1 V_{RMS} input, which will result in rated output power (250 W into 8 Ω).

8.10 Efficiency

Figures 17 and 18 show efficiency characteristics of the EVAL_AUDAMP24. The high efficiency is achieved by the following factors:

- Low conduction loss due to the CoolGaN™ offering low $R_{DS(ON)}$
- Low switching loss due to the CoolGaN™ offering low input capacitance for fast rise and fall times
- Secure dead-time provided by the IRS20957SPBF, avoiding cross-conduction

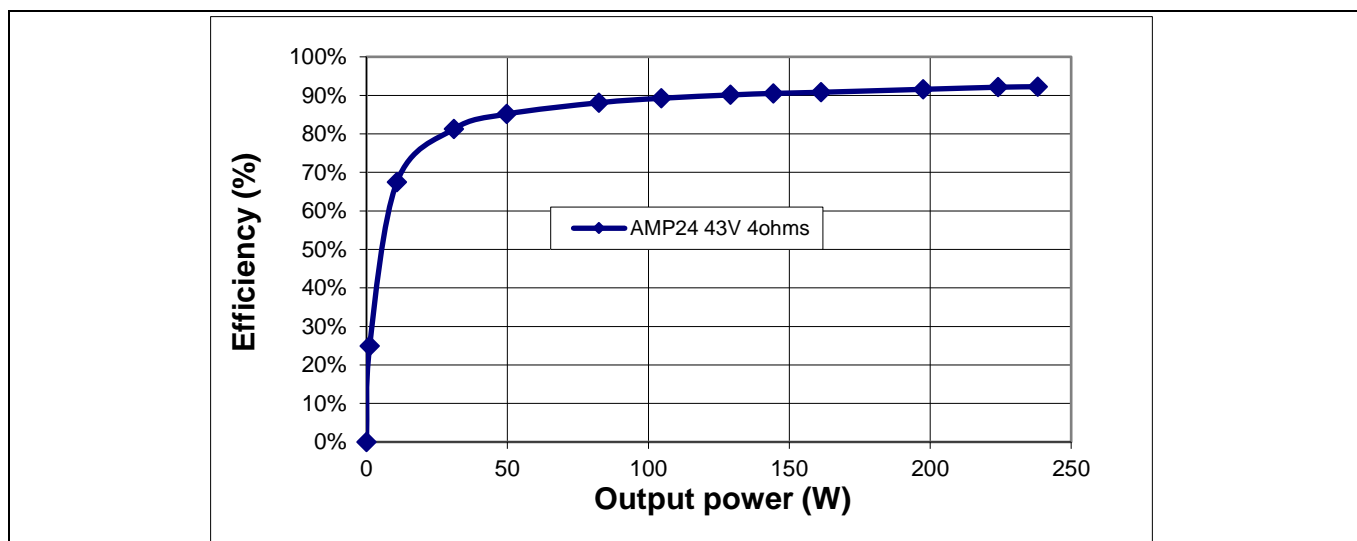


Figure 17 EVAL_AUDAMP24 4 Ω load stereo, ±B supply = ±43 V

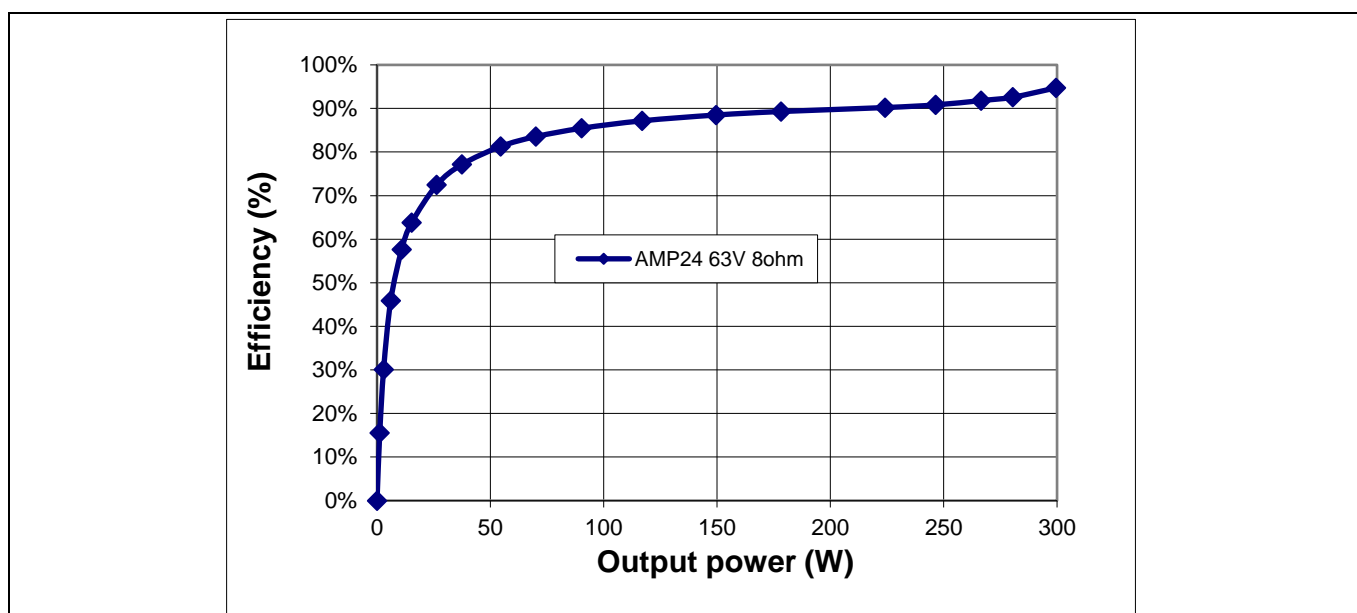


Figure 18 EVAL_AUDAMP24 8 Ω load stereo, ±B supply = ±63 V

8.11 Output filter design and preamplifier

The audio performance of the EVAL_AUDAMP24 depends on a number of different factors. The section entitled “Typical Performance” presents performance measurements based on the overall system, including the preamp and output filter. While the preamp and output filter are not part of the class D power stage, they have a significant effect on the overall performance.

8.11.1 Output filter

The amplified PWM output is reconstructed back to an analog signal by the output LC LPF. Demodulation LC LPF, formed by L4 and C34, filters out the class D switching carrier signal, leaving the audio output at the speaker load. A single-stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.

Since the output filter is not included in the control loop of the EVAL_AUDAMP24, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to understand what characteristics are preferable when designing the output filter:

- The DC resistance of the inductor should be minimal and within 20 mΩ or less
- The linearity of the output inductor and capacitor should be high with respect to load current and voltage

8.11.2 Preamplifier

The preamp allows partial gain of the input signal, and in the EVAL_AUDAMP24 it controls the volume. The preamp itself will add distortion and noise to the input signal, resulting in a gain through the class D output stage and appearing at the output. Even a few microvolts of noise can add significantly to the output noise of the overall amplifier. In fact, the output noise from the preamp contributes more than half of the overall noise to the system.

It is possible to evaluate the performance without the preamp and volume control, by moving resistors R154 and R155 to R157 and R156, respectively. This effectively bypasses the preamp and connects the RCA inputs directly to the class D power stage input. Improving the selection of the preamp and/or output filter will improve the overall system performance to approach that of the standalone class D power stage.

8.12 Self-oscillating PWM modulator

The EVAL_AUDAMP24 class D audio power amplifier features a self-oscillating type PWM modulator for the lowest component count and robust design. This topology represents an analog version of a second-order sigma-delta modulation, having a class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, the IRS20957SPBF gate-driver propagation delay, the IGT40R070D1 E8220 switching speed, the time-constant of the front-end integrator (e.g., R50 + R49, C38 and C42 for CH1) and variations in the supply voltages are critical factors of the self-oscillating frequency. Under normal conditions, the switching frequency is around 500 kHz with no audio input signal.

8.13 Adjustments of self-oscillating frequency

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching time becomes significant, while at lower frequencies, the

Functional descriptions

bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range. Normally when adjusting the self-oscillating frequency of the different channels, it is best to either match the frequencies accurately, or have them separated by at least 25 kHz.

Table 5 Potentiometers for adjusting self-oscillating frequency

| | |
|-----|-----------------------------|
| R49 | Switching frequency for CH1 |
| R74 | Switching frequency for CH2 |

Note: Adjustments must be made in an idling condition with no signal input.

8.14 Switches and indicators

There are two different indicators on the reference design:

- A red LED, signifying a fault/shutdown condition when lit
- A green LED on the motherboard, signifying conditions are normal and no fault condition is present

There are three switches on the reference design:

- Switch S1 is an oscillator selector. This three-position switch is selectable for internal self-oscillator (middle position – “SELF”), or either internal (“INT”) or external (“EXT”) clock synchronization.
- Switch S2 is an internal clock-sync phase difference selector. This feature allows the designer to modify the clock-sync phase separation in order to avoid synchronized switching noise interference. With S2 set to “off”, the sync-clock phase difference value is 180 degrees. With S2 set to “INT”, the clock-sync phase is set by potentiometer R100. With S2 set to “STG”, one channel’s clock is quadrature-lagging.
- Switch S3 is a trip and reset push-button. Pushing this button has the same effect as a fault condition. The circuit will restart about 3 s after the shutdown button is released.

8.15 Start-up and shutdown

One of the most important aspects of any audio amplifier is the start-up and shutdown procedure. Typically, transients occurring during these intervals can result in audible pop- or click-noise on the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the start-up transients have passed and disconnects the speaker prior to shutting down the amplifier. It is interesting to note that the audible noise of the relay opening and closing is not considered “click noise”, although in some cases, it can be louder than the click noise of non-relay-based solutions.

The EVAL_AUDAMP24 does not use any series relay to disconnect the speaker from the audible transient noise, but rather a shunt-based click-noise reduction circuit that yields audible noise levels that are far less than those generated by the relays they replace. This results in a more reliable, superior performance system.

For the start-up and shutdown procedures, the activation (and deactivation) of the click-noise reduction circuit, the class D power stage and the audio input (mute) controls have to be sequenced correctly to achieve the required click-noise reduction. The overall start-up sequencing, shutdown sequencing and shunt circuit operation are described below.

Functional descriptions

8.16 Click and pop noise reduction

To reduce the turn-on and turn-off click noise, a low-impedance shunting circuit is used to minimize the voltage across the speaker during transients. For this purpose, the shunting circuit must include the following characteristics:

- An impedance significantly lower than that of the speaker being shunted. In this case, the shunt impedance is $\sim 100\text{ m}\Omega$, compared to the normal $8\text{ }\Omega$ speaker impedance.
- When deactivated, the shunting circuit must be able to block voltage in both directions due to the bi-directional nature of the audio output.
- The shunt circuit requires some form of OCP. If one of the class D output CoolGaN™ HEMTs fails, or is conducting when the speaker mute (SP MUTE) is activated, the shunting circuit will effectively try to short one of the two supplies ($\pm B$).

The implemented click-noise reduction circuit is shown in [Figure 19](#). Before start-up or shutdown of the class D power stage, the click-noise reduction circuit is activated through the SP MUTE control signal. With the SP MUTE signal high, the speaker output is shorted through the back-to-back CoolGaN™ HEMTs (U5 for Channel 1) with an equivalent on-resistance of about $100\text{ m}\Omega$. The two transistors (U7 for Channel 1) are for the OCP circuit.

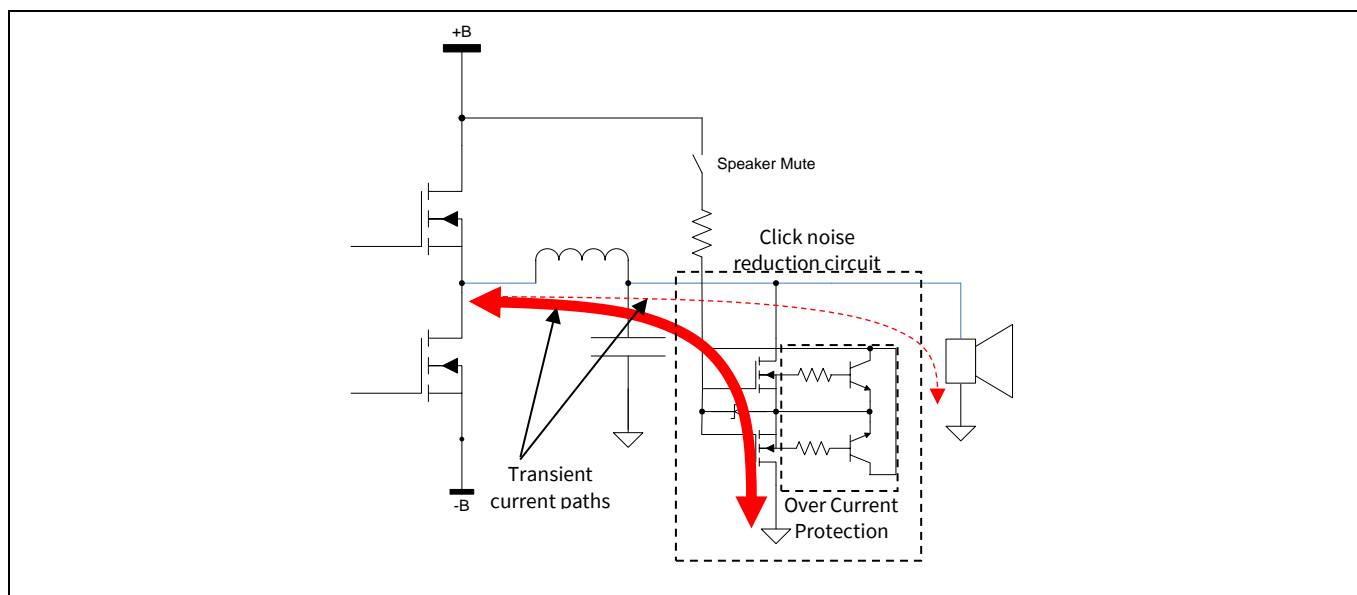


Figure 19 Class D output stage with click-noise reduction circuit

8.17 Start-up and shutdown sequencing

The EVAL_AUDAMP24 sequencing is achieved through the charging and discharging of the CStart capacitor C66. This, coupled to the charging and discharging of the voltage of CSD (C11 on daughter board for CH1) of the IRS20957SPBF, is all that is required for complete sequencing. The conceptual start-up and shutdown timing diagrams are shown in [Figure 20](#).

Functional descriptions

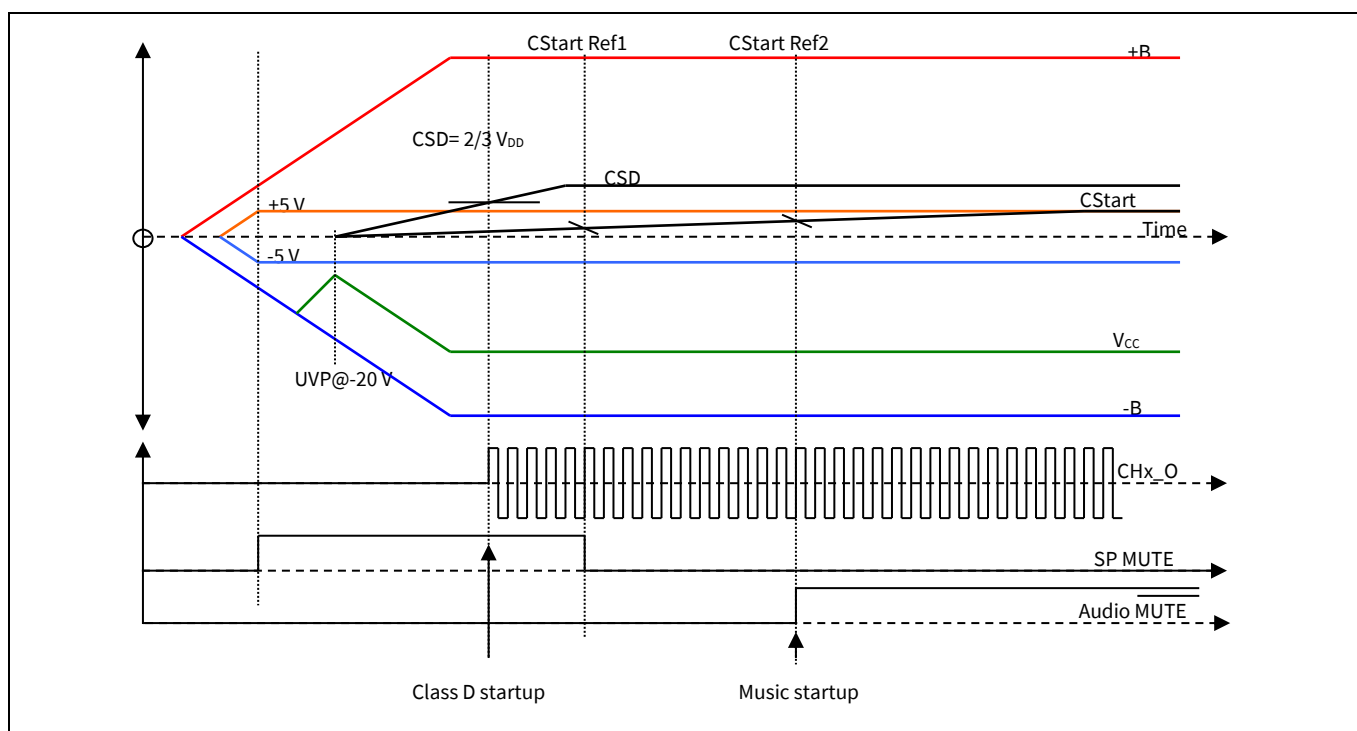


Figure 20 Conceptual start-up sequencing of power supplies and audio section timing

For start-up sequencing, $\pm B$ supplies start up at different intervals. As $\pm B$ supplies reach +5 V and -5 V respectively, the analog supplies (± 5 V) start charging and, once +B reaches ~ 16 V, V_{CC} charges. Once -B reaches -20 V, the UVP is released and CSD and CStart start charging. Once ± 5 V is established, the click-noise reduction circuit is activated through the SP MUTE control signal. As CSD reaches two-thirds V_{DD} , the Class D stage starts oscillating. Once the start-up transient has passed, SP MUTE is released (CStart reaches Ref1). The class D amplifier is now operational, but the preamp output remains muted until CStart reaches Ref2. At this point, normal operation begins. The entire process takes less than 3 s.

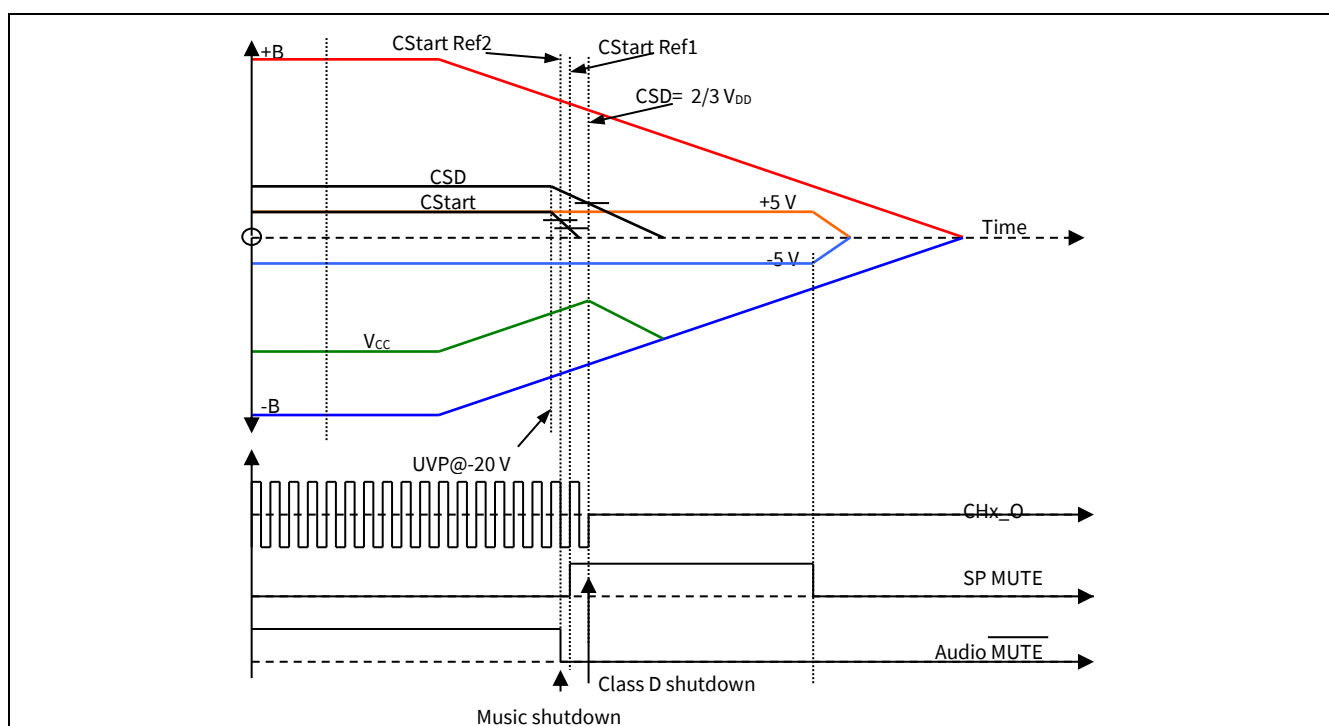


Figure 21 Conceptual shutdown sequencing of power supplies and audio section timing

Functional descriptions

Shutdown sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS20957SPBF trips UVP. Once UVP is activated, CSD and CStart are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. Once CStart reaches threshold Ref1, the click-noise reduction circuit is activated (SP MUTE). It is then possible to shut down the class D stage (CSD reaches two-thirds V_{DD}). This process takes less than 200 ms.

For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as start-up).

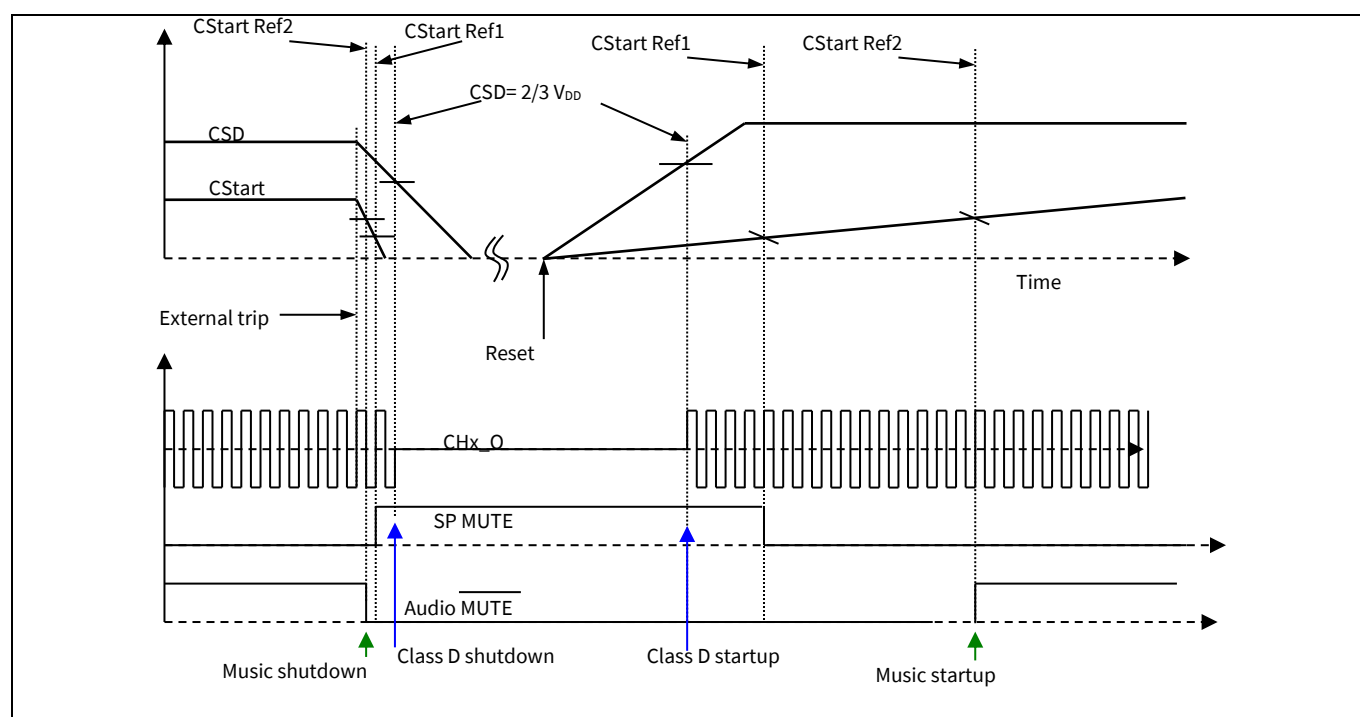


Figure 22 Conceptual click-noise reduction sequencing at trip and reset

8.18 Selectable dead-time

The IRS20957SPBF determines its dead-time based on the voltage applied to the DT pin. An internal comparator translates which pre-determined dead-time is being used by comparing the DT voltage with internal reference voltages. A resistive voltage divider from V_{CC} sets threshold voltages for each setting, negating the need for a precise absolute voltage to set the mode. The threshold voltages between dead-time settings are set internally, based on different ratios of V_{CC} as indicated in the diagram below. In order to avoid drift from the input bias current of the DT pin, a bias current of greater than 0.5 mA is suggested for the external resistor-divider circuit. Suggested values of resistance that are used to set a dead-time are given below. Resistors with up to 5 percent tolerance can be used.

Table 6 Recommended resistor values for dead-time selection

| Dead-time mode | Dead-time | R12A/B | R10A/B | DT voltage |
|----------------|-----------|-----------------|-----------------|-------------------|
| DT1 | ~15 ns | Less than 10 kΩ | Open | V_{CC} |
| DT2 | ~25 ns | 5.6 kΩ | 4.7 kΩ | 0.46 (V_{CC}) |
| DT3 | ~35 ns | 8.2 kΩ | 3.3 kΩ | 0.29 (V_{CC}) |
| DT4 | ~45 ns | Open | Less than 10 kΩ | COM |

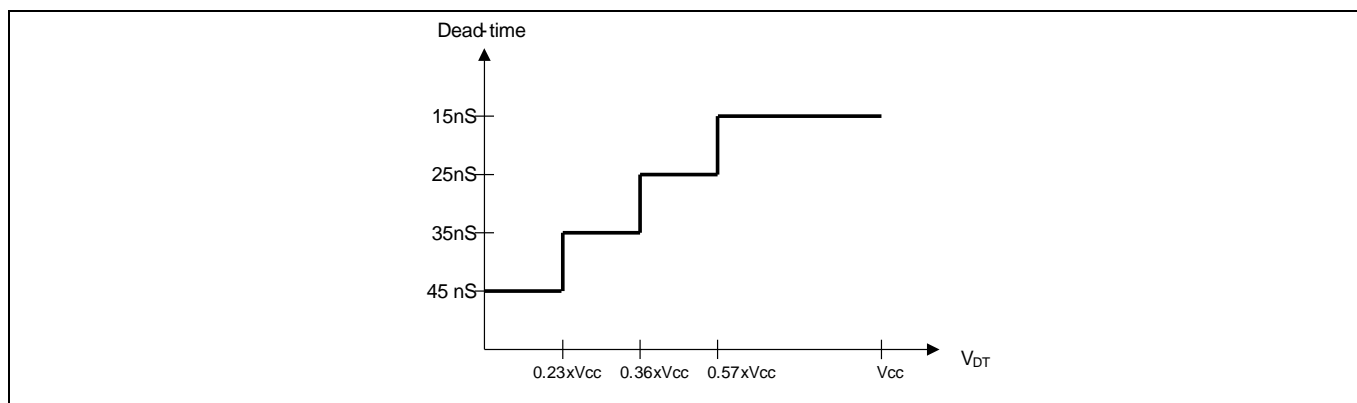


Figure 23 Dead-time setting vs. V_{DT} voltage

8.19 Protection system overview

The IRS20957SPBF integrates OCP inside the IC. The rest of the protections, such as OVP, UVP and OTP, are detected externally to the IRS20957SPBF.

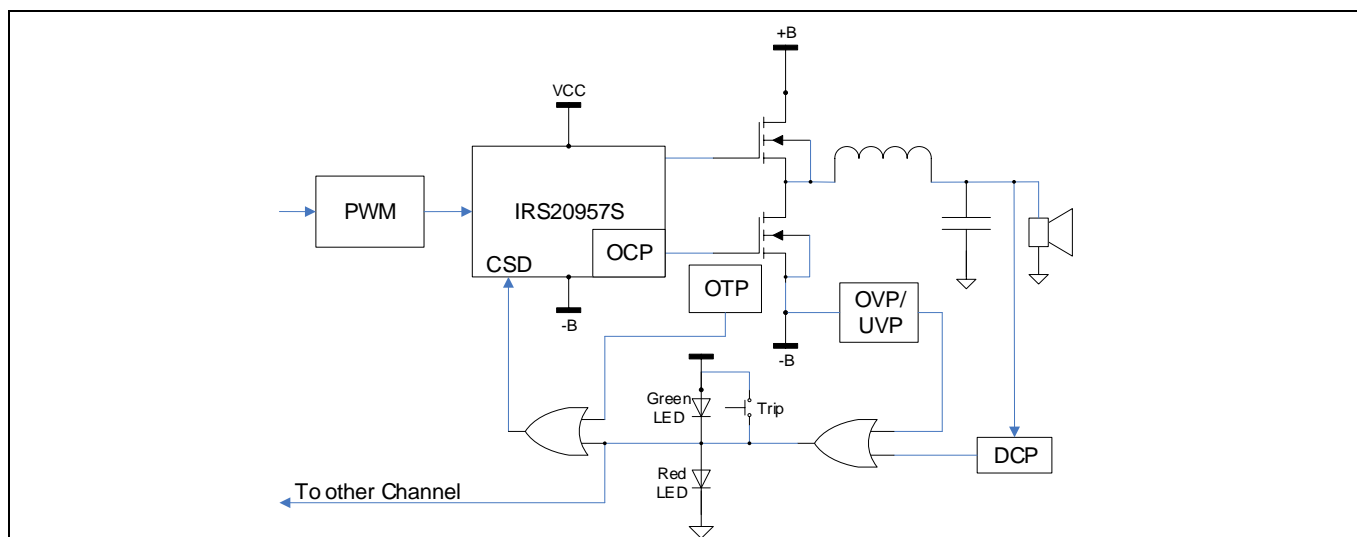


Figure 24 Functional block diagram of protection circuit implementation

The external shutdown circuit will disable the output by pulling down CSD pins. If the fault condition persists, the protection circuit stays in shutdown until the fault is removed.

8.19.1 Over-Current Protection (OCP)

The OCP internal to the IRS20957SPBF shuts down the IC if an OCP is sensed in either of the output CoolGaN™ HEMTs. For a complete description of the OCP circuitry, please refer to the IRS20957SPBF datasheet. Following is a brief description:

8.19.1.1 Low-side current sensing

The low-side current sensing feature protects the low-side CoolGaN™ from an over-load condition from negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on-state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

Functional descriptions

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage becomes higher than the OCSET voltage during low-side conduction, the IRS20957SPBF turns the outputs off and pulls CSD down to -VSS.

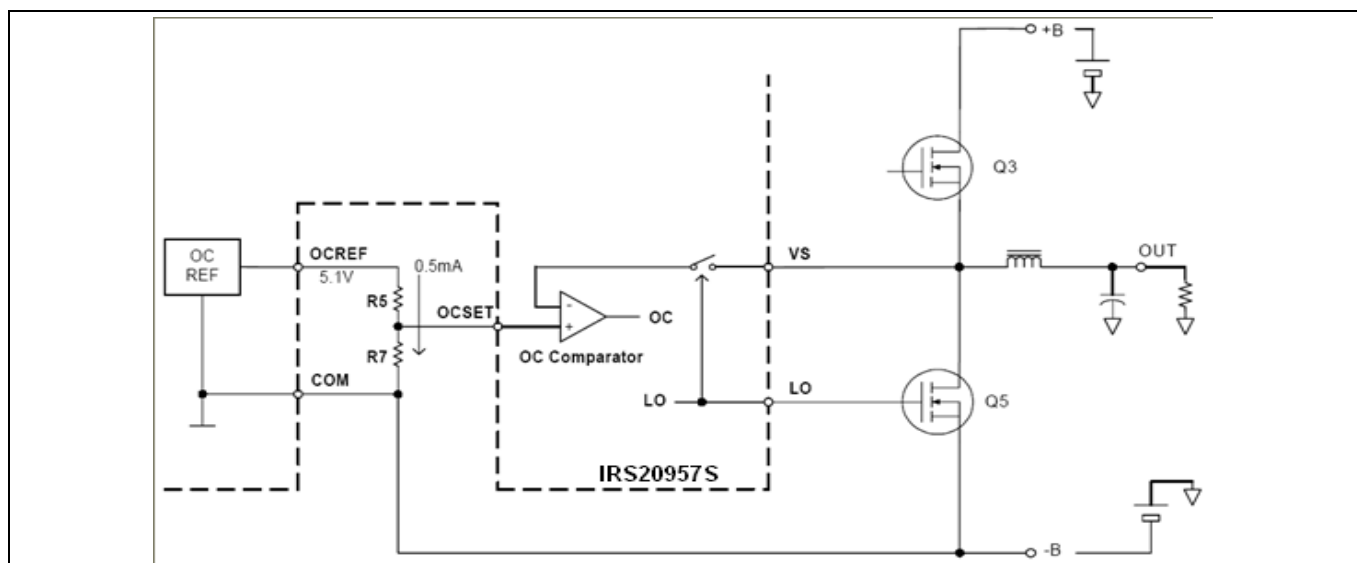


Figure 25 Simplified functional block diagram of low-side current sensing

8.19.1.2 High-side current sensing

The high-side current sensing protects the high-side CoolGaN™ from an overload condition from positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on-state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side CoolGaN™ during the on-state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side CoolGaN™. In contrast to the low-side current sensing, the threshold of the CSH pin to trigger OC protection is internally fixed at 1.2 V. An external resistive divider, R16A/B, R17A/B and R18A/B, is used to program a threshold. An external reverse blocking diode D4A/B is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6 V at D4A/B, the minimum threshold that can be set for the high-side is 0.6 V across the drain-to-source.

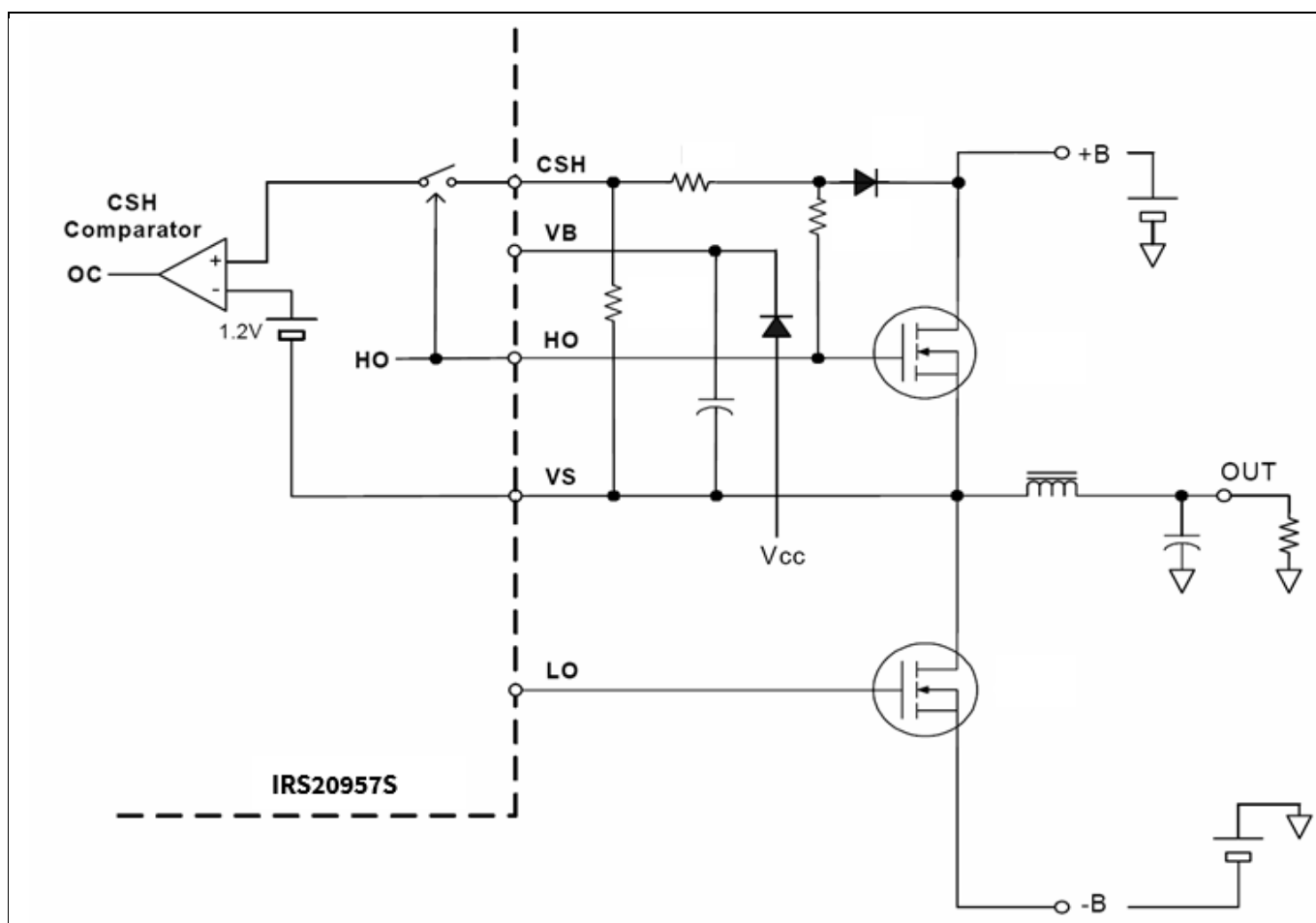


Figure 26 Simplified functional block diagram of high-side current sensing

8.19.2 Over-Voltage Protection (OVP)

OVP is provided externally to the IRS20957SPBF. OVP shuts down the amplifier if the bus voltage between GND and -B exceeds 82 V. The threshold is determined by a Zener diode Z9. OVP protects the board from harmful excessive supply voltages, such as due to bus pumping at very low-frequency continuous output in stereo mode.

8.19.3 Under-Voltage Protection (UVP)

UVP is provided externally to the IRS20957SPBF. UVP prevents unwanted audible noise output from unstable PWM operation during power-up and -down. UVP shuts down the amplifier if the bus voltage between GND and -B falls below a voltage set by Zener diode Z8.

8.19.4 Speaker DC-voltage Protection (DCP)

DCP protects speakers against DC output current feeding to the voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by an CoolGaN™ HEMT's failure because one of the high-side or low-side CoolGaN™ HEMTs short-circuited and remained in the on-state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ± 2.1 V triggers DCP.

Functional descriptions

8.19.5 Offset null (DC offset) adjustment

The EVAL_AUDAMP24 is designed such that no output-offset nullification is required. DC offsets are tested to be less than ± 5 mV.

8.19.6 Over-Temperature Protection (OTP)

A separate PTC resistor is placed in close proximity to the high-side IGT40R070D1 E8220 CoolGaN™ for each of the amplifier channels. If the resistor temperature rises above 90°C, OTP is activated. The OTP protection will only shut down the relevant channel by pulling the CSD pin low and will recover once the temperature at the PTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the CoolGaN™ of about 100°C. This setting is limited by the PCB material and not by the operating range of the CoolGaN™.

8.20 Thermal information

8.20.1 Peak power duration thermal information

Test conditions:

Input signal = 1 kHz

Both channel driven

$F_{PWM} = 500$ kHz

Table 7 Peak power

| Load (Ω) | $\pm V_{bus}$ (V) | 1 percent THD+N power (W) | Duration |
|-------------------|-------------------|---------------------------|--|
| 4 | 43 | 225 | More than 1 minute no thermal shutdown at $T_{HEATSINK} = 100^\circ\text{C}$ |
| 8 | 63 | 250 | More than 1 minute no thermal shutdown at $T_{HEATSINK} = 100^\circ\text{C}$ |

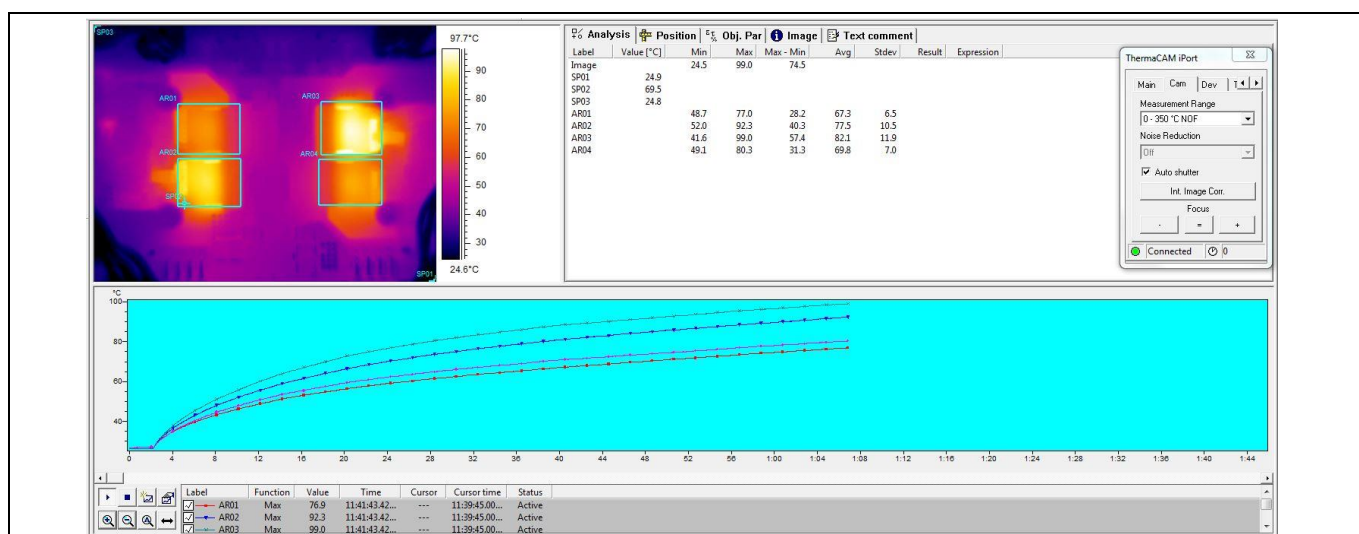
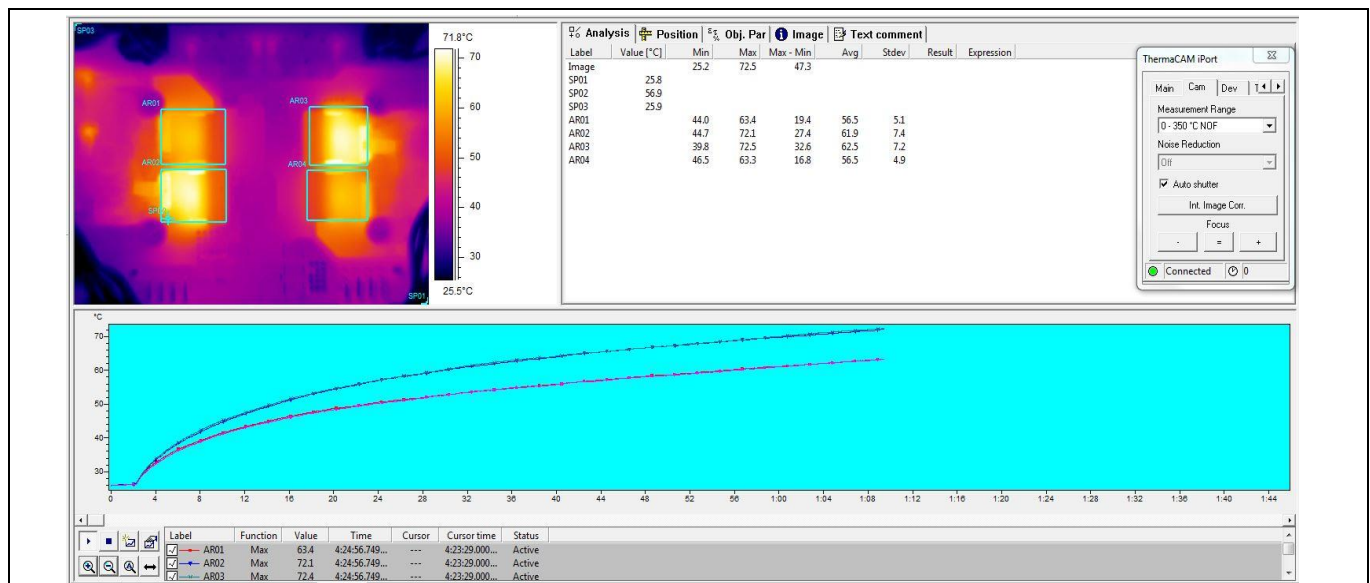


Figure 27 Peak power $P_{out} = 225$ W with 4 Ω load ± 43 V

Note: Maximum temperature 99.0°C at 1 minute.

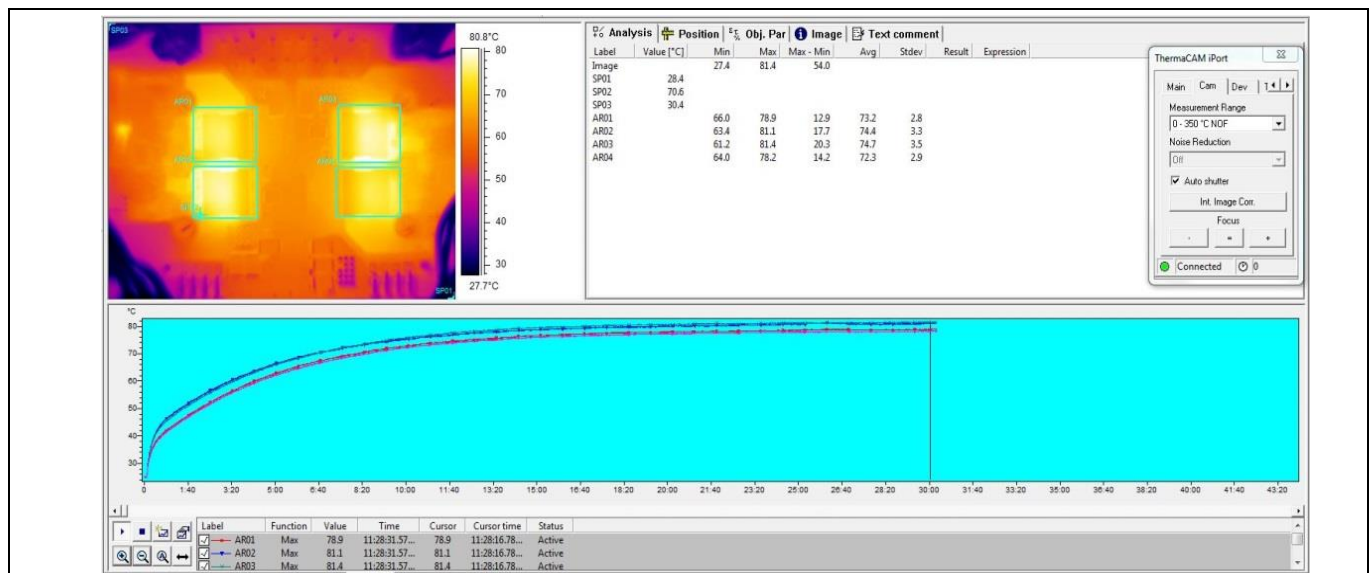
Functional descriptions

Figure 28 Peak power $P_{out} = 250\text{ W}$ with $8\ \Omega$ load $\pm 63\text{ V}$

Note: Maximum temperature 72.5°C at 1 minute.

Table 8 1/8 power test

| Load (Ω) | $\pm V_{bus}$ (V) | Max. T-case ($^\circ\text{C}$) | 1/8 power (W) | Duration (minutes) |
|-------------------|-------------------|----------------------------------|---------------|--------------------|
| 4 | 43 | 81.1 | 28.1 | 30 |
| 8 | 63 | 85.5 | 31.25 | 30 |

Figure 29 1/8 power = 28.1 W with $4\ \Omega$ load $\pm 43\text{ V}$

Note: Maximum temperature 81.1°C at 30 minutes, room temperature = 25°C .

EVAL_AUDAMP24

IRS20957SPBF + IGT40R070D1 E8220 evaluation board

Functional descriptions

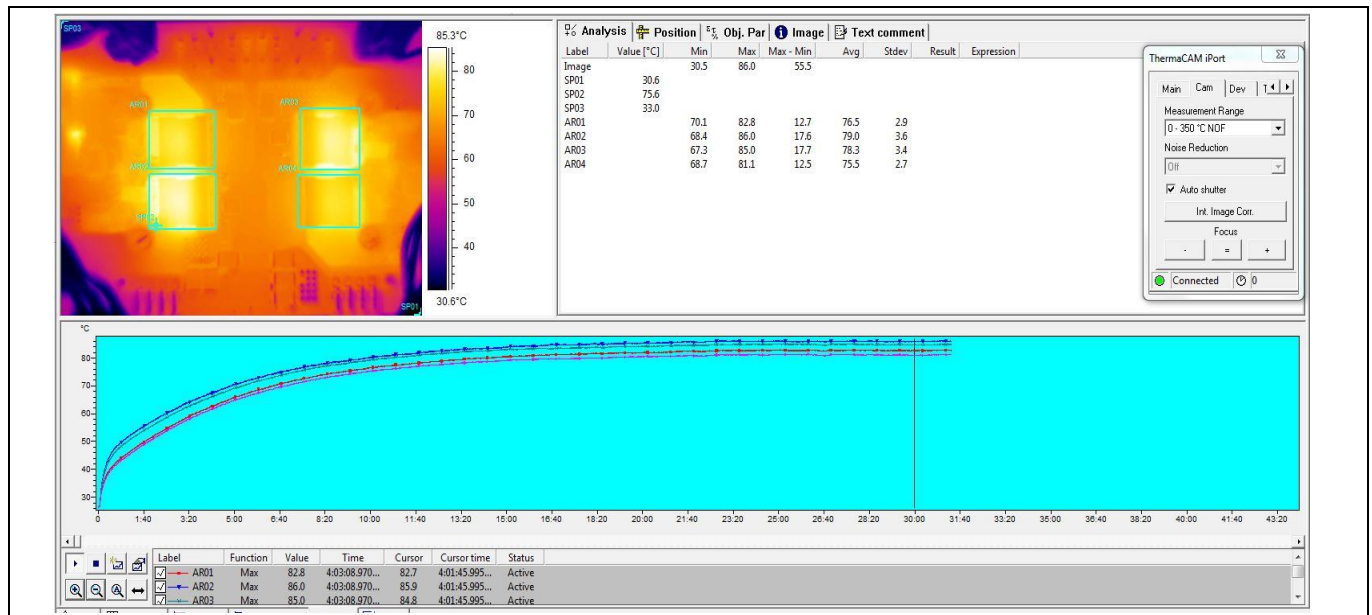


Figure 30 1/8 power = 31.25 W with 8 Ω load ±63 V

Note: Maximum temperature 85.5°C at 30 minutes, room temperature = 25°C.

Functional descriptions

8.20.2 Thermal Interface Materials (TIMs)

Recommend TIMs for heatsink attachment.

| Common Thermal Interface Materials Cost Trades | | | | | | | | |
|--|----------------|----------------------------------|------------------|-------------------|----------------|--------------|------------------------------|-----------------------|
| Mfr. | Material | Type | Thickness (mils) | Pressure Required | Dispense/Apply | Clips/Screws | Can be applied to heat sink? | Mechanical Placement? |
| Dow Corning | 1-4173 | 1 part heat-cured adhesive | # | Yes | Dispense | Clips | N | Y |
| Dow Corning | SE 4451 | 2 part heat-cured adhesive | # | Yes | Dispense | Clips | N | Y |
| Dow Corning | 3-6652 | 2 part heat-cured adhesive | # | Yes | Dispense | Clips | N | Y |
| Dow Corning | TP-1500 Pad | Tacky - Phase Change at 52°C | 10 | >5psi, 20psi typ. | Apply | Clips | Y | Y |
| Bergquist | Gap Pad 3000 | conformable filled polymer sheet | 15 | >10psi | Apply | Clips/Screws | N | Y |
| Bergquist | Gap Pad 2000 | conformable filled polymer sheet | 10 | >10psi | Apply | Clips/Screws | N | Y |
| Bergquist | Hi Flow 300 | Phase Change at 55°C | 2.4 | >10psi | Apply | Clips | Y | * |
| Bergquist | Hi Flow 625 | Phase Change at 65°C | 5 | >10psi | Apply | Clips | Y | * |
| Bergquist | Hi Flow 818 | Phase Change at 65°C | 5.5 | >10psi | Apply | Clips | Y | * |
| Bergquist | Sil Pad 800 | Conformable silicone elastomer | 5 | >10 higher better | Apply | Clips/Screws | Y | * |
| Bergquist | Sil Pad 900 | Conformable silicone elastomer | 9 | >10 higher better | Apply | Clips/Screws | Y | * |
| Bergquist | Sil Pad A1500 | Conformable silicone elastomer | 10 | 10-50psi | Apply | Clips/Screws | Y | * |
| Bergquist | Sil Pad A2000 | Conformable silicone elastomer | 10 | 10-50psi | Apply | Clips/Screws | Y | * |
| Bergquist | Bond Ply 100 | Pressure sensitive adhesive tape | 5 | >10psi | Apply | Clips | Y | Y |
| Bergquist | Bond Ply 100 | Pressure sensitive adhesive tape | 11 | >10psi | Apply | Clips | Y | Y |
| Thermoset (Lord) | Gelease MG-120 | Thermal grease/gel | # | 5-7lbf | Dispense | Clips | N | Y |
| Shin Etsu | X-23-7783D | Thermal grease | # | - | Dispense | Clips | N | Y |
| Shin Etsu | X-23-7762 | Thermal grease | # | - | Dispense | Clips | N | Y |

Figure 31 TIM recommendations

9 Schematic

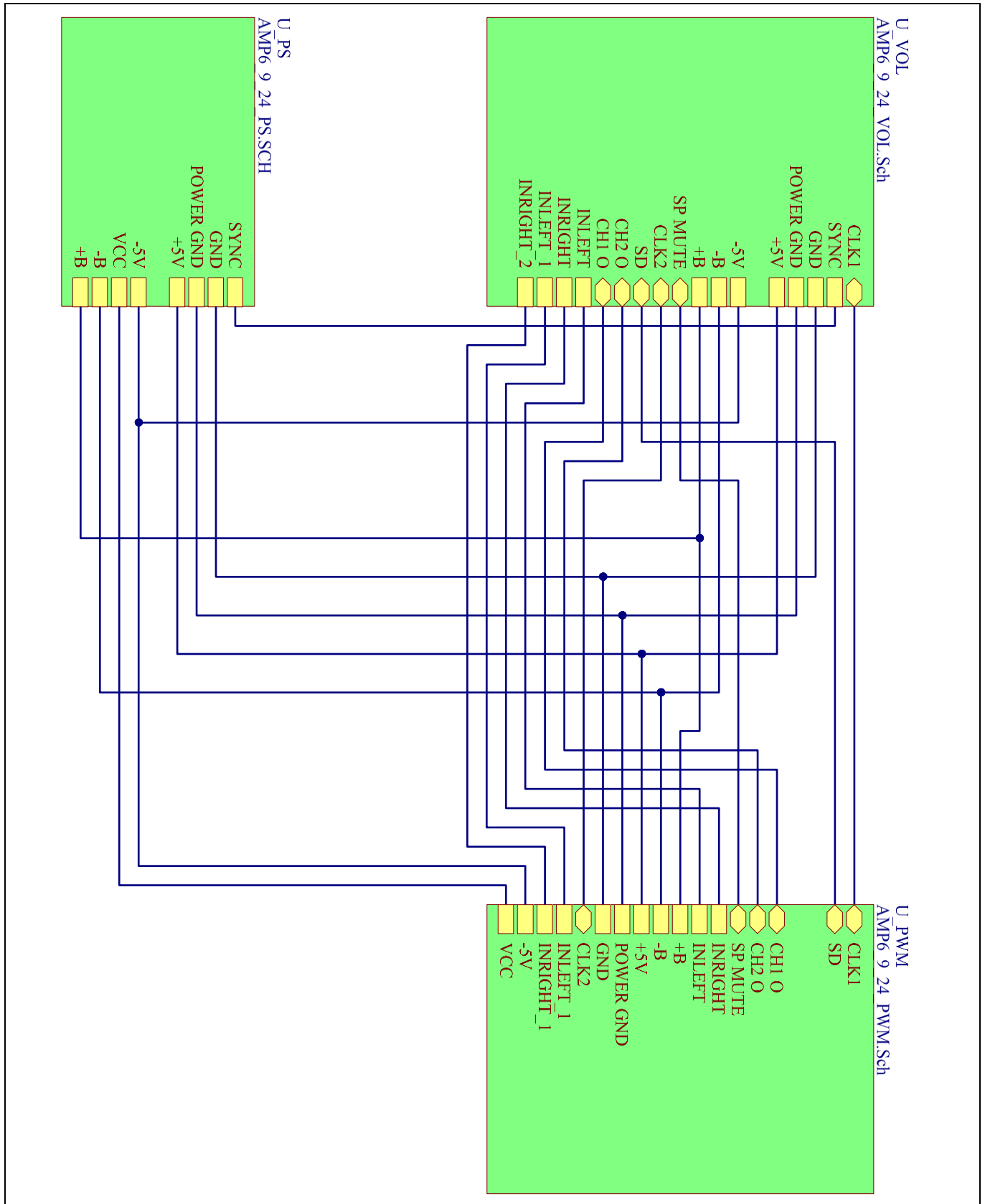


Figure 32 Motherboard schematic 1

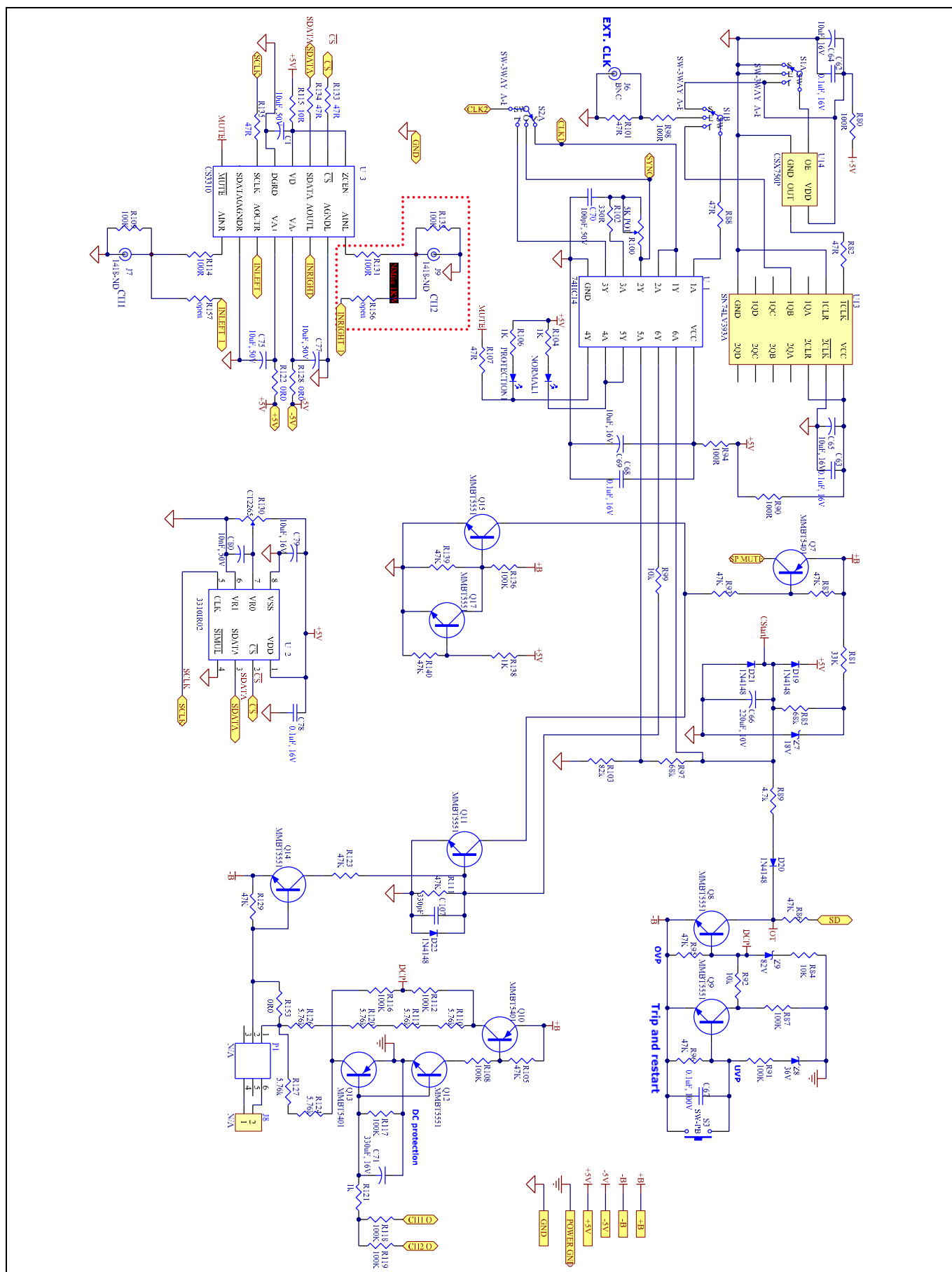


Figure 33 Motherboard schematic 2

Schematic

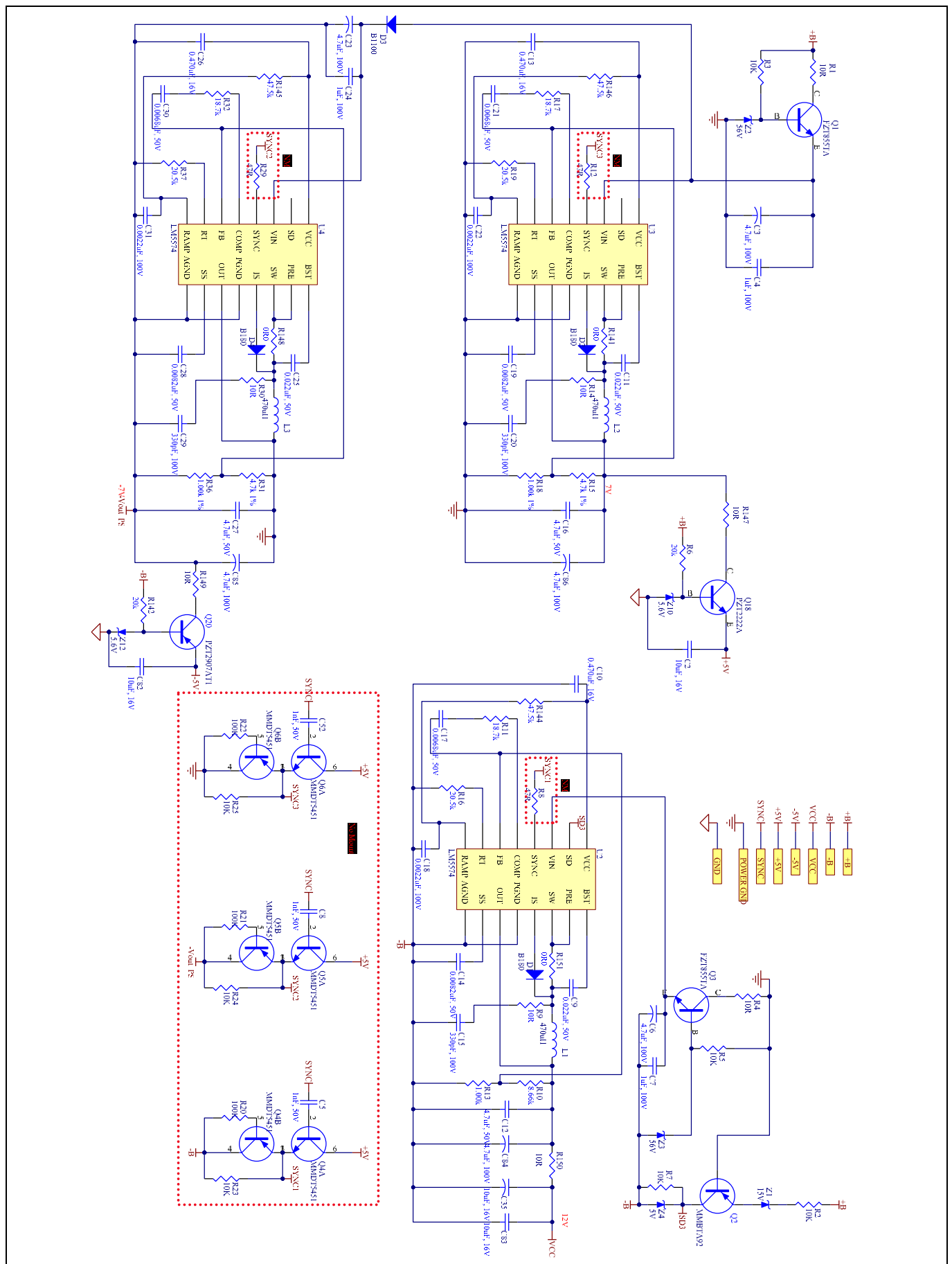


Figure 34 **Motherboard schematic 3**

Schematic

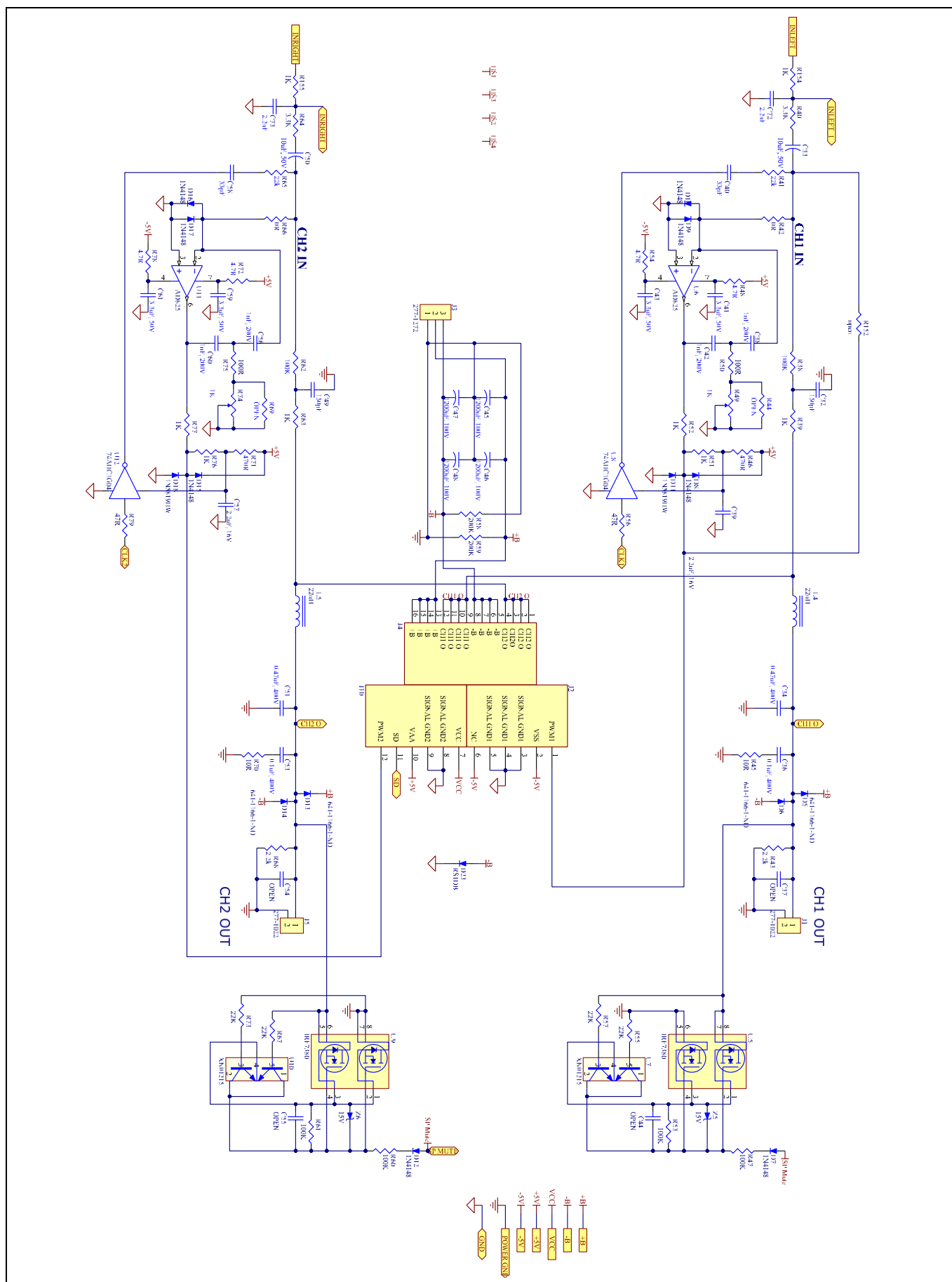


Figure 35 **Motherboard schematic 4**

PCB**10 PCB****10.1 PCB specification**

1. Two-layer SMT PCB with through-holes
2. 1/16 thickness
3. 2/0 oz. Cu
4. FR4 material
5. 20 mil lines and spaces
6. Solder mask to be green enamel EMP110 DBG (CARAPACE) or Enthone endplate DSR-3241 or equivalent
7. Silk screen to be white epoxy non-conductive per IPC–RB 276 standard
8. All exposed copper must be finished with tin-lead Sn 60 or 63 for 100 μ inches thick
9. Tolerance of PCB size shall be 0.010 to 0.000 inches
10. Tolerance of all holes is/- 0.003 inches
11. PCB acceptance criteria as defined for class II PCB standards

10.2 PCB layout

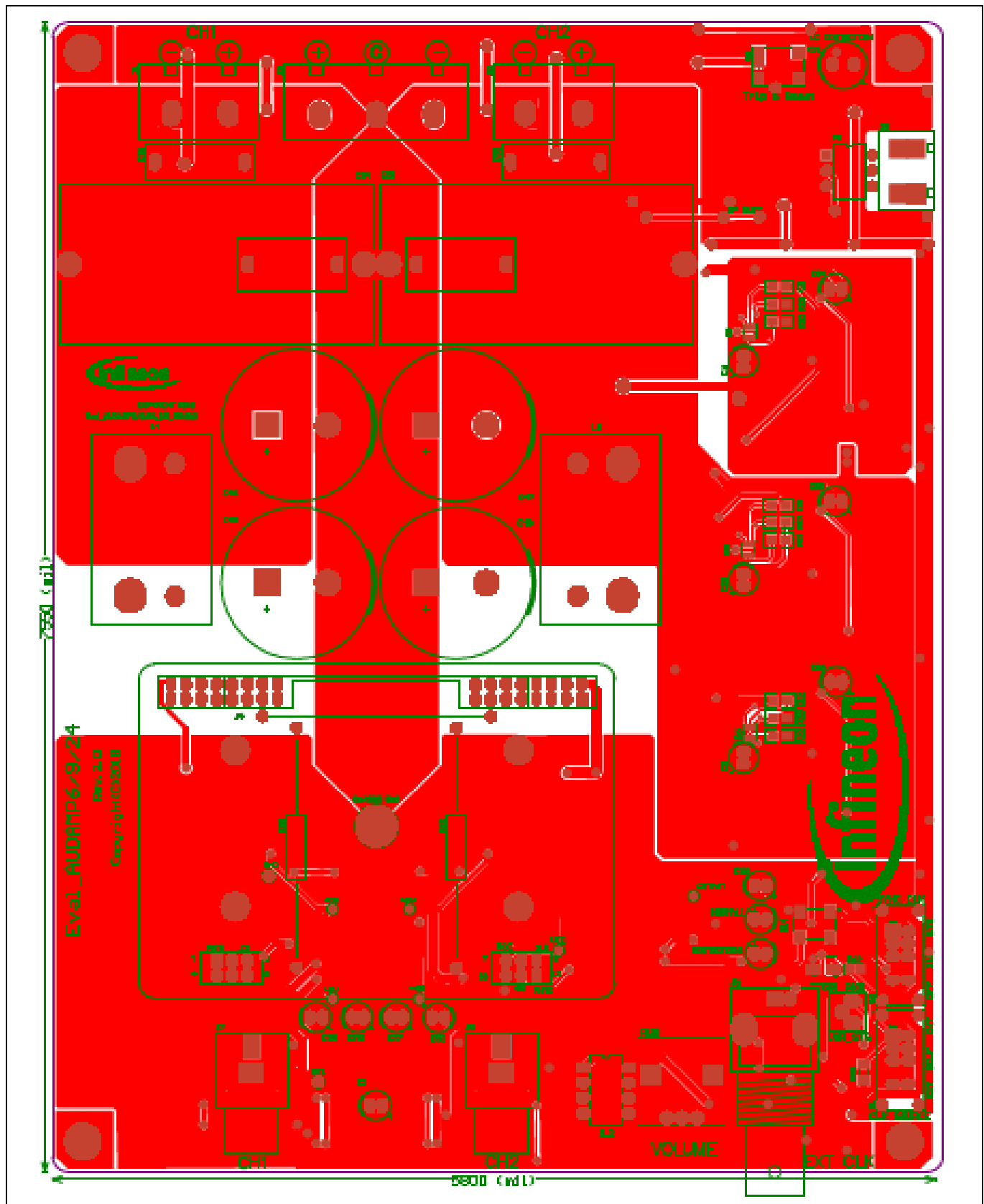


Figure 37 Motherboard top view

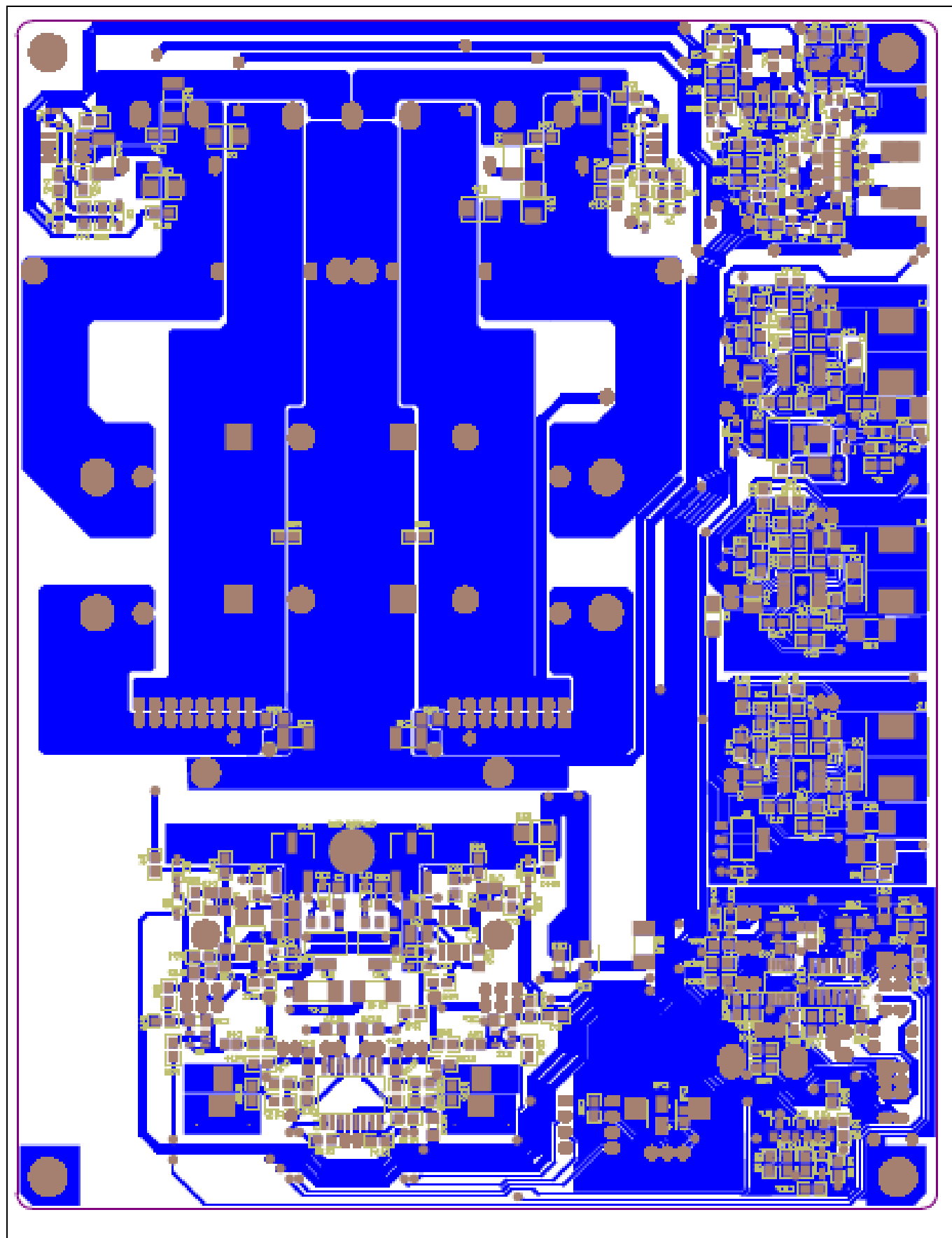


Figure 38 Motherboard bottom view

PCB

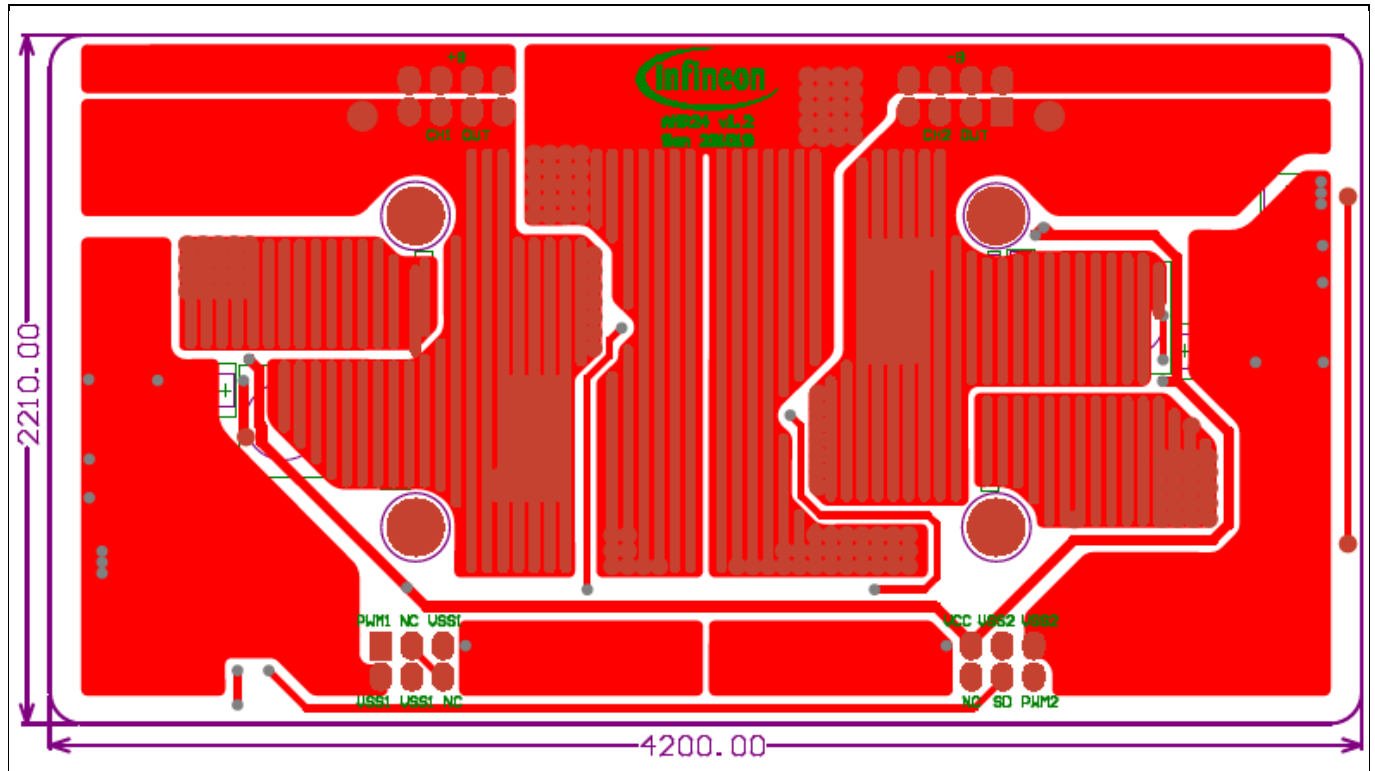


Figure 39 Daughter board top view

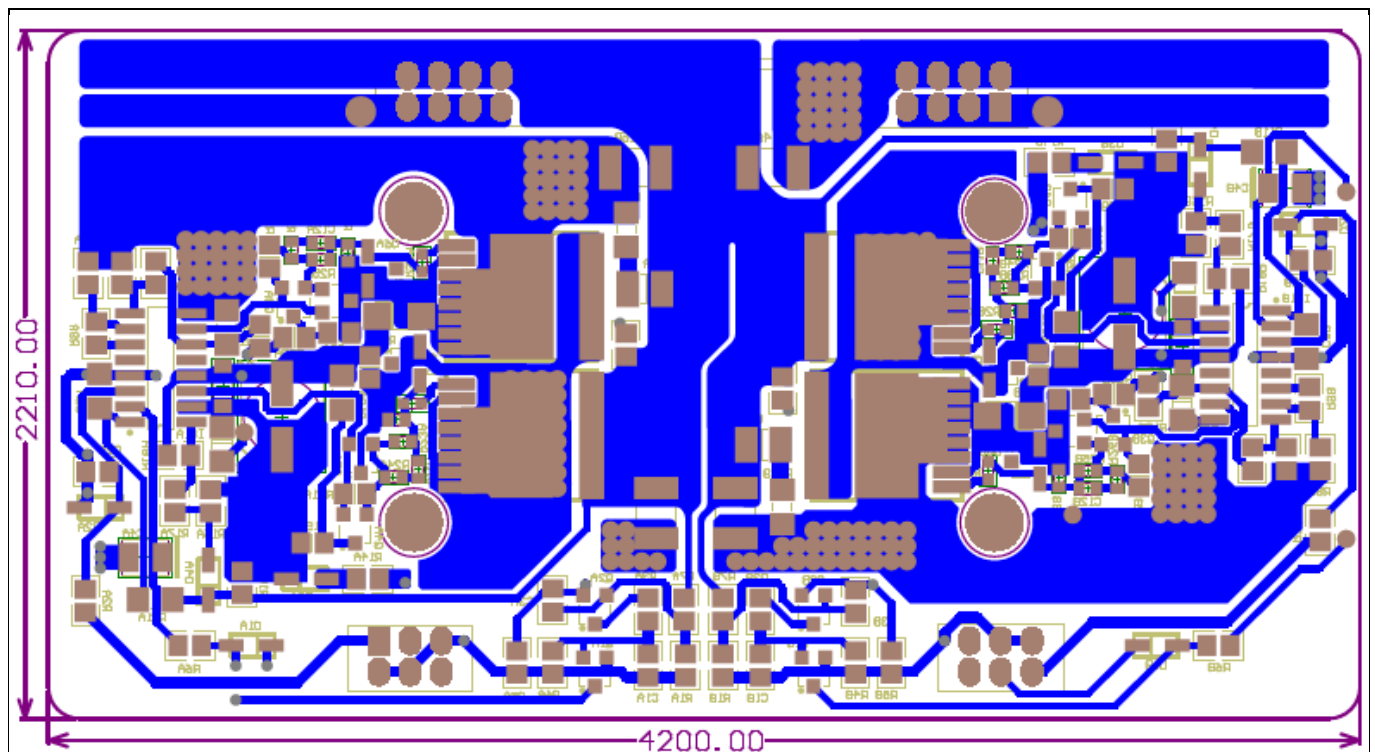


Figure 40 Daughter board bottom view

Bill of Materials (BOM)

11 Bill of Materials (BOM)

Table 9 Motherboard BOM

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|---------------|----------------------------|--|----------|---------|
| 1 | 565-1106-ND | C1, C33, C50, C75, C77 | Capacitor 10 μ F 50 V elect. SMG RAD | 5 | Digikey |
| 2 | PCC13491CT-ND | C2, C82, C83 | Capacitor 10 μ F 16 V ceramic X7R 1206 | 3 | Digikey |
| 3 | 565-1147-ND | C3, C6, C23, C84, C85, C86 | Capacitor 4.7 μ F 100 V elect. SMG RAD | 6 | Digikey |
| 4 | 490-1857-1-ND | C4, C7, C24 | Ceramic capacitor 1.0 μ F 100 V 10 percent X7R 1210 | 3 | Digikey |
| 5 | 490-1644-1-ND | C9, C11, C25 | Ceramic capacitor 22000 pF 50 V 5 percent C0G 0805 | 3 | Digikey |
| | 732-8076-1-ND | Substitute | | | |
| 6 | 478-1403-1-ND | C10, C13, C26 | Ceramic capacitor 0.47 μ F 10 percent 16 V X7R 0805 | 3 | Digikey |
| | 732-7662-1-ND | Substitute | | | |
| 7 | 490-1864-1-ND | C12, C16, C27 | Ceramic capacitor 4.7 μ F 50 V 10 percent X7R 1210 | 3 | Digikey |
| 8 | 445-2685-1-ND | C14, C19, C28 | Ceramic capacitor 8200 pF 50 V C0G 5 percent 0805 | 3 | Digikey |
| 9 | PCC1982CT-ND | C15, C20, C29 | Capacitor 330 pF 100 V ceramic X7R 0805 | 3 | Digikey |
| 10 | 478-3772-1-ND | C17, C21, C30 | Ceramic capacitor 6800 pF 5 percent 50 V X7R 0805 | 3 | Digikey |
| | 732-8073-1-ND | Substitute | | | |
| 11 | 478-3746-1-ND | C18, C22, C31 | Ceramic capacitor 2200 pF 5 percent 100 V X7R 0805 | 3 | Digikey |
| 12 | 445-2378-1-ND | C32, C49 | Ceramic capacitor 150 pF 3000 V C0G 10 percent 1812 | 2 | Digikey |
| 13 | 338-1178-ND | C34, C51 | Capacitor 0.33 μ F 2000 V DC poly-film AXL | 2 | Digikey |
| 14 | PCE3995CT-ND | C35, C64, C65, C69, C79 | Capacitor 10 μ F 16 V elect. FC SMD | 5 | Digikey |
| 15 | 495-1311-ND | C36, C53 | 0.1 μ F Film Capacitor 200 V 400 V Polypropylene (PP), Metallized Radial | 2 | Digikey |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|-------------------|-------------------------------------|--|----------|---------|
| 16 | PCC2009CT-ND | C38, C42, C56, C60 | Ceramic capacitor AMIC 1000 pF 200 V NP0 1206 | 4 | Digikey |
| 17 | PCC1931CT-ND | C39, C57 | Capacitor 2.2 μ F 16 V ceramic X7R 1206 | 2 | Digikey |
| 18 | 478-1281-1-ND | C40, C58 | Ceramic capacitor 33 pF 5 percent 100 V NP0 0805 | 2 | Digikey |
| 19 | 445-1432-1-ND | C41, C43, C59, C61 | Ceramic capacitor 3.3 μ F 50 V X7R 20 percent 1210 | 4 | Digikey |
| 20 | 565-1161-ND | C45, C46, C47, C48 | Capacitor 1200 μ F 100 V elect. SMG RAD | 4 | Digikey |
| 21 | PCC1812CT-ND | C62, C63, C68, C78 | Capacitor .1 μ F 16 V ceramic X7R 0805 | 4 | Digikey |
| | 732-8045-1-ND | Substitute | | | |
| 22 | 1189-4150-ND | C66 | Aluminum capacitor 220 μ F 20 percent 10 V radial | 1 | Digikey |
| 23 | 445-1418-1-ND | C67 | Ceramic capacitor 0.10 μ F 100 V X7R 10 percent 0805 | 1 | Digikey |
| 24 | PCC101CGCT-ND | C70 | Capacitor 100 pF 50 V ceramic chip 0805 SMD | 1 | Digikey |
| | 732-8062-1-ND | Substitute | | | |
| 25 | 493-1042-ND | C71 | Capacitor 330 μ F 16 V elect. VR radial | 1 | Digikey |
| 26 | 445-2322-1-ND | C72, C73 | Ceramic capacitor 2200 pF 100 V C0G 5 percent 0805 | 2 | Digikey |
| 27 | PCC103BNCT-ND | C80 | Capacitor 10000 pF 50 V ceramic chip 0805 | 1 | Digikey |
| | 732-8074-1-ND | Substitute | | | |
| 28 | 732-8065-1-ND | C107 | Ceramic capacitor 330 pF 50 V X7R 0805 | 1 | Digikey |
| 29 | B180DICT-ND | D1, D2, D4 | Schottky diode 80 V 1 A SMA | 3 | Digikey |
| 30 | B1100-FDICT-ND | D3 | Schottky diode 100 V 1 A SMA | 1 | Digikey |
| 31 | 641-1166-1-ND | D5, D6, D13, D14 | Standard diode 2 A 400 V SMB | 4 | Digikey |
| 32 | 1N4148WDICT-ND | D7, D8, D9, D10, D12, D15, D16, D17 | Switch diode 100 V 400 MW SOD-123 | 8 | Digikey |
| 33 | 1N5819HW-FDICT-ND | D11, D18 | Schottky diode 40 V 1 A SOD-123 | 2 | Digikey |
| 34 | 1N4148WTPMSCT-ND | D19, D20, D21, D22 | Switch diode 100 V 150 MA SOD-123 | 4 | Digikey |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|--------------------|---------------------------------|--|----------|----------------|
| 35 | RS1DB-FDICT-ND | D23 | Fast diode rec. 200 V 1 A SMB | 1 | Digikey |
| 36 | 277-1271-ND | J1, J5 | Conn. term. block 2-pos. 9.52 mm PCB | 2 | Digikey |
| 37 | A26453-ND | J2 | Conn. recept. 6-pos .100 vert. dual | 1 | Digikey |
| 38 | 277-1272-ND | J3 | Conn. term. block 3-pos. 9.52 mm PCB | 1 | Digikey |
| 39 | A26454-ND | J4 | Conn. recept. 8-pos .100 vert. dual | 1 | Digikey |
| 40 | A32248-ND | J6 | Conn. jack BNC R/A 50 Ω PCB tin | 1 | Digikey |
| 41 | CP-1418-ND | J7, J9 | Conn. RCA jack R/A black PCB | 2 | Digikey |
| 42 | N/A | J8 | Terminal block 7.50 mm vert. 2-pos | 1 | Digikey |
| 43 | A26453-ND | J10 | Conn. recept. 6-pos .100 vert. dual | 1 | Digikey |
| 44 | 513-1051-1-ND | L1, L2, L3 | Inductor shield PWR 470 μH SMD | 3 | Digikey |
| 45 | 7G31A-220M-R | L4, L5 | Class D inductor 22 μH | 2 | Inductors, Inc |
| | CPD3119-220M | Substitute | | | CODACA |
| 46 | 160-1143-ND | NORMAL1 | LED 3 mm green transparent | 1 | Digikey |
| | 732-5008-ND | Substitute | | | |
| 47 | N/A | P1 | Power MOSFET photovoltaic relay | 1 | Infineon |
| 48 | 160-1140-ND | PROTECTION1 | LED 3 mm hi-eff red transparent | 1 | Digikey |
| | 732-5006-ND | Substitute | | | |
| 49 | FZT855CT-ND | Q1, Q3 | Transistor NPN 150 V 4000 MA SOT-223 | 2 | Digikey |
| 50 | MMBTA92DICT-ND | Q2 | Transistor PNP -300 V SOT-23 | 1 | Digikey |
| 51 | MMBT5401DICT-ND | Q7, Q10, Q13 | Transistor 150 V 350 MW PNP SMD SOT-23 | 3 | Digikey |
| 52 | MMBT5551-7DICT-ND | Q8, Q9, Q11, Q12, Q14, Q15, Q17 | Transistor 160 V 350 MW NPN SMD SOT-23 | 7 | Digikey |
| 53 | PZT2222ACT-ND | Q18 | Transistor amp NPN GP 40 V 0.5 A SOT-223 | 1 | Digikey |
| 54 | PZT2907AT1GOSCT-ND | Q20 | Transistor SS SW PNP 600 MA 60 V SOT-223 | 1 | Digikey |
| 55 | PT10XCT-ND | R1, R4, R9, R14, R30 | Resistor 10 Ω 1 W 5 percent 2512 SMD | 5 | Digikey |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|------------------|---|---|----------|---------|
| 56 | P10KACT-ND | R2, R3, R5, R7, R84, R92, R99 | Resistor 10 k Ω 1/8 W 5 percent 0805 SMD | 7 | Digikey |
| 57 | P20KACT-ND | R6, R142 | Resistor 20 k Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 58 | P47ACT-ND | R56, R79, R82, R88, R101, R107, R133, R134, R135 | Resistor 47 Ω 1/8 W 5 percent 0805 SMD | 9 | Digikey |
| 59 | RHM8.66KCRCT-ND | R10 | Resistor 8.66 k Ω 1/8 W 1 percent 0805 SMD | 1 | Digikey |
| 60 | P18.7KCCT-ND | R11, R17, R32 | Resistor 18.7 k Ω 1/8 W 1 percent 0805 SMD | 3 | Digikey |
| 61 | P1.00KCCT-ND | R13 | Resistor 1.00 k Ω 1/8 W 1 percent 0805 SMD | 1 | Digikey |
| 62 | P4.7KCCT-ND | R15, R31 | Resistor 4.70 k Ω 1/8 W 1 percent 0805 SMD | 2 | Digikey |
| 63 | P20.5KCCT-ND | R16, R19, R37 | Resistor 20.5 k Ω 1/8 W 1 percent 0805 SMD | 3 | Digikey |
| 64 | P1.00KCCT-ND | R18, R36 | Resistor 1.00 k Ω 1/8 W 1 percent 0805 SMD | 2 | Digikey |
| 65 | P100KACT-ND | R20, R21, R22, R47, R53, R60, R61, R87, R91, R108, R109, R112, R116, R117, R118, R119, R132, R136 | Resistor 100 k Ω 1/8 W 5 percent 0805 SMD | 15 | Digikey |
| 66 | PPC100KW-3JCT-ND | R38, R62 | Resistor 100 k Ω metal film 3 W 5 percent | 2 | Digikey |
| 67 | P1.0KECT-ND | R39, R63 | Resistor 1.0 k Ω 1/4 W 5 percent 1206 SMD | 2 | Digikey |
| 68 | P3.3KZCT-ND | R40, R64 | Resistor 3.3 k Ω 1/10 W 0.1 percent 0805 SMD | 2 | Digikey |
| 69 | P22KACT-ND | R41, R55, R57, R65, R67, R73 | Resistor 22 k Ω 1/8 W 5 percent 0805 SMD | 6 | Digikey |
| 70 | P0.0ACT-ND | R42, R66 | Resistor 0.0 Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 71 | PT2.2KXCT-ND | R43, R68 | Resistor 2.2 k Ω 1 W 5 percent 2512 SMD | 2 | Digikey |
| 72 | PT10XCT-ND | R45, R70 | Resistor 10 Ω 1 W 5 percent 2512 SMD | 2 | Digikey |
| 73 | 311-470ARCT-ND | R46, R71 | Resistor 470 Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 74 | P4.7ACT-ND | R48, R54, R72, R78 | Resistor 4.7 Ω 1/8 W 5 percent 0805 | 4 | Digikey |
| 75 | 3361P-102GCT-ND | R49, R74 | Trimpot 1 k Ω 6 mm ² SMD | 2 | Digikey |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|-----------------|---|---|----------|---------|
| 76 | P100ECT-ND | R50, R75, R80, R90, R94 | Resistor 100 Ω 1/4 W 5 percent 1206 SMD | 5 | Digikey |
| 77 | P1.0KACT-ND | R51, R52, R76, R77, R104, R106, R121, R138 | Resistor 1.0 k Ω 1/8 W 5 percent 0805 SMD | 8 | Digikey |
| 78 | P200KACT-ND | R58, R59 | Resistor 200 k Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 79 | P33KACT-ND | R81 | Resistor 33 k Ω 1/8 W 5 percent 0805 SMD | 1 | Digikey |
| 80 | P47KACT-ND | R83, R86, R93, R95, R96, R105, R111, R123, R129, R139, R140 | Resistor 47 k Ω 1/8 W 5 percent 0805 SMD | 11 | Digikey |
| 81 | P68KACT-ND | R85, R97 | Resistor 68 k Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 82 | P4.7KACT-ND | R89 | Resistor 4.7 k Ω 1/8 W 5 percent 0805 SMD | 1 | Digikey |
| 83 | P100ACT-ND | R98, R114, R131 | Resistor 100 Ω 1/8 W 5 percent 0805 SMD | 3 | Digikey |
| 84 | 3362H-502LF-ND | R100 | Pot 5.0 k Ω 1/4 in. square ceramic SL ST | 1 | Digikey |
| 85 | P330ACT-ND | R102 | Resistor 330 Ω 1/8 W 5 percent 0805 SMD | 1 | Digikey |
| 86 | P82KACT-ND | R103 | Resistor 82 k Ω 1/8 W 5 percent 0805 SMD | 1 | Digikey |
| 87 | P5.76KFCT-ND | R110, R113, R120, R124, R126, R127 | Resistor 5.76 k Ω 1/4 W 1 percent 1206 SMD | 6 | Digikey |
| 88 | P10ECT-ND | R115 | Resistor 10 Ω 1/4 W 5 percent 1206 SMD | 1 | Digikey |
| 89 | P0.0ECT-ND | R122, R128 | Resistor 0 Ω 1/4 W 5 percent 1206 SMD | 2 | Digikey |
| 90 | P3G7103-ND | R130 | Pot 10 k Ω 9 mm vert. metal bushing | 1 | Digikey |
| 91 | RMCF1/100RCT-ND | R141, R148, R151 | Resistor 0.0 Ω 1/8 W 0805 SMD | 3 | Digikey |
| 92 | P47.5KCCT-ND | R144, R145, R146 | Resistor 47.5 k Ω 1/8 W 1 percent 0805 SMD | 3 | Digikey |
| 93 | PT10XCT-ND | R147, R149, R150 | Resistor 10 Ω 1 W 5 percent 2512 SMD | 3 | Digikey |
| 94 | open | R152 | 0 Ω for 1 kW | 1 | Digikey |
| 95 | P0.0ACT-ND | R153 | Resistor 1.0 k Ω 1/8 W 5 percent 0805 SMD | 1 | Digikey |
| 96 | 311-1.0KARCT-ND | R154, R155 | Resistor 1.0 k Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 97 | open | R156, R157 | Bypass vol. ctrl | 2 | |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|---------------------|------------|--|----------|----------------|
| 98 | EG1944-ND | S1, S2 | Slide switch DP3T 0.2 A L = 6 mm | 2 | Digikey |
| 99 | P8010S-ND | S3 | 6 mm light touch SW H = 5 | 1 | Digikey |
| 100 | LM5574MT-ND | U2, U3, U4 | IC reg. buck 75 V 0.5 A 16-TSSOP | 3 | Digikey |
| 101 | IRF7380 | U5, U9 | 80 V dual n-MOSFET SO8 | 2 | Infineon |
| 102 | AD825ARZ-ND | U6, U11 | IC amp JFET HS GEN-PURP 8-SOIC | 2 | Digikey |
| 103 | FMG4AT148CT-ND | U7, U10 | Transistor 2NPN pre-bias 0.3 W SMT5 | 2 | Digikey |
| 104 | 296-1089-1-ND | U8, U12 | IC single inverter gate SOT23-5 | 2 | Digikey |
| 105 | 296-11643-1-ND | U13 | Dual 4-bit binary counters | 1 | Digikey |
| 106 | CTX290CT-ND | U14 | XTAL OSC XO 1.5440 MHZ HCMOS TTL | 1 | Digikey |
| 107 | 296-1194-1-ND | U_1 | IC HEX SCHMITT-TRIG INV 14-SOIC | 1 | Digikey |
| 108 | 3310IR02 | U_2 | Standalone controller | 1 | Tachyonix |
| 109 | 598-1599-ND | U_3 | Amplifiers – audio stereo digital volume control | 1 | Digikey/Mouser |
| 110 | BZT52C15-7DICT-ND | Z1 | Zener diode 15 V 500 mW SOD-123 | 1 | Digikey |
| 111 | MMSZ5263BT1OSCT-ND | Z2, Z3 | Zener diode 500 mW 56 V SOD-123 | 2 | Digikey |
| 112 | BZT52C5V1-7DICT-ND | Z4 | Zener diode 5.1 V 500 mW SOD-123 | 1 | Digikey |
| 113 | BZT52C15-FDICT-ND | Z5, Z6 | Zener diode 500 mW 15 V SOD123 | 2 | Digikey |
| 114 | BZT52C18-FDICT-ND | Z7 | Zener diode 500 mW 18 V SOD123 | 1 | Digikey |
| 115 | BZT52C36-7DICT-ND | Z8 | Zener diode 36 V 500 mW SOD-123 | 1 | Digikey |
| 116 | MMSZ5268BT1GOSCT-ND | Z9 | Zener diode 82 V 500 mW SOD-123 | 1 | Digikey |
| 117 | BZT52C5V6-FDICT-ND | Z10, Z12 | Zener diode 5.6 V 500 mW SOD123 | 2 | Digikey |

Bill of Materials (BOM)

Table 10 Daughterboard BOM

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|----------------------------|---------------------------|--|----------|---------|
| 1 | 445-2276-1-ND | C1A, C1B, C3A, C3B | Ceramic capacitor 47000 pF 100 V X7R 10 percent 0805 | 4 | Digikey |
| 2 | PCC470CGCT-ND | C2A, C2B | Capacitor 47 pF 50 V ceramic chip 0805 SMD | 2 | Digikey |
| | 1276-1156-1-ND | Substitute | | | |
| 3 | 399-9725-1-ND | C4A, C4B | Tantalum capacitor 33 μF 16 V 10 percent SMD | 2 | Digikey |
| 4 | 587-1329-1-ND | C5A, C5B, C7A, C7B | Ceramic capacitor 2.2 μF 25 V X7R 1206 | 4 | Digikey |
| | 732-7571-1-ND | Substitute | | | |
| 5 | 490-14441-2-ND | C6A, C6B | Ceramic capacitor 10 μF 25 V X7R 1206 | 2 | Digikey |
| | 732-7700-1-ND | Substitute | | | |
| 6 | 493-2263-1-ND | C8A, C8B | Aluminum capacitor 150 μF 20 percent 16 V SMD | 2 | Digikey |
| 7 | DNP | C9A, C9B, C10A, C10B | NM | 4 | Digikey |
| 8 | 399-7867-1-ND | C11A, C11B, C12A, C12B | Ceramic capacitor 1800 pF 50 V X7R 0603 | 4 | Digikey |
| 9 | 445-2296-1-ND | C13A, C13B | Ceramic capacitor .22 μF 250 V X7R 10 percent 1210 | 2 | Digikey |
| 10 | 445-2300-1-ND | C14A, C14B, C15A, C15B | Ceramic capacitor .10 μF 630 V X7R 10 percent 1812 | 4 | Digikey |
| 11 | 1N4148WTPMSCT-ND | D1A, D1B | Switch diode 100 V 150 mA SOD-123 | 2 | Digikey |
| 12 | B130LAW-FDICT-ND | D2A, D2B | Schottky diode 1 A 30 V SOD-123 | 2 | Digikey |
| 13 | RF071M2SCT-ND | D3A, D3B, D4A, D4B | General-purpose diode 200 V 700 mA PMDU | 4 | Digikey |
| 14 | BAV199-FDICT-ND | D5A, D5B, D6A, D6B | General-purpose diode array 85 V 140 mA SOT- 23-3 | 4 | Digikey |
| 15 | RF071M2SCT-ND | D7A, D7B | General-purpose diode 200 V 700 mA PMDU | 2 | Digikey |
| 16 | IRS20957SPBFTRPBFCT- ND | IC1A, IC1B | IC gate driver | 2 | Digikey |
| 17 | SAM1030-03-ND | J1, J2 | Conn. recept. 6-pos .100 vert. dual | 2 | Digikey |
| | 732-5295-ND | Substitute for J1, J2 | | | |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|-----------------------------------|-------------------------------------|---|----------|----------|
| 18 | SAM1030-04-ND | J3 | Conn. recept. 8-pos .100 vert. dual | 2 | Digikey |
| | 732-5296-ND | Substitute for J3 | | | |
| 19 | MMBT5551-7DICT-ND | Q1A, Q1B | Transistor 160 V 300 mW NPN SMD SOT-23 | 2 | Digikey |
| 20 | MMBT5401DICT-ND | Q2A, Q2B | Transistor 150 V 300 mW PNP SMD SOT-23 | 2 | Digikey |
| 21 | DNP | Q3A, Q3B, Q4A, Q4B | NM | 4 | Digikey |
| 22 | DNP | Q5A, Q5B, Q6A, Q6B | NM | 4 | Digikey |
| 23 | IGT40R070D1 | Q7A, Q7B, Q8A, Q8B | 400 V CoolGaN™ TOLL | 4 | Infineon |
| 24 | P100KACT-ND | R1A, R1B, R3A, R3B, R5A, R5B | Resistor 100 kΩ 1/8 W 5 percent 0805 SMD | 6 | Digikey |
| 25 | P0.0ACT-ND | R2A, R2B, R21A, R21B, R22A, R22B | Resistor 0.0 Ω 1/8 W 5 percent 0805 SMD | 6 | Digikey |
| 26 | P10KACT-ND | R4A, R4B, R16A, R16B | Resistor 10K 1 Ω 8 W 5 percent 0805 SMD | 4 | Digikey |
| 27 | 2019- RK73H1JTTD1002FCT- ND | R28A, R28B, R29A, R29B | Resistor 10 K Ω 1/10 W 1 percent 00603 SMD | 4 | Digikey |
| 28 | P100ACT-ND | R6A, R6B | Resistor 100 Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 29 | P1.0KACT-ND | R7A, R7B | Resistor 1.0 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 30 | RHM6.2KCPCT-ND | R8A, R8B | Resistor 6.2 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 31 | P4.7KACT-ND | R9A, R9B | Resistor 4.7 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 32 | P4.7KACT-ND | R10A, R10B | Resistor 4.7 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 33 | 311-18.0KCRCT-ND | R11A, R11B | Resistor 18 kΩ 1/4 W 5 percent 1206 SMD | 2 | Digikey |
| 34 | P10ACT-ND | R13A, R13B | Resistor 10 Ω 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 35 | P4.7ACT-ND | R14A, R14B | Resistor 4.7 Ω 1/8 W 5 percent 0805 | 2 | Digikey |
| 36 | P33KACT-ND | R15A, R15B | Resistor 33 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 37 | RHM6.2KCPCT-ND | R17A, R17B | Resistor 6.2 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 38 | 541-4143-6-ND | R18A, R18B | Resistor 3.3 kΩ 1/8 W 5 percent 0805 SMD | 2 | Digikey |
| 39 | DNP | R19A, R19B, R20A, R20B | NM | 4 | Digikey |

Bill of Materials (BOM)

| No. | Part number | Designator | Description | Quantity | Vendor |
|-----|---------------------|------------------------|--|----------|---------|
| 40 | 311-560HRCT-ND | R23A, R23B, R25A, R25B | Resistor SMD 560 Ω 1 percent 0.1 W 0603 | 4 | Digikey |
| 41 | 311-15GRCT-ND | R24A, R24B, R26A, R26B | Resistor SMD 15 Ω 1 percent 1/10 W 0603 | 4 | Digikey |
| 42 | RMCF0805FT5R10CT-ND | R27A, R27B | Resistor SMD 5.1 Ω 1 percent 1/8 W 0805 | 2 | Digikey |
| 43 | RMCF1206ZT0R00CT-ND | R30A, R30B | Resistor SMD 0.0 Ω jumper 1/4 W 1206 | 2 | Digikey |
| 44 | P0.0GCT-ND | R31A, R31B, R32A, R32B | Resistor 0 Ω 0603 | 4 | Digikey |
| 45 | 490-6993-1-ND | RpA, RpB | Thermistors PTC temp. prot. 90°C | 2 | Digikey |
| 46 | MMSZ5242BT1GOSCT-ND | Z1A, Z1B | Zener diode 12 V 500 mW SOD-123 | 2 | Digikey |

Table 11 Mechanical BOM

| No. | Part number | Description | Quantity | Vendor |
|-----|--------------|--|----------|---------------------|
| 1 | BER229-ND | Thermal pad 8 x 16 x 0.080 inch GP1500 | | Digikey |
| 2 | DCC5837U-18B | Heatsink 57.9 x 36.8 x 17.8 mm | 1 | Alpha Novatech Inc. |
| 3 | S001YZ1H | PIP 3.175 x 8.5 [TH] | 4 | Alpha Novatech Inc. |
| 4 | S001YJ1D | Spring | 4 | Alpha Novatech Inc. |

Revision history**Revision history**

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| V 1.0 | 2020-03-19 | First release |
| | | |
| | | |

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Edition 2020-03-19

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

UM_1904_PL88_1910_133036

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