AN-EVAL 2x8-ISO1I813T

ISOFACE™ Evaluation Board for galvanically isolated 8-Channel Digital Input ICs with IEC61131-2 compatible characteristics for industrial applications

ISO1I813T EVAL - Board

Application Note

V 1.0, 2011-09-09

Industrial & Multimarket

Edition 2011-09-09

Published by
Infineon Technologies AG
81726 Munich, Germany

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1 Introduction

Application

This Application Note describes an Evaluation Board with two isolated 8 Channel IEC61131-2 compatible Digital Input ICs for a wide range of industrial applications.

The board is designed to allow easy exploration of the features of the ISOFACE™ Digital Input part. It contains two ISO1I813T as an electrically isolated 8 bit data input interface in TSSOP-48 package. These parts are used to detect the signal states of up to eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground.

An 8 bit parallel/serial µC compatible interface allows to connect the IC directly to a µC system. The input interface supports also a direct control mode and is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer from input to output side across the galvanic isolation uses Infineon's Coreless Transformer Technology.

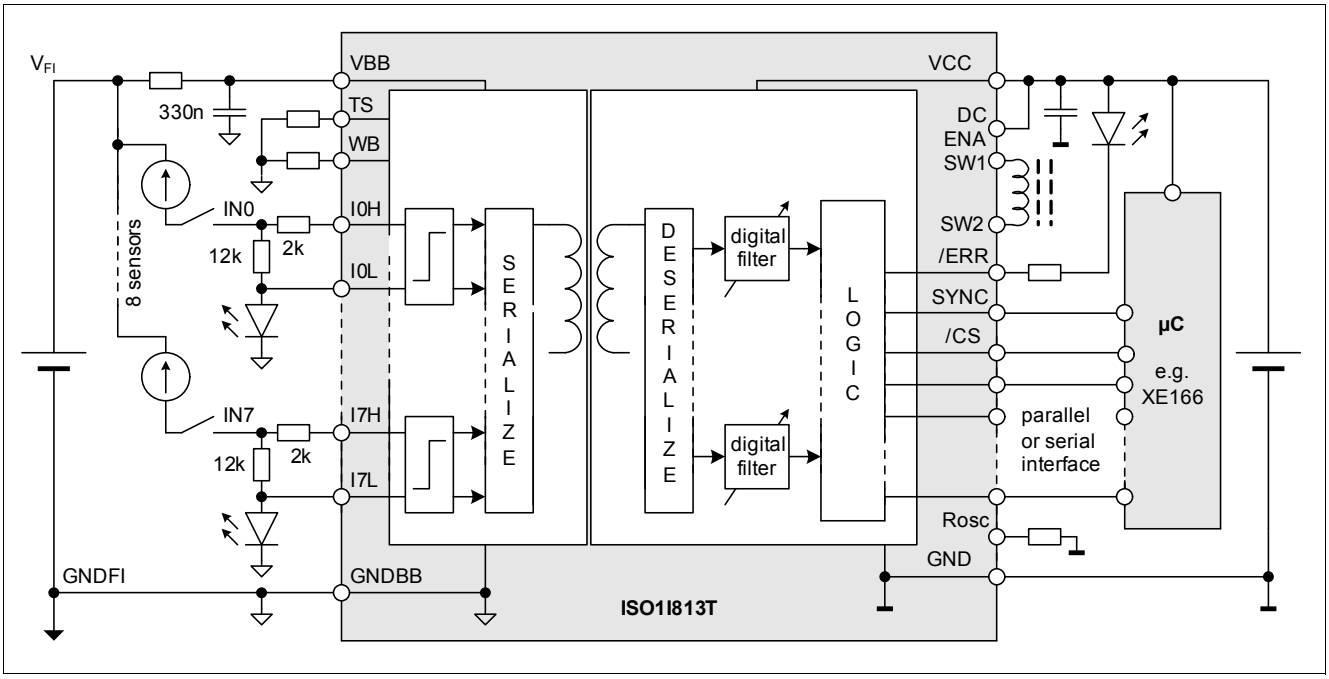


Figure 1 Typical Application

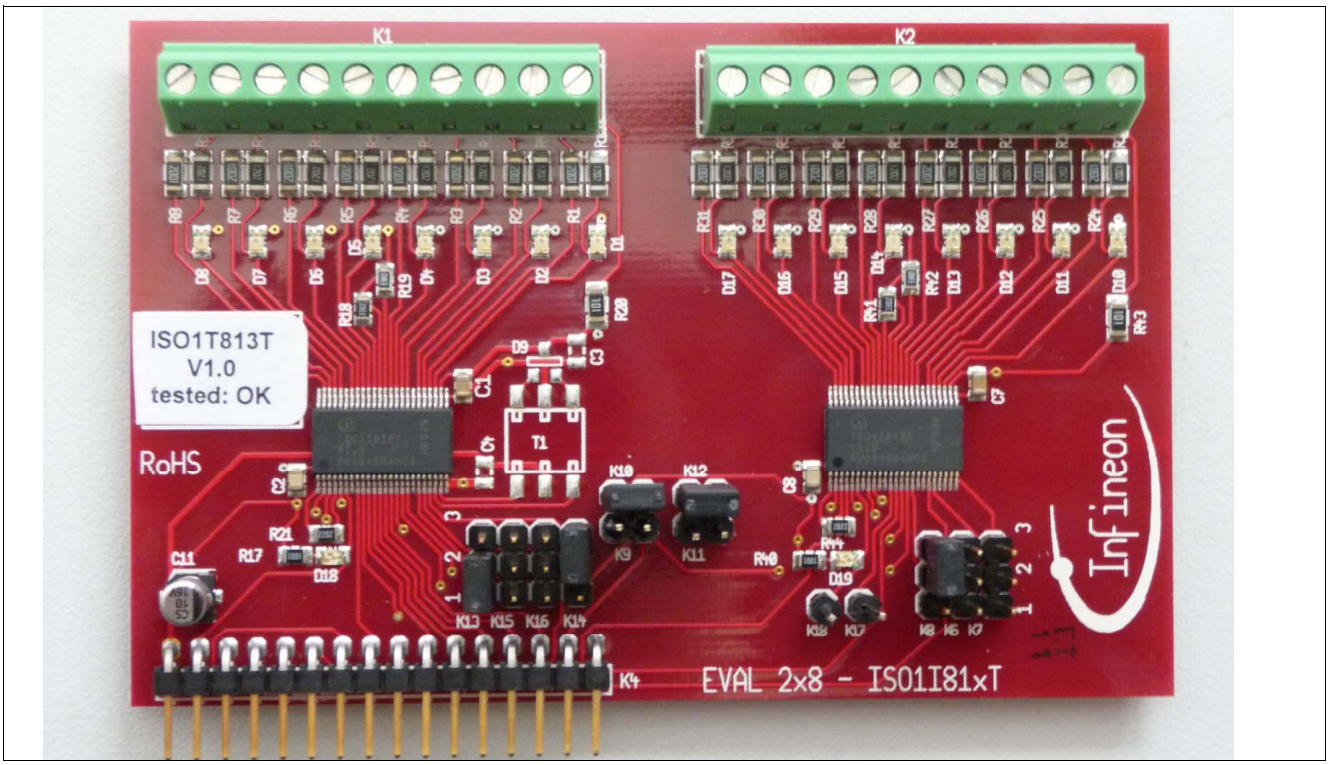


Figure 2 EVAL 2x8-ISO1I813T

2 Board Characteristics

Table 1 Board Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{BB} Input Voltage	V_{BB}	9.6	–	35	V	
VINx Input Voltage	V_{INx}	-35		35	V	
V_{CC} Input Voltage	V_{CC}	3.0	–	5.5	V	
Logic Signals uC Interface	V_{IL}	-0.3	–	0.3 x V_{CC}	V	
	V_{IH}	0.7 x V_{CC}	–	V_{CC} + 0.3 V	V	
Oscillator Frequency		50		500	kHz	set to 500kHz using R_{OSC} 22k

For a complete description of the characteristics of the ISO1I813T please consult respective Data Sheet available at: **www.infineon.com/isoface**

Note: this board is intended to be used in the lab to explore the functionality of the ISO1I813T device. It is not designed to be used in professional applications!

3 Functional Description

This board contains two ISO1I813T as an electrically isolated 8 bit data input interface in TSSOP-48 package. These parts are used to detect the signal states of up to eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground.

For operation in accordance with IEC61131-2, it is necessary for the ISO1I813T to be wired with resistors rated R_{IN} and R_{LED}. (it is recommended to use resistors with an accuracy of 2%, in any case < 5% - mandatory, temperature-coefficients < 200ppm are allowed)

A parallel/serial µC compatible interface allows to connect the Board directly to a µC system.

If the parallel interface is used, only IC1 can be operated. In serial mode either IC1 can be used with 8 Bit SPI or IC1 and IC2 can be put into a Daisy Chain configuration with 16 Bit SPI.

The isolated data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

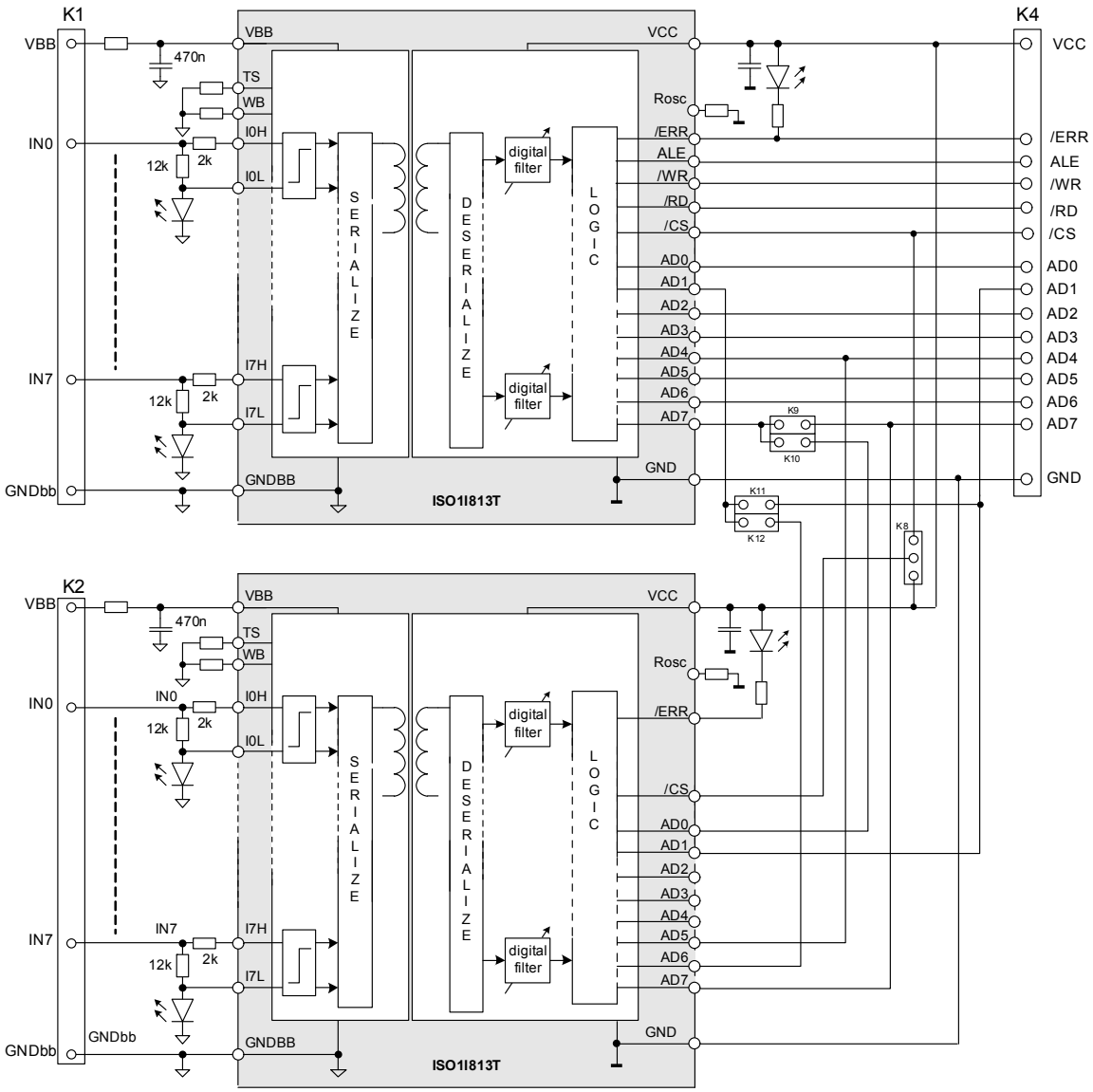


Figure 3 Block Diagram

3.1 Power Supply

The IC contains 2 electrically isolated voltage domains that are independent from each other. The microcontroller interface is supplied via pin VCC and the input stage is supplied via pin VBB. The different voltage domains can be switched on at different time. If the VCC and VBB voltage have reached their operating range and the internal data transmission have been started successfully, the IC indicates the end of the Start-Up procedure by setting the pin /ERR to logic high.

3.2 Oscillator

The frequency of the internal oscillator can be set by the resistor R_{OSC}. This internal oscillator provides the clock for the data sampling and transmission as well as for the digital averaging filter. For adjusting the frequency of the oscillator the values of R_{OSC} can be taken out of the diagram in the ISO1I813T datasheet.

3.3 Parallel Interface

The ISO1I813T contains a parallel interface that can be selected by pulling the pin SEL to logic low state (see also **Table 2**).

This interface can be directly controlled by the microcontroller output signals.

Table 2 Mode Select

Mode	**K13**	**K9**	**K10**	**K11**	**K12**	**K8**
Parallel (IC1)	2 - 3	close	open	close	open	1 - 2
Serial 8 Bit (IC1)	1 - 2	close	open	close	open	1 - 2
Serial 16 Bit	1 - 2	open	close	open	close	2 - 3

3.3.1 µC Control Mode

$\overline{\text{CS}}$ - Chip select. The system microcontroller selects the ISO1I813T by means of the pin $\overline{\text{CS}}$. Whenever the pin is in a logic low state, data can be transferred from or to the µC.

$\overline{\text{RD}}$, **$\overline{\text{WR}}$** (Read / Write) By pulling one of these pins down, a read or write transaction is initiated on the AddressData bus and the data becomes valid. These pins have internal Pull-Up resistors.

ALE (Address Latch Enable) the pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). When ALE is pulled high, addresses are transferred and latched over the bit AD0 to AD7. During the Low State of ALE all read or write transactions hit the same adress. This pin has an internal Pull-Down resistor.

The pins **AD0 .. AD7** are the bidirectional input / outputs for data write and read. Depending on the state of the ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$ pins, register addresses or data can be transferred between the internal registers and e.g. the microcontroller.

The µC Control Mode can be operated by connecting a Processor Board to the corresponding Signals of Connector K4. The timing requirements for the µC Control Mode are shown in **Figure 5**.

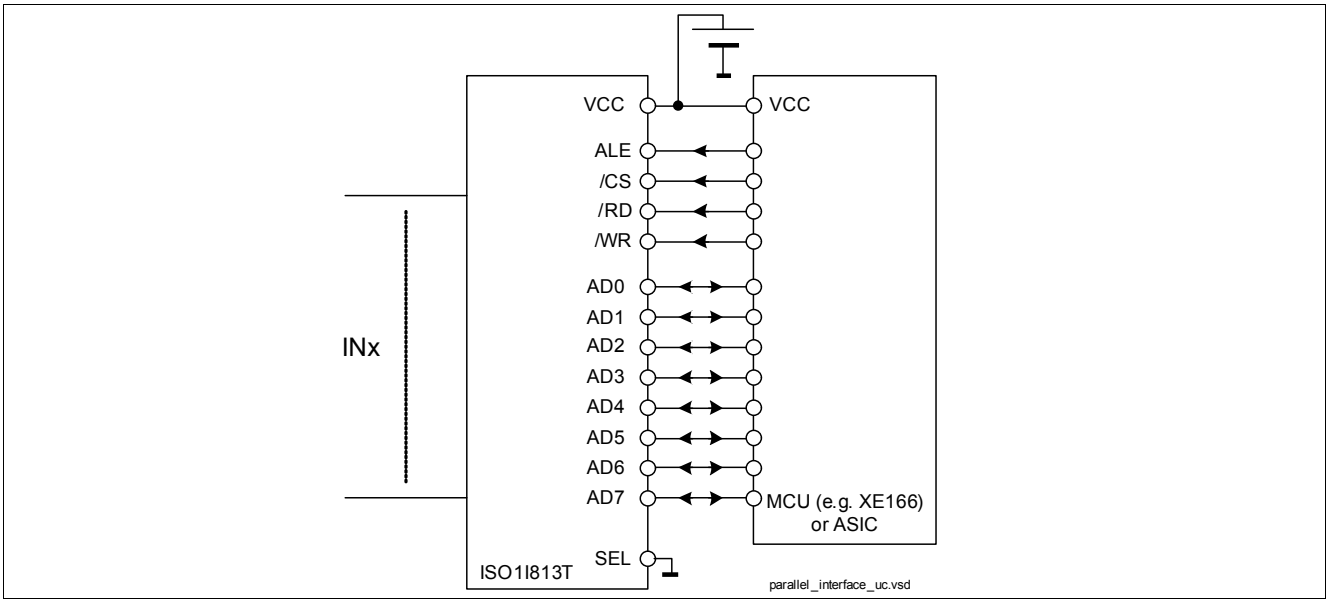


Figure 4 µC Control Mode

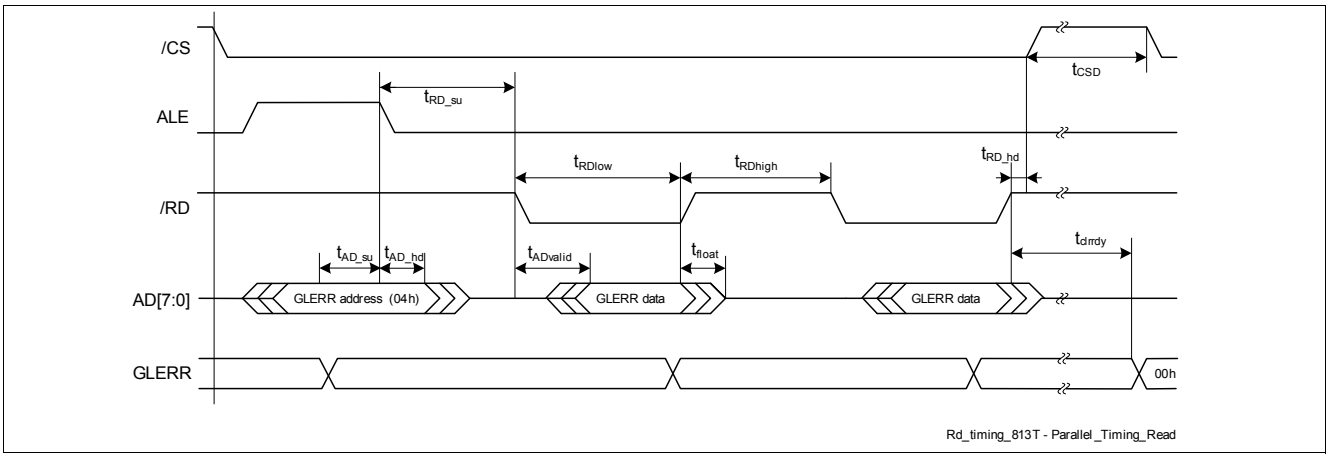


Figure 5 Timing Diagram µC Control Mode Read

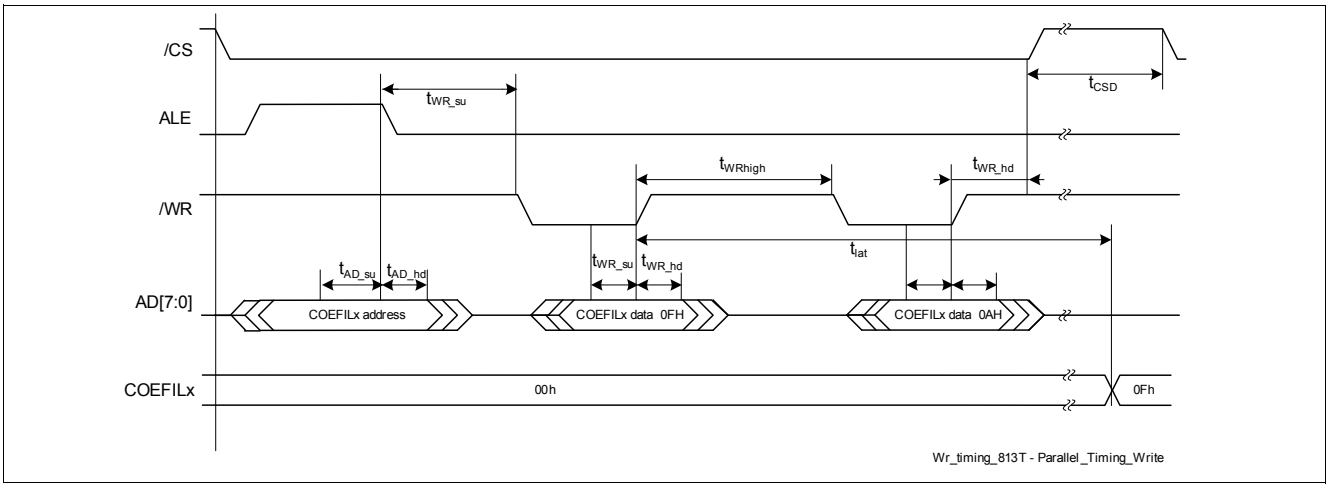


Figure 6 Timing Diagram µC Control Mode Write

3.4 Serial Interface

The ISO1I813T contains two serial interfaces that can be activated by pulling the SEL pin to logic High state. The interface can be directly controlled by the microcontroller output ports. The output pins SDO and SSO are in state “Z” as long as CS=1. Otherwise, the bits are sampled with the falling edge of CS. With every falling edge of SCLK the bits are provided serially to the pin SDO and SSO, respectively. At the same time, the inputs to SDI, SSI are registered into input-FIFO buffers (sampled with the rising edge of SCLK). When all internally sampled bits have been transferred to SDO/SSO, the buffered bits from the inputs SDI/SSI are provided to these pins (daisy-chain support).

The timing requirements for the serial interface are shown in **Figure 8**.

The serial interface can be set to 8 Bit operation by using IC1 only or to 16 Bit operation by using IC1 and IC2 in daisy-chain mode. For this purpose the jumpers K8, K9, K10 have to be set in the according manner (see also **Figure 7**)

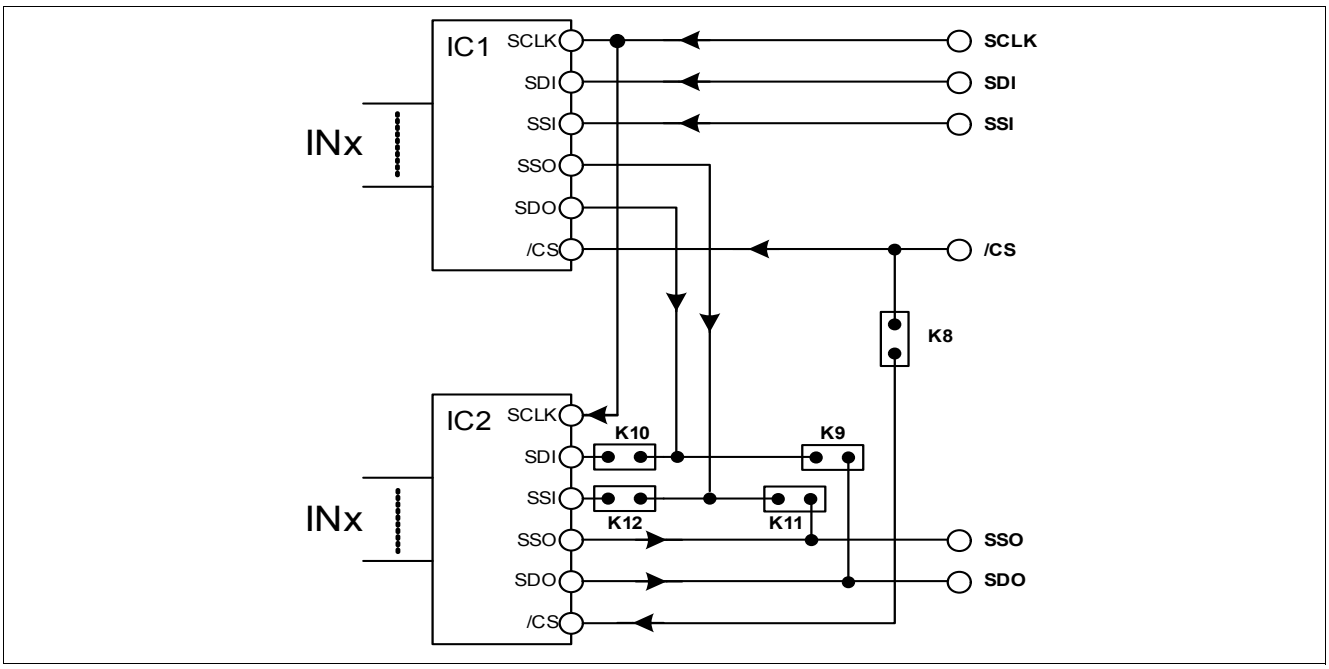


Figure 7 SPI Configuration

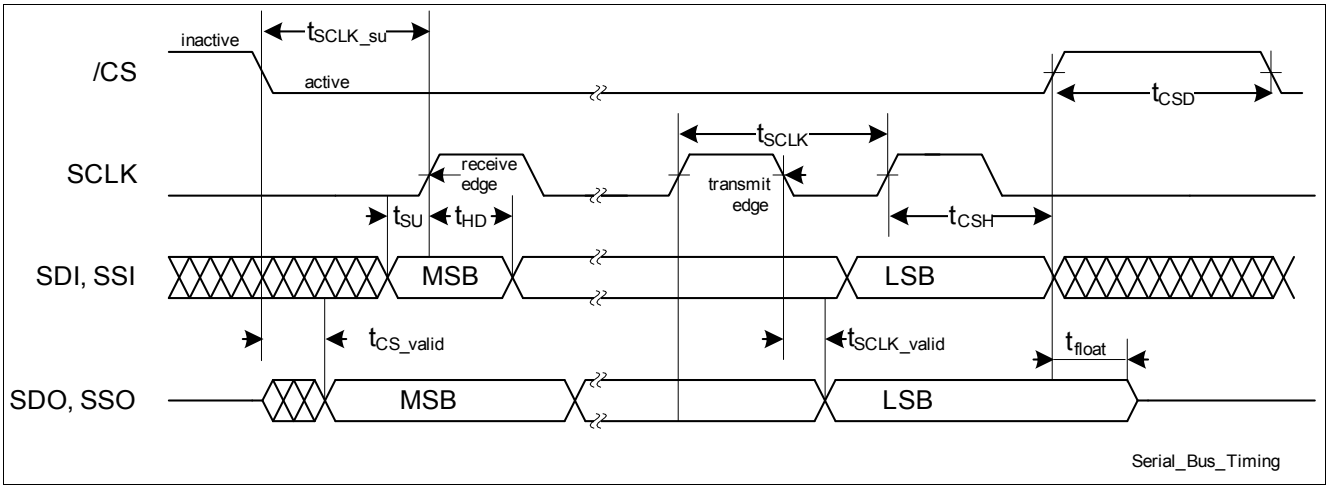


Figure 8 Timing Diagram Serial Mode

3.5 Sensor Input Stage

The sensor input structure is shown in **Figure 9**. Due to its active current a I-V-characteristic as shown in **Figure 10** is maintained. This I-V-curve is well within the IEC 61131 standard requirements of Type 1 and Type 3 sensors, respectively. Type 2 sensors are supported as well with the restriction that 2 input channels have to be used in parallel i.e. only 4 channels are available. Additionally R_{IN} and R_{LED} has to be modified according **Figure 9**. It is recommended to choose for the external resistors R_{IN}, R_{LED} an accuracy of 2 % (< 5% is mandatory) otherwise the I/V-characteristic shown in **Figure 10** cannot be attained. The Input Type 1, 2, 3 can be selected by modifying R_{TS} according **Table 3**.

Table 3 Type Select

Input Characteristic according IEC61131-2	Type 1	Type 2	Type 3
R_{TS}	33R	33k	330k

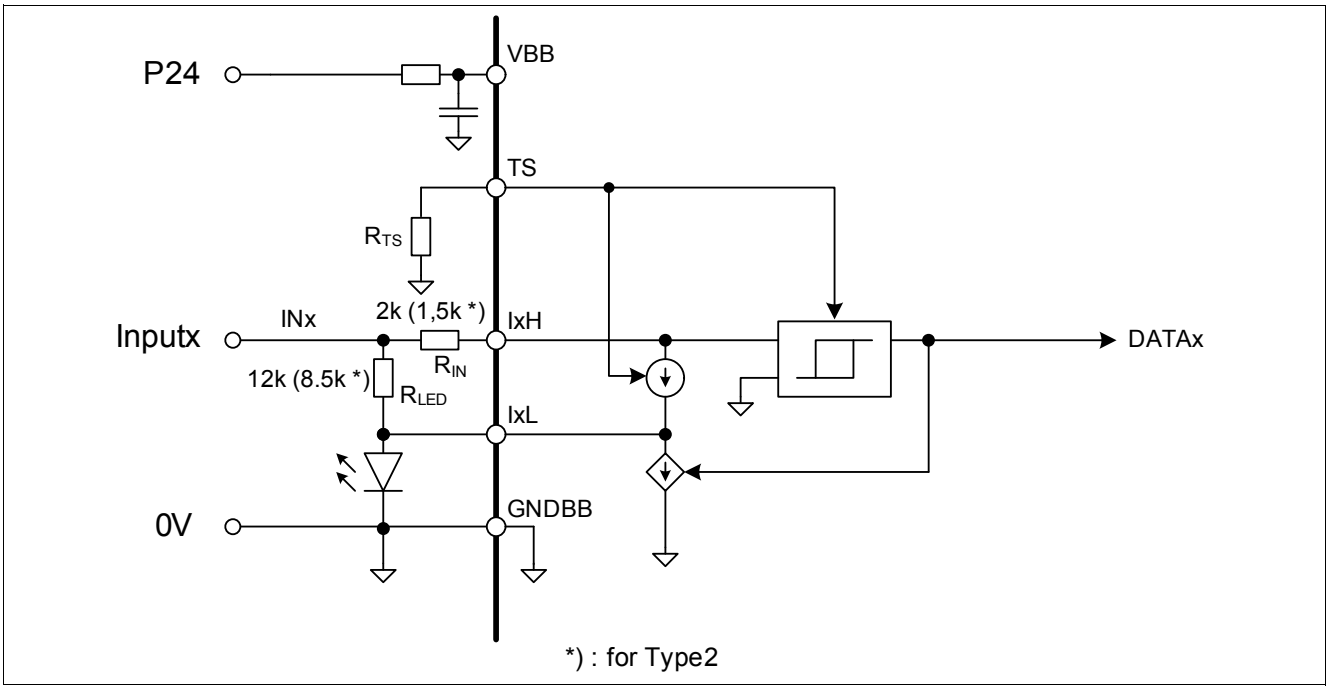


Figure 9 Sensor Input

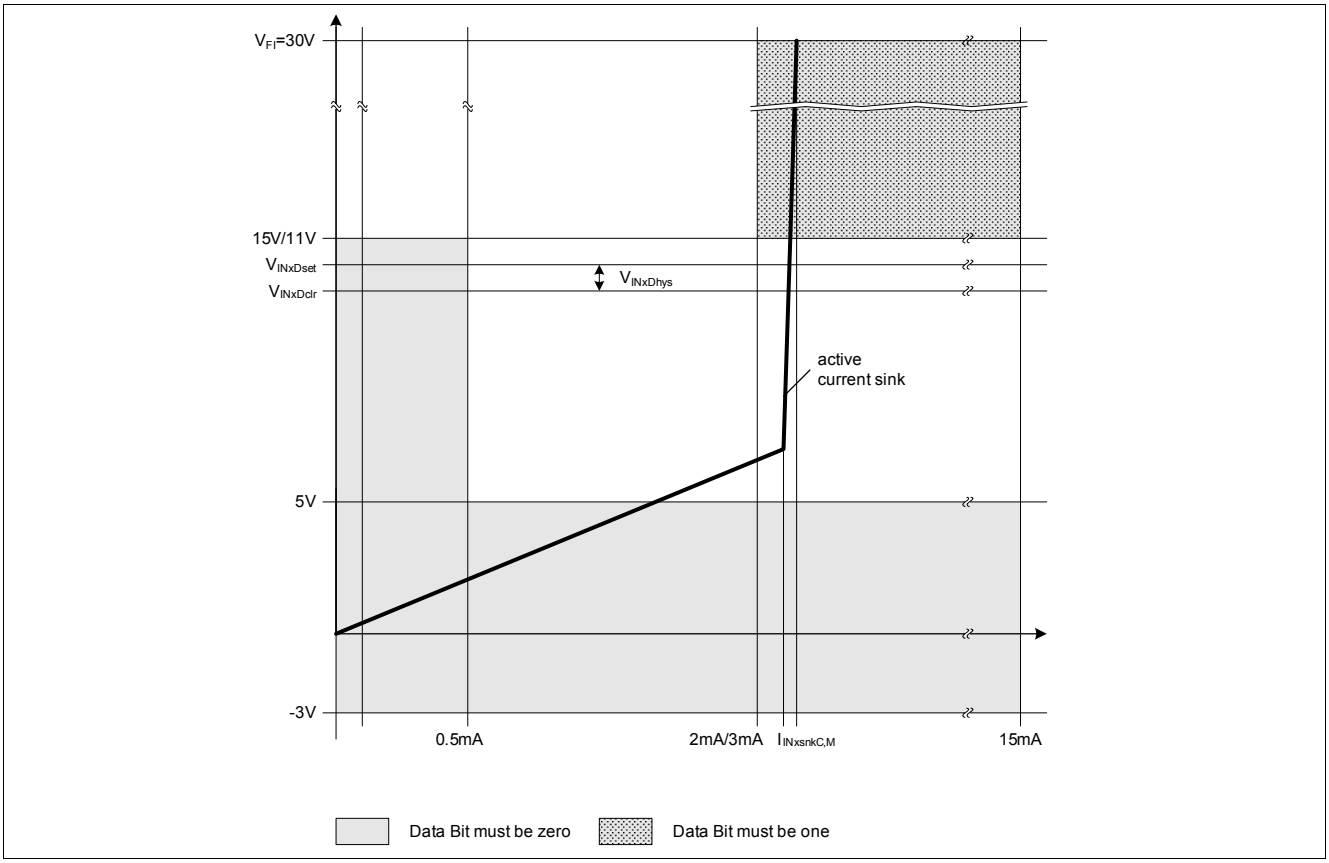


Figure 10 Sensor Input Characteristic

3.6 Wire Break Detection

The wire-break detection current can be adjusted by the R_{WB}-resistor value connected to the pin WB (**Figure 11**). The minimum wirebreak-current can be choosen only when a LED- or Zener-Diode is connected to the pin IxL with a forward current in the range of few uA in the voltage range below 1 V. In the case of a connected resistor at IxL a great current is flowing across the external resistor Rext and the IxL-resistor (R_{LED}). This part cannot be measured internally and has to be added to the internal current part. In this case the minimum adjustable current is 230uA (R_{LED} = 2kOhm). The currently assembled WB resistor of 33kOhm leads to a WB detection limit of 80...160uA for Type 1/3 Sensor Interfaces. The WB bits in the status register have a sticky (latched) property and remains set as long as they are not cleared by a read access and the fault condition is not detected anymore.

In case that a relay contact is connected to the input interface, the contact needs to be bypassed with a resistor to provide the needed WB current

If the wire-break function is not needed, it can be switched off by setting the MWB bit in the registers COEFIL0-7.

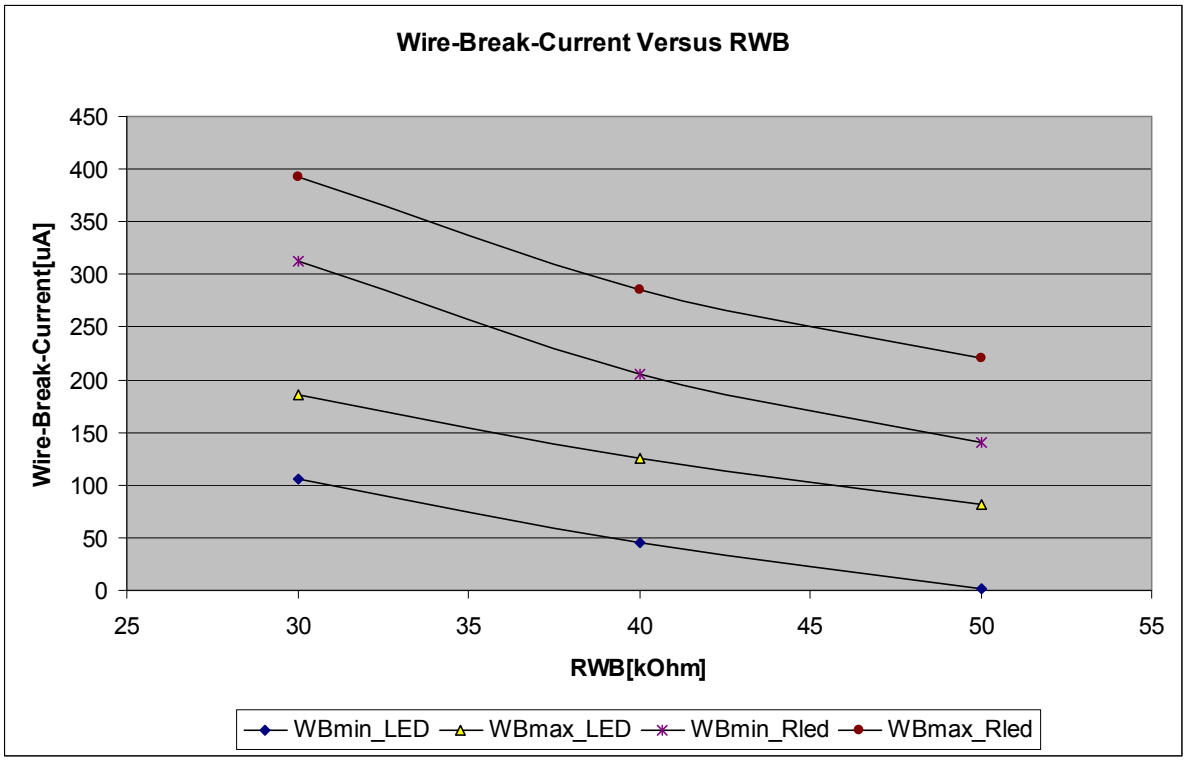


Figure 11 Wire Break Detection for Type 1/3 (typ. @ 25°C)

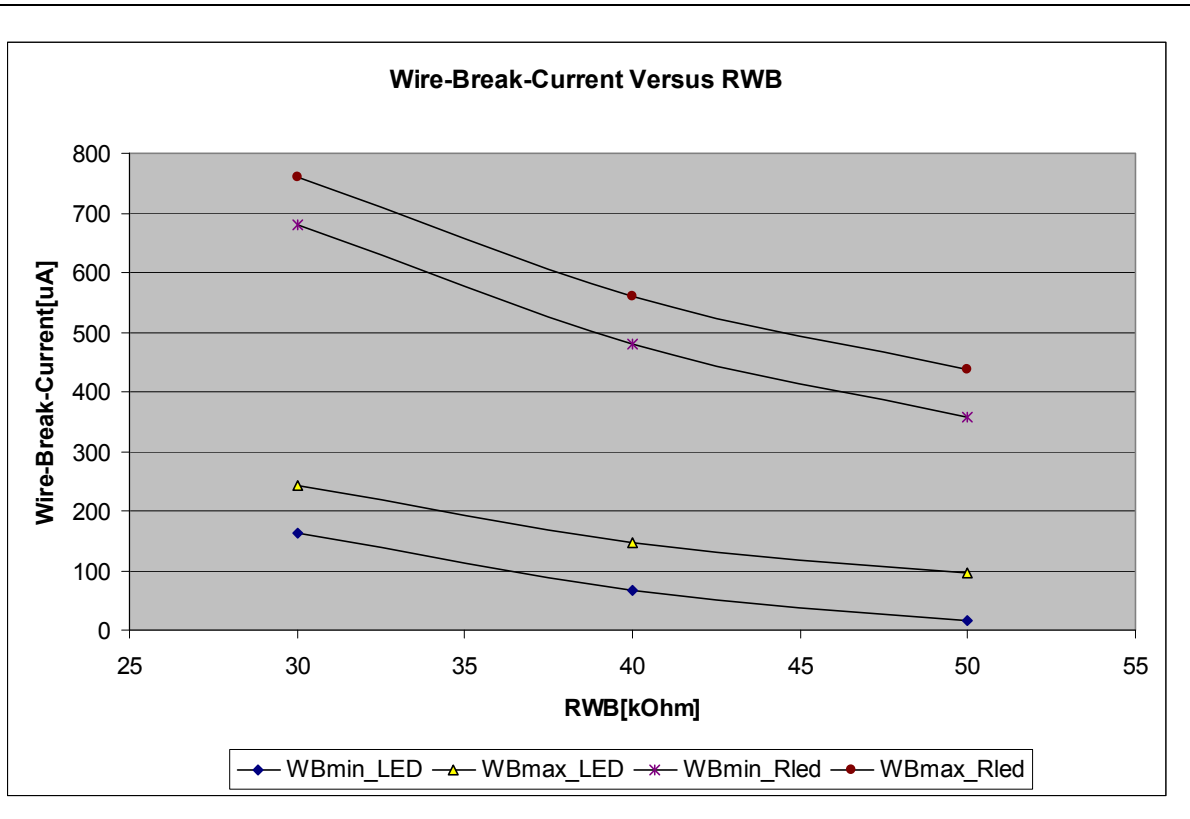


Figure 12 Wire Break Detection for Type 2 (typ. @ 25°C)

In the case of Type 2 two sense inputs need to be switched in parallel to achieve 2 * 3 mA (**Figure 12**). In each sense input a mimimum wirebreak current of 60 uA can be measured which means in sum a minimum wirebreak current of 120 uA. It is not recommended to use external resistors at the pins IxL in case of wirebreak measurements. The recommended value would be R_{LED} = 1.2 kOhm which has been choosen in order not to produce a large voltage drop between IxL and GNDBB which in turn would limit the voltage drop across the sink. But the low value of R_{LED} would cause a high external current in case of wirebreak-measurements which has to be multiplied by two due to the parallel circuitry of the sense inputs.

3.7 Filter Setting

The sensor data bits can be filtered by a configurable digital input filter. If selected, the filter changes its output according to an averaging rule with a selectable average length. When the sensor state changes without any spikes and noise the change is delayed by the averaging length. Sensor spikes that are shorter than the averaging length are suppressed. The averaging length is selected for each channel individually using the configuration registers COEFIL0-7. The programmed filter time apply for both the data and the diagnostics of one channel. See ISO1I813T datasheet for the different setting options including filter bypass. The filters are dimensioned for the nominal internal sampling fscannom. The corresponding filter delays can be adjusted by changing the oscillator frequency i.e. by tuning the resistor at the pin R_{OSC}.

The filters are dimensioned for the nominal internal sampling fscannom. The corresponding filter delays can be adjusted by changing the oscillator frequency i.e. by tuning the resistor at the pin R_{OSC}.

3.8 DC/DC Supply

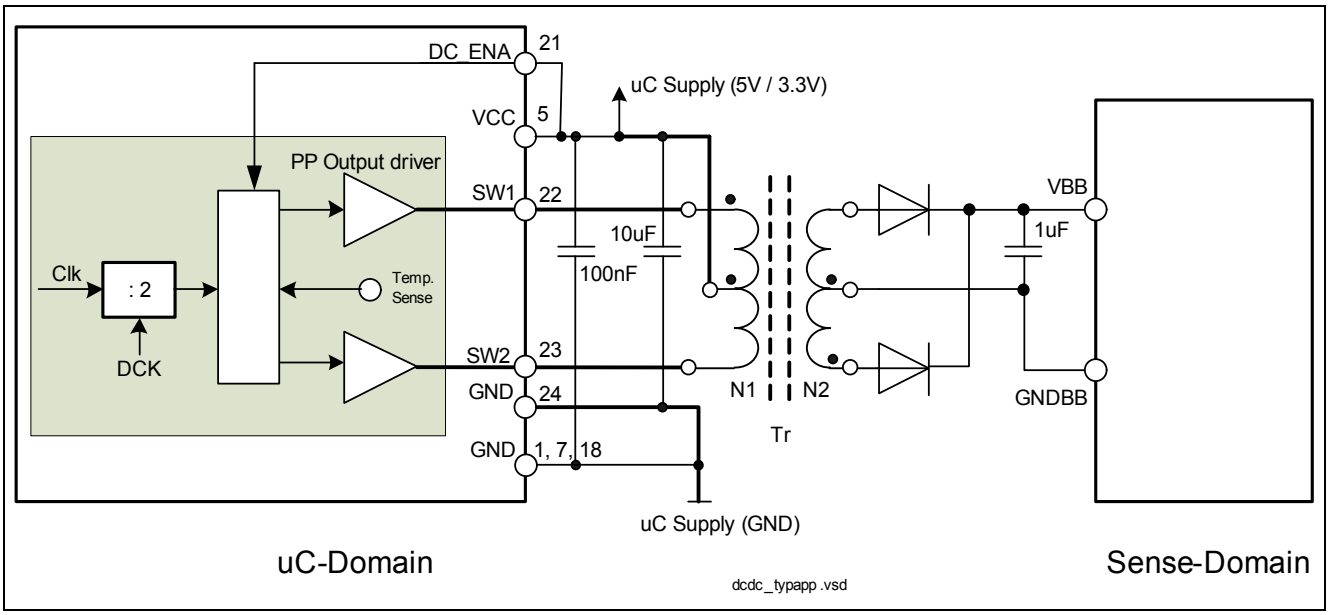


Figure 13 Typical Circuitry for Self Powered Mode with Push-Pull Converter

The IC can as well operate in self powered mode. In this case, the Process Side can be supplied at VBB with an isolated push-pull converter connected to the Micro-controller Side and driven by the pins SW1 and SW2 . The internal driver stage at SW1 and SW2 is designed to power up two ISO1I813T parts. The DC/DC-Converter is driven by the internal clock. Parameters are calculated with the internal clock = 500 kHz. By setting the bit DCK in the GLCFG register a prescaler by 2 can be activated. This may be useful to improve the EMI behaviour. Should the user adjusts another different frequency the transformer has to be adjusted accordingly.

The built in short-circuit protection uses a temperature sensor located close to the drivers (**Figure 13**) and disables the driver stages when a predefined temperature is reached. That means that the drivers are switched off at a temperature of 160 °C and switched on at a temperature of <=150°C

The transformer will be offered by EPCOS as a dedicated product for this ISO1I813T part.

Order number for 3.3V to 12V @ 500kHz: **DS-T7389-51-02** (see also **Chapter 8**).

Special effort have to be spent on a proper layout, in order to minimize the noise caused by the DC/DC converter. As it can be seen in **Figure 13** the current path of the DC/DC converter has to be layouted separately, using the ground pin 24.

Please Note: the transformer as well as the necessary diode and capacitors are not assebled on the board. The recommended parts can be seen in the bill of material (**Chapter 7**).

4 Connectors

Table 4 K1, K2 Connector

Pin Number	K1 (IC1)	K3 (IC2)
1	V_{BB}	V_{BB}
2	Input0	Input0
3	Input1	Input1
4	Input2	Input2
5	Input3	Input3
6	Input4	Input4
7	Input5	Input5
8	Input6	Input6
9	Input7	Input7
10	GND_{BB}	GND_{BB}

Table 5 K4 Connector

Pin Number	Serial Mode	Parallel Mode
1	VCC	VCC
2	$\overline{ERR}$	$\overline{ERR}$
3	SYNC	SYNC
4		$\overline{RD}$
5	DS0	$\overline{WR}$
6	DS1	ALE
7	$\overline{CS}$	$\overline{CS}$
8	SDI	D0
9	SSO	D1
10		D2
11		D3
12	$\overline{CRCERR}$	D4
13	SCLK	D5
14	SSI	D6
15	SDO	D7
16	GND	GND

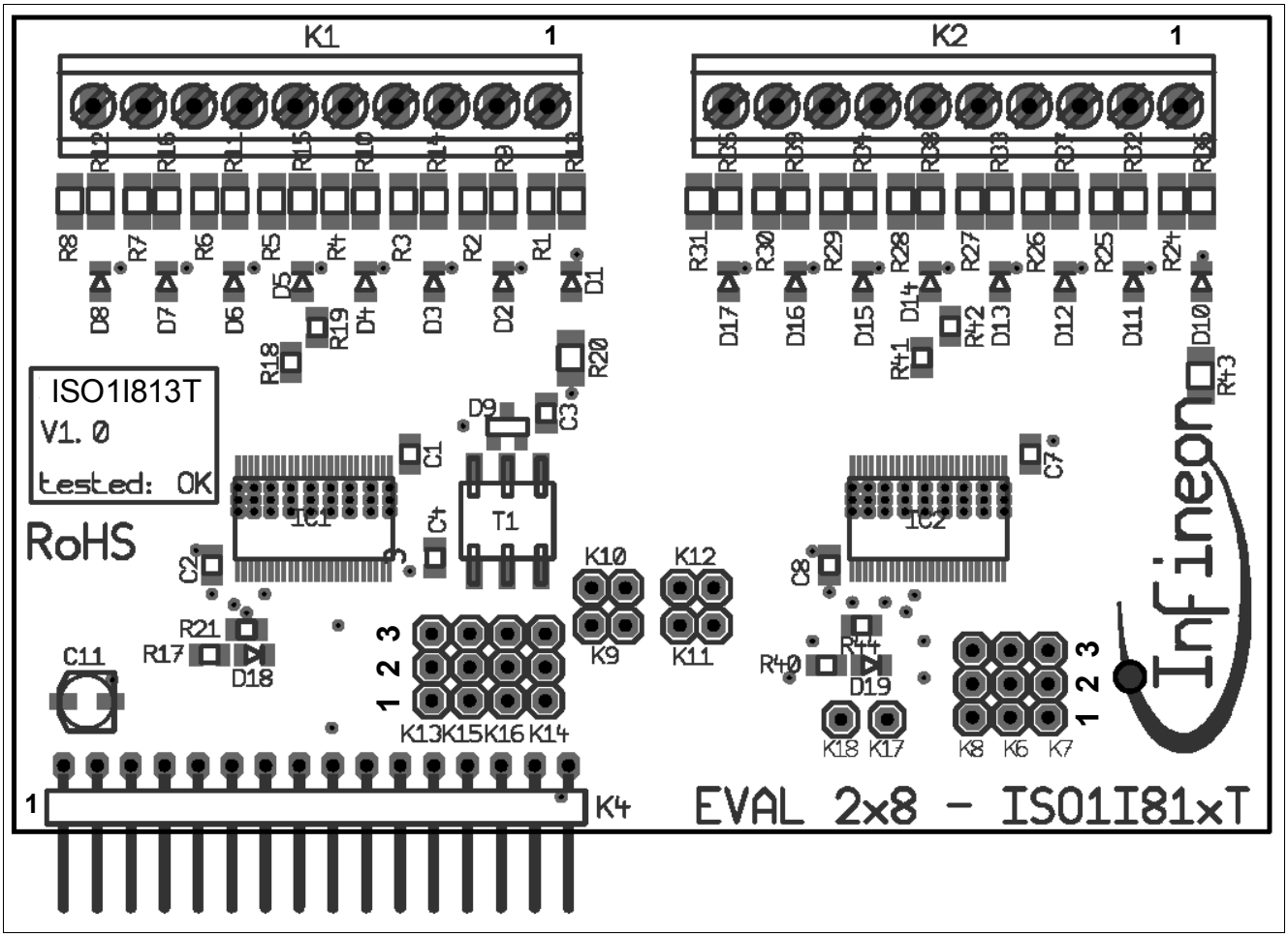


Figure 14 Board Assembly

5 Schematic

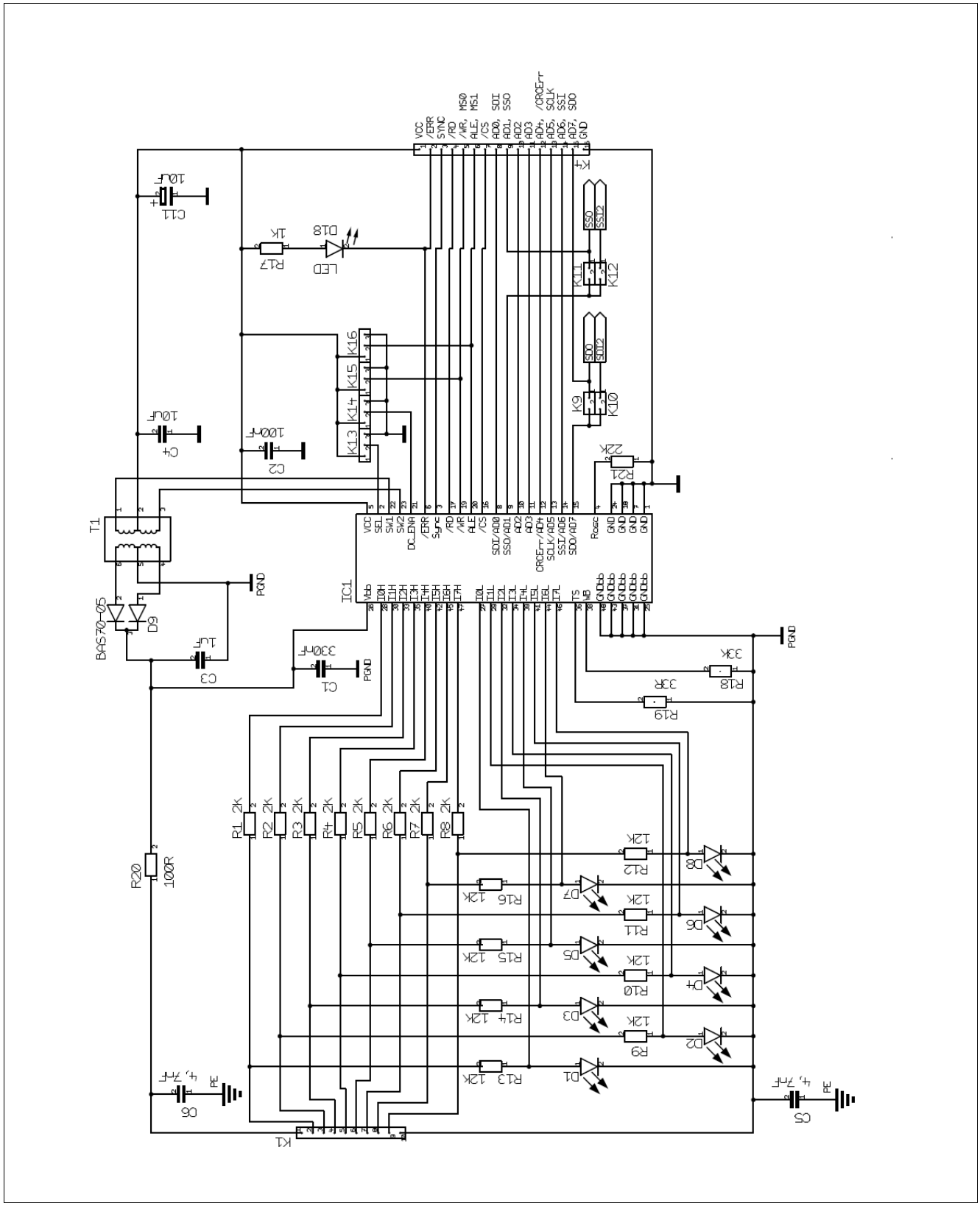


Figure 15 Schematic Page 1

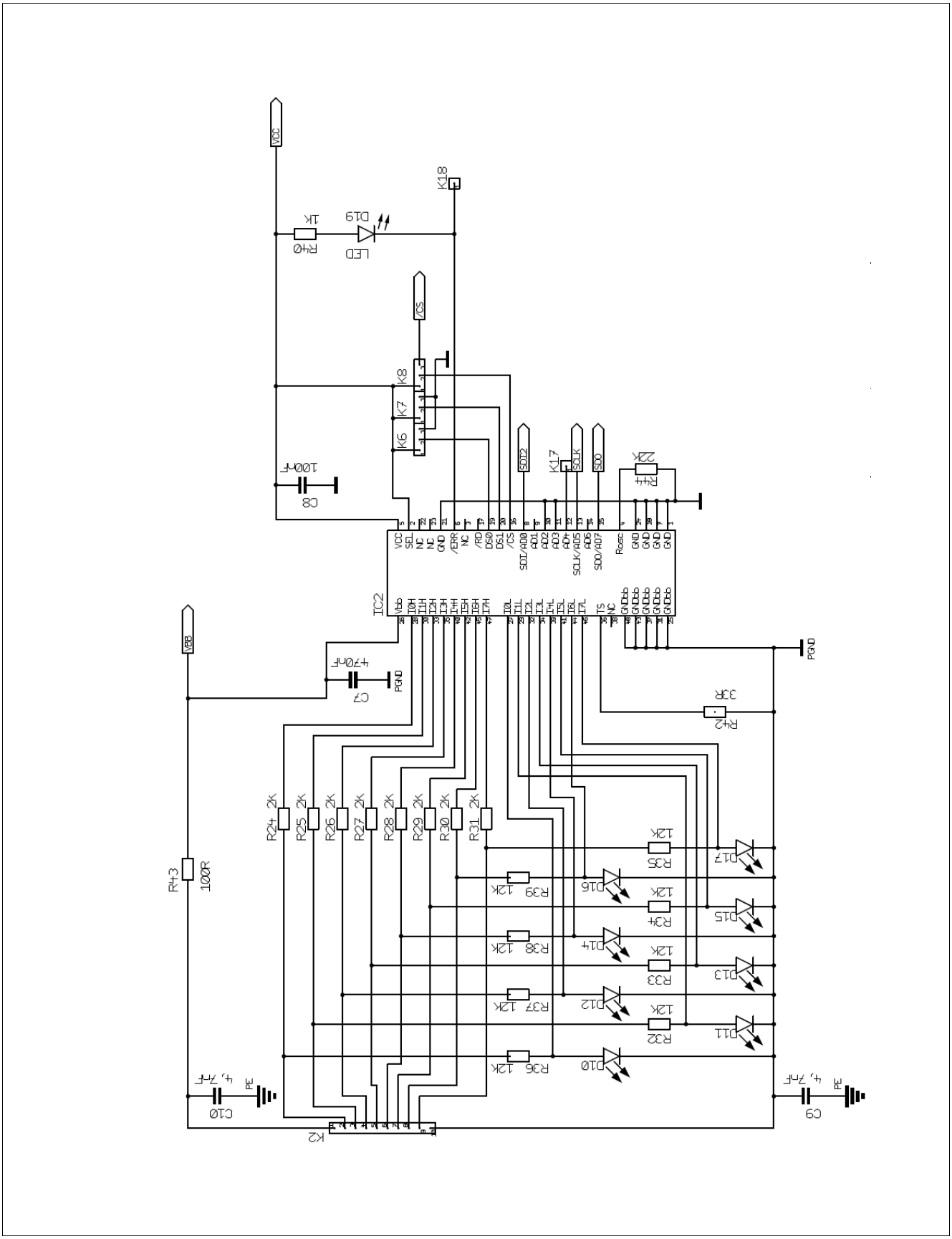


Figure 16 Schematic Page 2

6 PCB Layout

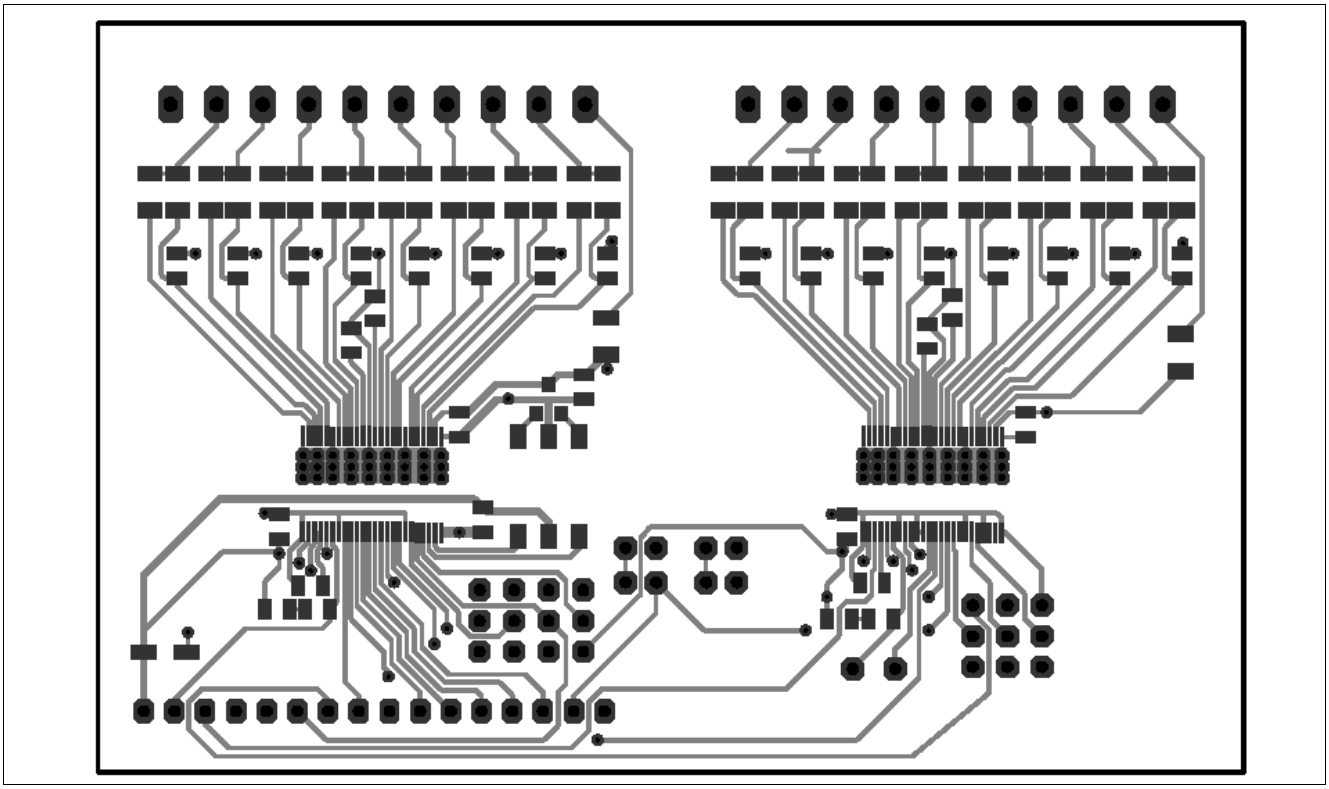


Figure 17 Board Layout - Component Side

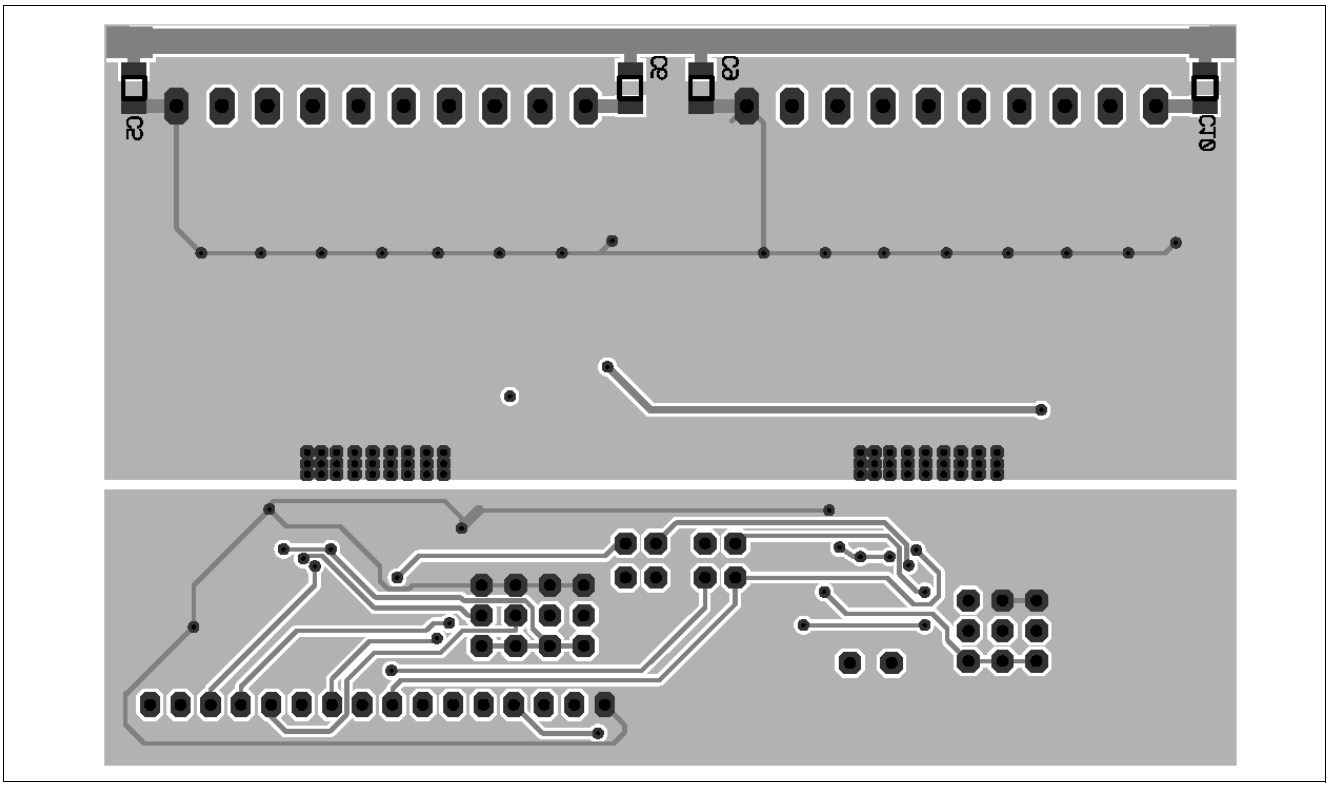


Figure 18 Board Layout - Bottom Side (mirror view)

7 Bill of Material

Nr	Count	Pos.	Value	Package
1	2	C1, C7	470nF, 50V	805
2	1	C11	10uF,10V	C_AL_B
3	2	C2, C8	100nF, 50V	805
4	0	C3	1uF, 50V	805
5	0	C4	10uF, 10V	805
6	4	C5, C6, C9, C10	4,7nF, 500V	1206
7	16	D1, D2, D3, D4, D5, D6, D7, D8, D10, D11, D12, D13, D14, D15, D16, D17	LED, gn KPHCM-2012CGCK	0805-DIODE
8	2	D18, D19	LED, rt KPHCM-2012EC-T	0805-DIODE
9	0	D9	BAS70-05	SOT-23
10	2	IC1, IC2	ISO1I813T	TSSOP48
11	2	K1, K3	MKDS 1/10-3,81	KLEMME_10_3,81
12	4	K9, K10, K11, K12	Connector 2pol	1X02
13	7	K6, K7, K8, K13, K14, K15, K16	Connector 3pol	1X03
14	2	K17, K18	Connector 1pol	1X01
15	1	K4	Connector 16pol	1X16-90
16	16	R1, R2, R3, R4, R5, R6, R7, R8, R24, R25, R26, R27, R28, R29, R30, R31	2k, 1%	1206
17	2	R17, R40	1k	805
18	2	R18, R41	33k	805
19	2	R19, R42	33R	805
20	2	R20, R43	100R	1206
21	2	R21, R44	22k	805
22	16	R9, R10, R11, R12, R13, R14, R15, R16, R32, R33, R34, R35, R36, R37, R38, R39	12k, 1%	1206
23	0	T1	DS-T7389-51-02	E6,3 SMD
24	5		Spacer D8mm , H2,8mm	

8 Transformer

In corporation by courtesy of EPCOS

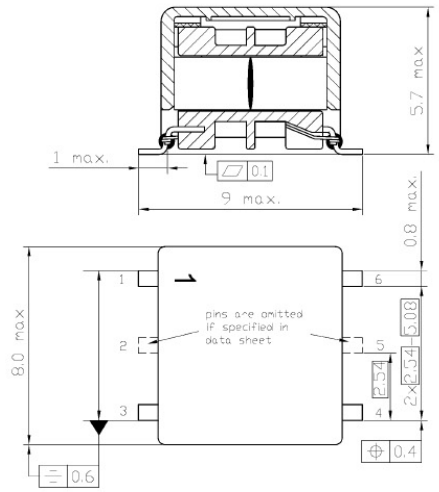
EPCOS

E6.3 Transformer		18.08.2011	T7389/51/02
Preliminary Datasheet	**Engineering samples**	Ordering Code:	

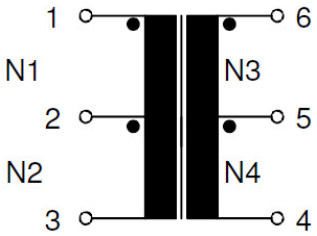
Page 1/3

Spec.: 3.3V prim., 12V sec., 250mW, 500kHz, 500Vrms dielectric strength

Dimensions [mm]:



Schematics:



Marking:

EPCOS
middle block
date code

Electrical Characteristics: (specified @25°C if not mentioned otherwise) *) typical value

All values without tolerances are typical values !

Inductance: L(4-6)	439µH +58/-48%	50 kHz, 100 mV
N1 : N2 : N3 : N4	1 : 1 : 4.25 : 4.25	< 1 turn tolerance
HV: N1, N2 against N3, N4	500 Vrms	50Hz, 1s

Packaging:

Blistertape

Packaging unit: 900 Pcs

Operating Temperature Range: -25 - +125°C

References

[1] ISO1I813T, Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics, Data Sheet, Infineon Technologies

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