

MOSFET

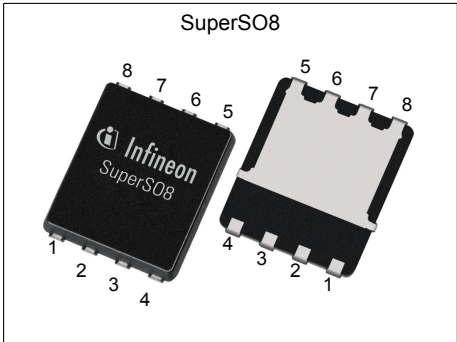
OptiMOS™ 3 Power-Transistor, 40 V

Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant;
- Halogen-free according to IEC61249-2-21

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	1.6	mΩ
I_D	100	A



Type / Ordering Code	Package	Marking	Related Links
BSC016N04LS G	PG-TDSON-8	016N04LS	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_J=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	100 100 100 100 31	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Avalanche current, single pulse ⁽³⁾	I_{AS}	-	-	50	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	295	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	139 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{(1)}$
Operating and storage temperature	T_J , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.9	K/W	-
Device on PCB, 6 cm ² cooling area ⁽¹⁾	R_{thJA}	-	-	50	K/W	-

⁽¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁽²⁾ See figure 3 for more detailed information

⁽³⁾ See figure 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}$, $I_D=85\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.8 1.3	2.3 1.6	m Ω	$V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$
Gate resistance	R_G	-	1.5	-	Ω	-
Transconductance	g_{fs}	95	190	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	8900	12000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	1800	2400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	100	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Rise time	t_r	-	7.6	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	56	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Fall time	t_f	-	9.4	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	25	-	nC	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	14	-	nC	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	11	-	nC	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	23	-	nC	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	113	150	nC	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	54	-	nC	$V_{DD}=20\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	106	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	69	-	nC	$V_{DD}=20\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	100	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.8	1.2	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery charge	Q_{rr}	-	125	-	nC	$V_R=20\text{ V}$, $I_F=I_S$, $di_F/dt=400\text{ A/}\mu\text{s}$

4 Electrical characteristics diagrams

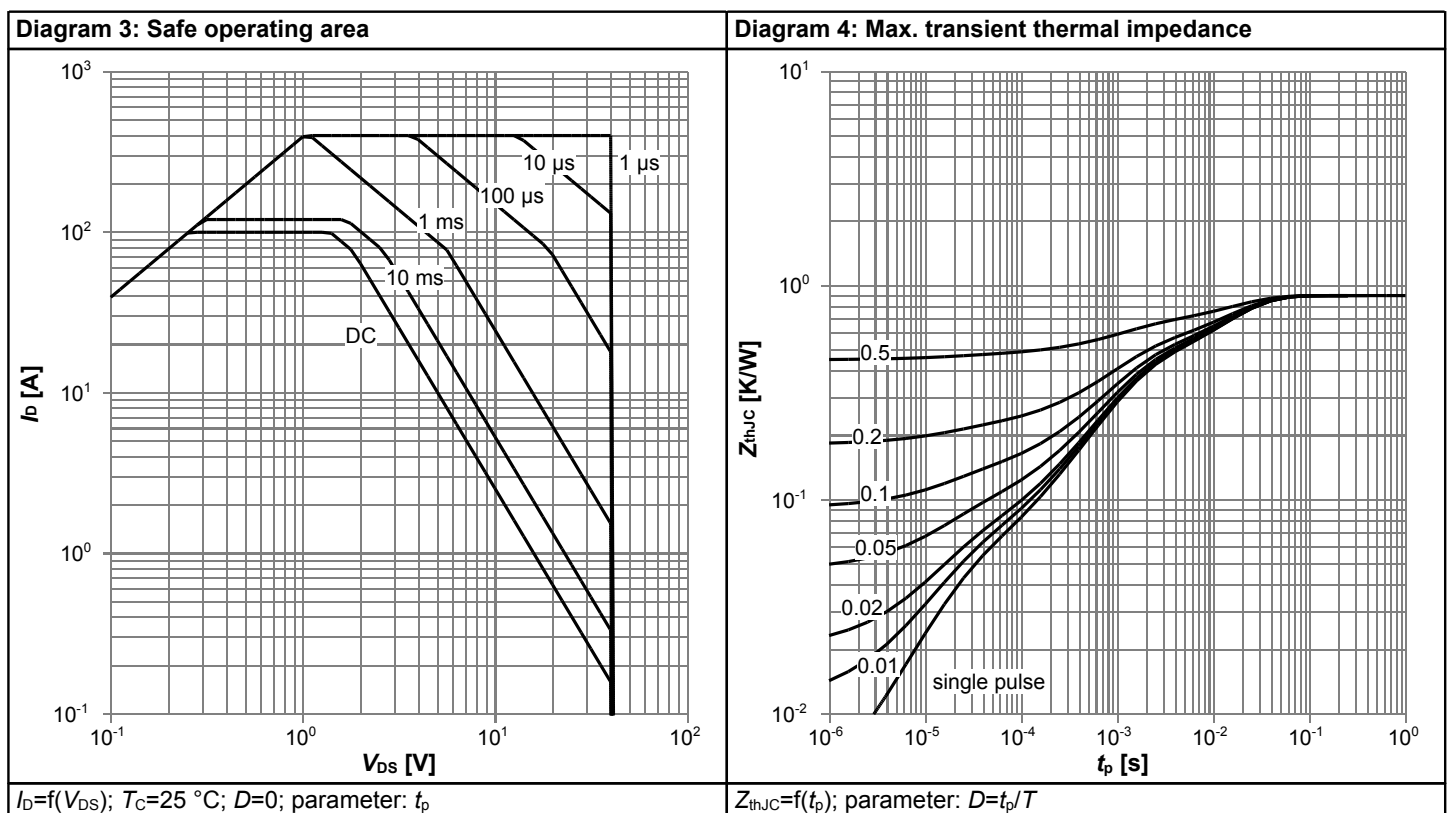
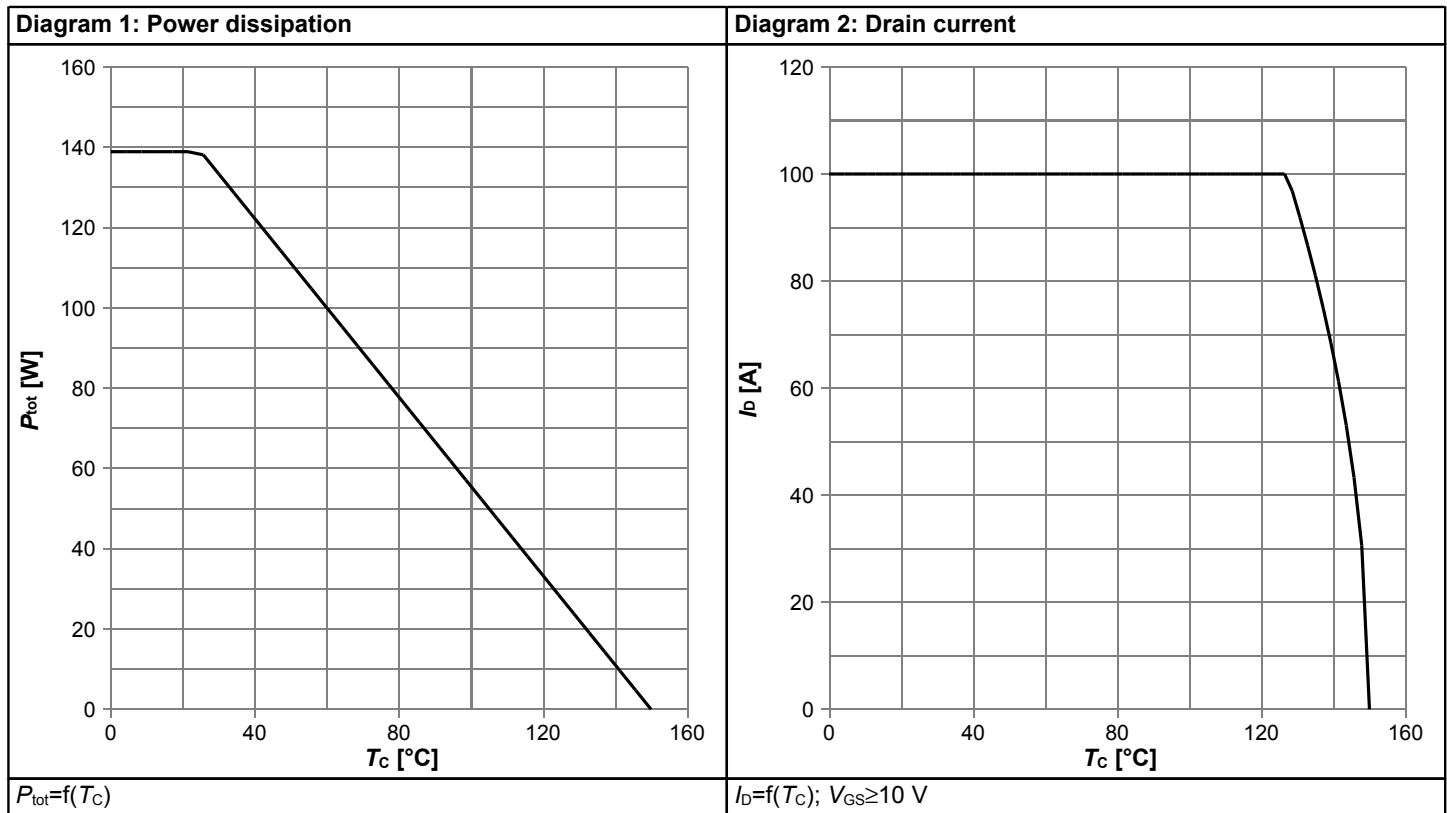
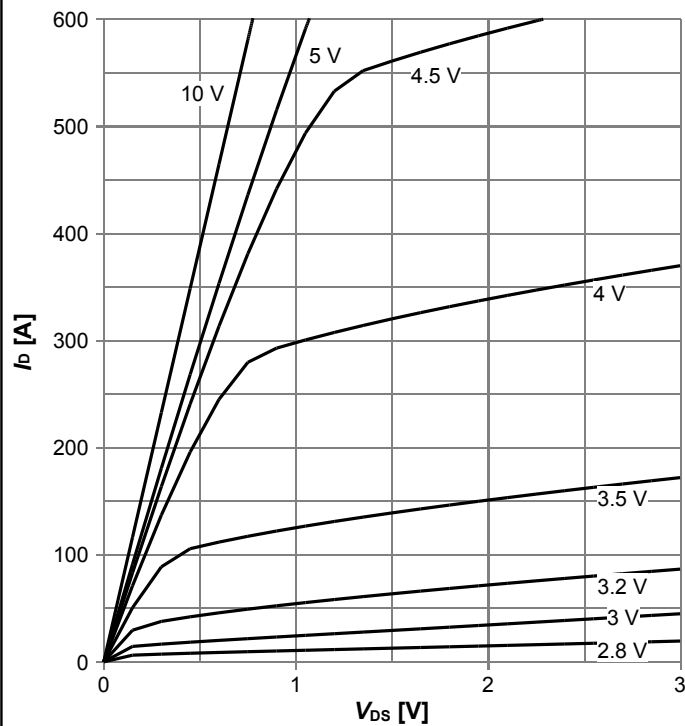
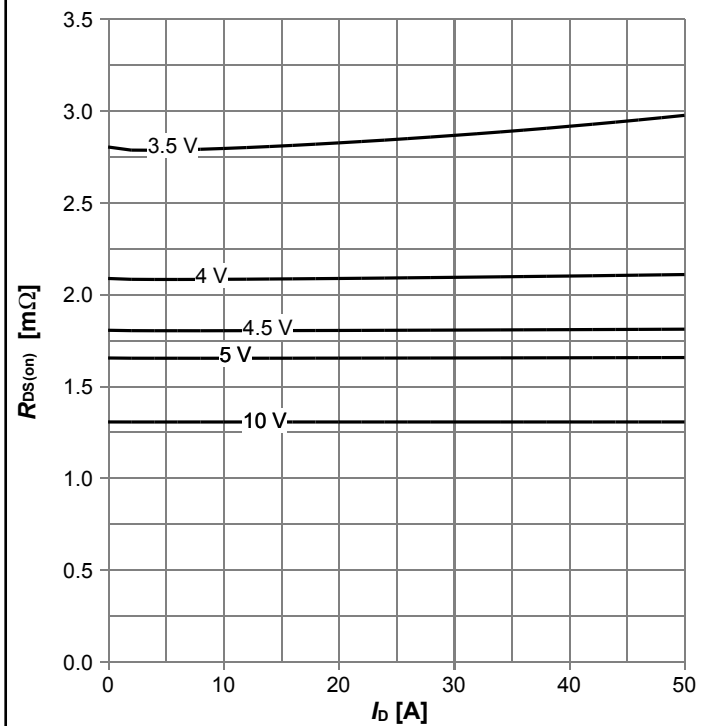


Diagram 5: Typ. output characteristics



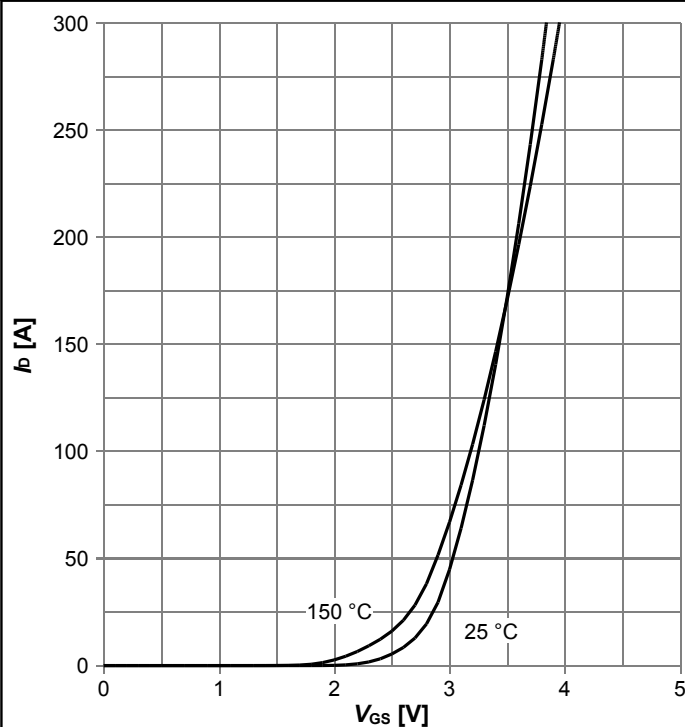
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



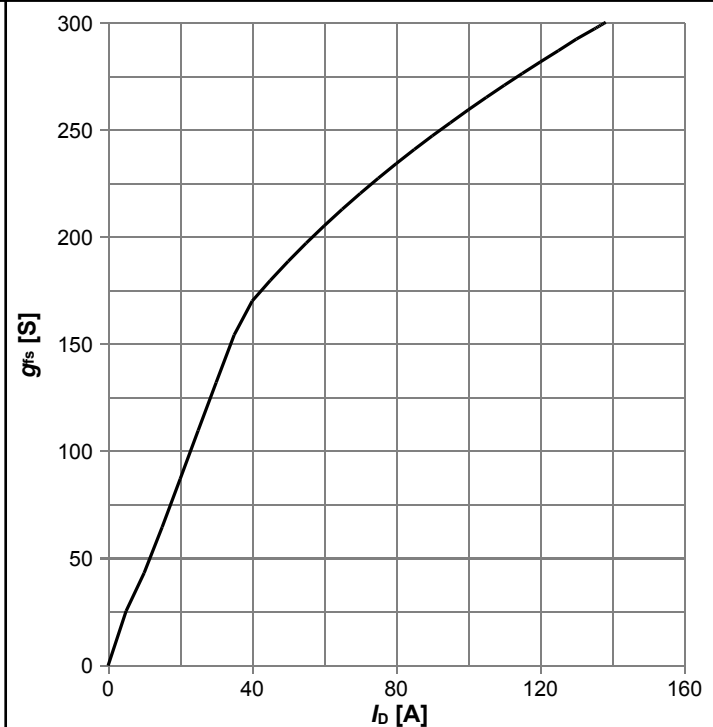
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



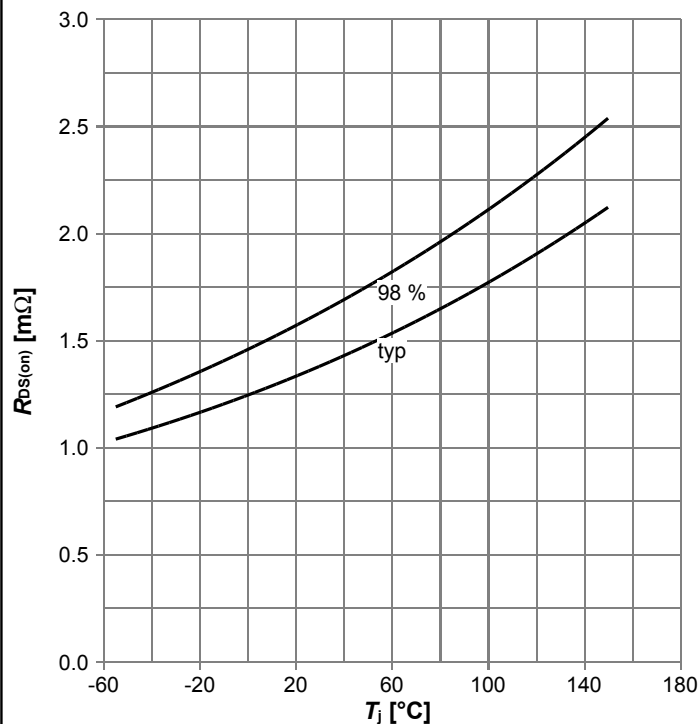
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



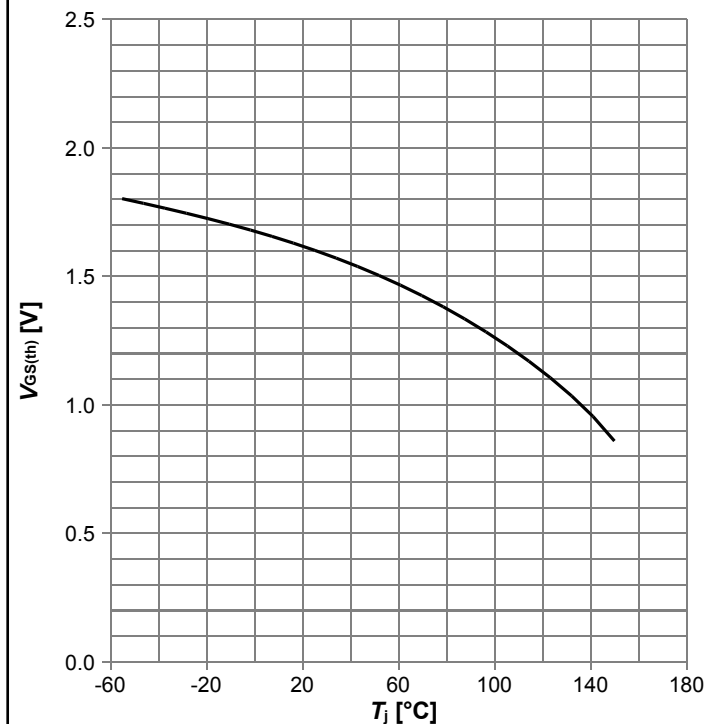
$g_{fs} = f(I_D)$; $T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



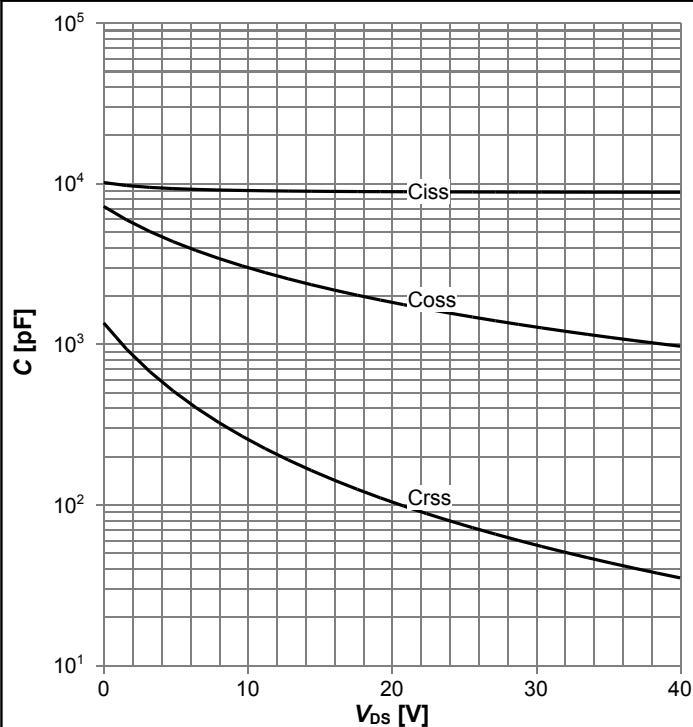
$R_{DS(on)} = f(T_j)$; $I_D = 50$ A; $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



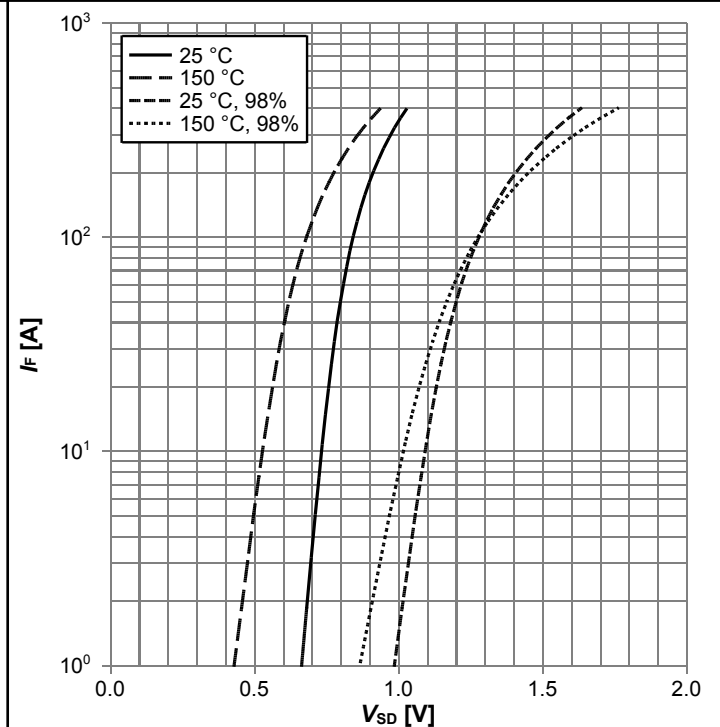
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 85$ μ A

Diagram 11: Typ. capacitances



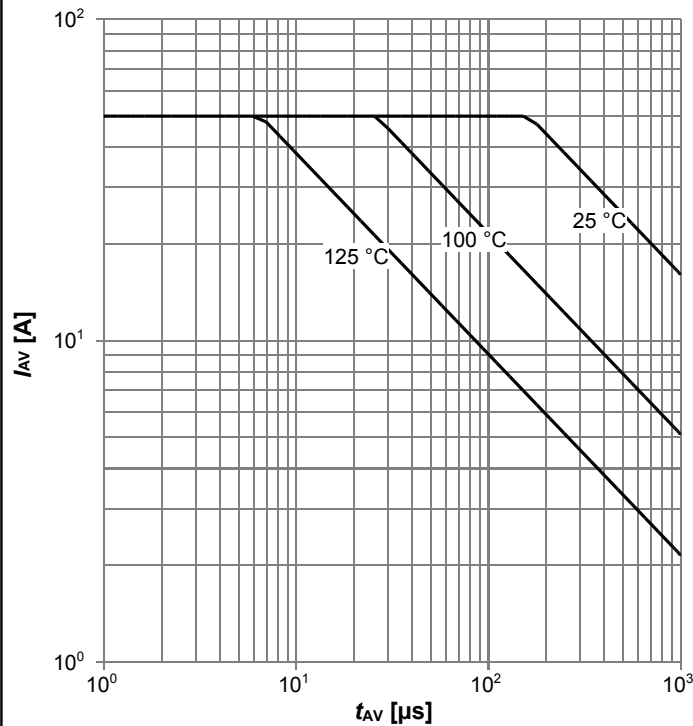
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



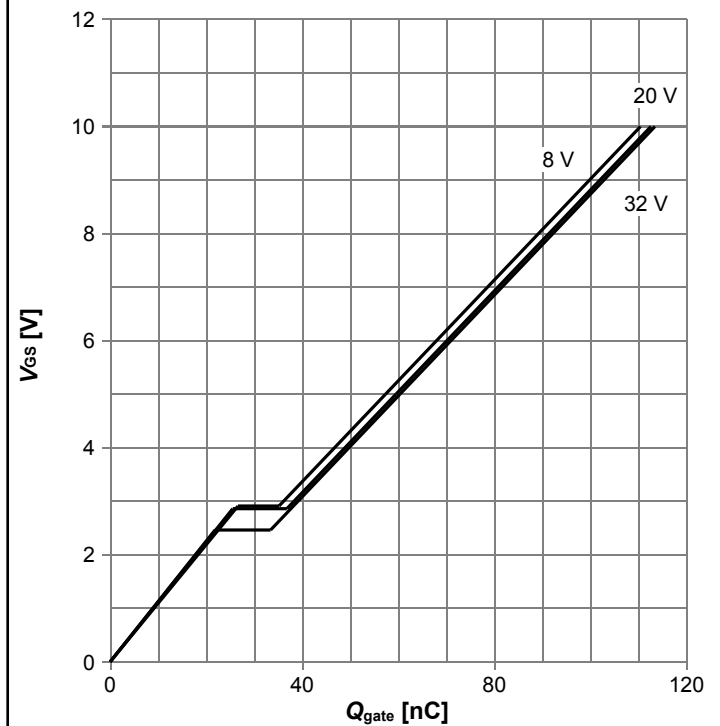
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



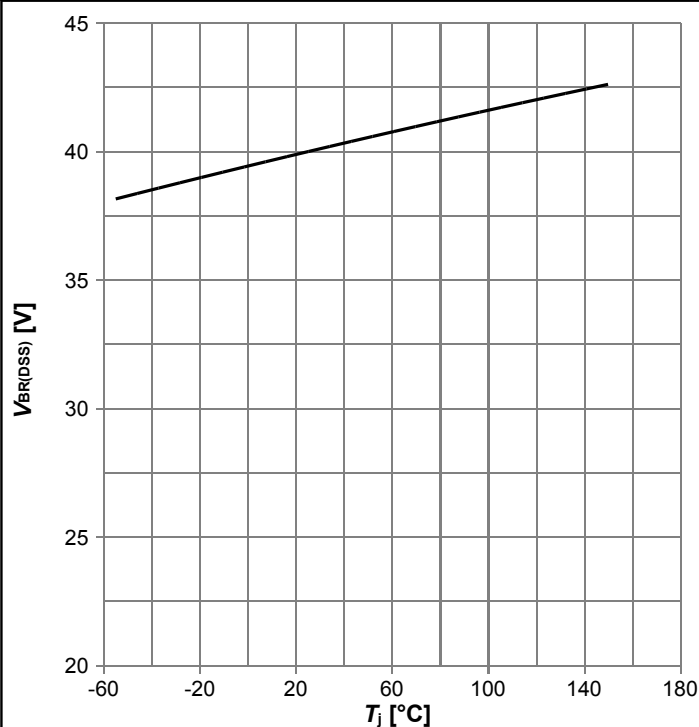
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



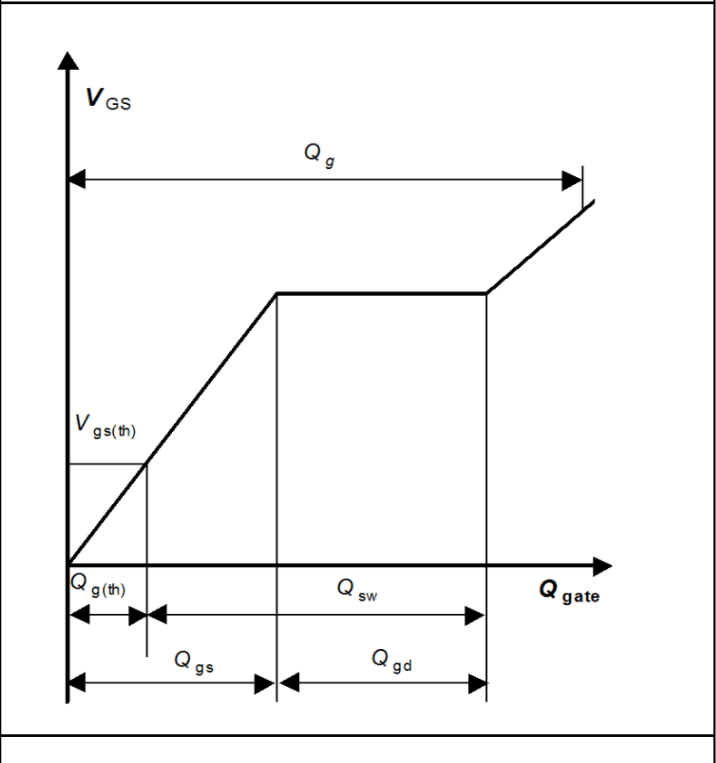
$V_{GS}=f(Q_{gate})$; $I_D=30\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



- 1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

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REVISION 07
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EUROPEAN PROJECTION
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Figure 1 Outline PG-TDSON-8, dimensions in mm

PG-TDSON-8: Recommended Boardpads & Apertures

The drawing illustrates the recommended board pads and apertures for the PG-TDSON-8 package. It includes a top view (left) and a bottom view (right) of the package, showing the copper, solder mask, and stencil apertures. Dimensions are provided in millimeters.

Top View Dimensions:

- Overall width: 1.905
- Overall height: 4.455
- Top pad width: 1.27 (3x)
- Top pad spacing: 0.6
- Top pad thickness: 0.8
- Left pad width: 1.27 (3x)
- Left pad spacing: 0.5
- Left pad thickness: 0.925
- Bottom pad width: 1.27 (3x)
- Bottom pad spacing: 0.5
- Bottom pad thickness: 0.925
- Right pad width: 1.27 (3x)
- Right pad spacing: 0.5
- Right pad thickness: 0.925

Bottom View Dimensions:

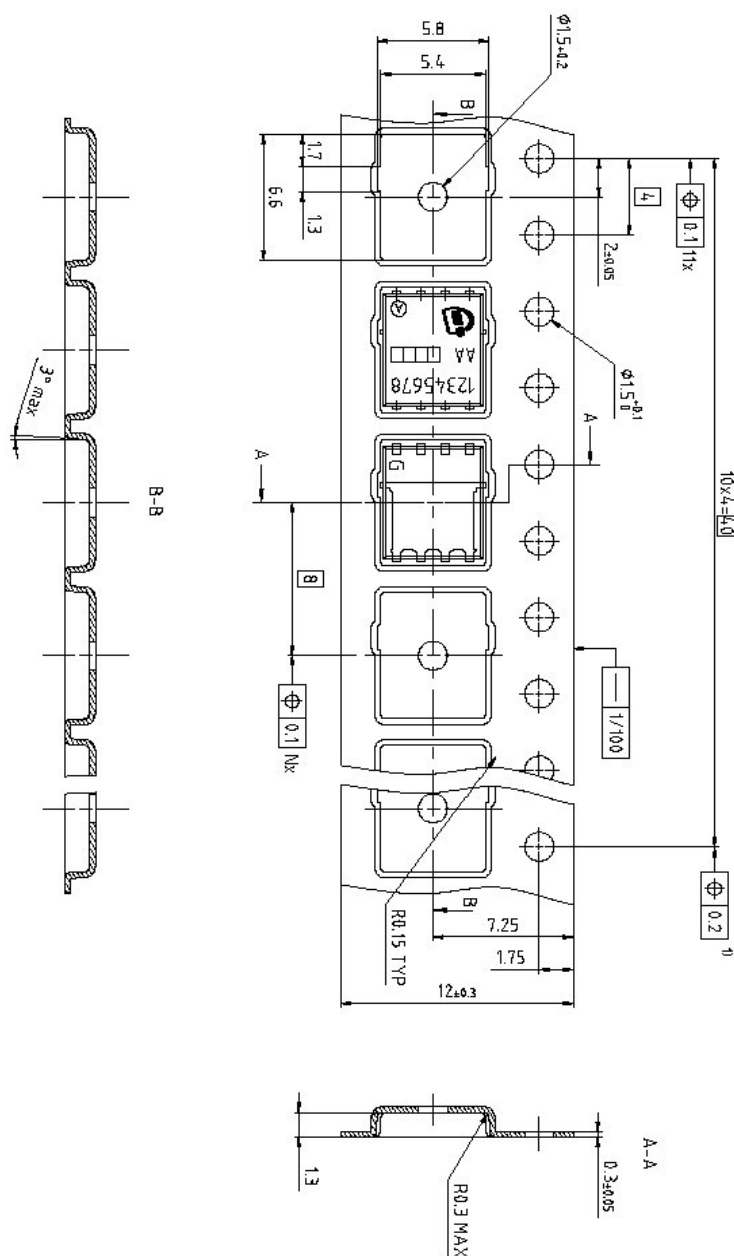
- Overall width: 1.905
- Overall height: 2.9
- Top pad width: 1.27 (3x)
- Top pad spacing: 0.6
- Top pad thickness: 0.8
- Left pad width: 1.27 (3x)
- Left pad spacing: 0.5
- Left pad thickness: 0.925
- Bottom pad width: 1.27 (3x)
- Bottom pad spacing: 0.5
- Bottom pad thickness: 0.925
- Right pad width: 1.27 (3x)
- Right pad spacing: 0.5
- Right pad thickness: 0.925

Legend:

- copper
- solder mask
- stencil apertures

all dimensions in mm

Figure 2 Outline Boardpads (TDSO-8), dimensions in mm



Dimension in mm

Figure 3 Outline Tape (TDSON-8)

Revision History

BSC016N04LS G

Revision: 2020-02-07, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2020-02-07	Update package drawings and footnotes

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