

OptiMOS™3 Power-MOSFET

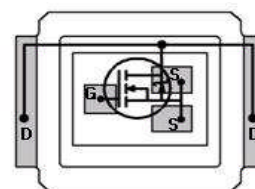
Features

- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- Dual sided cooling
- low parasitic inductance
- Low profile (<0.7mm)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Compatible with DirectFET® package MN footprint and outline²⁾

Product Summary

V_{DS}	80	V
$R_{DS(on),max}$	4.4	mΩ
I_D	90	A

CanPAK™ M
MG-WDSO-2



Type	Package	Outline	Marking
BSB044N08NN3 G	MG-WDSO-2	MN	0208

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$	90	A
		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$	68	
		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=58\text{ K/W}^{2)}$	18	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	360	mJ
Avalanche energy, single pulse	E_{AS}	$I_D=30\text{ A}$, $R_{GS}=25\text{ Ω}$	660	
Gate source voltage	V_{GS}		±20	V

¹⁾ J-STD20 and JESD22

²⁾ DirectFET® is a trademark of International Rectifier Corporation

BSB028N06NN3 G uses DirectFET® technology licensed from International Rectifier Corporation

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	78	W
		$T_A=25\text{ °C}$, $R_{\text{thJA}}=58\text{ K/W}^{(2)}$	2.2	
Operating and storage temperature	T_j, T_{stg}		-40 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	1.0	-	K/W
		top	-	-	1.6	
Device on PCB	R_{thJA}	6 cm ² cooling area ⁽²⁾	-	-	58	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$, $I_{\text{D}}=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=97\text{ }\mu\text{A}$	2	2.8	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=80\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	10	μA
		$V_{\text{DS}}=80\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}$, $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}$, $I_{\text{D}}=30\text{ A}$	-	3.7	4.4	
Gate resistance	R_{G}		-	0.5	-	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$, $I_{\text{D}}=30\text{ A}$	36	72	-	S

⁽²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁽³⁾ See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	4300	5700	pF
Output capacitance	C_{oss}		-	1100	1450	
Reverse transfer capacitance	C_{rss}		-	38	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_G=1.6\ \Omega$	-	14	-	ns
Rise time	t_r		-	9	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	7	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	17	-	nC
Gate to drain charge	Q_{gd}		-	11	-	
Switching charge	Q_{sw}		-	17	-	
Gate charge total	Q_g		-	55	73	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V
Output charge	Q_{oss}	$V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$	-	75	99	

Reverse Diode

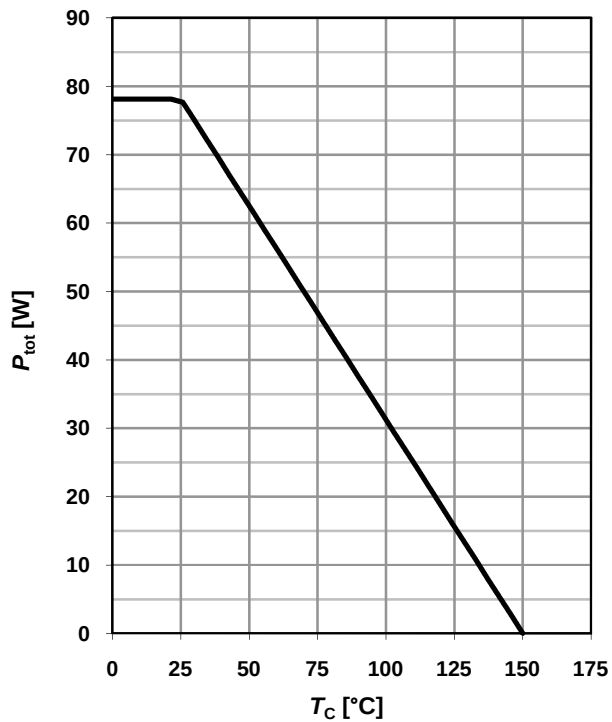
Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	120	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	$V_R=40\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	55	-	ns
Reverse recovery charge	Q_{rr}		-	110	-	nC

⁴⁾ See figure 13 for more detailed information

⁵⁾ See figure 16 for gate charge parameter definition

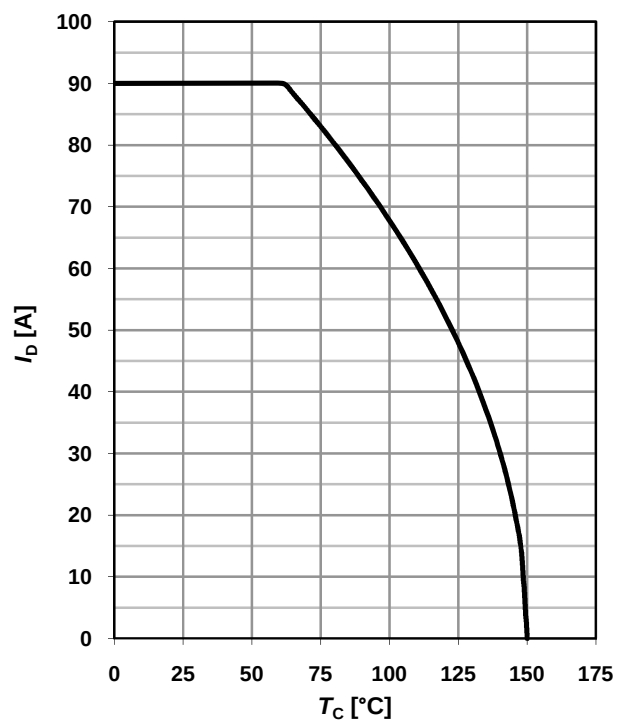
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

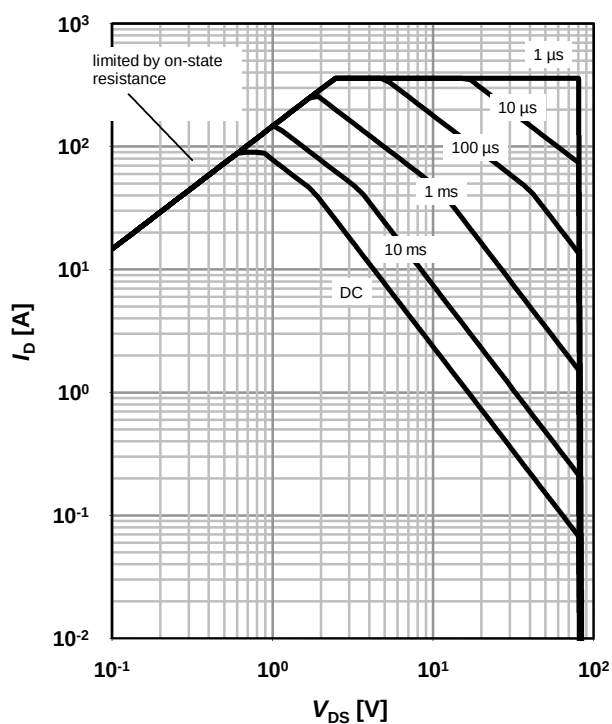
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

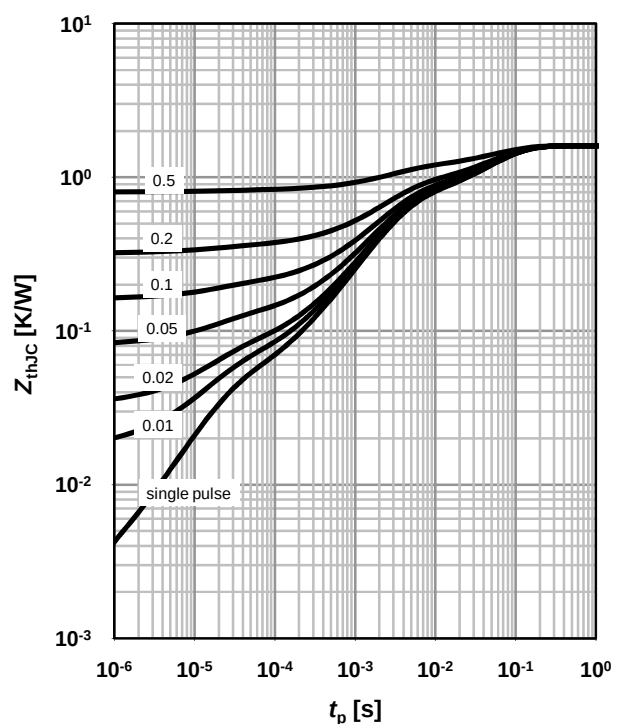
parameter: t_p



4 Max. transient thermal impedance

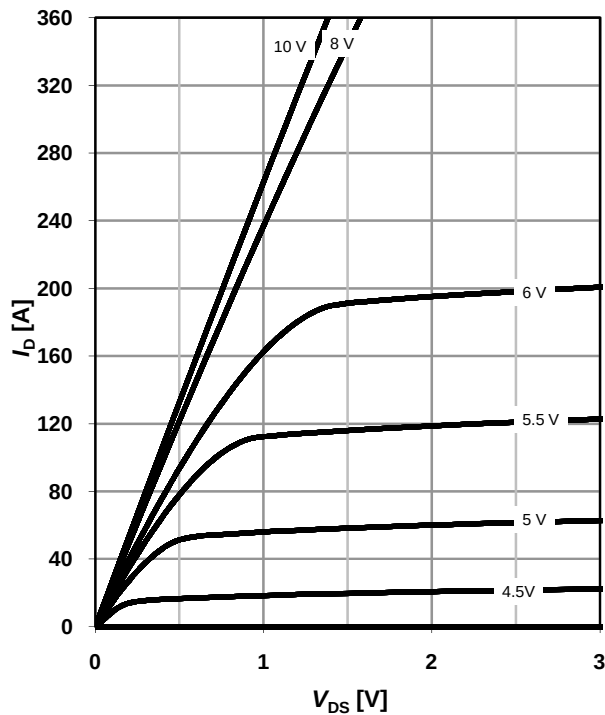
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



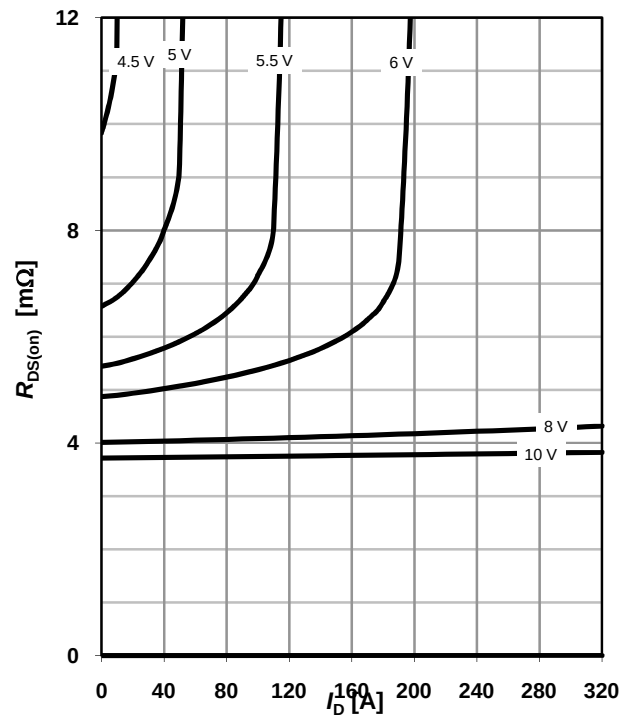
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


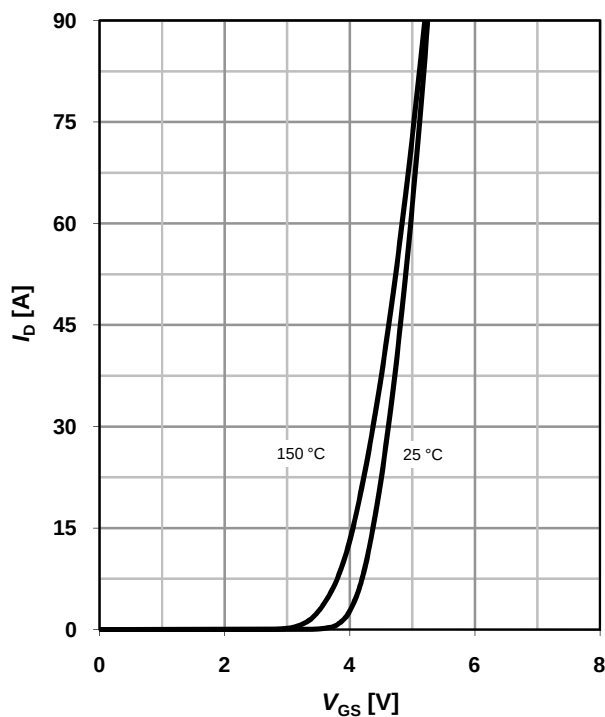
6 Typ. drain-source on resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

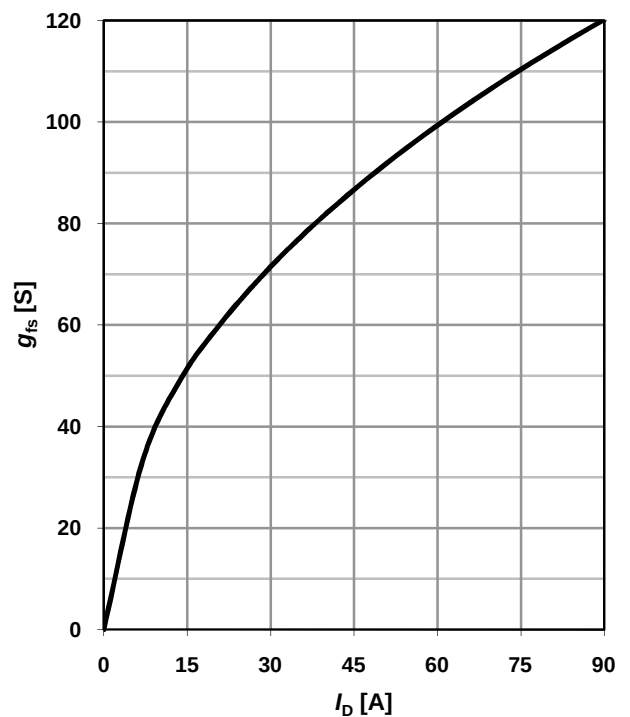
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

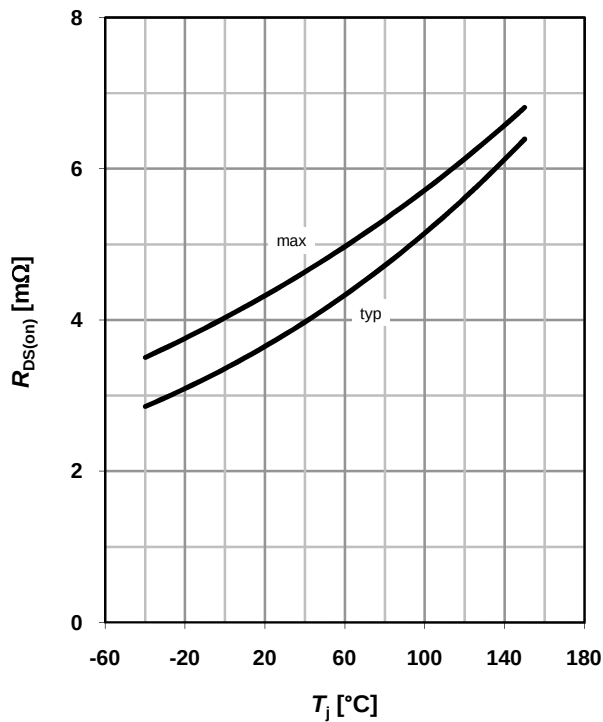
parameter: T_j


8 Typ. forward transconductance

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$


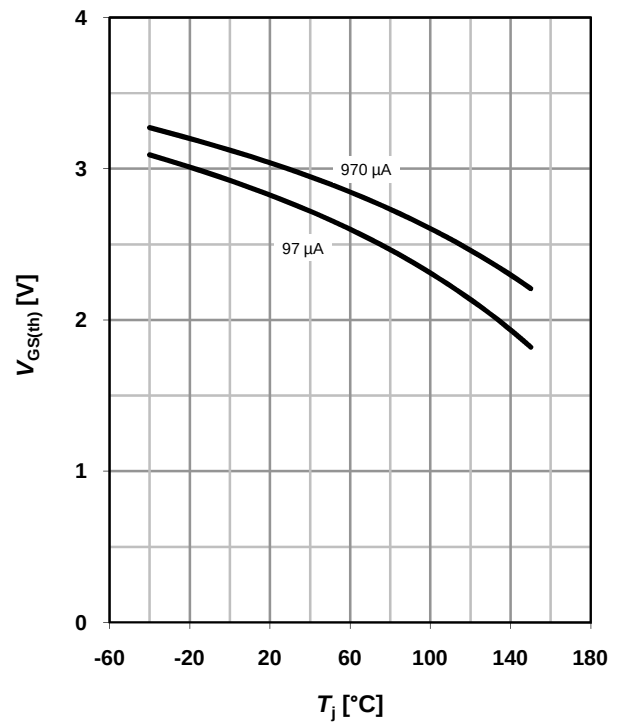
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$$



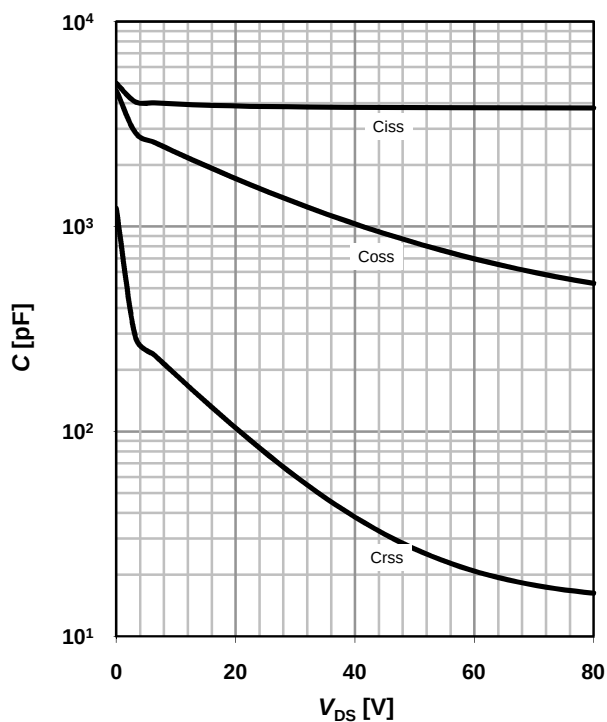
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$



11 Typ. capacitances

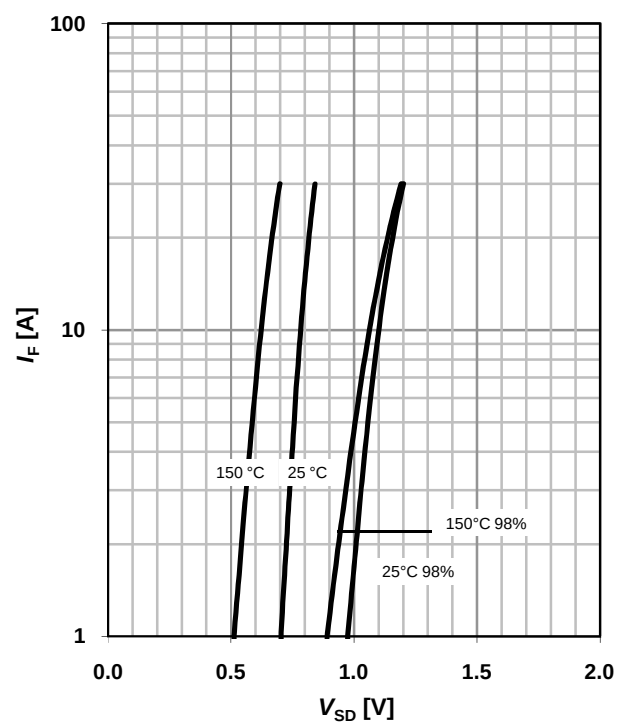
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

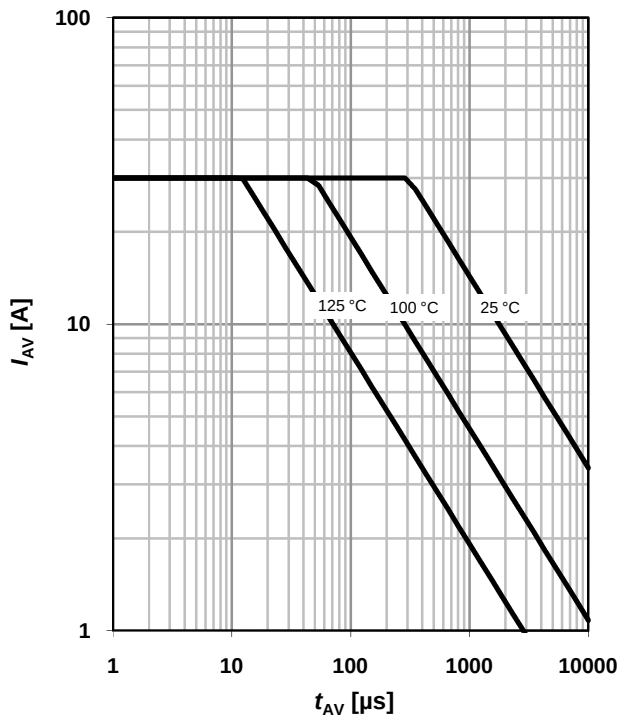
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

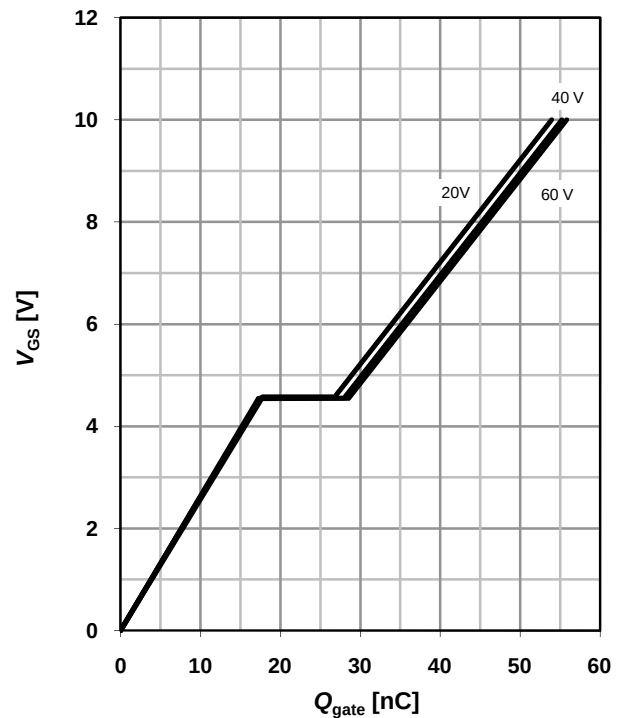
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

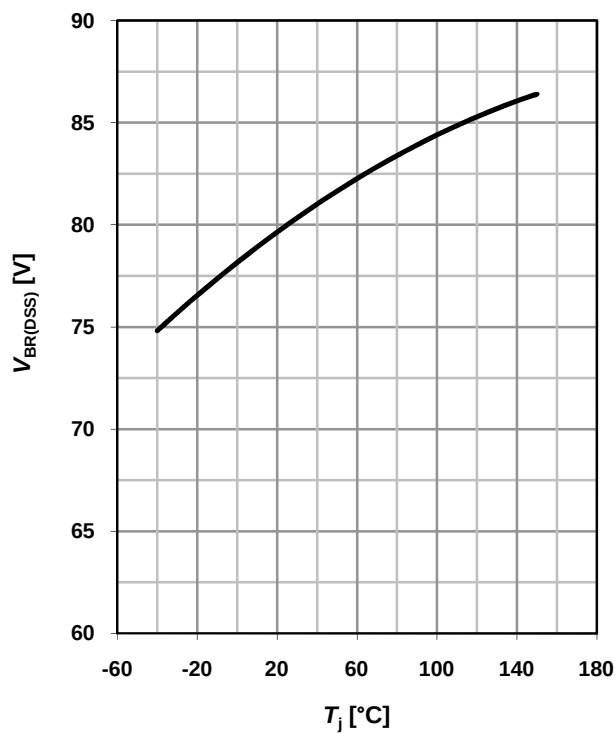
$$V_{GS}=f(Q_{\text{gate}}); I_D=30\ \text{A pulsed}$$

parameter: V_{DD}

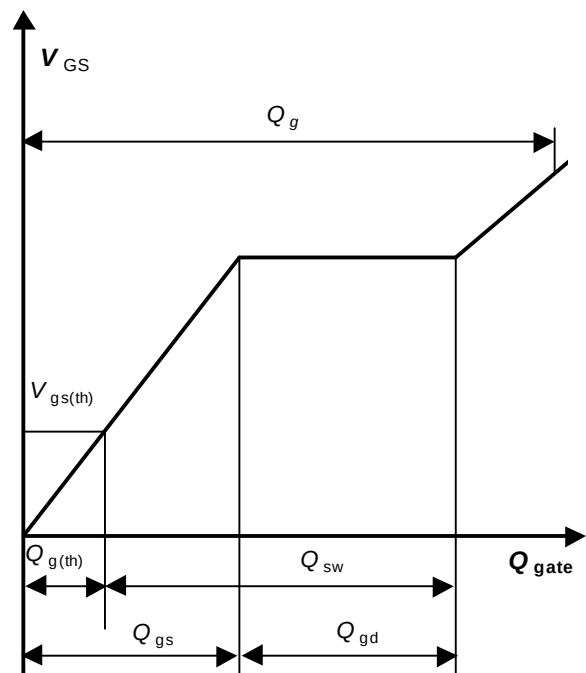


15 Drain-source breakdown voltage

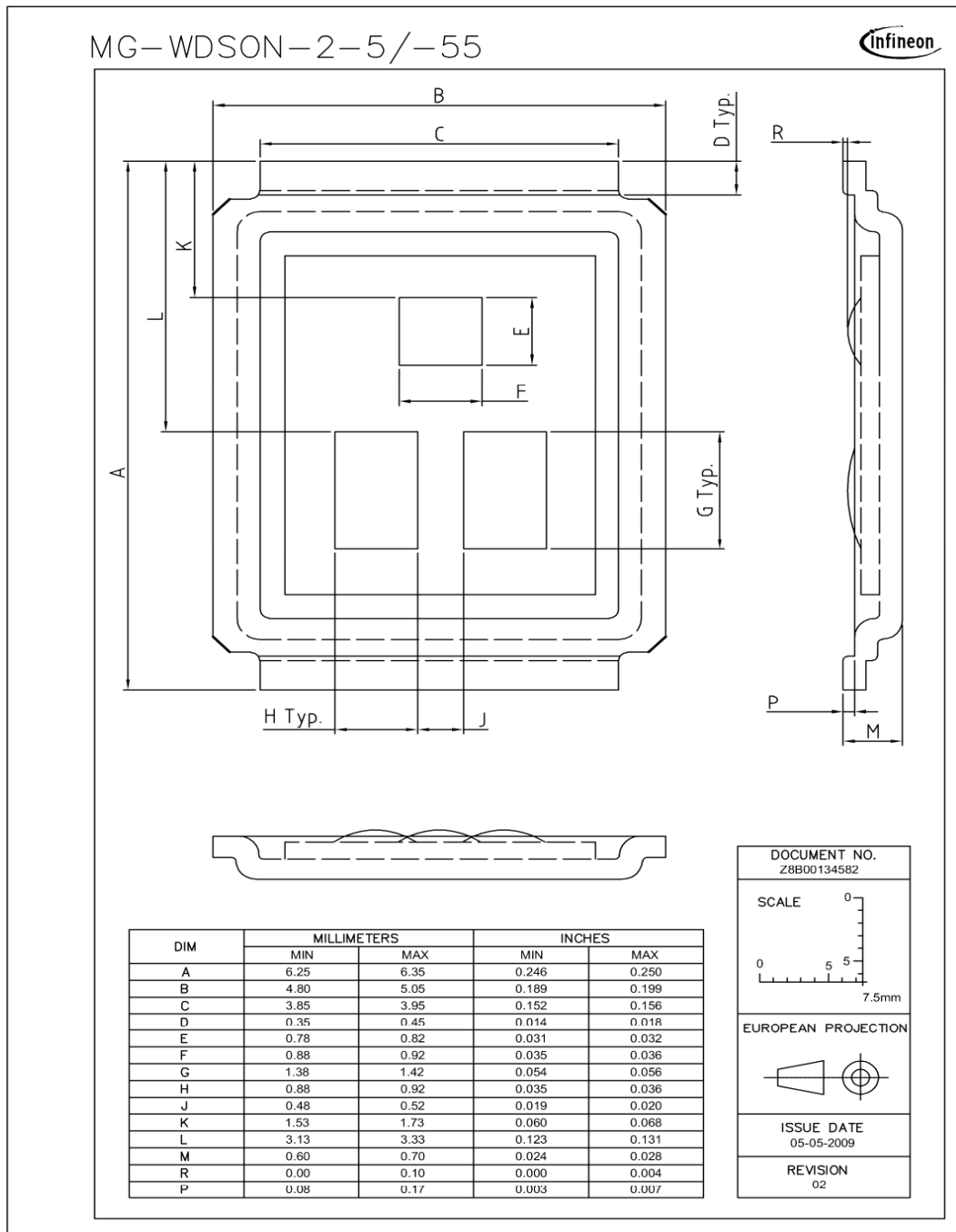
$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$



16 Gate charge waveforms



Package Outline

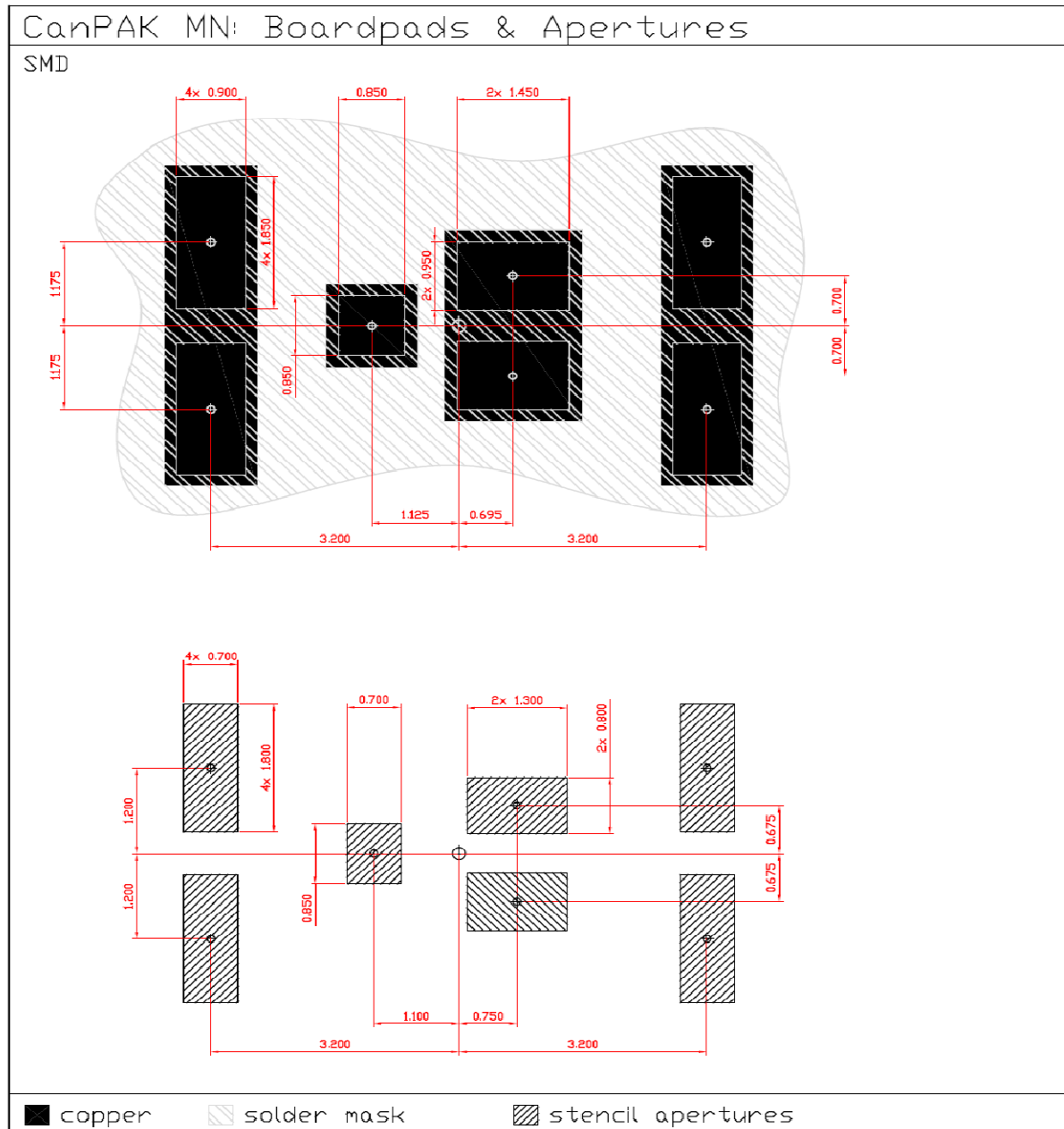
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Technical drawing of a rectangular plate with the following dimensions and features:

- Overall width: $12.00^{+0.30}_{+0.10}$
- Overall height: 1.20 ± 0.10
- Top edge features:
 - Left corner: 5.50 ± 0.05
 - Top edge center: 4.00
 - Right edge: 0.30 ± 0.05
- Internal features:
 - Top edge: 8.00 ± 0.10
 - Bottom edge: 6.60 ± 0.10
 - Left edge: 5.20 ± 0.05
 - Right edge: 0.95 ± 0.10
 - Bottom edge: 5.10 ± 0.10
- Other dimensions:
 - Top edge: 2.00 ± 0.05
 - Bottom edge: 1.75
 - Internal feature: $\phi 1.50 \text{ Min}$

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CanPAK™ M MG-WDSO-2



Dimensions in mm

Raccomended stencil thickness 150 µm

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