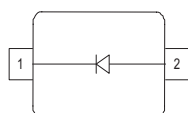


Silicon PIN Diode

- Optimized for low current antenna switches in hand held applications
- Very low forward resistance
(typ. 1.5Ω @ $I_F = 1 \text{ mA}$)
- Low capacitance at zero volt reverse bias at frequencies above 1 GHz (typ. 0.28 pF)
- Very low signal distortion
- Pb-free (RoHS compliant) package



BAR88-02LRH
BAR88-02V



Type	Package	Configuration	L_S (nH)	Marking
BAR88-02LRH	TSLP-2-7	single, leadless	0.4	U8
BAR88-02V	SC79	single	0.6	U

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	80	V
Forward current	I_F	100	mA
Total power dissipation	P_{tot}		mW
BAR88-02LRH $T_S \leq 133^\circ\text{C}$		250	
BAR88-02V, $T_S \leq 123^\circ\text{C}$		250	
Junction temperature	T_j	150	$^\circ\text{C}$
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}		K/W
BAR88-02LRH		≤ 65	
BAR88-02V		≤ 105	

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Breakdown voltage $I_{(BR)} = 5 \mu\text{A}$	$V_{(BR)}$	80	-	-	V
Reverse current $V_R = 60 \text{ V}$	I_R	-	-	50	nA
Forward voltage $I_F = 1 \text{ mA}$ $I_F = 100 \text{ mA}$	V_F	- - -	0.75 0.95	0.9 1.2	V

¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

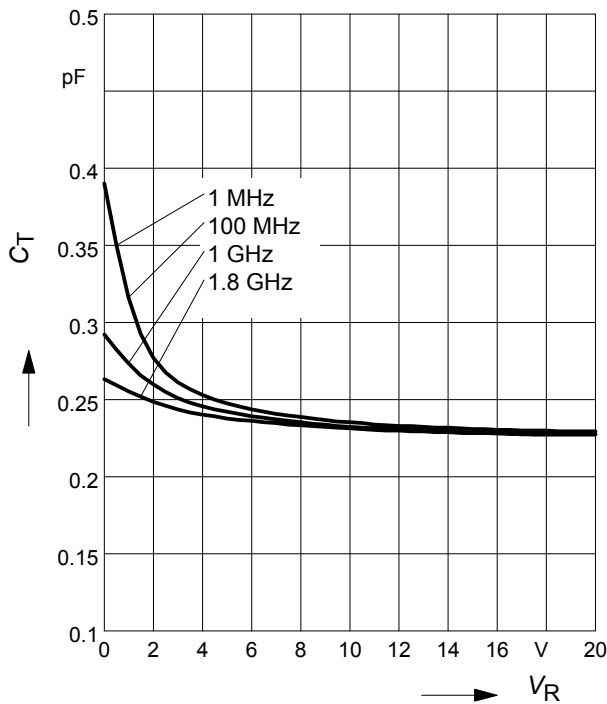
Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Diode capacitance $V_R = 1\text{ V}, f = 1\text{ MHz}$ $V_R = 0\text{ V}, f = 100\text{ MHz}$ $V_R = 0\text{ V}, f = 1\text{ GHz}$ $V_R = 0\text{ V}, f = 1.8\text{ GHz}$	C_T	- - - -	0.3 0.4 0.28 0.25	0.4 - - -	pF
Reverse parallel resistance $V_R = 0\text{ V}, f = 100\text{ MHz}$ $V_R = 0\text{ V}, f = 1\text{ GHz}$ $V_R = 0\text{ V}, f = 1.8\text{ GHz}$	R_P	- - -	65 2.5 1.5	- - -	kΩ
Forward resistance $I_F = 1\text{ mA}, f = 100\text{ MHz}$ $I_F = 5\text{ mA}, f = 100\text{ MHz}$ $I_F = 10\text{ mA}, f = 100\text{ MHz}$	r_f	- - -	1.5 0.8 0.6	2.5 - -	Ω
Charge carrier life time $I_F = 10\text{ mA}, I_R = 6\text{ mA}$, measured at $I_R = 3\text{ mA}$, $R_L = 100\text{ }\Omega$	τ_{rr}	-	500	-	ns
I-region width	W_I	-	13	-	μm
Insertion loss ¹⁾ $I_F = 1\text{ mA}, f = 1.8\text{ GHz}$ $I_F = 5\text{ mA}, f = 1.8\text{ GHz}$ $I_F = 10\text{ mA}, f = 1.8\text{ GHz}$	I_L	- - -	0.11 0.07 0.06	- - -	dB
Isolation ¹⁾ $V_R = 0\text{ V}, f = 0.9\text{ GHz}$ $V_R = 0\text{ V}, f = 1.8\text{ GHz}$ $V_R = 0\text{ V}, f = 2.45\text{ GHz}$	I_{SO}	- - -	15 11 9	- - -	

¹⁾BAR88-02LRH in series configuration, $Z = 50\Omega$

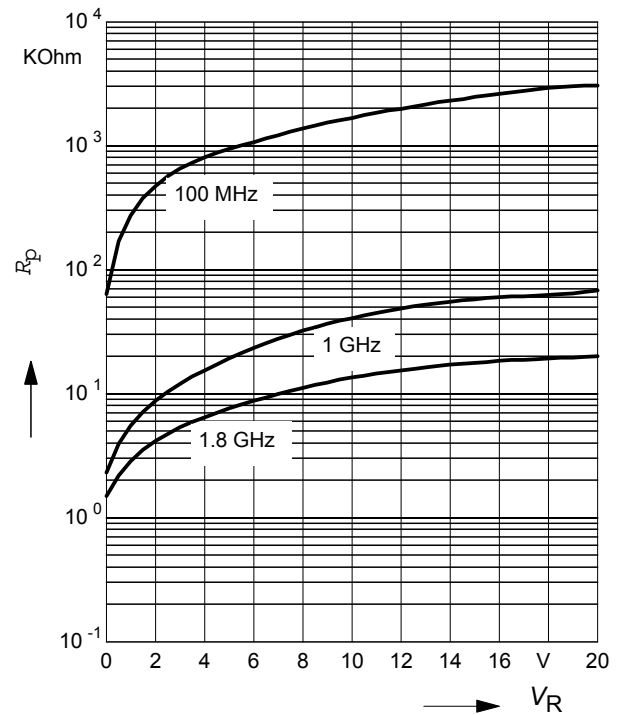
Diode capacitance $C_T = f(V_R)$

f = Parameter



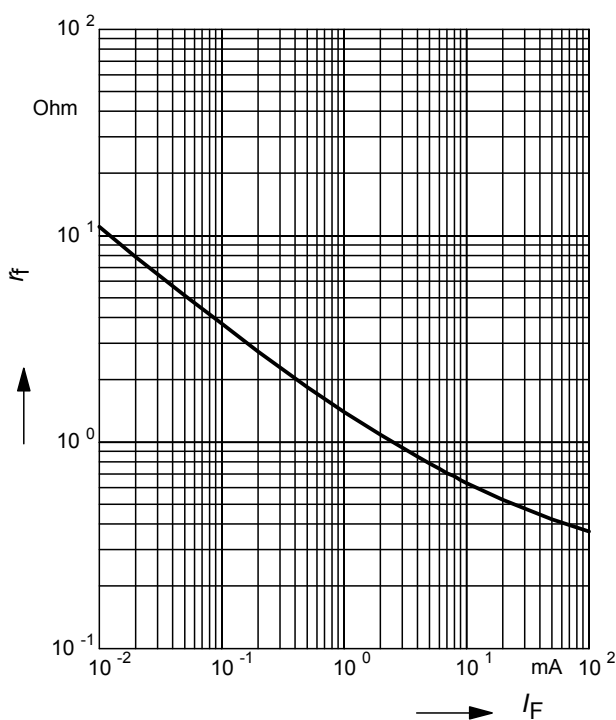
Reverse parallel resistance $R_P = f(V_R)$

f = Parameter



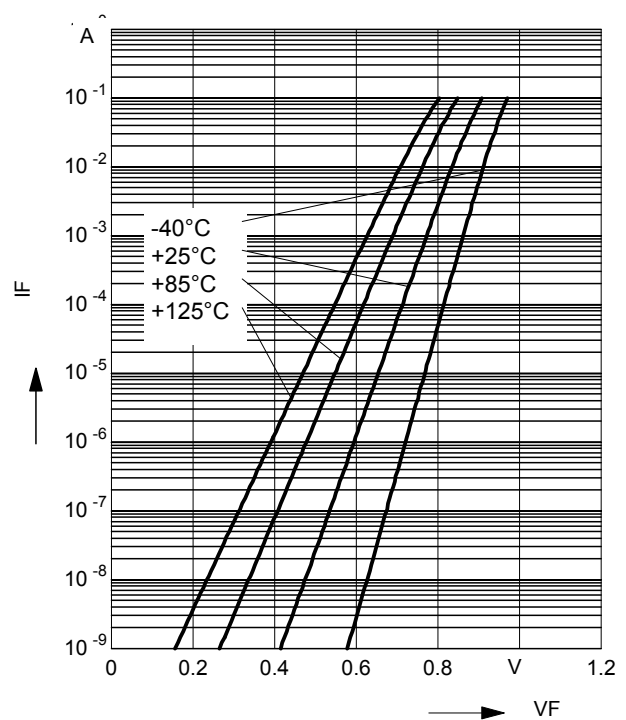
Forward resistance $r_f = f(I_F)$

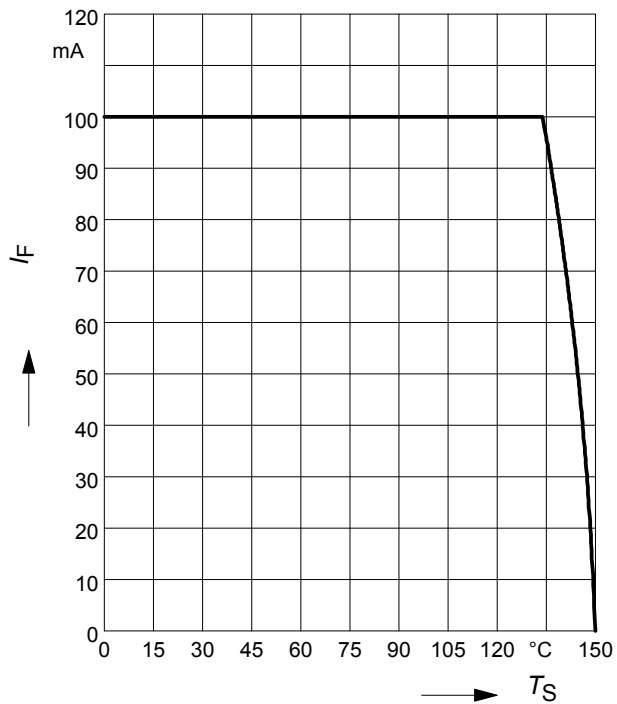
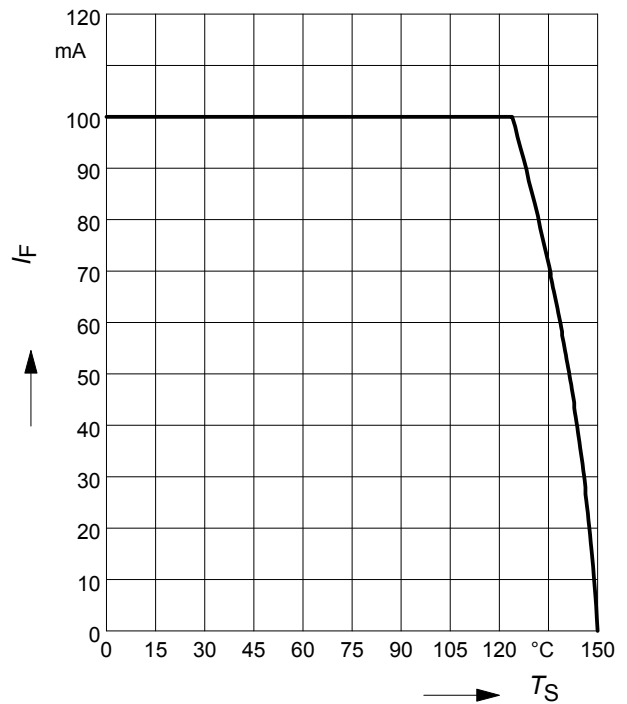
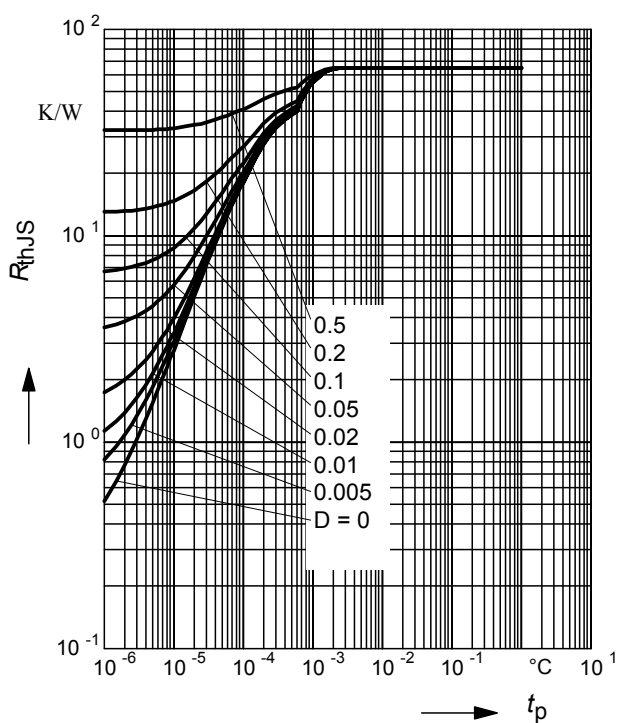
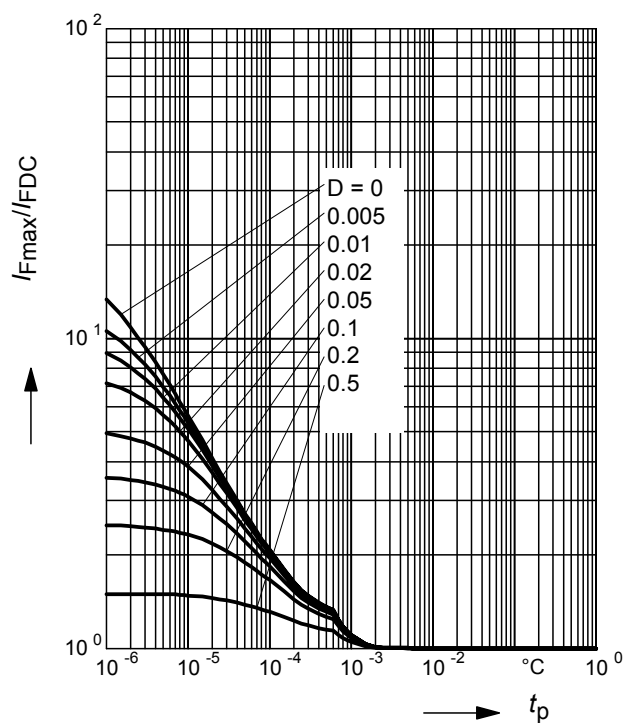
f = 100MHz



Forward current $I_F = f(V_F)$

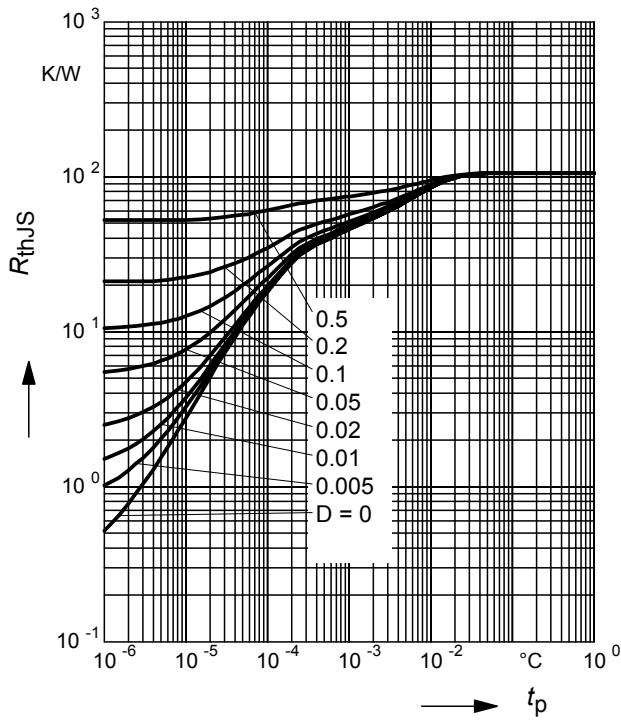
T_A = Parameter



Forward current $I_F = f(T_S)$
BAR88-02LRH

Forward current $I_F = f(T_S)$
BAR88-02V

Permissible Puls Load $R_{thJS} = f(t_p)$
BAR88-02LRH

Permissible Pulse Load
 $I_{Fmax}/I_{FDC} = f(t_p)$, BAR88-02LRH


Permissible Puls Load $R_{thJS} = f(t_p)$

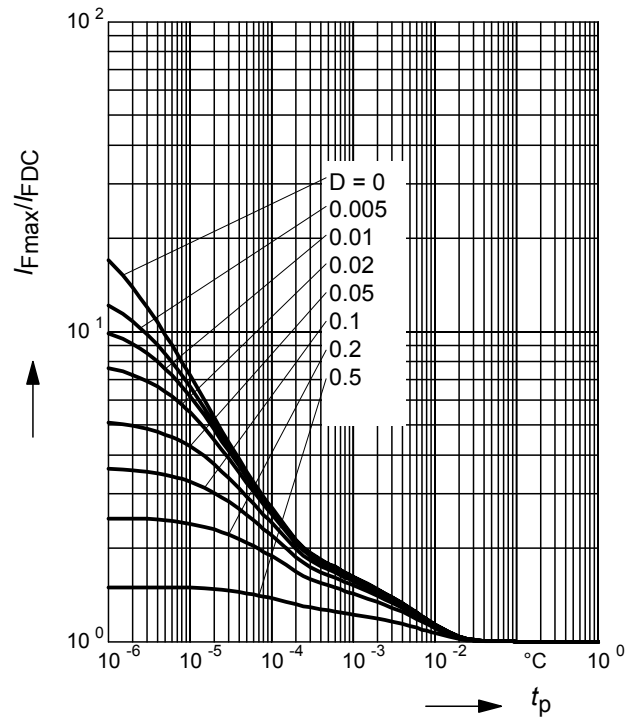
BAR88-02V



Permissible Pulse Load

$$I_{Fmax}/I_{FDC} = f(t_p)$$

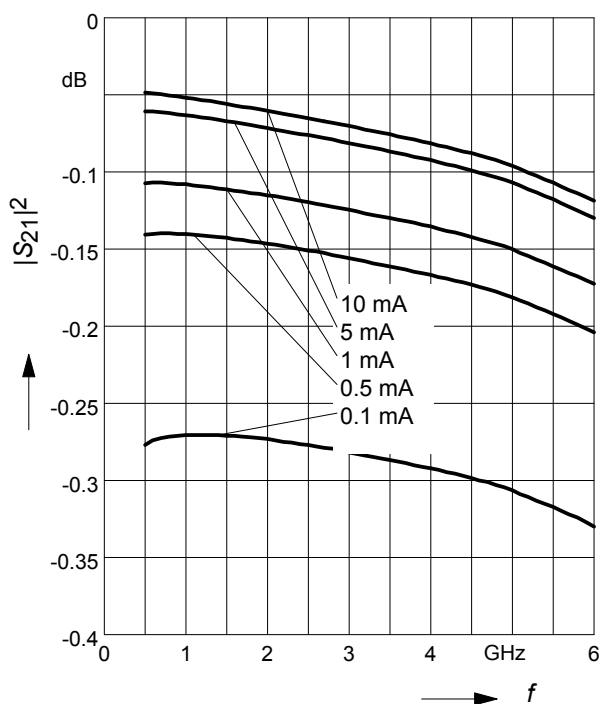
BAR88-02V



Insertion loss $I_L = -|S_{21}|^2 = f(f)$

I_F = Parameter

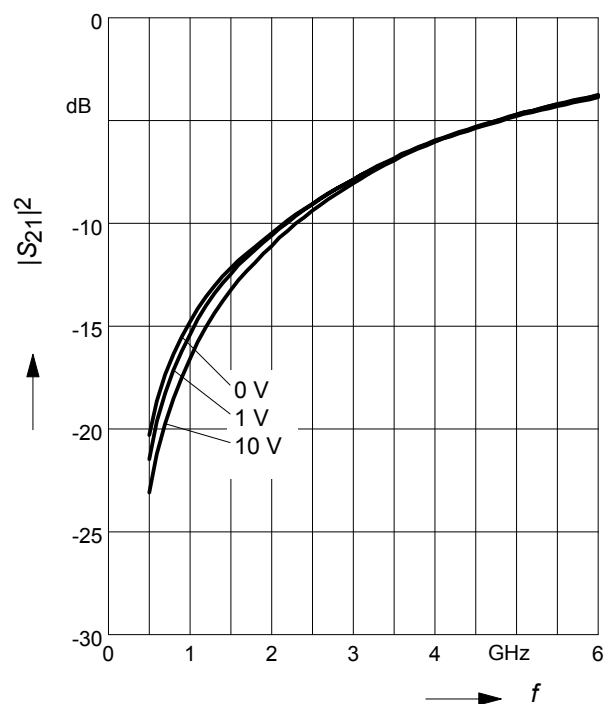
BAR88-02LRH in series configuration, $Z = 50\Omega$



Isolation $I_{SO} = -|S_{21}|^2 = f(f)$

V_R = Paramter

BAR88-02LRH in series configuration, $Z = 50\Omega$



The drawing shows the 100-01 package with the following dimensions:

- Top View:**
 - Overall width: 0.8 ± 0.1
 - Overall height: 0.3 ± 0.05
 - Pin 1 location: Indicated by a square with the number 1.
 - Cathode marking: Indicated by a square with the number 2.
- Side View:**
 - Maximum height: 1.6 ± 0.1
 - Maximum width: 10°MAX.
 - Maximum length: 10°MAX.
 - Maximum thickness: 1.2 ± 0.1
 - Maximum width at base: 0.55 ± 0.04
 - Maximum thickness at base: 0.2 ± 0.05

2005, June
Date code

GF

BAR63-02V
Type code

Cathode marking
Laser marking

The figure contains three technical drawings of cathode marking components:

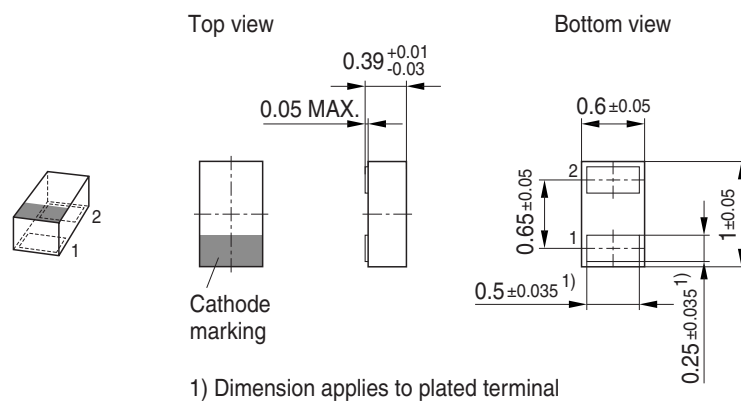
- Standard:** A top-down view of a component with a width of 8. It features two circular holes with a diameter of 1.33 and two rectangular markings with a width of 1.96. The distance between the holes is 4. The distance from the left edge to the first hole is 0.4. The distance from the left edge to the first marking is 0.93. A cathode marking is indicated on the left.
- Reel with 2 mm Pitch:** A top-down view of a component with a width of 2. It features two circular holes with a diameter of 1.33 and two rectangular markings with a width of 1.96. The distance between the holes is 2. The distance from the left edge to the first hole is 0.4. The distance from the left edge to the first marking is 0.93. A cathode marking is indicated on the left.
- Side View:** A side view of the component showing a thickness of 0.66 and a width of 0.2.

Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

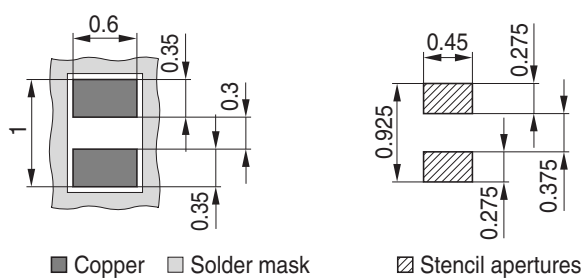
1) New Marking Layout for SC75, implemented at October 2005.

Package Outline

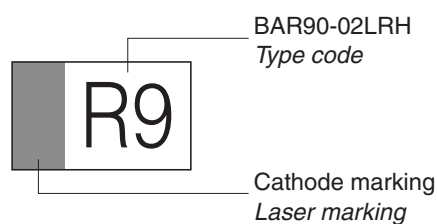


Foot Print

For board assembly information please refer to Infineon website "Packages"

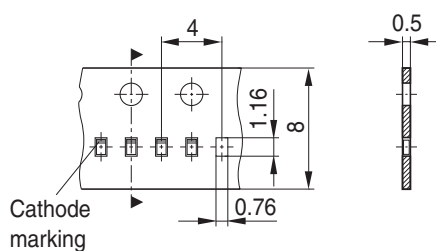


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel
Reel ø330 mm = 50.000 Pieces/Reel (optional)



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