15 W 5 V Adapter Reference Board

with ICE2QS03G, IR1161, IPS65R1K5CE, BSZ100N06LS3 G and BASW21-03W

About this document

Scope and purpose

This document is an engineering report that describes 15 W 5 V USB adapter reference design board using Quasi-Resonant PWM IC ICE2QS03G (DSO-8) with CoolMOS™ IPS65R1K5CE (IPAK SL) and secondary side synchronous rectification IC IR1161 (5-Pin SOT-23) with OptiMOS™ BSZ100N06LS3 G (S3O8, 3x3 mm style SuperSO8). The reference USB adapter board is specially designed in a very small form factor, high efficiency, low standby power, various modes of protections for a high reliable system and it pass conductive EMI, ESD and Lightning surge test. This board can be used for production by customers after final verification with minor changes.

Intended audience

This document is intended for power supply design/application engineer, students, etc.) who wish to design 15 W 5 V AC-DC adapter in short period of time, high efficiency, high reliability and very small form factor with Infineon CoolMOS™ CE series, OptiMOS™, Quasi-Resonant PWM IC ICE2QS03G and synchronous rectification IC IR1161.

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Abstract

1 Abstract

This application note is an engineering report of a very small form factor reference design for universal input 15 W 5 V adapter. The adapter is using **ICE2QS03G**, a second generation current mode control Quasi-Resonant flyback topology controller, **IR1161**, µSmartRectifier™ for synchronous rectification, **IPS65R1K5CE**, a **CE** series of high voltage power CoolMOS™ and **BSZ100N06LS3 G**, a third series of medium voltage power logic level OptiMOS™ , optimized for logic level driver of Synchronous Rectification. The distinguishing features of this reference design are very small form factor, best-in-class low standby power, very high efficiency, good EMI performance and various modes of protection for high reliable system.

2 Reference board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

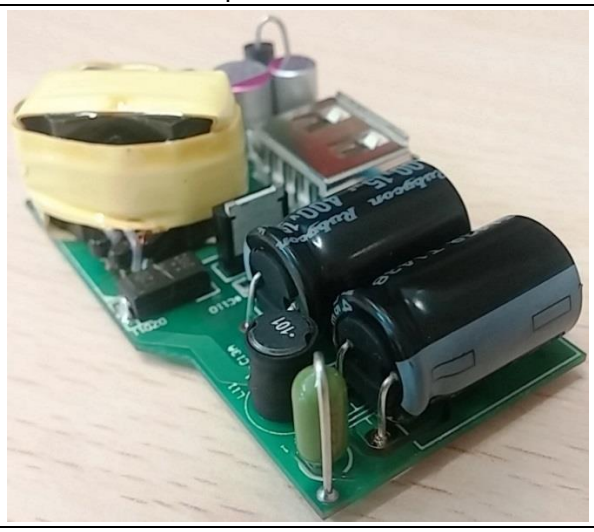


Figure 1 REF-15W_IR_Opti3 ADAPTER [Dimensions L x W x H: 47mm x 31mm x 16mm]

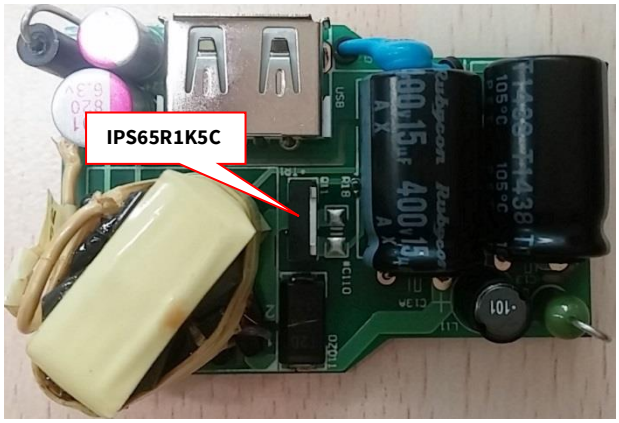


Figure 2 REF-15W_IR_Opti3 ADAPTER (Top view)

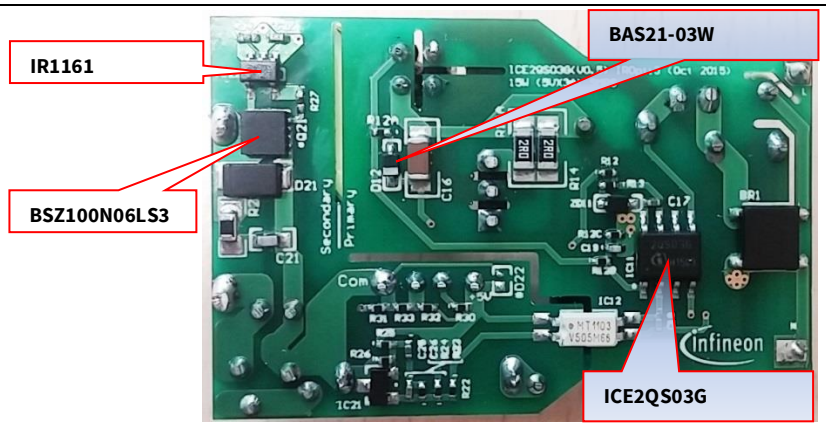


Figure 3 REF-15W_IR_Opti3 ADAPTER (Bottom view)

3 Specification of Reference Board

Table 1 Specification of REF-15W_IR_Opti3 ADAPTER

Input voltage and frequency	85 V_{AC} (60 Hz)~265 V_{AC} (50 Hz)
Output voltage, current & power	5 V/3 A/15 W
Output voltage rise time	<30 ms
Start up delay time (V_{AC} 115 V, 60 Hz, Full Load)	<250 ms
Hold up time (V_{AC} 115 V, 60 Hz, Full Load)	>5 ms
Dynamic load response (50mA to full load, slew rate at 1.5 A/µs, 100 Hz)	±3% of nominal output voltage ($V_{ripple\_p\_p}$ <300 mV)
Output ripple voltage (full load, 85 V_{AC} ~265 V_{AC})	±1% of nominal output voltage ($V_{ripple\_p\_p}$<100 mV)
Active mode four point average efficiency (25%,50%,75%,100%load) (EU CoC Version 5, Tier 2 and EPS of DOE USA) 10% load efficiency (EU CoC Version 5, Tier 2) No load power consumption (EU CoC Version 5, Tier 2 and EPS of DOE USA)	>88% at 115 V_{AC} & >87% at 230 V_{AC} >87% at 115 V_{AC} & >84% at 230 V_{AC} <30 mW at 265 V_{AC}
Conducted emissions (EN55022 class B)	Pass with 10 dB margin for 115 V_{AC} and 6 dB margin for 230 V_{AC}
Safety Leakage Current (50 µA @ V_{AC} = 265 V,L to FG & N to FG)	<50 µA @ V_{AC} = 265 V_{AC}
ESD immunity (EN61000-4-2)	Level 4 (±8 kV: contact discharge)
Surge immunity (EN61000-4-5)	Installation class 3 (2 kV: common mode)
Form factor case size (L x W x H)	(47 x 31 x 16) mm^3

4 Circuit description

4.1 Mains input rectification and filtering

The AC line input side comprises the input fuse F1 as over-current protection. A rectified DC voltage (120 V ~ 374 V) is obtained through a bridge rectifier BR1 and a pi filter C13, FB21 and C22. The pi filer also attenuates the differential mode conducted EMI.

4.2 PWM control and switching MOSFET

The PWM pulse is generated by the Quasi Resonant PWM current-mode Controller **ICE2QS03G** and this PWM pulse drives the high voltage power CoolMOS™, **IPS65R1K5CE (CE)** which designed according to the revolutionary Superjunction (SJ) principle. The CoolMOS™ CE provides all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. It achieves extremely low conduction and switching losses and can make switching applications more efficient, more compact, lighter and cooler. The PWM switch-on is determined by the zero-crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. **ICE2QS03G** also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

4.3 Snubber network

A snubber network DZD11 dissipates the energy of the leakage inductance and suppress ringing on the SMPS transformer.

4.4 Output stage

On the secondary side, 5 V output, the PWM pulse is generated by synchronous rectification controller **IR1161**. The synchronous rectification pulse drives the logic level medium voltage power OptiMOS™, **BSZ100N06LS3 G** which is optimized for synchronous rectification such as the lowest R_{DS}(on), the perfect switching behavior of fast switching, the smallest footprint (S3O8, 3x3 mm style SuperSO8) and highest power density. The capacitors C22 provides energy buffering following with the LC filter FB21 and C24 to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency considerably. Storage capacitor C22 is designed to have an internal resistance (ESR) as small as possible. This is to minimize the output voltage ripple caused by the triangular current.

4.5 Feedback loop

For feedback, the output is sensed by the voltage divider of R26 and R25 and compared to TL431 internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of TL431 is converted to the current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

5 Circuit operation

5.1 Startup operation

Since there is a built-in startup cell in the **ICE2QS03G**, there is no need for external start up resistor, which can improve standby performance significantly. When V_{CC} reaches the turn on voltage threshold 18V, the IC begins with a soft start. The soft-start implemented in **ICE2QS03G** is a digital time-based function. The preset soft-start time is 12 ms with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.32 V to 1 V finally. After IC turns on, the V_{CC} voltage is supplied by auxiliary windings of the transformer.

5.2 Normal mode operation

The secondary output voltage is built up after startup. The secondary regulation control is adopted with TL431 and optocoupler. The compensation network C25, C26 and R24 constitutes the external circuitry of the error amplifier of TL431. This circuitry allows the feedback to be precisely controlled with respect to dynamically varying load conditions, therefore providing stable control.

5.3 Primary side peak current control

The MOSFET drain source current is sensed via external resistor R14 and R14A. Since **ICE2QS03G** is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle.

5.4 Digital frequency reduction

During normal operation, the switching frequency for **ICE2QS03G** is digitally reduced with decreasing load. At light load, the CoolMOS™ **IPS65R1K5CE** will be turned on not at the first minimum drain-source voltage time, but on the n^{th}. The counter is in range of 1 to 7, which depends on feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

5.5 Burst mode operation

At light load condition, the SMPS enters into Active Burst Mode. At this stage, the controller is always active but the V_{CC} must be kept above the switch off threshold. During active burst mode, the efficiency increase significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.
For determination of entering Active Burst Mode operation, three conditions apply:
1. The feedback voltage is lower than the threshold of V_{FBEB}(1.25 V). Accordingly, the peak current sense voltage across the shunt resistor is 0.1667;
2. The up/down counter is 7;
3. And a certain blanking time (t_{BEB}=24 ms).
Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.
During active burst mode, the maximum current sense voltage is reduced from 1 V to 0.34 V so as to reduce the conduction loss and the audible noise. At the burst mode, the FB voltage is changing like a sawtooth between 3.0 and 3.6 V.

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 34% during Active Burst Mode a certain load is needed so that feedback voltage can exceed V_{FBLB} (4.5 V). After leaving active burst mode, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to 1 immediately after leaving Active Burst Mode. This is helpful to decrease the output voltage undershoot.

6 Protection features

6.1 VCC over voltage and under voltage protection

During normal operation, the V_{CC} voltage is continuously monitored. When the V_{CC} voltage increases up to $V_{CC,OVP}$ or V_{CC} voltage falls below the under voltage lock out level $V_{CC,off}$, the IC will enter into autorestart mode.

6.2 Over load/Open loop protection

In case of open control loop, feedback voltage is pulled up with internally block. After a fixed blanking time, the IC enters into auto restart mode. In case of secondary short-circuit or overload, regulation voltage V_{FB} will also be pulled up, same protection is applied and IC will auto restart.

6.3 Auto restart for over temperature protection

The IC has a built-in over temperature protection function. When the controller's temperature reaches 140°C, the IC will shut down switch and enters into auto restart. This can protect power MOSFET from overheated.

6.4 Adjustable output overvoltage protection

During off-time of the power switch, the voltage at the zero-crossing pin ZC is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7 V for a preset period 100 µs, the IC is latched off.

6.5 Short winding protection

The source current of the MOSFET is sensed via external resistor R14 and R14A. If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68 V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an accidental latch off, a spike blanking time of 190 ns is integrated in the output of internal comparator.

6.6 Foldback point protection

For a quasi-resonant flyback converter, the maximum possible output power is increased when a constant current limit value is used for all the mains input voltage range. This is usually not desired as this will increase additional cost on transformer and output diode in case of output over power conditions.
The internal foldback protection is implemented to adjust the V_{CS} voltage limit according to the bus voltage. Here, the input line voltage is sensed using the current flowing out of ZC pin, during the MOSFET on-time. As the result, the maximum current limit will be lower at high input voltage and the maximum output power can be well limited versus the input voltage.

7 Circuit Diagram

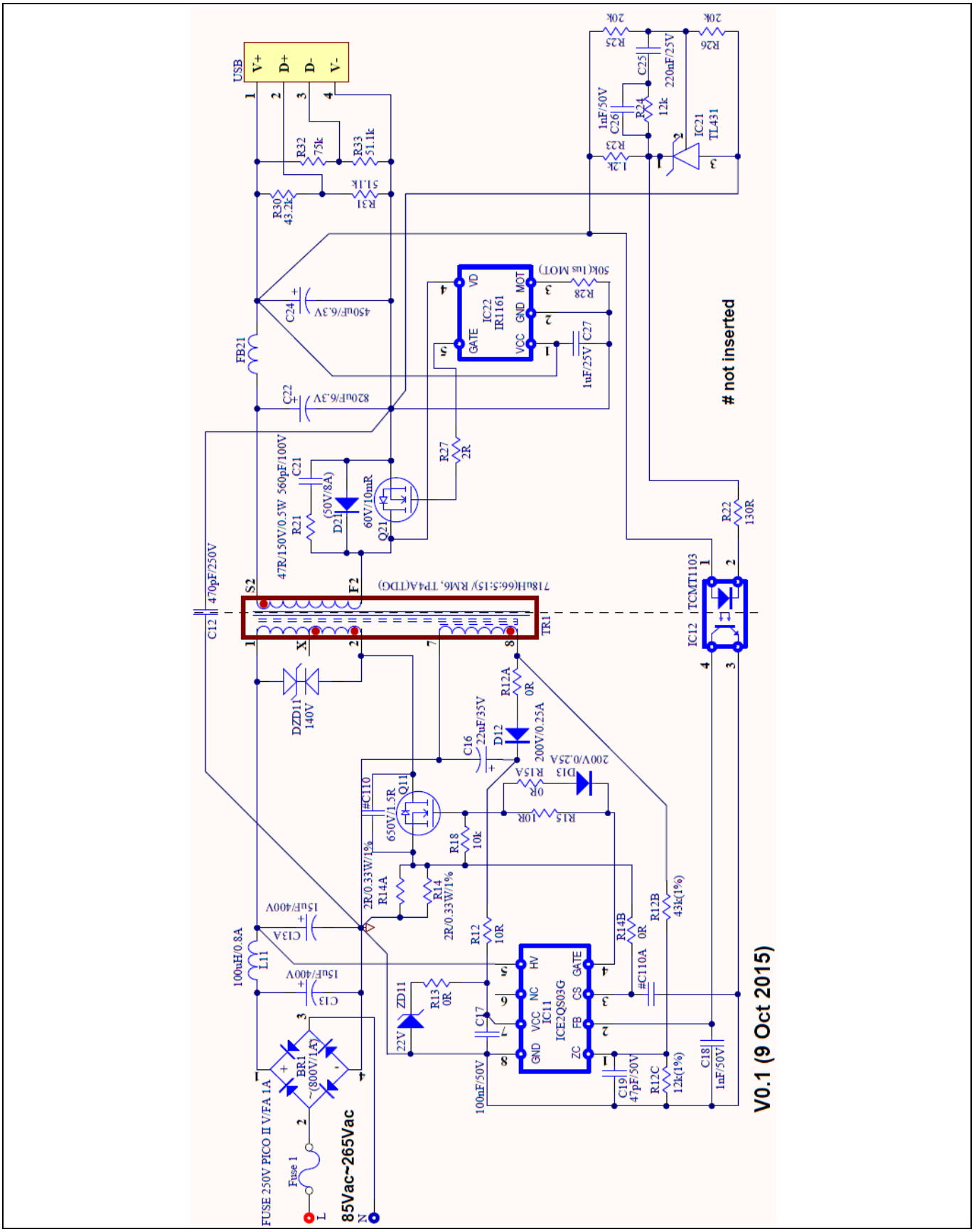


Figure 4 Schematic of REF-15W_IR_Opti3 ADAPTER

8 PCB layout

8.1 Top side

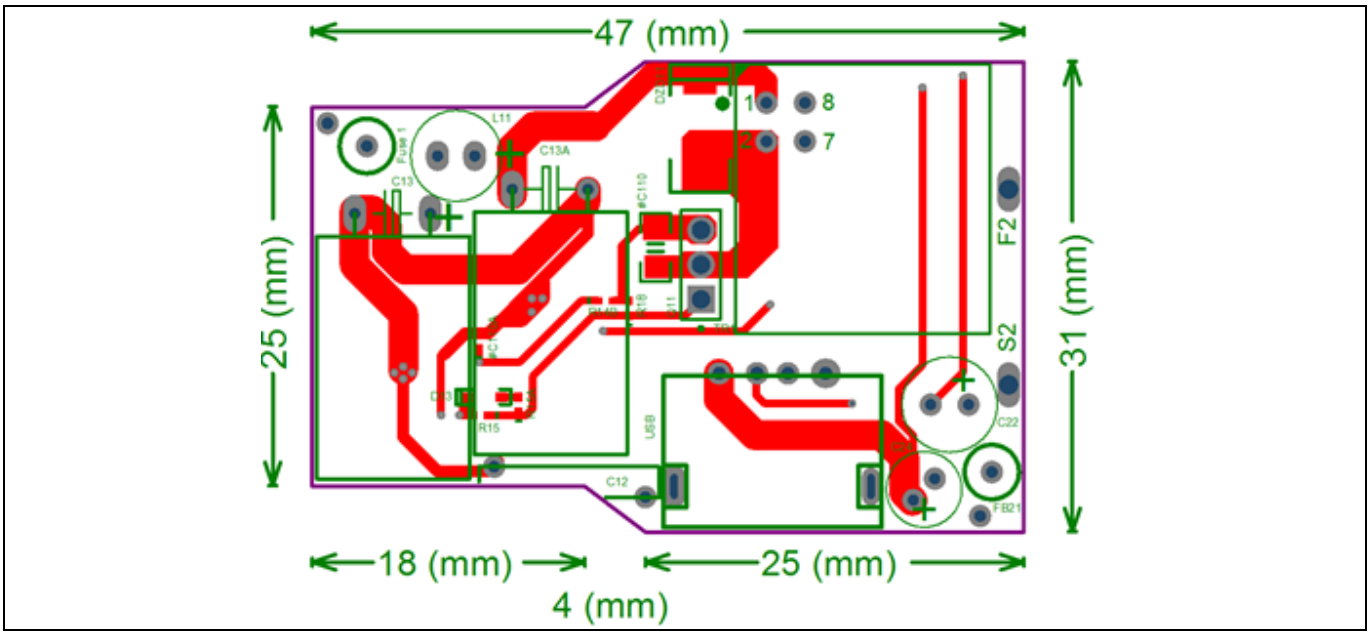


Figure 5 Top side copper and component legend

8.2 Bottom side

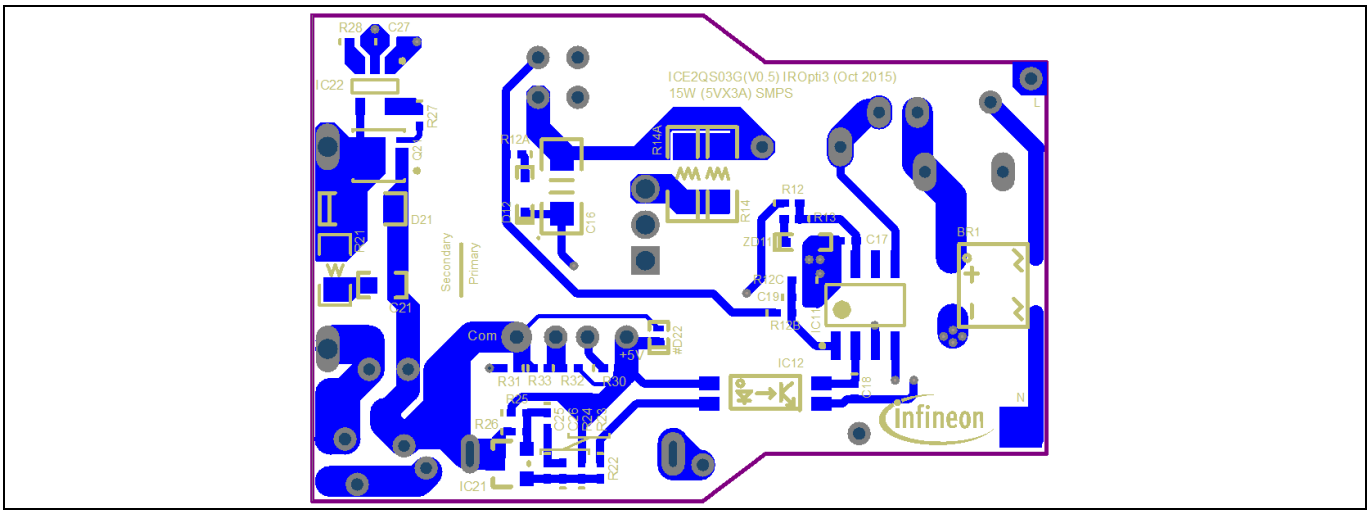


Figure 6 Bottom side copper and component legend

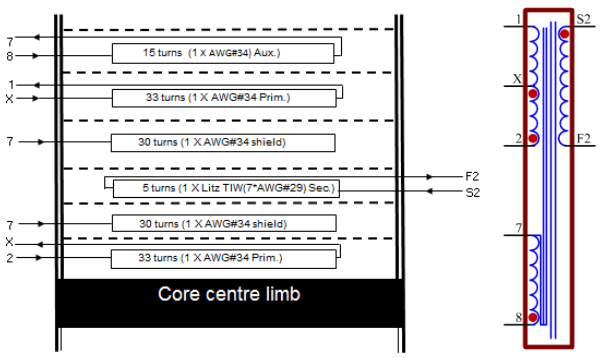
9 Component list

Table 2 Bill of materials (V0.2)

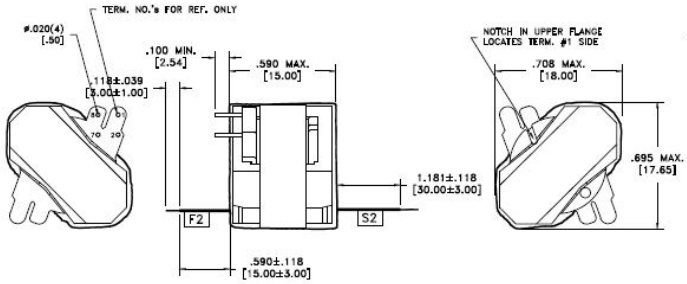
No.	Designator	Description	Footprint	Part Number	Manufacturer	Quantity
1	BR1	(800V/1A)	SOP-4	D1UBA80	SHINDENGEN	1
2	C12	470pF/250V	MKT3/13/10_0M8	DE1B3KL471KC4BNA1S	MURATA	1
3	C13, C13A	15uF/400V	RB10H(10x16)	400AX15M10X16	RUBYCON	2
4	C16	22uF/35V	1206	C3216X5R1V226M	TDK	1
5	C17	100nF/50V	0402	GRM155R71H104KE14D	MURATA	1
6	C18, C26	1nF/50V	0402	GRM155R71H102KA01D	MURATA	2
7	C19	47pF/50V	0402	GRM1555C1H470JA01D	MURATA	1
8	C21	560pF/100V	0603	GRM1885C2A561JA01D	MURATA	1
9	C22	820uF/6.3V	RB6.3	MP6RL820MC8	MATSUKI POLYMER	1
10	C24	450uF/6.3V	RB5	MP6RL450MB8	MATSUKI POLYMER	1
11	C25	220nF/25V	0402	GRM155C81E224KE01D	MURATA	1
12	C27	1uF/25V	0402	GRM155R61E105KA12D	MURATA	1
13	D12,D13	200V/0.25A	SOD323	BAS21-03W	INFINEON	2
14	D21	50V/8A	DO-221BC(SMPA)	V8PAN50-M3/I		1
15	DZD11	140V	2F	ST02D-140F2	SHINDENGEN	1
16	F1	250V/1A	AXIAL0.4_V 3mm	0263001.HAT1L		1
17	FB21	FAIR RITE	AXIAL0.4_V 3mm	2743002112		1
18	FB11,FB22,FB23	Pin 2 of Q2, leads of C12		B64290P0035X038	EPCOS	3
19	IC11	ICE2QS03G	SO-8	ICE2QS03G	INFINEON	1
20	IC12	TCMT1103	half pitch mini flat	TCMT1103		1
21	IC21	TL431	SOT-23	TL431BFDT		1
22	IC22	IR1161	5-Pin SOT-23	IR1161LPBF	INTERNATIONAL RECTIFIER	1
23	L11	100µH/0.8A	CH6	7447462101	WURTH ELECTRONICS	1
24	Q11	650V/1.5Ω	IPAK	IPS65R1K5CE	INFINEON	1
25	Q21	60V/10mΩ	PG-TSDSON-8	BSZ100N06LS3	INFINEON	1
26	R12, R15	10R	0402			2
27	R12A, R13, R14B, R15A	0R	0402			4
28	R12B	43k/1%	0402			1
29	R12C	12k/1%	0402			1
30	R14, R14A	2R/0.33W/1%	1206	ERJ8BQF2R0V		2
31	R18	10k	0402			1
32	R21	47R/0.5W	0805	ERJP6WF47R0V		1
33	R22	130R	0402			1
34	R23	1.2k	0402			1
35	R24	12k	0402			1
36	R25, R26	20k	0402			2
37	R27	2R	0402			1
38	R28	50k	0402			1
40	R30	43.2k	0402			1
41	R31, R33	51.1k	0402			1
42	R32	75k	0402			1
43	TR1	718µH(66:5:15)	TR_RM6_THT8Pin			1
44	USB Port	USBPORT	USB2 Short	JL-CAF-001		1
45	ZD11	22V Zener	SOD323	UDZS22B		1

10 Transformer construction

Core and material: RM6 TP4A
Bobbin: RM6 with 4 pin
Primary Inductance, Lp=718 µH (±10%), measured between pin 2 and pin 1



Start	Stop	No. of turns	Wire size	Layer
2	X	33	1XAWG#34	1/2 Primary
7	floating	30	1XAWG#34	Shield
S2 Flying wire 15mm	F2 Flying wire 15mm	5	1XLitz TIW(7 X AWG#29)	Secondary
7	floating	30	1XAWG#34	Shield
X	1	33	1XAWG#34	1/2 Primary
8	7	15	1XAWG#34	Auxiliary

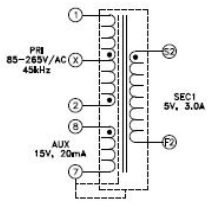


ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	2–1	@20°C	1.936 ohms Max
D.C. RESISTANCE	8–7	@20°C	0.556 ohms Max
D.C. RESISTANCE	S2–F2	@20°C	0.015 ohms Max
INDUCTANCE	2–1	50kHz, 100mVAC, Ls	718uH ±10%
LEAKAGE INDUCTANCE	2–1	tie(8+7+S2+F2), 100kHz, 100mVAC, Ls	15.0 uH max.
DIELECTRIC	1–S2	tie(2+7), 6250VDC, 1 second	5000VDC, 1 min.
DIELECTRIC	S2–Core	6250VDC, 1 second	5000VDC, 1 min.
TURNS RATIO		(2–1):(8–7)	4.4:1, ±2%
TURNS RATIO		(2–1):(S2–F2)	13.2:1, ±2%

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: −40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC60950–1,
– Reinforced insulation for a primary circuit at a working voltage of 265VAC.



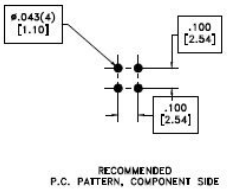


Figure 7 Transformer structure

11 Test results

11.1 Efficiency, regulations and output ripple

Table 3 Efficiency, regulation & output ripple

Input (V_{AC}/Hz)	P_{in} (W)	V_{out} (V_{DC})	I_{out} (A)	V_{OutRPP} (mV)	P_{out} (W)	Efficiency (η) (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85 V_{AC}/60 Hz	0.02157	5.01	0.00	69.00				20.82	3.52
	1.72	5.01	0.30	80.00	1.50	87.38			
	4.25	5.01	0.75	48.00	3.76	88.41	87.62		
	8.51	5.01	1.50	52.00	7.52	88.31			
	12.83	5.01	2.25	55.00	11.27	87.86			
	17.50	5.01	3.00	68.00	15.03	85.89			
115 V_{AC}/60 Hz	0.02256	5.01	0.00	72.00				21.00	3.60
	1.71	5.01	0.30	84.00	1.50	87.89			
	4.24	5.01	0.75	45.00	3.76	88.62	88.43		
	8.45	5.01	1.50	52.00	7.52	88.93			
	12.72	5.01	2.25	52.00	11.27	88.62			
	17.17	5.01	3.00	58.00	15.03	87.54			
230 V_{AC}/50 Hz	0.02469	5.01	0.00	86.00				21.01	3.72
	1.78	5.01	0.30	88.00	1.50	84.44			
	4.38	5.01	0.75	44.00	3.76	85.79	87.13		
	8.63	5.01	1.50	51.00	7.52	87.08			
	12.83	5.01	2.25	53.00	11.27	87.86			
	17.12	5.01	3.00	56.00	15.03	87.79			
265V_{AC}/50 Hz	0.02689	5.01	0.00	94.00				21.17	3.75
	1.80	5.01	0.30	91.00	1.50	83.50			
	4.52	5.01	0.75	42.00	3.76	83.13	86.26		
	8.64	5.01	1.50	52.00	7.52	86.98			
	12.89	5.01	2.25	54.00	11.27	87.45			
	17.18	5.01	3.00	56.00	15.03	87.49			

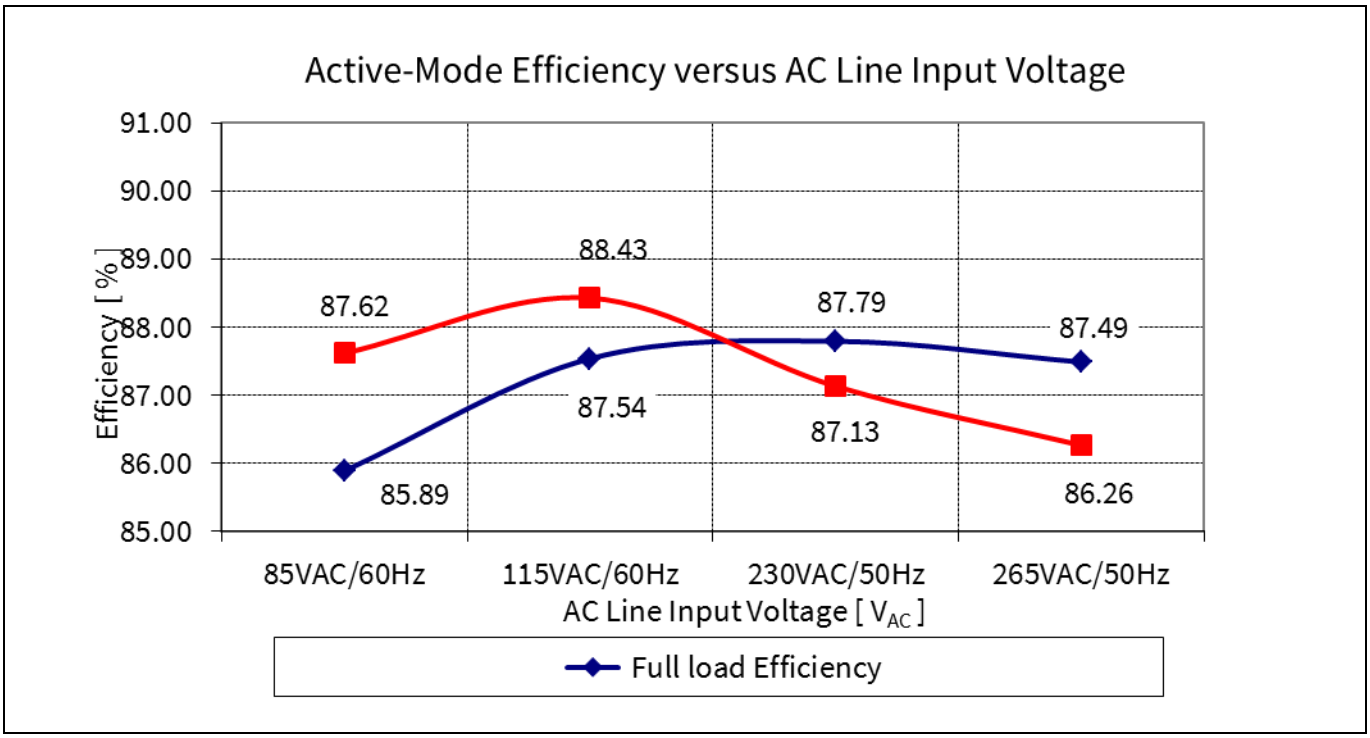


Figure 8 Efficiency vs AC line input voltage

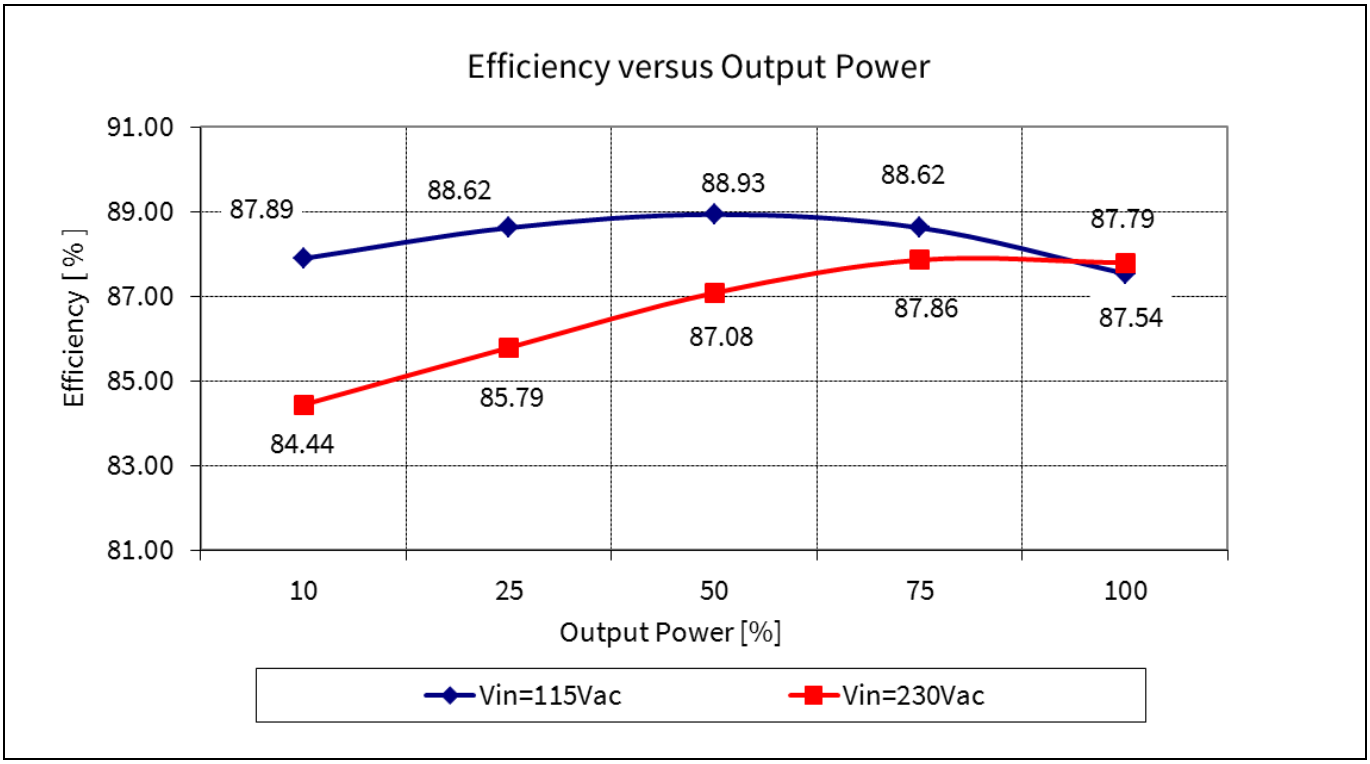


Figure 9 Efficiency vs output power at 115 V_{AC} and 230 V_{AC} line

11.2 Standby power

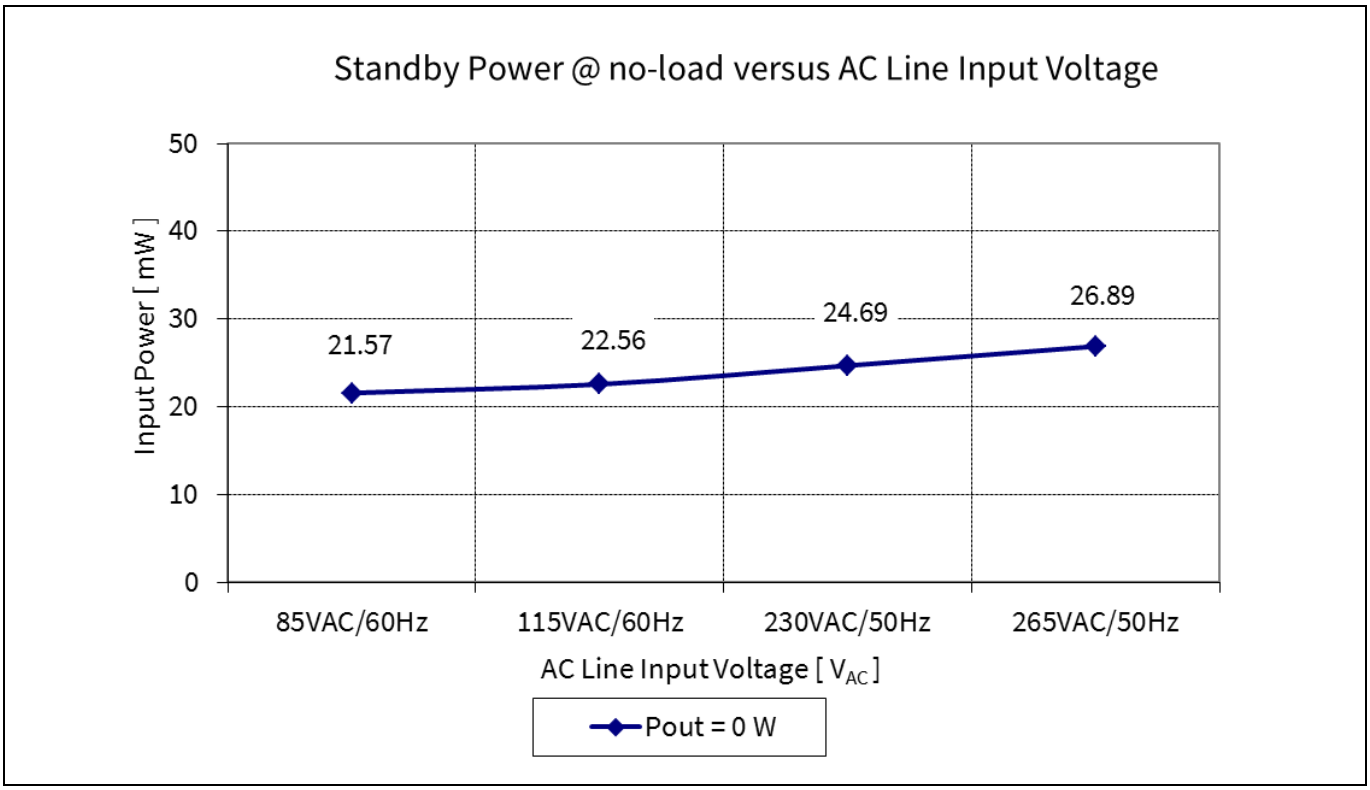


Figure 10 Standby power at no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

11.3 Line regulation

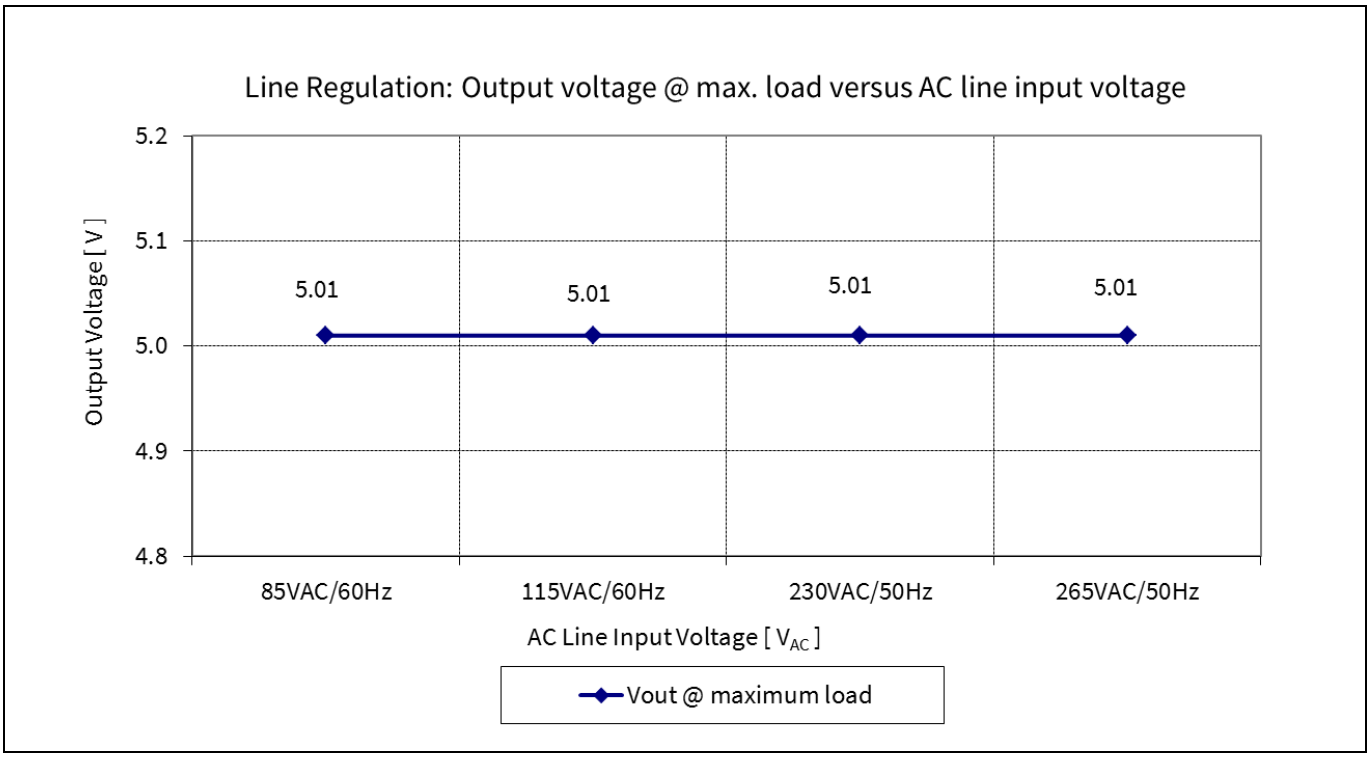


Figure 11 Line regulation Vout at full load vs AC line input voltage

11.4 Load regulation

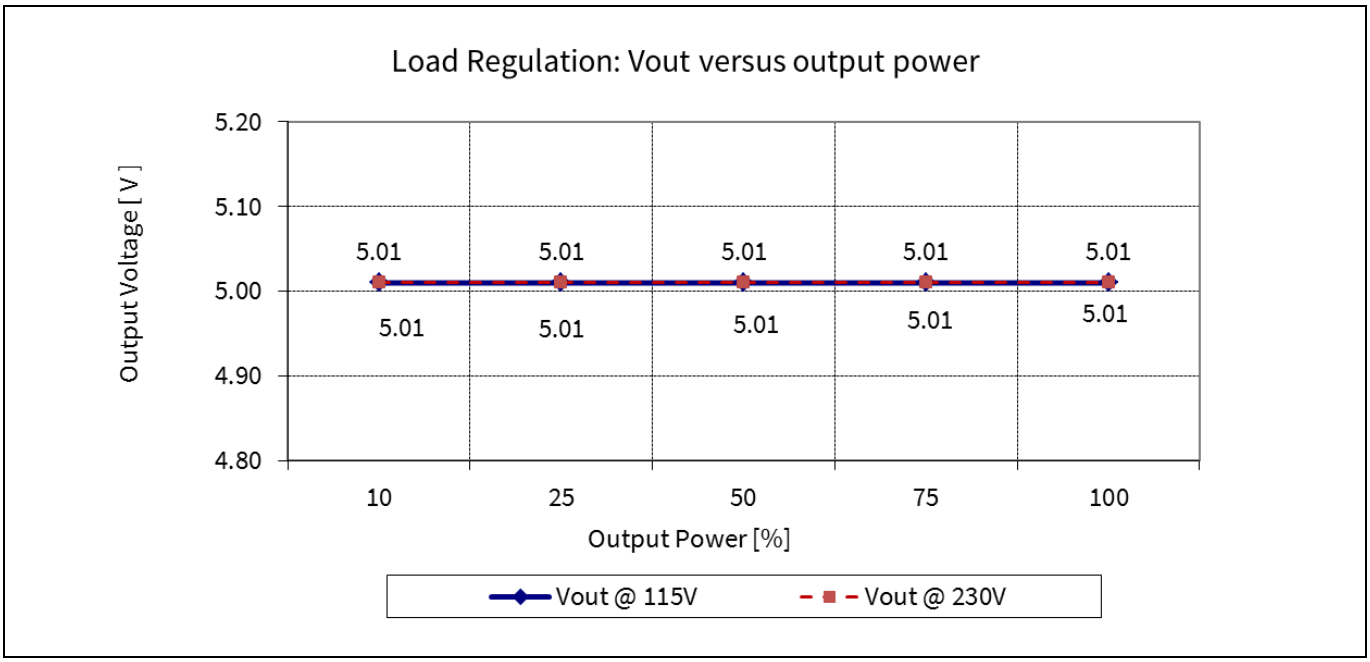


Figure 12 Load regulation V_{out} vs output power

11.5 Maximum input power

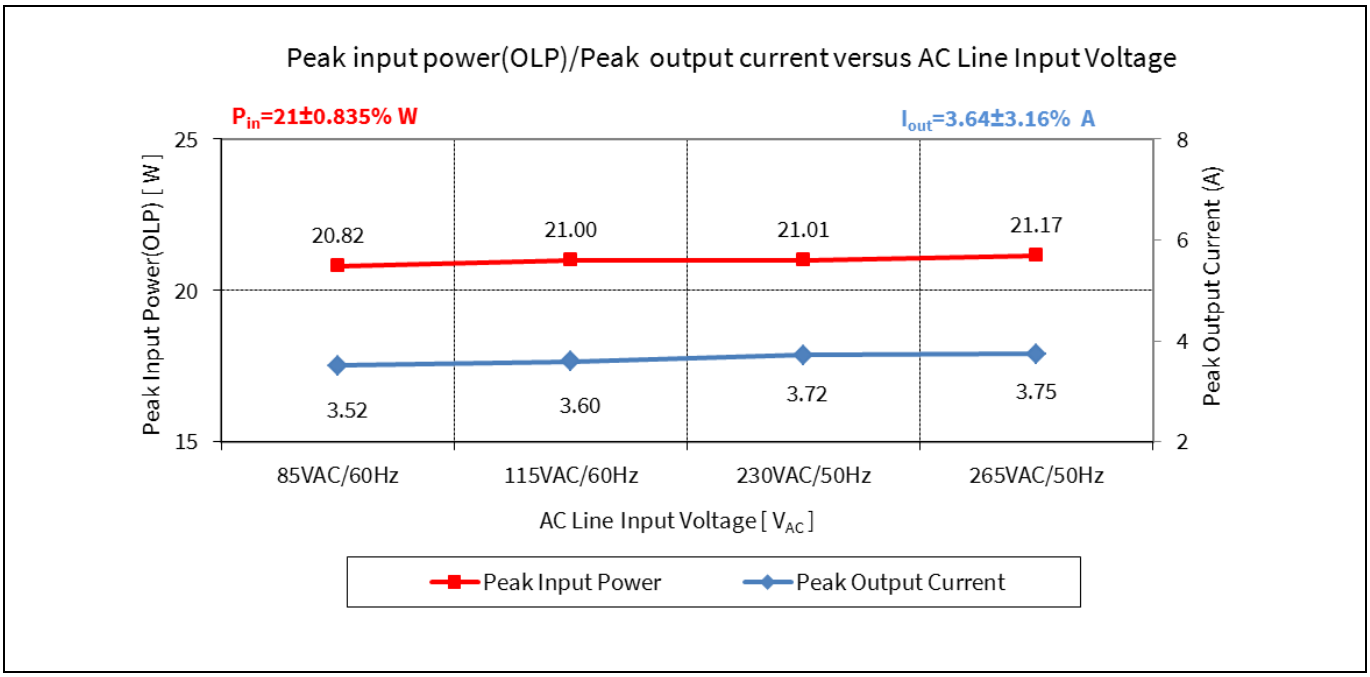


Figure 13 Maximum input power (before over-load protection) vs AC line input voltage

11.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 Level 3 (±8 kV for contact discharge).

11.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 3 (±2 kV for line to earth).

11.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR2503) and followed the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (15 W) with input voltage of 115 V_{AC} and 230 V_{AC}.

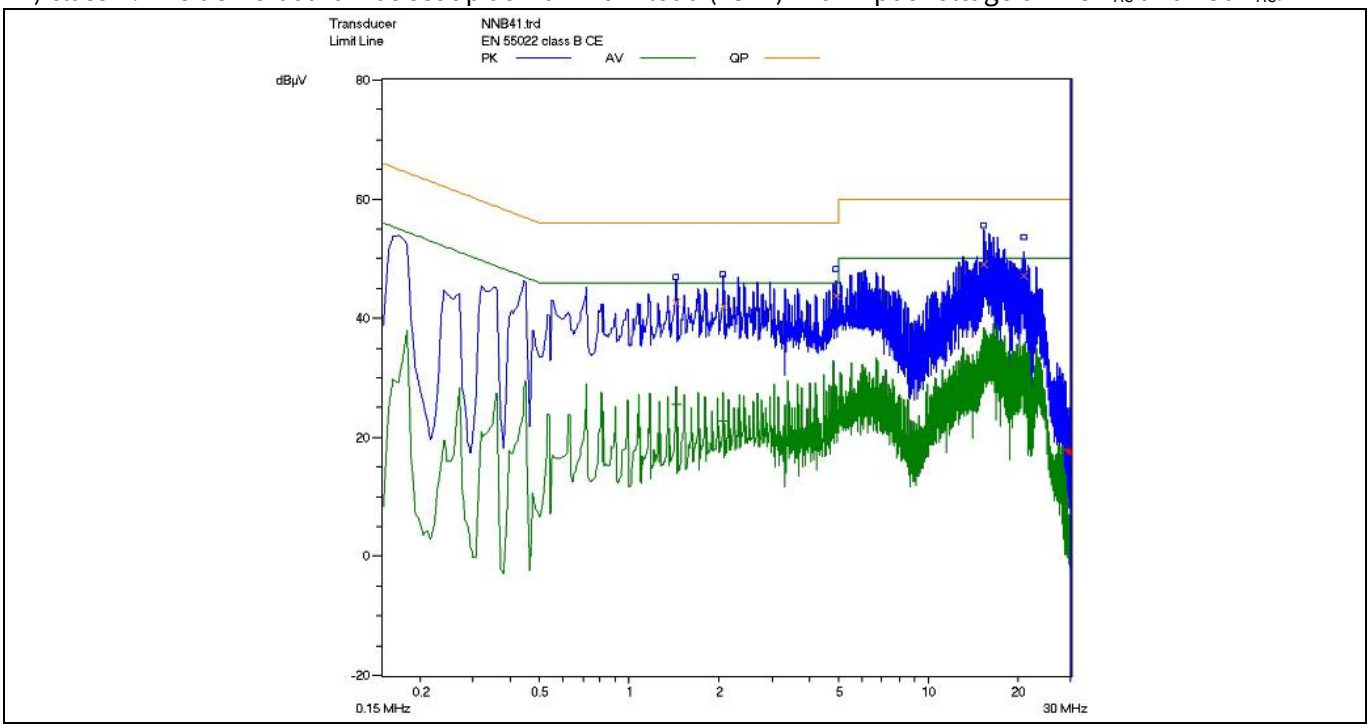


Figure 14 Conducted emissions(Line) at 115 V_{AC} and maximum Load

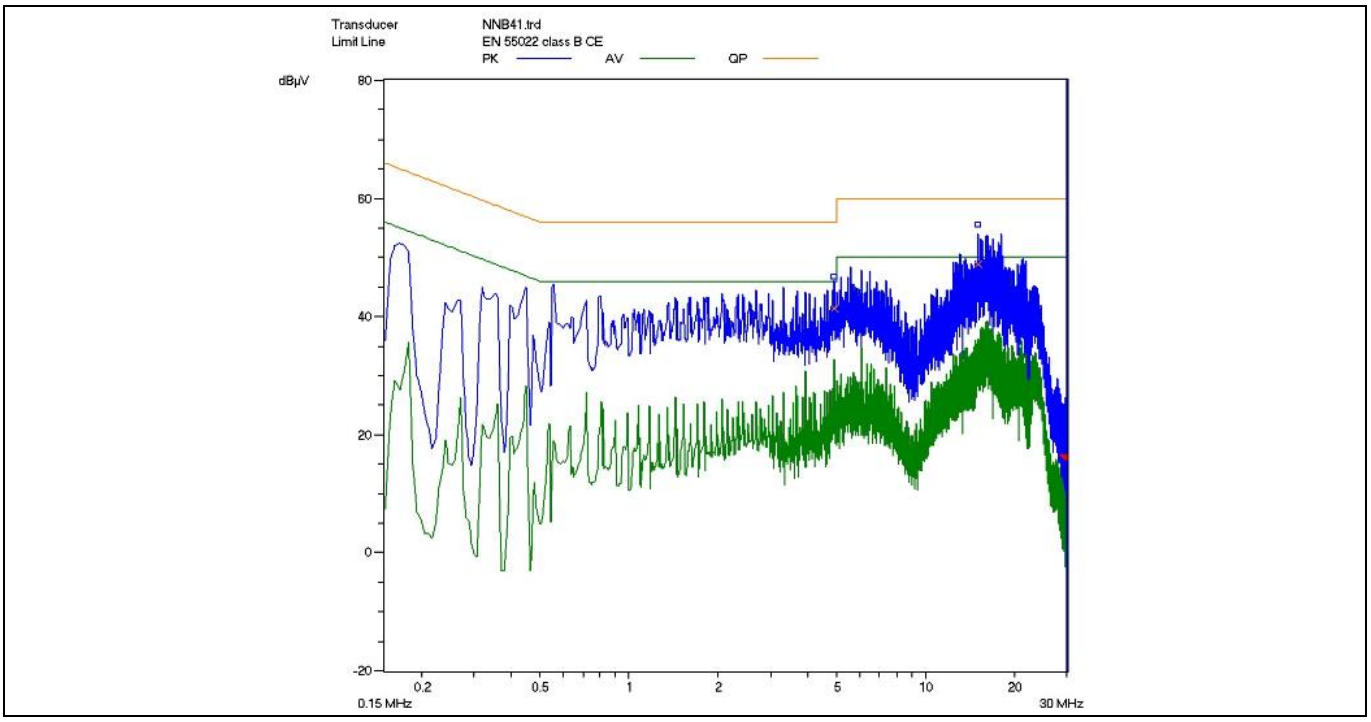


Figure 15 Conducted emissions(Neutral) at 115 V_{AC} and maximum Load

Pass conducted emissions EN55022 (CISPR 22) class B with 10 dB margin for quasi peak limit at low line (115 V_{AC}).

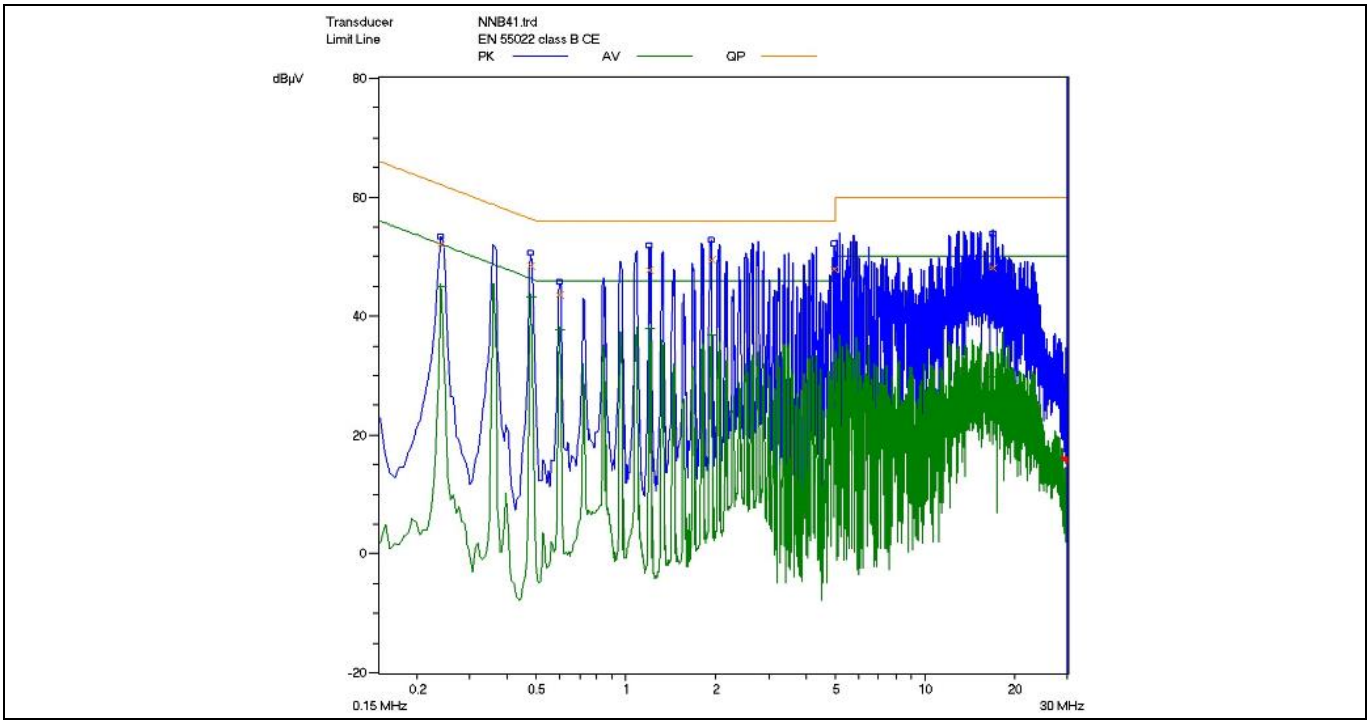


Figure 16 Conducted emissions(Neutral) at 230 V_{AC} and maximum Load

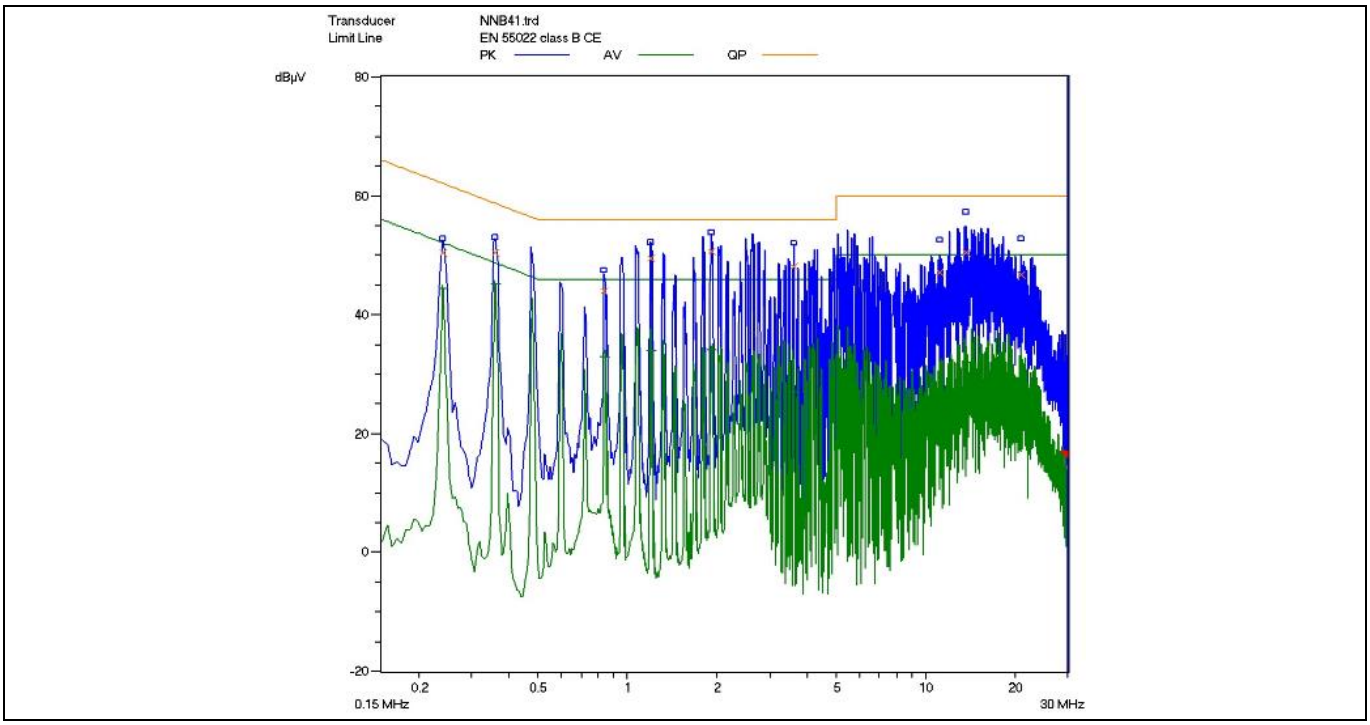


Figure 17 Conducted emissions(Neutral) at 230 V_{AC} and maximum Load

Pass conducted emissions EN55022 (CISPR 22) class B with 6 dB margin for quasi peak limit at high line (230 V_{AC}).

11.9 Thermal measurement

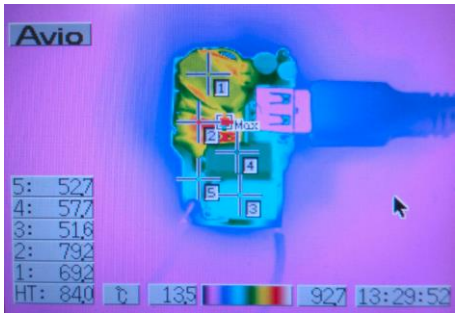
The reference adapter's open frame thermal test was done by thermal infrared camera (TVS-500EX) at the ambient temperature 25 ^{0}C. The thermal measures were taken after two hours running with full load.

Table 4 Thermal measurement of REF-15W_IR_Opti3 ADAPTER

No.	Component	85 V_{AC} & 15 W load (°C)	265 V_{AC} & 15 W load (°C)
1	Q11 (IPS65R1K5CE)	84	90.6
2	Q21 (BSZ100N06LS3 G)	78.5	75.5
3	IC22 (IR1161)	63.3	65.2
4	TR1 (Transformer)	69.2	66.1
5	IC11 (ICE2QS03G)	69.7	66.9
6	BR1 (bridge diode)	66.2	47.8
7	DZD11(Snubber zenor diode)	79.2	77.4
8	C13A (Bulk Cap)	57.7	50.3
9	L11 (Differnetial Choke)	52.7	43.2
10	R14 (Current sense resistor)	48.6	44.9
11	Ambient	25	25

(PCB bottom side, 85 V_{AC} & full load)

(PCB bottom side, 265 V_{AC} & full load)



(PCB top side, 85 V_{AC} & full load)

(PCB top side, 265 V_{AC} & full load)

Figure 18 Infrared thermal image of REF-15W_IR_Opti3 ADAPTER

12 Waveforms and scope plots

All waveforms and scope plots were recorded with a TELEDYNELECROY 606Zi oscilloscope.

12.1 Start up at low and high AC line input voltage with maximum load

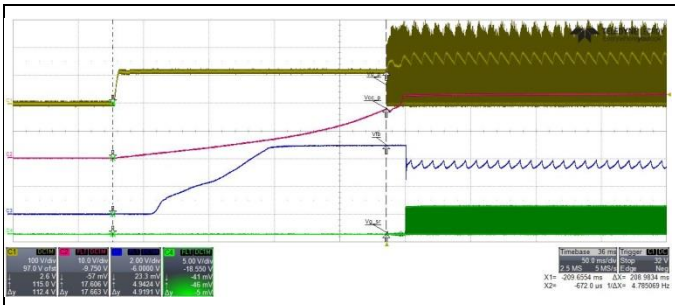
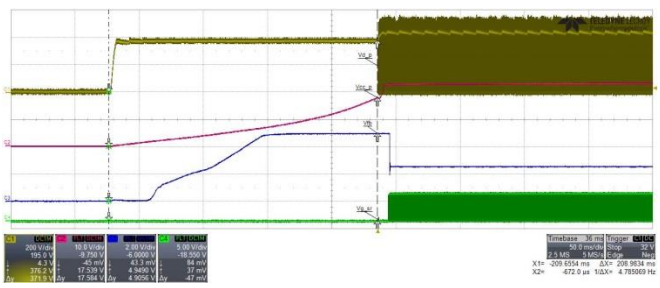
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : SR Gate voltage(V_{G_SR})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : SR Gate voltage(V_{G_SR})
Startup time at 85 V_{AC} & maximum load ≈ 209 ms	Startup time at 265 V_{AC} & maximum load ≈ 209 ms

Figure 19 Start up

12.2 Soft start

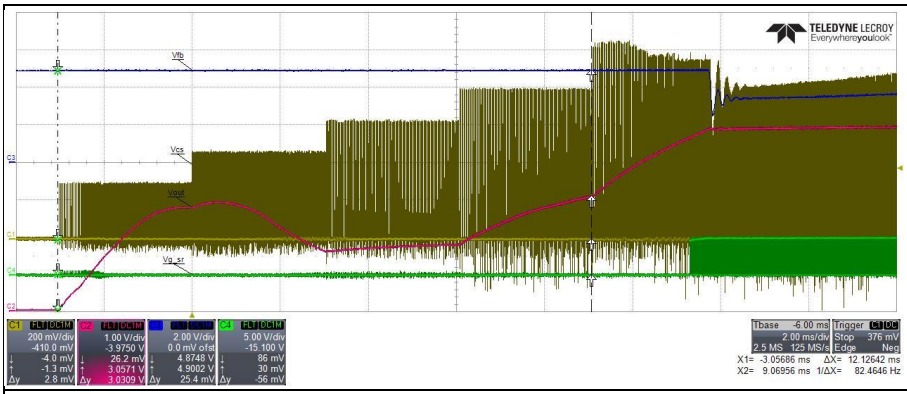

C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Output voltage (V_{out}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : SR Gate voltage(V_{G_SR})
Soft start time at 85 V_{AC} and maximum load ≈ 12 ms

Figure 20 Soft start

12.3 Start up delay and output voltage rise time

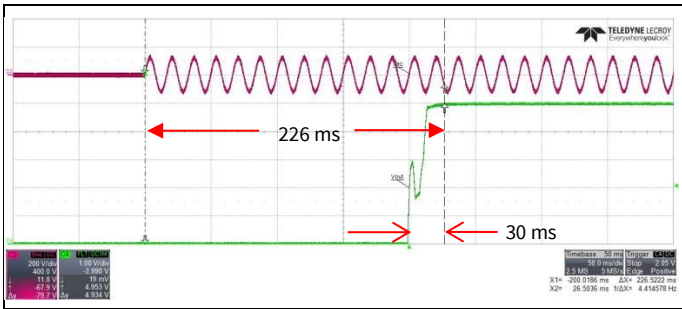
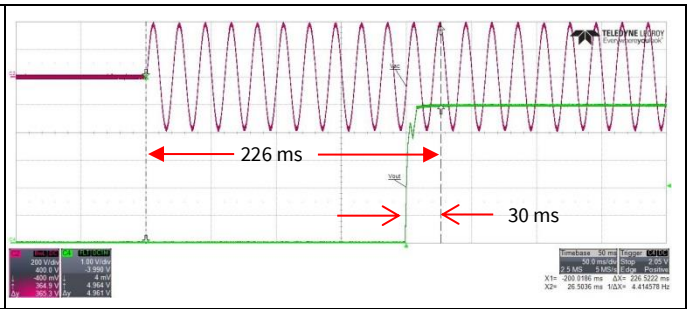
	
C2 (Purple) : Mains AC voltage (V_{AC}) C4 (Green) : Output voltage (V_{out})	C2 (Purple) : Mains AC voltage (V_{AC}) C4 (Green) : Output voltage (V_{out})
85 V_{AC} :start up delay time ≈ 226 ms :output voltage rise time ≈ 30 ms	265 V_{AC} :start up delay time ≈ 226 ms :output voltage rise time ≈ 30 ms

Figure 21 Start up delay and output voltage rise time

12.4 Hold up time

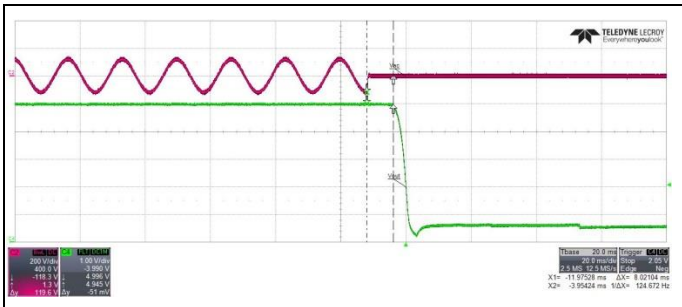
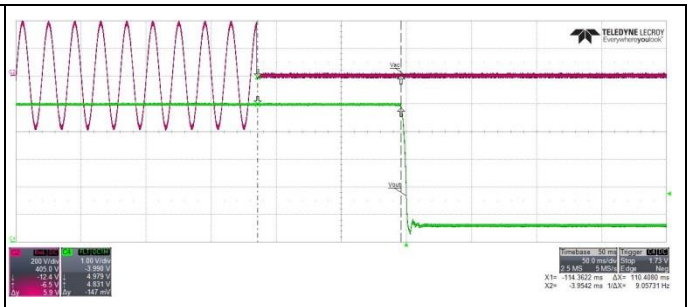
	
C2 (Purple) : Mains AC voltage (V_{AC}) C4 (Green) : Output voltage (V_{out})	C2 (Purple) : Mains AC voltage (V_{AC}) C4 (Green) : Output voltage (V_{out})
85 V_{AC} :hold up time ≈ 8 ms	265 V_{AC} :hold up time ≈ 110 ms

Figure 22 Hold up time

12.5 Drain and current sense voltage at maximum load

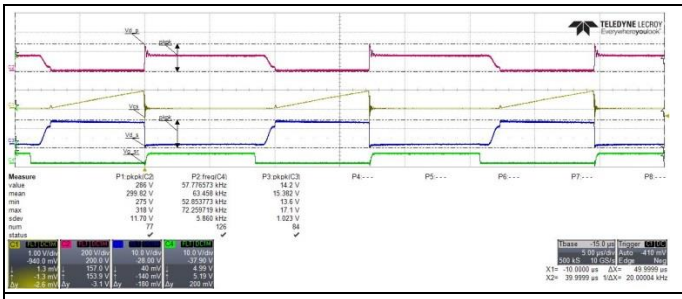
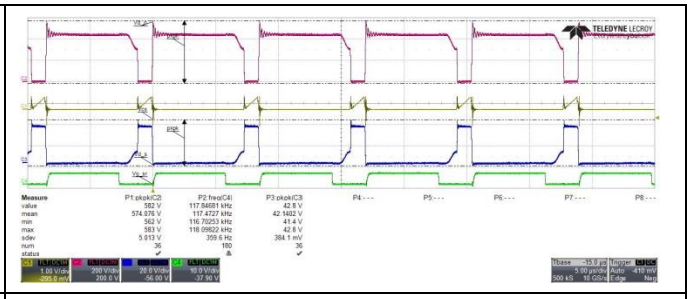
	
C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Drain voltage (V_{Drain}) C3 (Blue) : SR drain voltage (V_{Drain_SR}) C4 (Green) : SR Gate voltage(V_{G_SR})	C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Drain voltage (V_{Drain}) C3 (Blue) : SR drain voltage (V_{Drain_SR}) C4 (Green) : SR Gate voltage(V_{G_SR})
At 85 V_{AC} :V_{Drain_peak} ≈ 318 V :$V_{Drain\_SR\_peak}$ ≈ 17 V	At 265 V_{AC} : V_{Drain_peak} ≈ 583 V :$V_{Drain\_SR\_peak}$ ≈ 42 V

Figure 23 Drain and current sense voltage at maximum load

12.6 Zero crossing point during normal operation

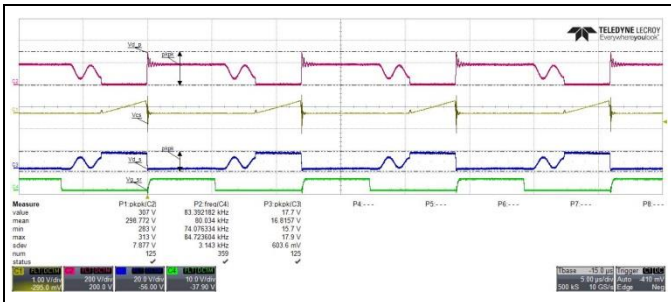
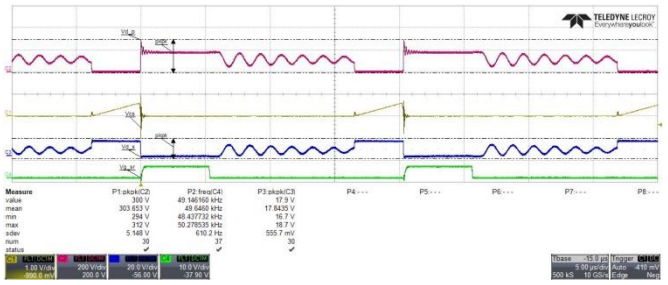
	
C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Drain voltage (V_{Drain}) C3 (Blue) : SR drain voltage (V_{Drain_SR}) C4 (Green) : SR Gate voltage(V_{G_SR})	C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Drain voltage (V_{Drain}) C3 (Blue) : SR drain voltage (V_{Drain_SR}) C4 (Green) : SR Gate voltage(V_{G_SR}))
At 85 V_{AC} , 2nd zero crossing	At 85 V_{AC} , 7th zero crossing

Figure 24 Zero crossing

12.7 Load transient response (Dynamic load)

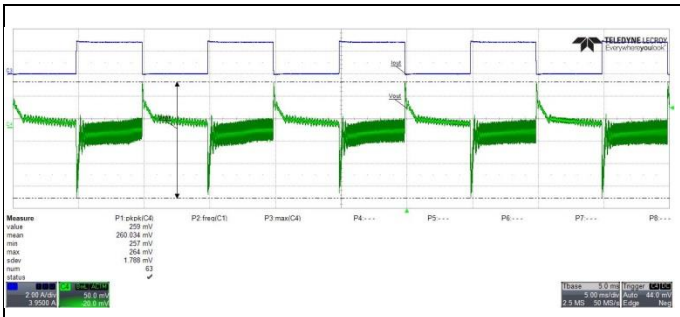
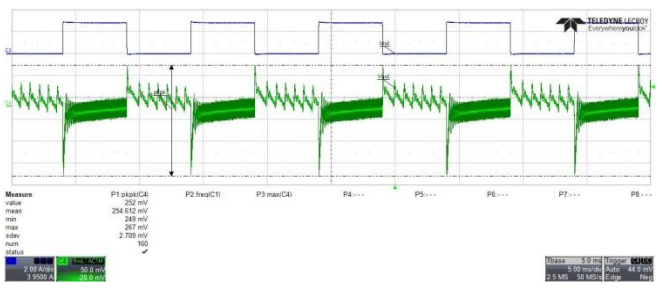
	
C3 (Blue) : Output current (I_{out}) C4 (Green) : Output ripple voltage (V_{out_ripple})	C3 (Blue) : Output current (I_{out}) C4 (Green) : Output ripple voltage (V_{out_ripple})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 264 mV (Load change from 50 mA to 3 A at 85 V_{AC},100 Hz,1.5 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 267 mV (Load change from 50 mA to 3 A at 85 V_{AC},100 Hz,1.5 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 25 Load transient response

12.8 Output ripple voltage at maximum load

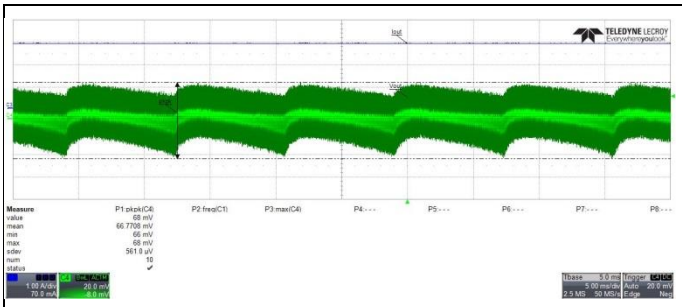
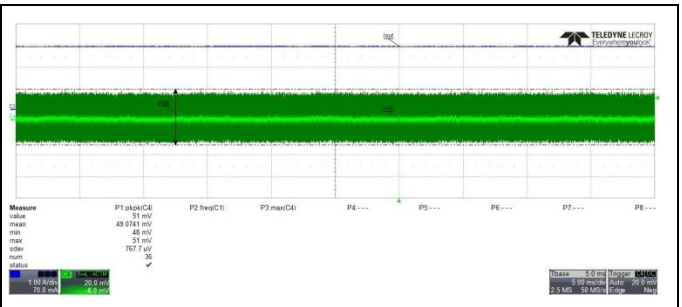
	
C3 (Blue) : Output current (I_{out}) C4 (Green) : Output ripple voltage (V_{out_ripple})	C3 (Blue) : Output current (I_{out}) C4 (Green) : Output ripple voltage (V_{out_ripple})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 70 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 53 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 26 Output ripple voltage at maximum load

12.9 Output ripple voltage at burst mode 1 W load

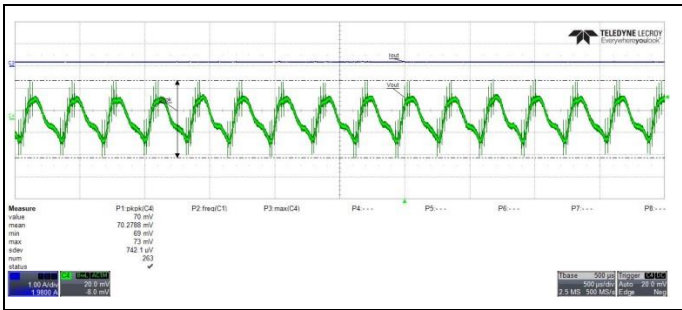
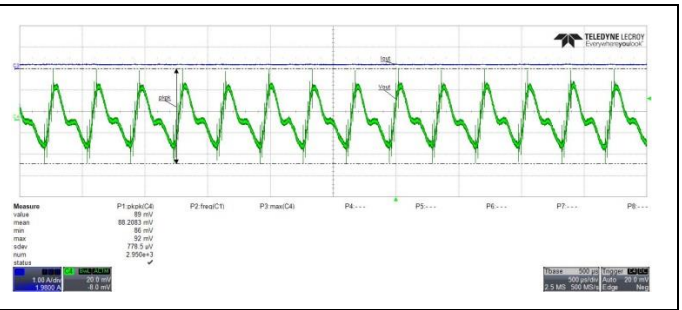
	
C3 (Blue) : Output current (I_{out}) C4 (Green) : Output ripple voltage (V_{out_ripple})	C3 (Blue) : Output current (I_{out}) C4 (Green) : Output ripple voltage (V_{out_ripple})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 39 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 92 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 27 Output ripple voltage at burst mode 1 W load

12.10 Active burst mode

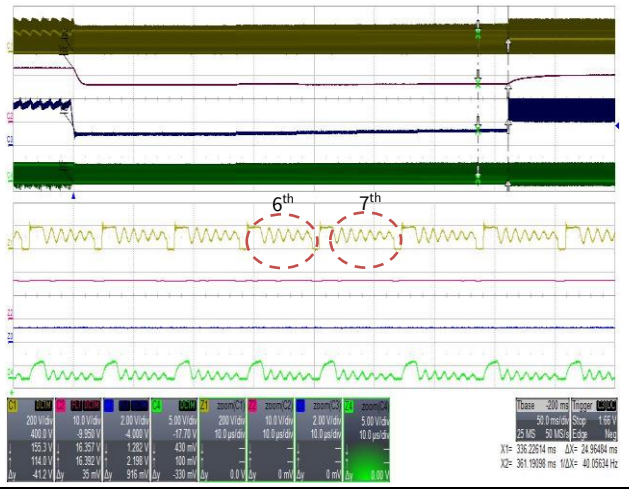
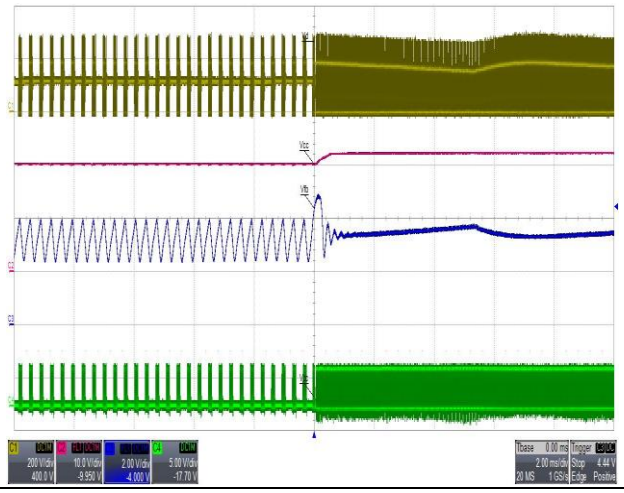
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Zero crossing voltage (V_{ZC})	C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : Zero crossing voltage (V_{ZC})
Condition: V_{FB}<1.2 V, N_{ZC}=7 and $t_{blanking}$ =24 ms (load change form full load to 1 W load)	Condition: V_{FB} > 4.5 V (load change form 1W load to full load)

Figure 28 Active burst mode at 85 V_{AC}

12.11 Over load protection (Auto Restart Mode)

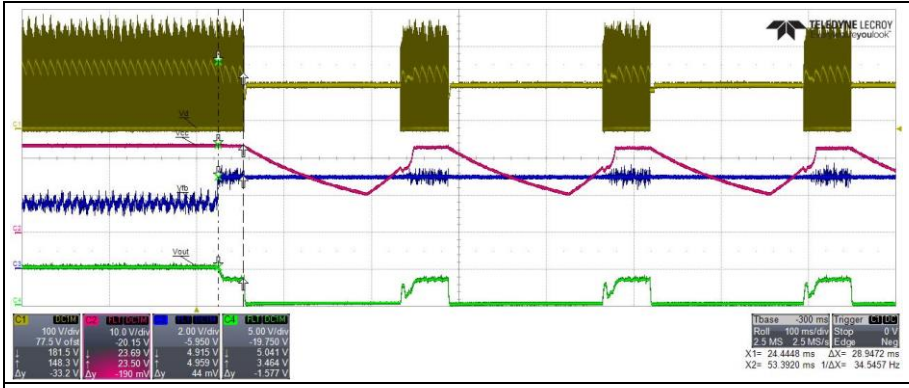
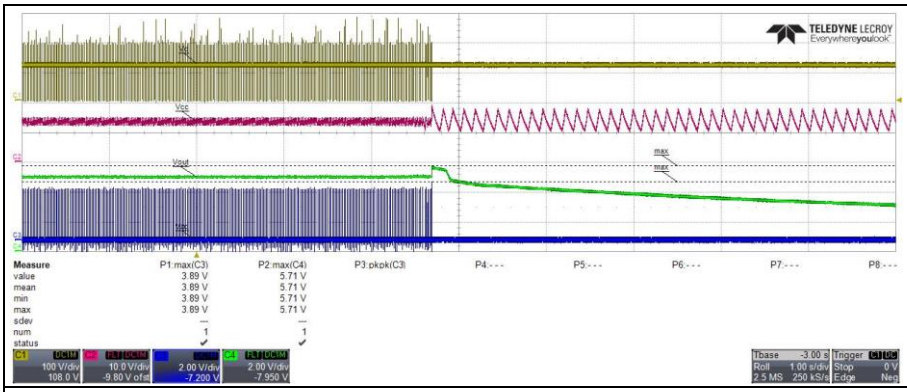

C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Output voltage (V_{out})
Condition: V_{FB} > 4.5 V & last for 30 ms blanking time (output load change from 3 A to 4.5 A at 85 V_{AC})

Figure 29 Over load protection

12.12 Output overvoltage protection (Latched mode)

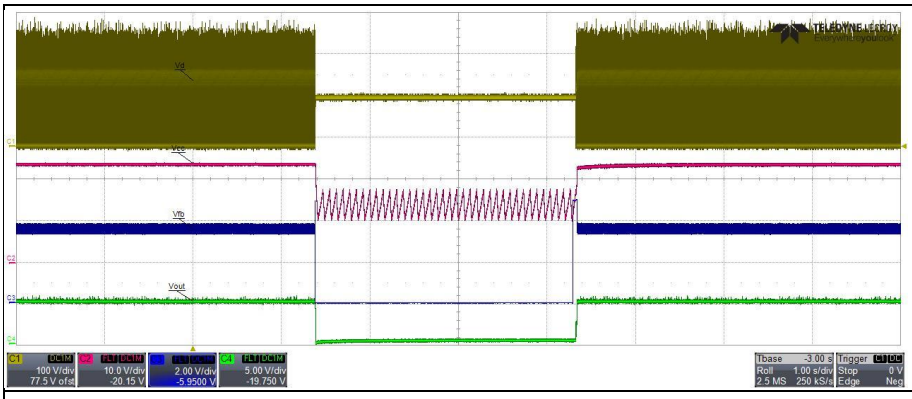


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{ZC})
C4 (Green) : Output voltage (V_{out})

Condition: V_{out} > 5.5 V (V_{ZC}>3.7 V)
(short R26 during system operation at no load and 85 V_{AC})

Figure 30 Output overvoltage protection

12.13 VCC under voltage/Short optocoupler protection (Auto restart mode)



C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C4 (Green) : Output voltage (V_{out})

Condition: V_{CC} <10.5 V
(short the transistor of optocoupler during system operating at full load and 85 V_{AC})

Figure 31 V_{VCC} under voltage/short optocoupler protection

13 References

[1] ICE2QS03G data sheet, Infineon Technologies AG
[2] IR1161 data sheet, International Rectifier
[3] IPS65R1K5CE data sheet, 650V CoolMOS™ CE Power Transistor, Infineon Technologies AG
[4] BSZ100N06LS3 G data sheet, 60V OptiMOS™ 3 Power Transistor, Infineon Technologies AG
[5] BAS21-03W data sheet, Infineon Technologies AG
[6] ICE2QS03G design guide. [ANPS0027]
[7] IR1161 dedsign notes, International Rectifier

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Major changes since the last revision

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