600 V CoolGaN™ half-bridge evaluation platform featuring GaN EiceDRIVER™

About this document

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Scope and purpose

This Application Note explains how to set-up and use the 600 V CoolGaN™ half-bridge evaluation board. The board features a half-bridge of 70 mΩ GaN power transistors, and a pair of EiceDRIVER™ GaN gate drivers, along with input logic that provides adjustable deadtime. Using an external inductor, the board can be configured for buck or boost-mode, double-pulse testing or continuous PWM operation, hard or soft-switching at power levels to several kW and frequencies into the MHz.

Intended audience

This document is intended for power electronic engineers and designers who are already familiar with MOSFET or IGBT-based converters, inverters and gate drivers, who are interested in looking at the similarities and differences of GaN power transistors compared to their Silicon counterparts.

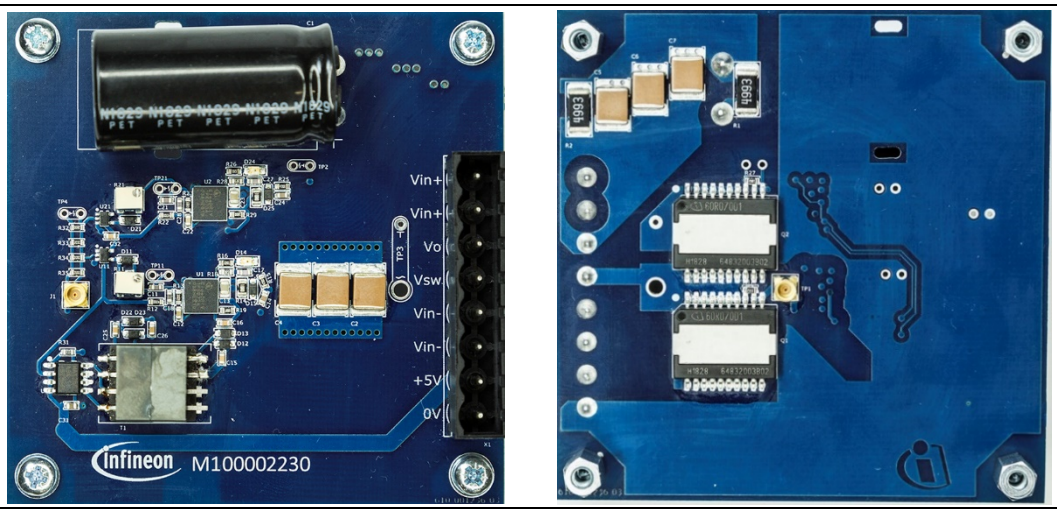

Figure 1 Front and back view of the CoolGaN™ half-bridge evaluation platform

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1 Introduction

This 600 V Gallium Nitride (GaN) half-bridge evaluation board enables easy, rapid setup and test of CoolGaN™ transistors along with the dedicated GaN EiceDRIVER™ isolated gate driver IC. The generic topology is configurable for boost or buck operation, pulse testing or continuous full-power operation. Test points provide easy access to connect signals to an oscilloscope for measuring the switching performance of CoolGaN™ transistors and gate driver. This board saves the user the time to design their own gate driver and power circuit to evaluate GaN power transistors.

The half-bridge circuit board has a single PWM input intended for connection to a 50 Ω pulse or signal generator. Board power comes from a single 5 V supply input, which powers everything including the isolated gate driver power supplies. Deadtime between the high and low-side is pre-set to 100 ns, but is adjustable via trimpots. An external (user-supplied) inductor connects to the supplied pluggable terminal-block connector. The output and bus voltage can range up to 450 V, limited by the capacitor rating. This half-bridge can switch continuous currents of 12 A, and peak currents of 35 A, hard or soft-switching. Operating frequency can be up to several MHz, depending on transistor dissipation (limited to about 15 W per device with appropriate heatsink and airflow).

1.1 Evaluation board specifications

Table 1 Evaluation board specifications and limits

Parameter	Values			Unit	Note
	Min.	Typ.	Max.		
Vcc input voltage	4.8	5.0	5.2	V	
Vcc input current	50	100	250	mA	Highest current at maximum frequency
PWM logic input levels	0		5	V	Standard 5 V TTL levels, 50 Ω terminated
Vin+ to Vin-	0	390	450	V	Limited by capacitor voltage ratings
VO to Vin-	0		450	V	(There may be ±30 V spikes appearing on Vo)
Transistor current, DC			12	A	Keep case temp below 125 °C
Transistor current, pulse			35	A	Keep case temp below 125 °C
Transistor power dissipation			15	W	With heatsink, airflow to keep T_{case}<125 °C
Operating frequency	(DC)		3	MHz	Within dissipation, temperature limits
PWM pulse width	130		∞	ns	With 100 ns deadtime setting
V_{SW} transition time		7		ns	8 A load, 10-90% rise, fall times
Gate drive voltage levels	-8		4	V	These are not limits, typical – and + values
Deadtime adjustment range	0		180	ns	Default setting is 100 ns. If longer deadtime is necessary, C11, 21 can be increased, thereby extending the adjustment range.

The PCB dimensions are 76x76 mm.

2 Functional description

A typical block diagram is shown in Figure 2 for a double-pulse test application setup. A 5 V power supply provides the circuit power, and a 0-400 V power supply provides the DC bus voltage. The input PWM signal is provided by a lab pulse generator. A test inductor is then connected from the DC bus to the switch-node output. An oscilloscope can then be used to measure the inductor current (with a current probe), switch-node voltage or any other signal on the board. The available test points are described in table 2.

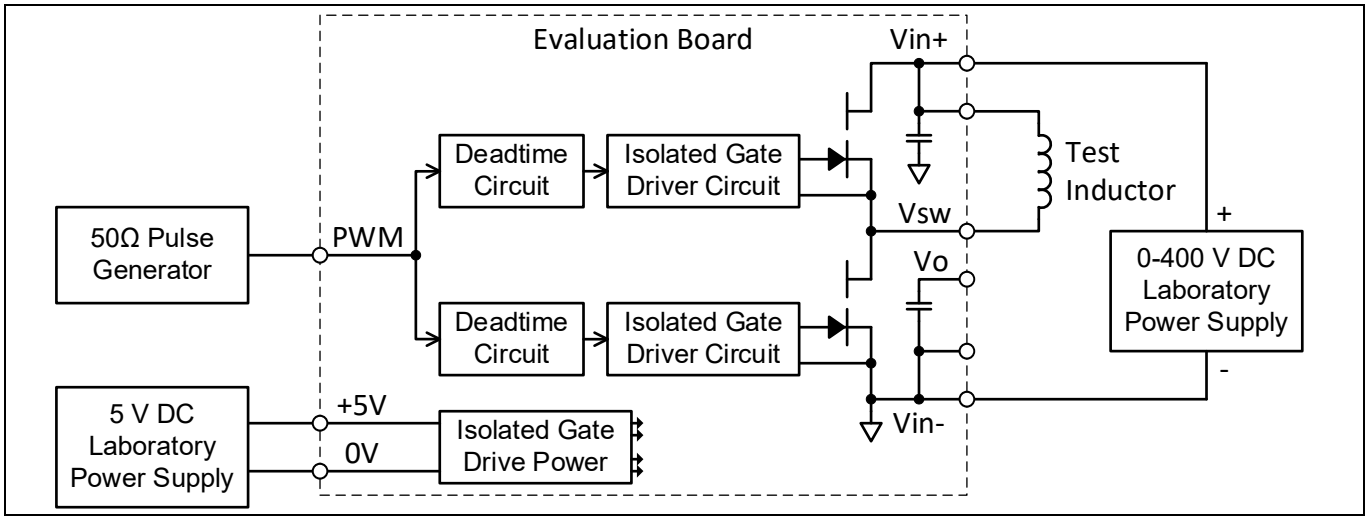

Figure 2 Evaluation board typical application example (double-pulse test)

Note that the inductor can be connected to either the positive DC bus as shown in Figure 2, or the negative bus (Vin-) for inverted double-pulse where the high-side is the active switch, and the low-side is the freewheeling synchronous rectifier (Figure 3).

The evaluation board can also be easily configured as a buck or boost topology. See section 4.2 for further details.

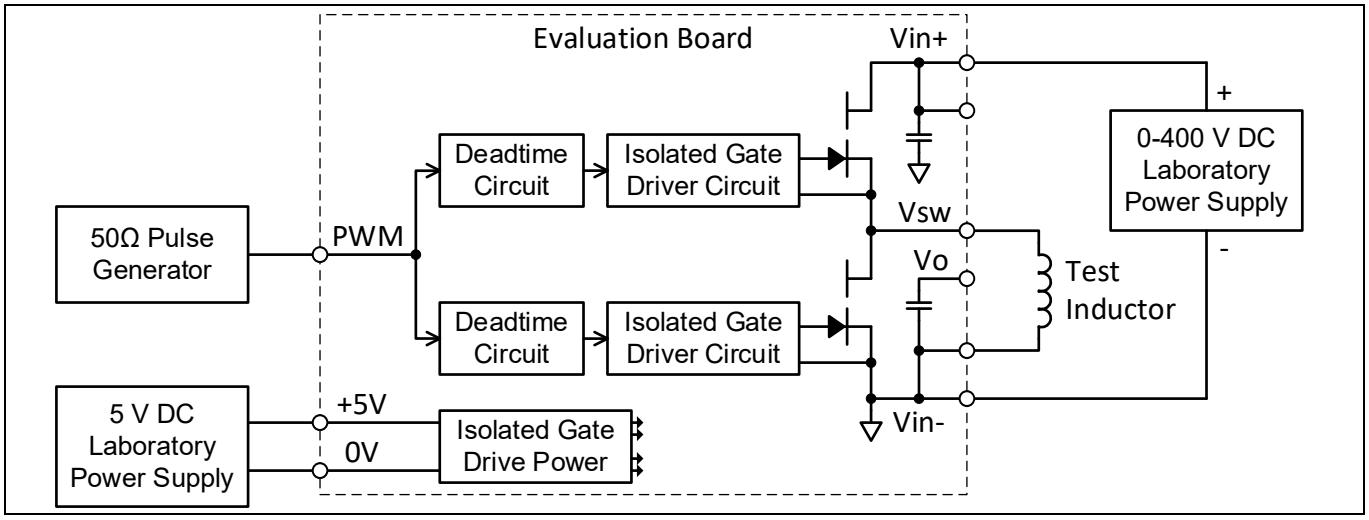

Figure 3 Evaluation board connected for inverted double-pulse test

3 Circuit description

The following sections explain each portion of the circuit in detail

3.1 Input logic and deadtime generator

Logic level PWM input connects to J1 (MMCX connector) which is terminated by 50 Ω (the parallel combination of R32-35). The input is buffered by noninverting buffer U11 for the high-side, and inverting buffer U21 for the low-side. These buffers are expecting standard logic-level input voltage from the PWM source, low ≤0.8 V and high 2-5 V. When the PWM input is low, the switch node V_{SW} is low (the low side GaN transistor turns on). Conversely, when the PWM input is high, the V_{SW} node is driven high as the high-side GaN transistor turns on.

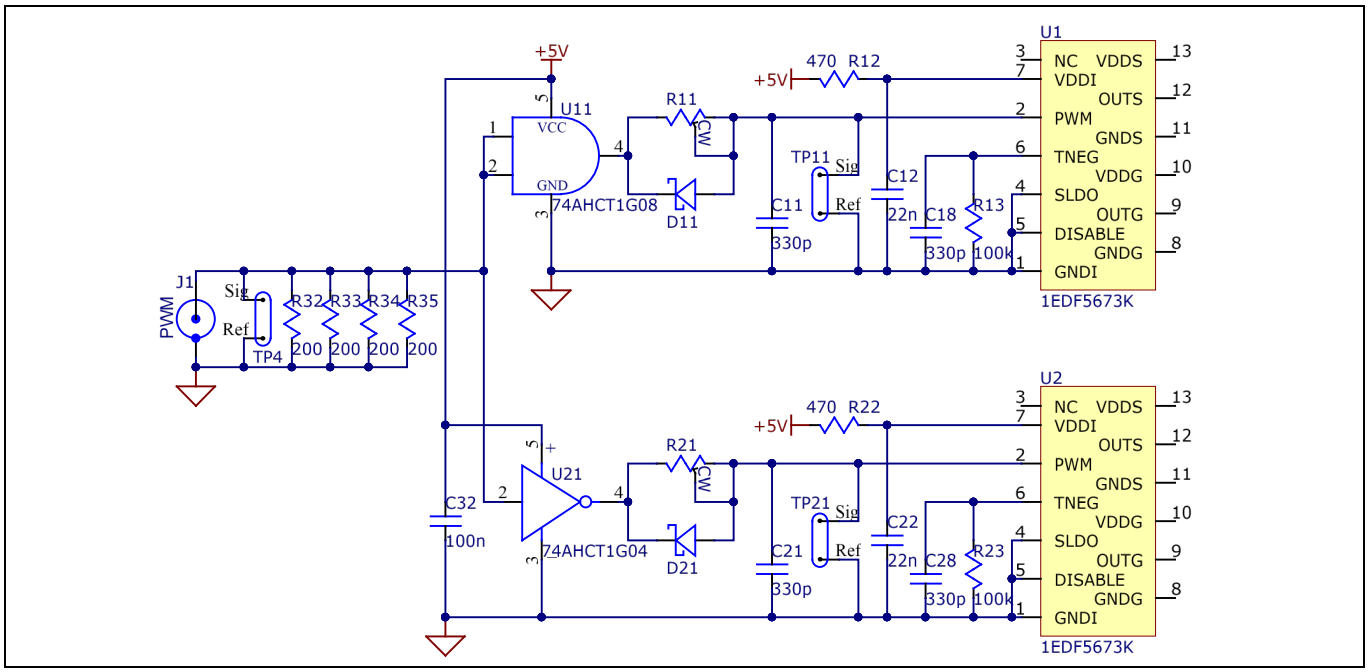

Figure 4 Input logic and deadtime generator

The purpose of the deadtime circuit is to make sure that the high and low-side GaN transistors are never on simultaneously. The deadtime should be set long enough that the high-side always fully turns-off before the low-side turns-on (with some margin), and vice-versa. A simple adjustable RCD delay circuit generates the deadtime. Whenever U11 or U21 outputs a positive (turn-on) edge, the Rx1-Cx1 lowpass filter delays the signal by the RC time constant to the Schmitt-trigger PWM input of the respective gate driver IC. But the turn-off edge is not delayed because the Schottky diodes Dx1 bypass the resistor. Thus, each driver IC input has a delayed turn-on edge, and a non-delayed turn-off edge. Even though the gate driver is capable of recognizing and delivering an input pulse as short as 18 ns, the deadtime circuit will cause such a short pulse to be ignored.

The practical minimum output pulse width at V_{SW} is about 30 ns. This would occur with an input PWM pulse width of 130 ns (minus the 100 ns deadtime as described above). Any input pulse width shorter than this is not recommended, as the resulting output pulse is so small it is really no longer effective. For extremely short output pulse widths, contact your local Infineon applications support team to discuss gate drive circuit optimization for the specific requirement.

The TNEG pins of U1 and U2 are connected to timing resistors R13 and R23 respectively. These resistors program the duration of the negative off voltage as explained in section 3.7 of the 1EDF5673K datasheet. 100 k sets the negative gate voltage timing to 180 ns. This value works well with the pre-set deadtime of 100 ns. If you adjust the deadtime to longer than 100 ns, then R13 and R23 should also be increased to ensure that the

negative gate voltage duration is always longer than the programmed deadtime. C18 and C28 are not mandatory and are not shown on the 1EDF5673K datasheet, but they can help reduce capacitively-coupled fast switching transient noise (due to fast dv/dt) injection into the TNEG pins, which can result in shift or “jitter” of the negative gate voltage timing.

The 5 V input power (VDDI) to the two gate driver ICs is bypassed with a 22 nF high-frequency bypass capacitor (Cx2), along with a 470 Ω resistor. This is per the recommendation in the gate driver datasheet to properly bias the built-in 3.3 V shunt regulator.

Note: If the PWM frequency is expected to exceed 1 MHz, then R12 and R22 should be reduced from 470 Ω to 390 Ω. Otherwise there may not be sufficient current to maintain 3.3 V regulator bias.

3.2 Isolated gate driver power supply

Power for the gate drivers is provided by a simple isolated DC-DC converter shown in Figure 5. It takes the +5 V input and provides two isolated 8 V outputs (VDD1-VSS1, and VDD2-VSS2). A small transformer T1 provides low-capacitance isolation and voltage scaling. The primary of T1 is driven by U31, a MAX256 isolated power supply driver. It provides 50% duty-cycle PWM, current-limited, balanced voltage to the transformer at about 500 kHz. The secondary sides are both voltage doublers consisting of Dx2, Dx3, Cx5, and Cx6. The voltage doublers are used instead of straight rectifiers because this reduces the transformer turns ratio, thus providing lower leakage inductance for better load regulation. A small green LED Dx4 provides a visible indication that both high and low-side bias supplies are functioning.

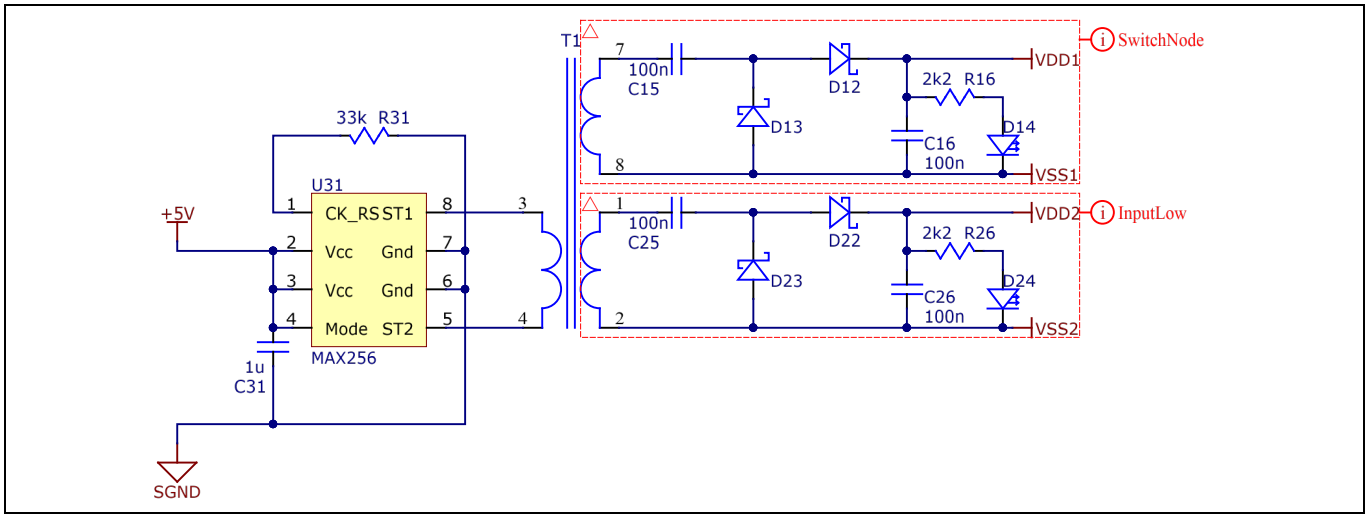

Figure 5 Isolated gate driver power supply

3.2.1 Gate driver power supply transformer

The transformer used in the gate driver power supply is specifically designed to operate with the driver IC U31 (in Figure 5) at 500 kHz, with the appropriate turns ratio to provide the twin isolated 8 V outputs with the doubler circuit. Moreover, the winding arrangement balances low inter-winding capacitance with good coupling (low leakage inductance) and >1000 V isolation. The low capacitance is important for minimizing common-mode current injection due to fast switching transients, and the low leakage helps with open-loop output voltage regulation.

The transformer is based on a Ferroxcube EP10-3C96 ungapped core set. The matching EP10 single-section bobbin is a part number CSHS-EP10-1S-8P-T. All 3 windings are made using 32 AWG magnet wire. The two

secondary windings are 9 turns each, and the primary is 10 turns, resulting in a magnetizing inductance of 87 µH. For full construction detail, contact your local Infineon applications support team.

3.3 Gate drive circuit

The output side of the gate driver circuit is shown in Figure 6. As explained in the GaN EiceDRIVER™ datasheet, the gate driver contains two separate drive circuits, one (OUTG) connected to the CoolGaN™ gate, and the other (OUTS) connected to the CoolGaN™ Kelvin source. VDDx is bypassed to VSSx with a 100 nF capacitor Cx3. The gate RC network described in the datasheet consists of Rx4, Cx4 and Rx5. The small Schottky diode Dx5 provides a low-impedance return-path for faster gate turnoff, effectively bypassing Rx4.

Note that this circuit has an extra RC lowpass filter not shown in the datasheet, between OUTS and the Kelvin source of the GaN. This circuit (Rx8 and Cx7) can help to provide a “cleaner” looking Vgs gate drive voltage: the rise and fall time of the OUTS pin is very fast, and the added 3.3 ns time-constant helps to keep high-frequency ringing to a minimum. These components are optional, and can be effectively removed by eliminating Cx7 and replacing Rx8 with a 0 Ω jumper.

Similarly, Rx9 is an optional 1Ω damping resistor that can help to provide slightly overdamped voltage waveforms at the gate. It can also be eliminated by replacing it with a 0Ω jumper if minimum component count is desired. Rx7 is a standard 10 k gate pull-down resistor that helps ensure the gate-source voltage remains at zero even when the gate driver is unpowered.

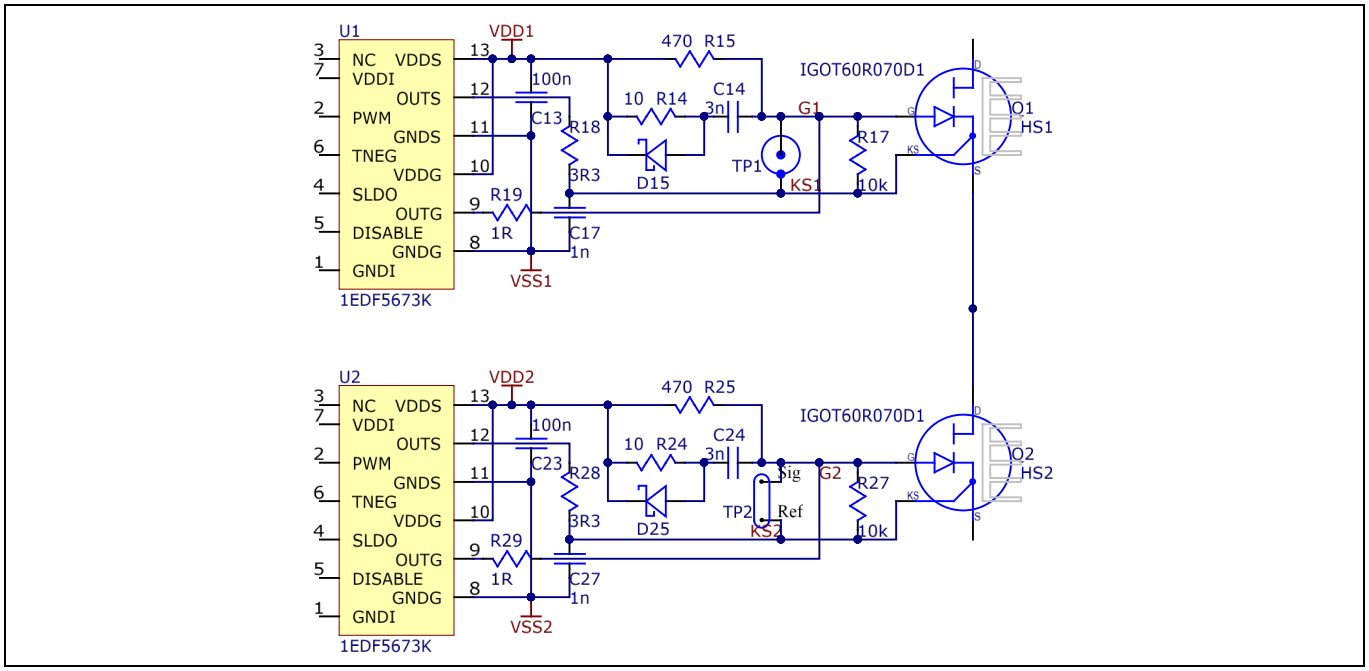

Figure 6 Gate driver output section

3.4 Half-bridge output circuit

GaN transistors Q1 and Q2 form the high and low-side transistors of the half-bridge, as shown in Figure 7. The drain of Q1 is connected to the DC bus (Vin+). Capacitors C2, 3, 4 are high-frequency ceramic bypass capacitors, and C1 is the bulk electrolytic bus capacitor. This capacitive network along with a low-inductance power-loop layout provides an extremely low-impedance bus with very little overshoot or ringing, as evidenced by the waveforms in Figure 14, where you can see 30 A commutating to the bus in a few ns, with less than 50 V overshoot. R1 is a bleeder resistor that drains the bus capacitor charge when the circuit is disconnected from a power supply.

Attention: ***Normally the bus capacitor is discharged when the lab power supply is switched-off. But if the power connector is removed while the capacitor is charged (not recommended!), the bus capacitor can store high voltage and takes several minutes to dissipate. Be sure to wait until the capacitor voltage is at a safe level before handling the board.***

There is a second DC bus labeled “Vo.” It is intended to be used as the output bus when the circuit is configured as a buck converter. It provides a convenient way to connect the inductor back to a low-impedance DC bus and minimize high-frequency voltage ripple due to the inductor ripple current. The Vo bus also has a bleed-down resistor to drain the bus capacitors when it is disconnected. See Figure 9 for the connections in this mode.

The evaluation board can also be configured for boost-mode operation. In that case, Vo becomes the input voltage, and Vin+ becomes the output bus. See section 4.2.3 for complete details.

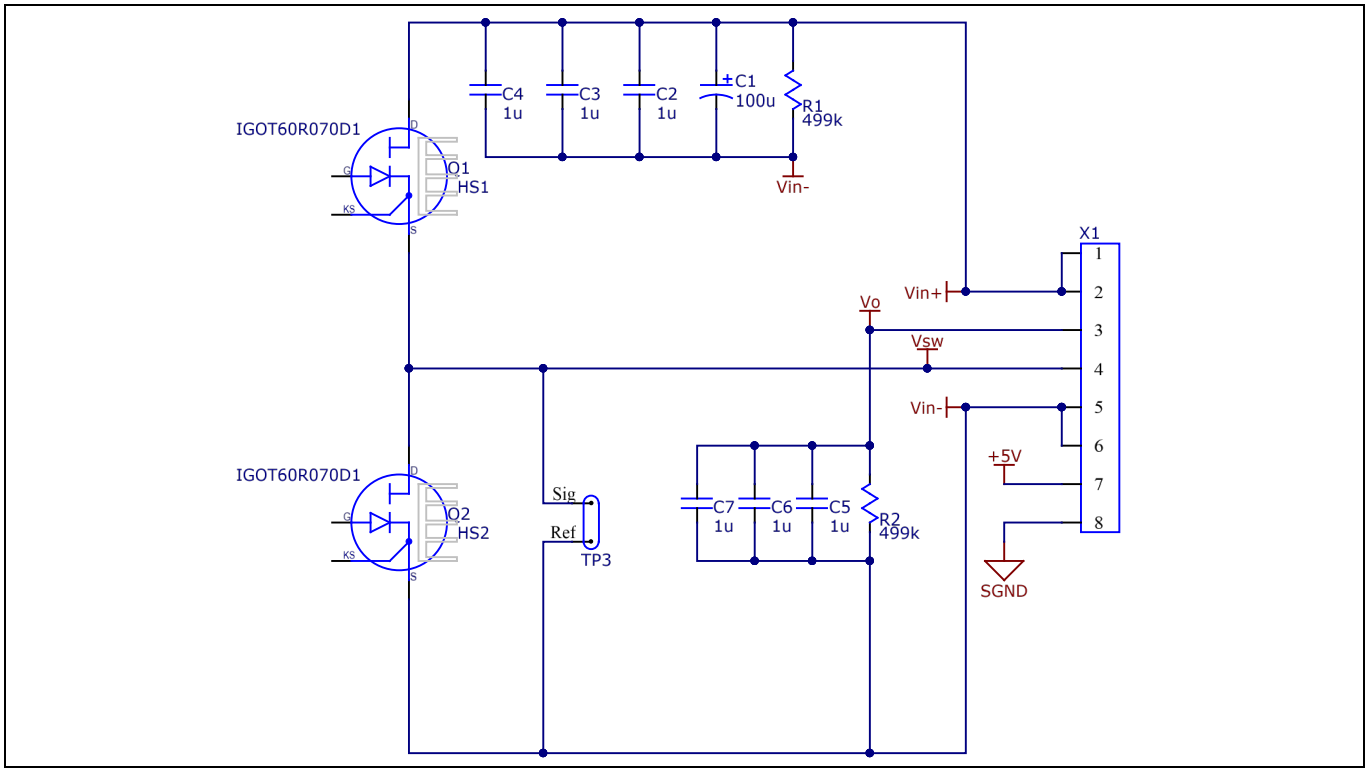

Figure 7 **Half-bridge output circuit**

4 Setup and use

Attention: ***This evaluation board has exposed high-voltage contacts. Use appropriate protective measures to avoid shock. The evaluation board has no overcurrent shutdown, so it is possible to drive the GaN transistors to currents far beyond their rating, which may result in their destruction. Use appropriate protective covers to prevent any possible injury from exploding components. Observe the maximum rating of the DC bus capacitor, and keep the bus voltage below 450 V. Exceeding this value risks the capacitor venting violently. Always set appropriate current limit values on the external lab power supplies to minimize catastrophic damage to the board in the event of a fault. It is up to you to set the PWM input signal appropriately to avoid damage.***

4.1 Test equipment needed

- 5 V power supply capable of 0.5 A output current to supply Vcc
- Bus voltage supply up to 450 V DC with sufficient current to supply the power needed for the planned testing. For short pulse testing even to maximum current, the current drawn from the bus voltage supply is very small, as the DC bus bulk storage capacitor provides the instantaneous energy.
- Signal generator to provide the necessary PWM drive command for the half-bridge. The generator must be capable of driving standard 5 V logic levels into a 50 Ω terminated load. Rise and fall time should be in the 5 ns range for best timing accuracy/repeatability.
- 1.2 mm slotted screwdriver for adjusting the deadtime trimpots R11 and R21
- Interconnect cable for PWM input: The PWM input connector is a 50 Ω terminated MMCX coaxial connector. Assuming the signal source is a conventional BNC connector, you will need a BNC male to MMCX plug cable (Fairview Microwave FMC0809315) or a BNC to MMCX adapter.
- Oscilloscope for measurement. Due to the fast transient voltage and current possible using GaN transistors, an oscilloscope with a bandwidth >500 MHz is recommended.
- For measuring the high-side gate voltage, a 1 GHz Isolated probe such as the Tektronix TIVM1 is recommended. An MMCX connector is provided for this purpose (TP1 on the back side of the board). We are not aware of any other isolated probe with sufficient common-mode transient immunity to accurately measure the high-side gate voltage.
- A standard (>500 MHz) passive probe with the short ground pin can be used to measure Q2 low-side gate voltage on TP2, but the test point reference on the Kelvin source of Q2 may have ground bounce compared to the Vsw measurement reference due to L di/dt ground bounce. A common-mode core on each passive probe cable can help minimize any measurement artifacts due to common-mode cable shield currents. Another effective solution is to use a 1 GHz active differential proble such as the Tektronix TDP1000. This can further minimize measurement errors/artifacts due to common-mode ground currents, but can be sensitive to coupled dv/dt from the TIVM1 probe snout.
- Make sure the voltage probe used on TP3 to measure the switch node voltage is rated appropriately for voltage and bandwidth. We recommend a Tektronix TPP0850 high-voltage probe with 800 MHz bandwidth.

4.2 Connections to the terminal block

With the exception of the coaxial PWM connection to J1, all other I/O and power connections to the evaluation board are made to the pluggable terminal-block X1. The pluggable terminal block makes it more convenient to remove the board from the test-bench for any component value changes during test, without having to disconnect and reconnect everything each time a change is made.

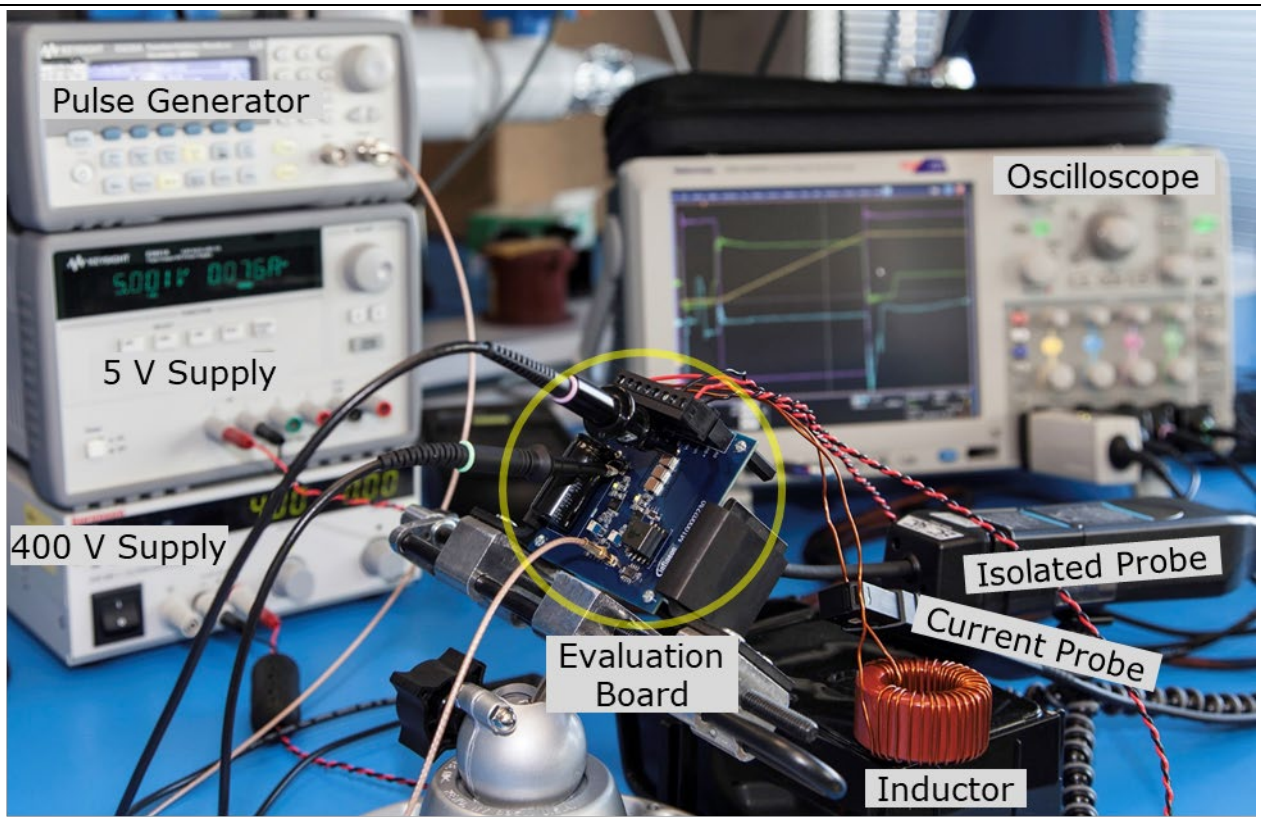

Figure 8 Typical test setup – example is shown for pulse testing

4.2.1 Connections for double-pulse testing

Refer back to Figure 2 for the proper setup and connections for double-pulse testing. Note that the single terminal block X1 has all 6 output power connections, plus the 5 V DC supply connections. The inductor also connects to the terminal block. No load is required for pulse testing – the inductor energy is dissipated in the freewheeling transistor.

4.2.2 Connections for buck topology

When the external inductor is connected between Vsw and Vo terminals, the circuit is configured as a buck converter. If a PWM signal is applied to the PWM input, the output voltage will be proportional to the input voltage times the PWM duty-cycle. With the appropriate inductor, PWM frequency can be set low (tens of kHz), or up to 3 MHz. The circuit can be operated continuously in this mode, provided that the temperature of the transistors is kept to a safe level. The circuit is entirely open-loop since there is no feedback control, so the output will not be load regulated. When operating at high frequencies, ensure that the inductor ripple-current always changes polarity each half-cycle, so that the circuit operates in ZVS mode. Otherwise, hard-switching at high-frequency will result is large power dissipation due to the switching loss.

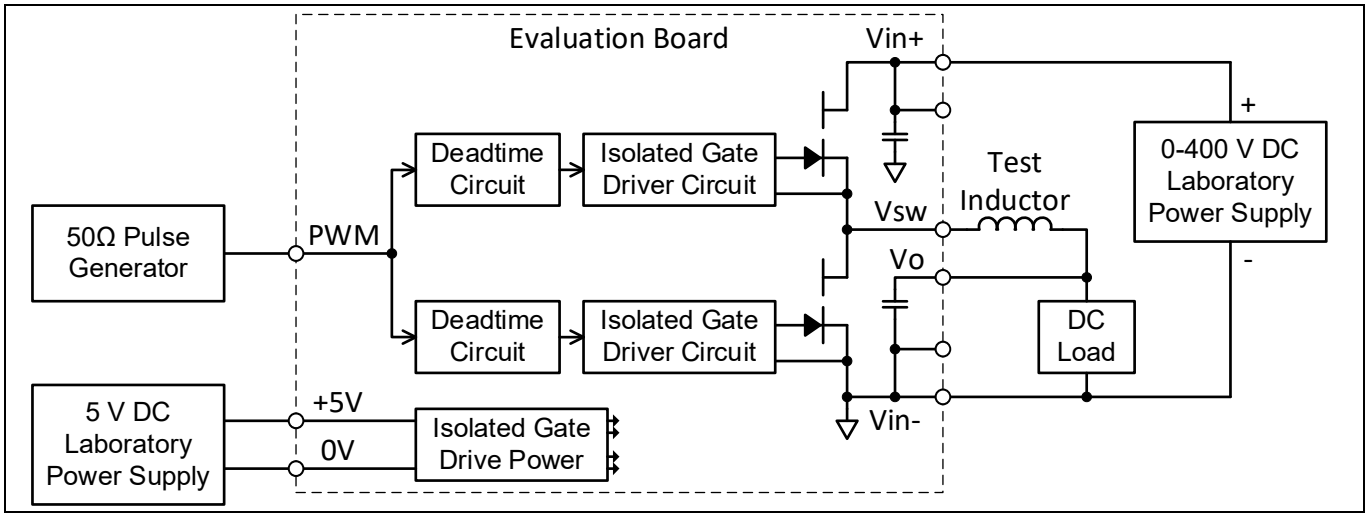

Figure 9 Connecting the evaluation board in the buck topology

Figure 10 shows example waveforms operating in ZVS buck mode at 1.5 MHz. The circuit is connected per Figure 9, using a 12 µH RF inductor (28 turns of 675/#48 Litz wire on Micrometals T80-2 toroidal core). The input voltage is 400 V, and the output voltage is about 260 V (65% duty-cycle). The load is set to 2.5 A, about 650 W output power.

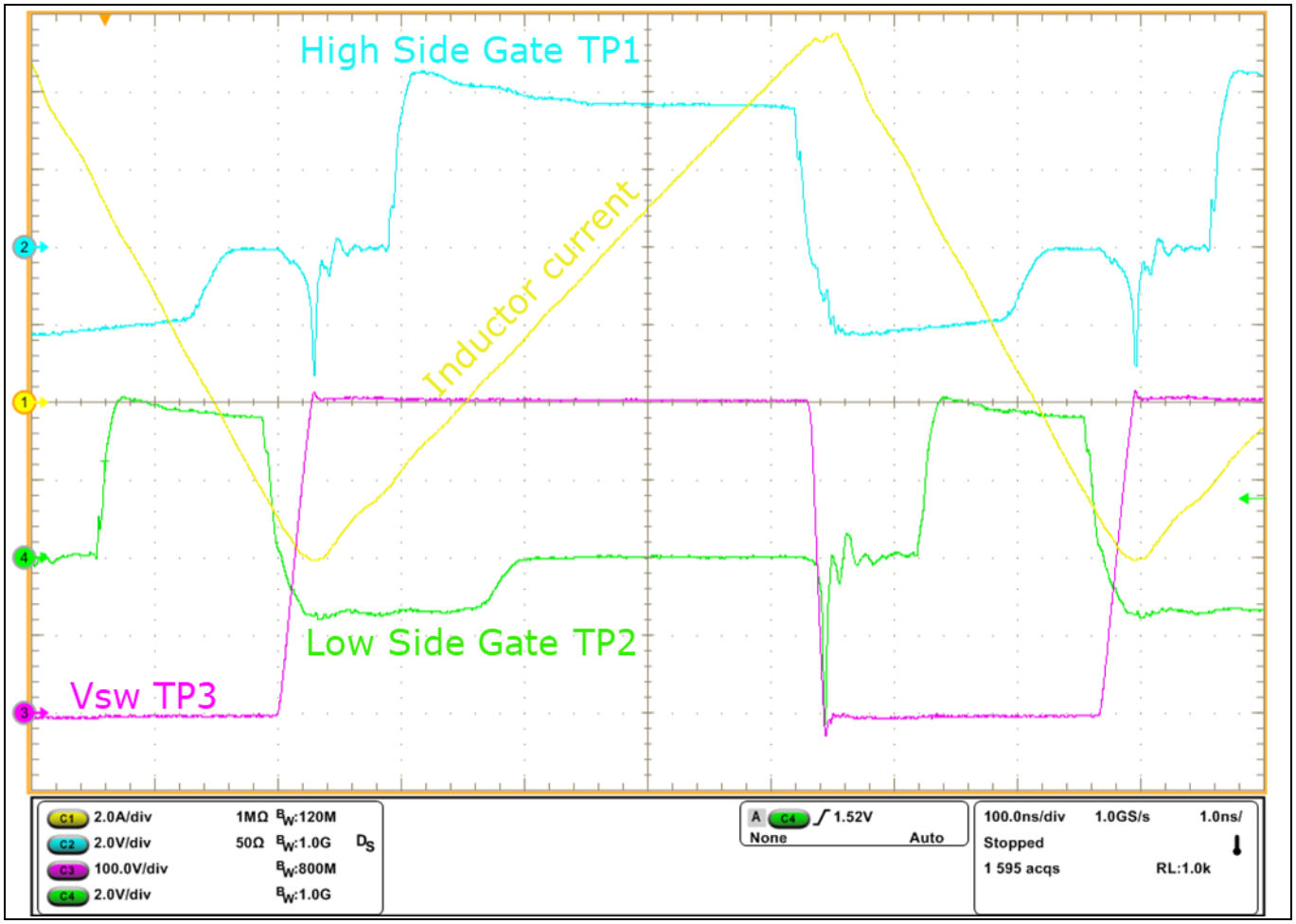

Figure 10 Operating waveforms ZVS buck-mode @ 1.5 MHz, 650 W load.

Note that the slew-rate of V_{SW} (TP3) is asymmetrical: this is because the rising-edge is driven by the -4 A inductor peak current, but the falling-edge is driven by the +9.5 A peak current, more than 2X larger current. The commutating slew-rate is directly proportional to the peak inductor current based on I=C dv/dt where I is the inductor current, and C is the total switch-node capacitance.

Also visible in Figure 10 are the negative voltage transients on V_{GS} commonly seen when the GaN transistor is driven rapidly into 3rd quadrant conduction. This is the 3-4 volt negative voltage transient that coincides with the switch-node transition. On the high-side V_{GS} waveform, this appears at 230 ns and 900 ns from the left edge of the waveform, and at 640 ns on the low-side V_{GS} waveform. The cause of this transient is the highly nonlinear gate-drain capacitance (Crss) of the GaN transistor, which can be found in figure 20 of the IGOT60R070D1 datasheet. The capacitance is extremely low over most of the range of V_{DS}, but increases sharply as V_{DS} approaches zero. So in this case of ZVS transitions, the inductor current is driving a nearly constant slew-rate of V_{DS} fro 400 to zero volts. But as V_{DS} transitions from about 50 V to zero, there is a large change in Crss, and thus a significant charge injected into the gate (approximately 3 nC). This charge in a short time (I=dq/dt) results in a short current-spike that pulls the gate voltage down for a moment.

4.2.3 Connections for boost topology

When operated in the boost mode, the roles of Vo and Vin+ are reversed. Figure 11 shows how the inductor is connected between the input voltage and the switch-node. The input power supply is connected to the Vo terminal for the stability provided by the high-frequency bypass capacitors. When the low-side transistor is on, inductor current is remped-up, then it is commutated to the “output” (the Vin+ bus) through the high-side transistor which acts as a synchronous rectifier. An appropriate load must be connected to the Vin+ terminal.

Attention: ***When operated in the boost-mode, it is possible to rapidly charge the Vin+ bus to voltages beyond its rating, which may result in catastrophic failure of the bus capacitors and other components. Always make sure that the input voltage, PWM signals and output load are coordinated to achieve the desired output voltage in this mode, as there is no closed-loop voltage control or limit.***

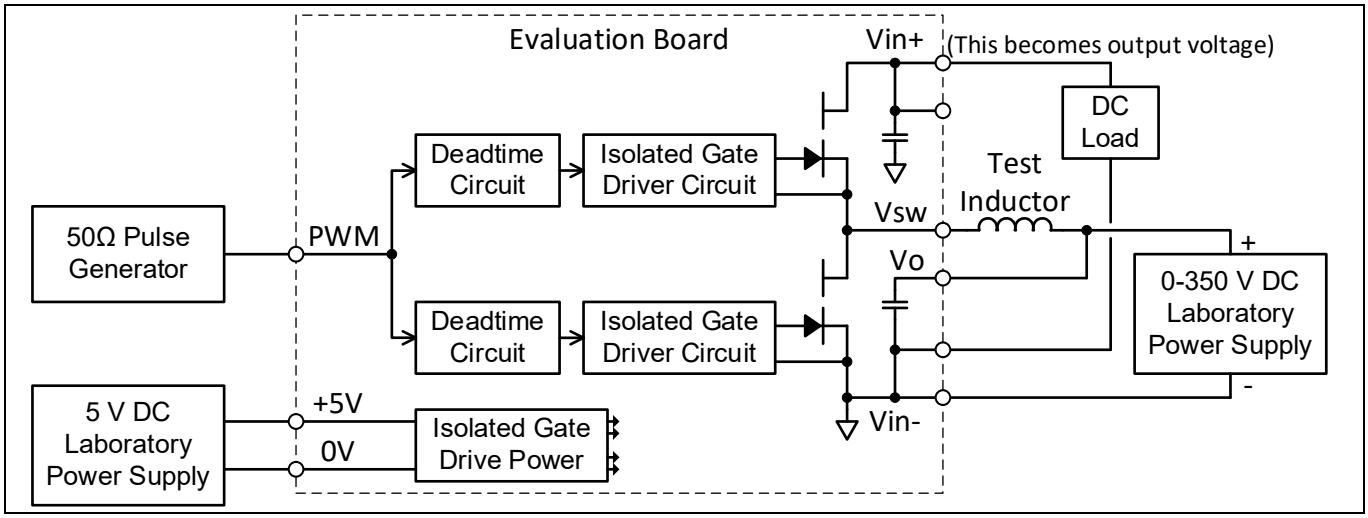

Figure 11 Connecting the evaluation board in the boost topology

4.3 Input PWM generator connections and settings

The PWM input is the logic command to the half-bridge output: when the PWM input is high, the half-bridge output Vsw is at its high state (connected to the Vin+ bus). Conversely, when the PWM input command is at

logic low, the half-bridge output Vsw is at 0 (-Vin). The input is an MMCX coaxial connector terminated in 50 Ω. Recommended signal/pulse generator settings are fastest rise/fall time, low level of 0V and high-level of 3.5V. The pulse generator can be set to pulse or burst-mode for double-pulse testing, or continuous operation for buck or boost modes, within the constraints of the warnings given in sections 4 and 4.2.3.

4.4 Measurement points

The evaluation board has 6 test points for connecting an oscilloscope to look at various signals. The test points are either a through-hole pad-pair, or an MMCX connector. The pad-pairs have a letterscreen symbol that identifies which pads are signal and reference (common): The signal pad is designated by the ~ symbol, and the reference pad is designated by the ⊥ symbol.

Table 2

Test Point Label	Description
TP4	PWM input – parallel to J1. For use in verifying the proper logic drive levels and timing into the 50Ω termination. Typical levels here should be 0 – 3.5 V
TP11	PWM input signal to the Schmitt trigger input of the high-side driver IC (U1). The rising-edge of this signal is delayed from TP4 by the deadtime circuit so it has an exponential risetime characteristic. Voltage level is standard 5 V AHCT logic level.
TP21	PWM input signal to the Schmitt trigger input of the low-side driver IC (U2). The rising-edge of this signal is delayed from TP4 by the deadtime circuit so it has an exponential risetime characteristic. Voltage level is standard 5 V AHCT logic level.
TP1	High-side gate voltage: signal is the gate of Q1, reference is the Kelvin source of Q1. This test point is an MMCX connector and is designed to be directly connected to the input of a Tektronix TIVM1 isolated probe. Note that the reference point (the barrel of TP1 MMCX connector) is essentially the output switch-node of the half-bridge so the common-mode voltage is a fast high-voltage signal – **do not use a non-isolated probe on TP1 or damage will occur**. The common-mode voltage is 0-Vin+, and the differential-mode measured signal at this point is typically in the range of -8 V to +4 V.
TP2	Low-side gate voltage: signal is the gate of Q2, reference is the Kelvin source of Q2. Since the reference is the Kelvin-source, there is some common-mode voltage bounce between this test point reference and “ground” (Vin- the reference point for TP3). See recommendations in section 4.1
TP3	This is the test-point to observe the half-bridge switch-node output. Since the bus voltage is typically in the range of 350 – 400 V, be sure to use a voltage probe with appropriate voltage rating. We recommend the Tektronix TPP0850 50X high-voltage 800 MHz probe with its short ground pin. TP3 diameter and spacing will accommodate this probe.

4.5 Power-up and power-down sequencing

The gate drivers are designed to keep V_{GS} below the turn-on threshold even if they are unpowered. Regardless, it is good practice to make sure the 5 volt power (and thus the gate drivers) is always applied before powering-up the high voltage bus. Conversely, power-down the high-voltage bus before powering-down the 5 volt supply. Recommended current limit on the 5 volt lab supply is 300 mA, and on the high-voltage supply, it depends on the expected load power. For basic double-pulse testing, even to 35 A peak, the HV supply can be limited to 0.2 A because the on-board bus capacitors will provide the peak current (for low-value inductors <100 µH).

4.6 Verifying and adjusting deadtime

The evaluation board has two independent deadtime adjustments. When the PWM input goes high, the low side gate driver turns off and then the high-side gate driver turns on after the rising-edge deadtime. This deadtime is adjusted with the trim potentiometer R11. On the falling-edge of PWM input, the high-side gate driver turns off, then the low-side gate driver turns on after the falling-edge deadtime. This is adjusted with the trim potentiometer R21. You will need a small (1.2 mm) slotted (flat-blade) screwdriver to andjust the trimpots.

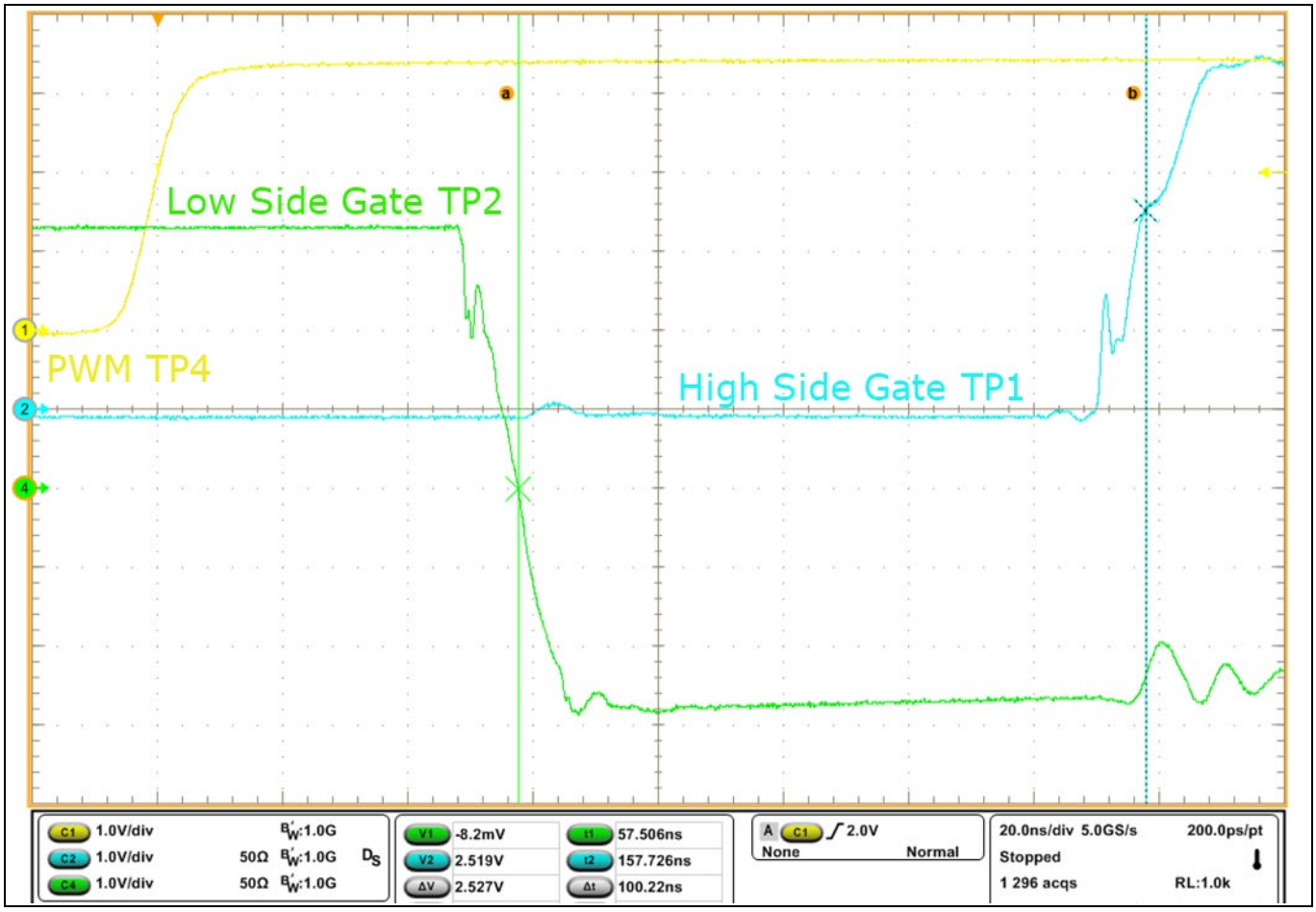

Figure 12 Measuring deadtime on the rising edge of PWM

To verify and adjust deadtime, connect a 5 V DC supply to the 5 V input on the eval board, and connect a pulse generator to the PWM input J1 (refer to section 4.3). Set the generator for a square-wave (50% duty-cycle) at 100 kHz and apply the 5 V power to the board. Connect an oscilloscope to TP4 as the reference PWM input. Connect a probe to TP2 (low-side gate), and an isolated probe (TIVM1 mentioned earlier) to the high-side gate test connector TP1. Be sure to follow the scope instructions for adjusting the scope channel timing-offset “de-skew” values to compensate for the group delay of each probe. Isolated probes can have significant delay times on the order of 30 ns, so that could result in a large error if the de-skew is not properly calibrated on the scope.

Note: If isolated probe is not available, standard passive probes can be used to measure the high-side gate signal for setting deadtime, as long as the high voltage bus is at 0 V. Just be sure to disconnect the passive probe from TP1 before applying any bus voltage

Apply power to the board and trigger on the rising edge of TP4. You should have a signal that looks similar to Figure 12. The cursors assume that turn-off is complete when TP2 crosses 0 V, and turn-on is assumed to begin

when TP1 reaches about 2.5 V. Adjust R11 (trimpot) to achieve the desired deadtime (factory preset is 100 ns). For the falling edge, set the scope trigger for the negative edge of TP4, and you should see a waveform similar to Figure 13. Adjust trimpot R21 to dial-in the deadtime to the desired value on the falling edge of PWM. Normally the rising and falling edge deadtimes are set to the same value. Turning the trimpots clockwise increases the deadtime.

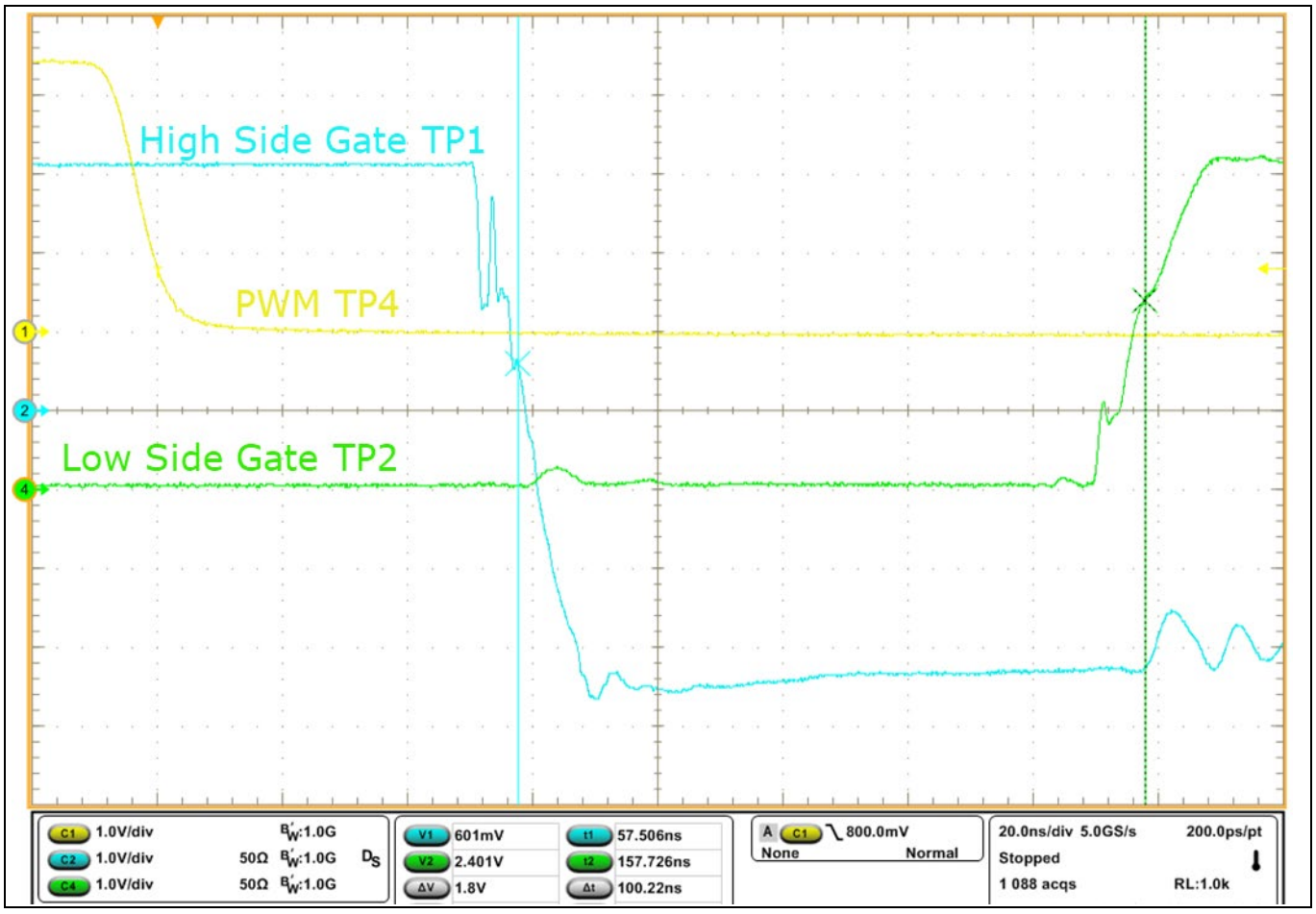

Figure 13 Measuring deadtime on the falling-edge of PWM

4.7 Test inductor recommendation

For best results, it is recommended that a good high-frequency capable inductor is used for testing. We recommend a Micrometals T200-2B toroidal core, with 34 turns of 14 gauge HPN enameled copper magnet wire in a single-layer. This provides a very linear, low-loss 25 µH inductor with a self-resonant frequency >20 MHz and a high saturation current, well beyond the rating of the 70 mΩ GaN peak current rating. While this may not provide the most space-efficient inductor, it will not “color” the measurement results. Lower performance inductors may have high self-capacitance and multiple resonaces that can mask or confuse the performance measuremet of the GaN half-bridge.

4.8 Initial checkout

Assuming the board is already set-up per section 4.6, the next step is to add an external inductor and bring-up the DC bus to operate at the desired test condition. This example shows how to set-up the board for double-pulse testing. In double-pulse testing, first the half-bridge turns on and ramps-up inductor current to a test value. Then the primary switch turns-off, and the current freewheels through the other device, which acts as a synchronous rectifier. The second pulse shows hard-switched turn-on performance on the leading-edge (at the

test current) and then continues the ramp to a higher current level. GaN devices perform particularly well on these tests because the freewheeling diode has zero reverse-recovery characteristic. Double –pulse testing is typically done 1 burst at a time (not continuously) in order to keep power dissipation low, even when testing to the voltage and current limits of the device.

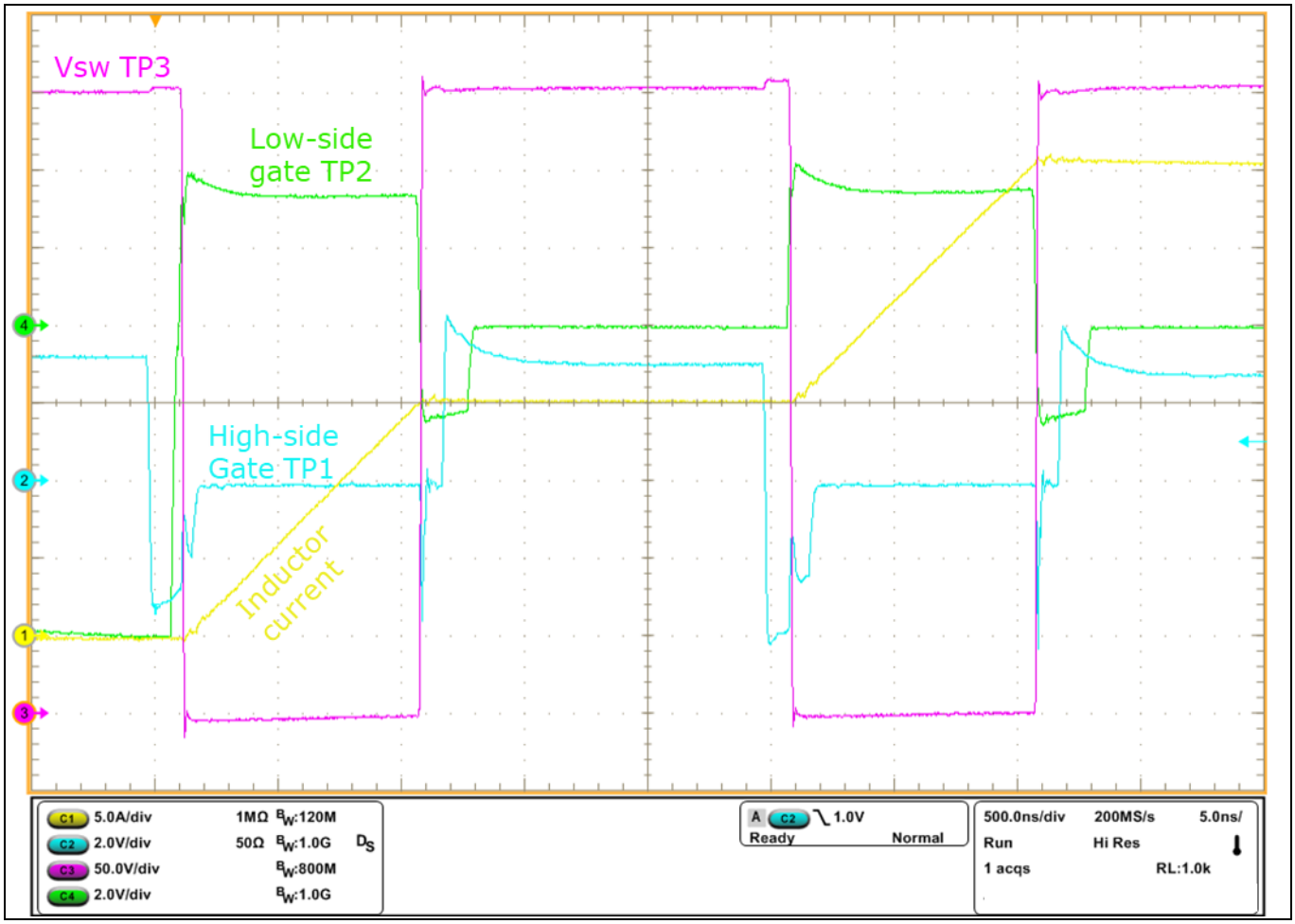

Figure 14 Double-pulse test waveform example

Connect the external 25 µH inductor and HV power supply as shown in Figure 2. Set the pulse generator for a pulse-width of 1 µs, and a period of 2.5 µs. set-up a 2-pulse burst (refer to Figure 14). It is recommended to set the pulse generator for manual mode, where each pulse set is triggered by a button-push.

Note: When the low-side switch is operated in the double-pulse test, the default state of the half-bridge is that the high-side synchronous rectifier is normally ON. Thus the logic input should be inverted – normally high with two pulses going low. Make sure to power-off the HV supply before shutting-off the output of the pulse generator: if the pulse generator is powered-off first, it will turn-on the low-side and ramp the current to uncontrolled value, unless the bus is at zero volts. The HV supply should always be the last thin to turn-on, and the first thing to turn-off when measurement is completed.

Start with a low-voltage on the DC bus – 25 V just to make sure that everyting is connected properly, and that the current is ramping-up as expected, the current probe polarity is correct, etc. If everything looks good, then continue to increase the bus voltage while checking test pulses to ensure the waveforms are as expected. This will also help to ensure that the inductor is not saturating and the current is within bounds. The typical test

condition is to set the bus voltage to 400 V, and keep the current peak to 35 A or lower. Adjust the pulse ON time to increase or decrease the current at the end of each pulse.

Refer to Figure 14 for the following timing sequence description: at the beginning of the waveform, the high-side has been on for a long time, and the low-side has been off. Note that the low-side gate is driven to -8V as it is in the “first-pulse” condition described in the gate driver datasheet. First, the high-side gate turns-off, followed by the low-side gate turning-on 100 ns later (100 ns deadtime). When the low-side transistor turns-on, the current in the inductor ramps up at a rate determined by $I_L = V_{BUS}t_{ON}/L$. Then the low-side switch turns-off, and the 15 A inductor current immediately commutates to the high-side transistor operating in 3rd quadrant conduction mode. You can see the switch-node voltage rises several volts above the bus during deadtime, due to the effective diode drop across the high-side transistor. 100 ns later, the high side transistor gate turns on, reducing the diode-mode voltage drop. The inductor current freewheels for a few microseconds, then the low-side turns-on again for pulse 2. The cycle repeats again as the inductor current ramps to about 30 amps (this could be lower if pulse 2 is shortened).

Note that both the gate and drain voltage are well-behaved, with minimal ringing or overshoot, despite the extremely fast switching performance. This is the performance that GaN can deliver to help reduce switching loss, while also decreasing conducted and radiated emissions at the same time.

4.9 Operation at high power levels

The half-bridge board uses topside-cooled transistors. With appropriate heatsink and airflow, each transistor is capable of dissipating approximately 15 W. Individual heatsinks can be bonded to each transistor using Bergquist Liquibond thermally-conductive adhesive or similar. The DSO-20-87 transistor package is also solderable, so a copper pin-fin heatsink could be soldered directly to the thermal pad on each transistor for best thermal conductivity. Alteratively, a single heatsink could be used for both transistors, provided the appropriate thermal interface material is used. The temperature of the transistors and heatsinks can be easily monitored in real-time using a FLIR infrared camera. Best accuracy of the infrared measurement is using a high emissivity coating (flat black) on the surfaces being monitored.

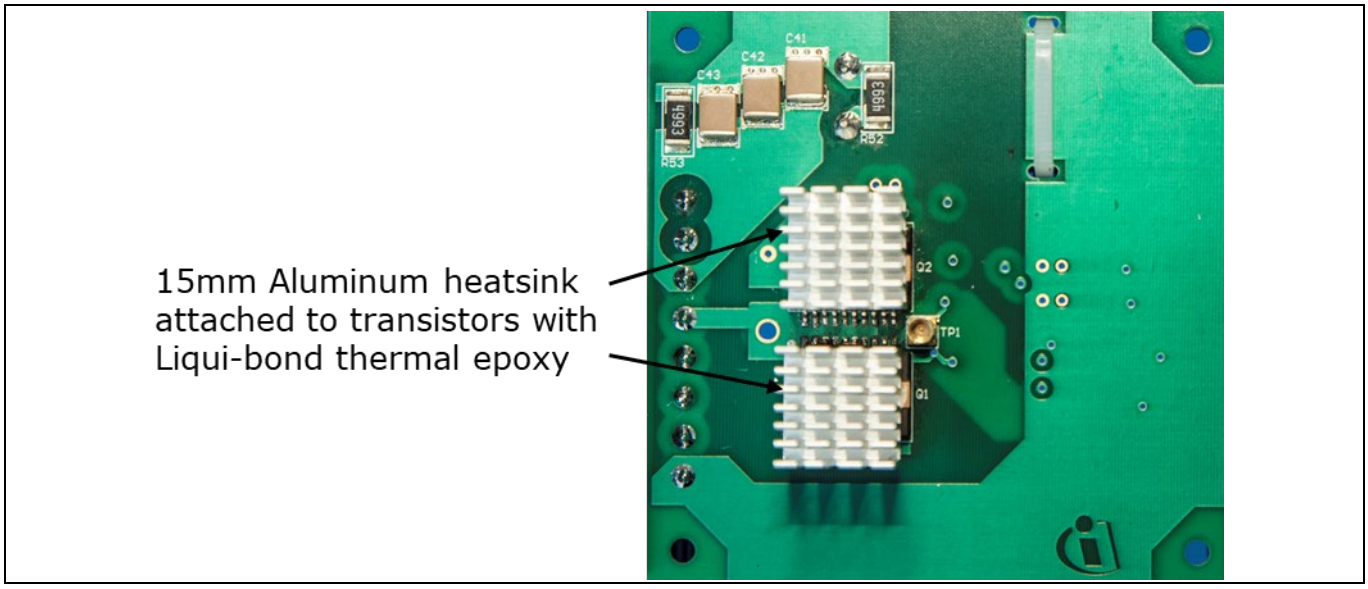

Figure 15 15 mm aluminum heatsink

5 Complete schematic

Note: Part numbers 1-9 are in the ouput power stage. 1x part numbers belong to the high-side gate drive, 2x are low-side gate drive, and 3x are input ground connected

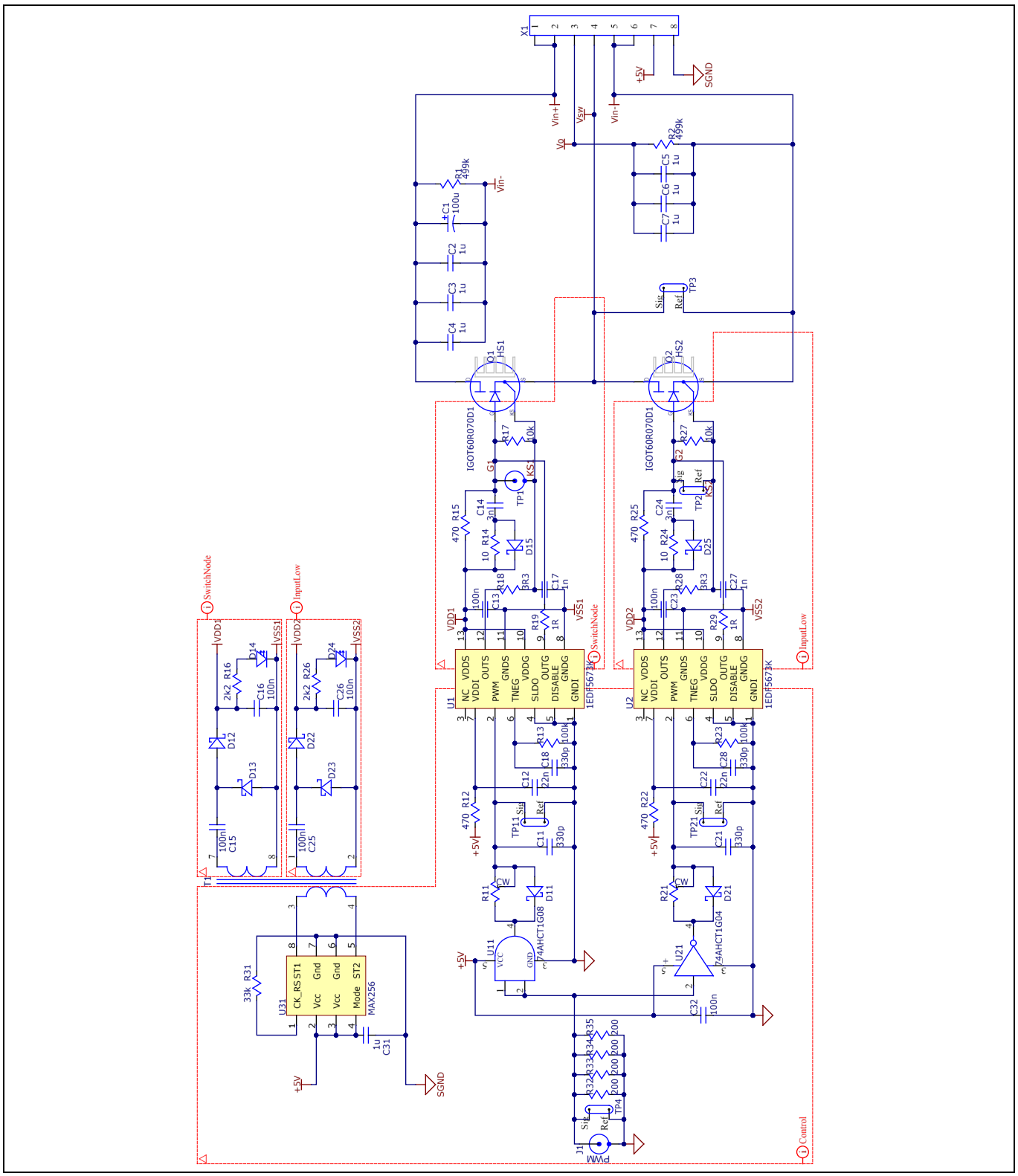

Figure 16 Schematic of half-bridge evaluation board

6 PCB layout

The evaluation board is 1.6 mm thick, with 4 evenly-spaced copper layers 35 µm thick. The layer stackup is depicted below.

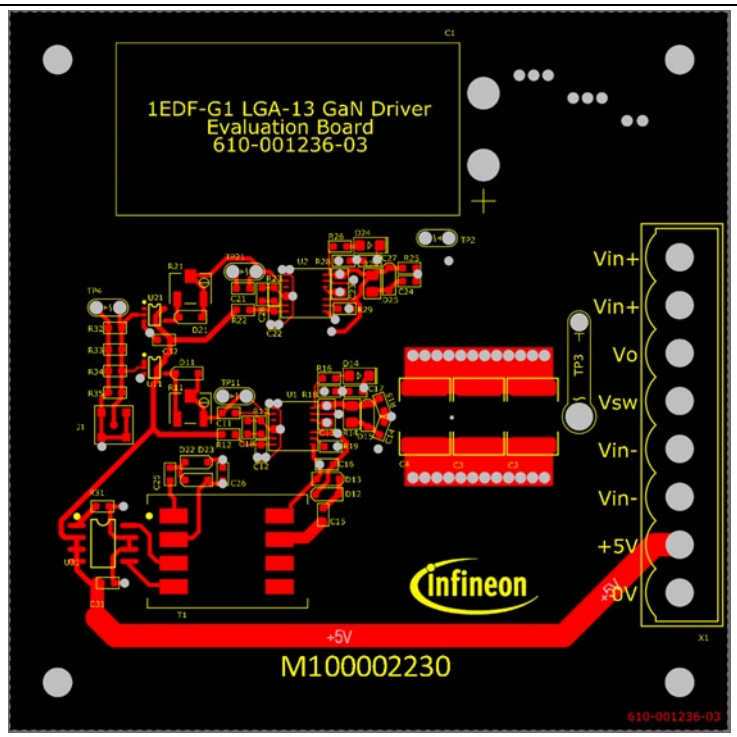

Figure 17 Top layer copper layer with top component overlay

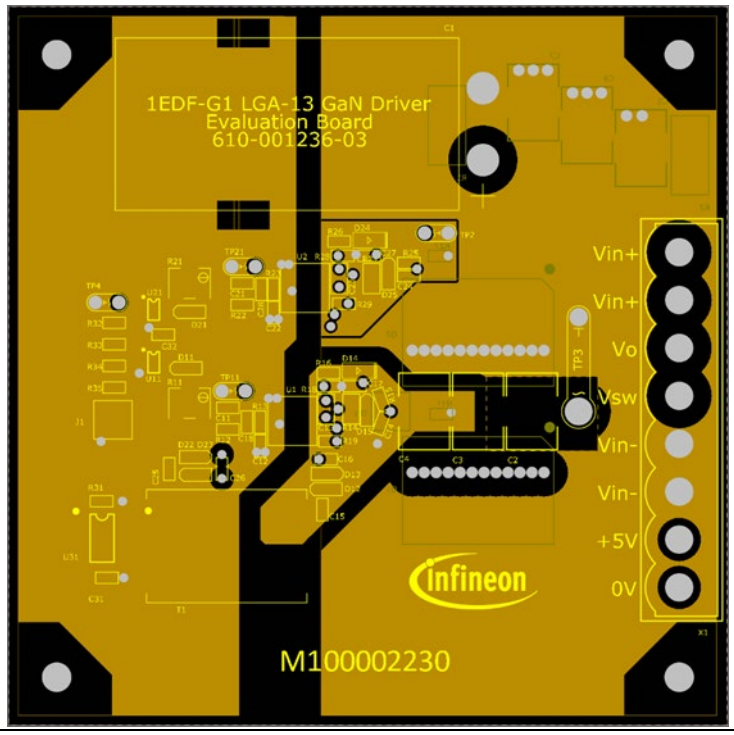

Figure 18 Upper middle copper layer with top and bottom component overlays

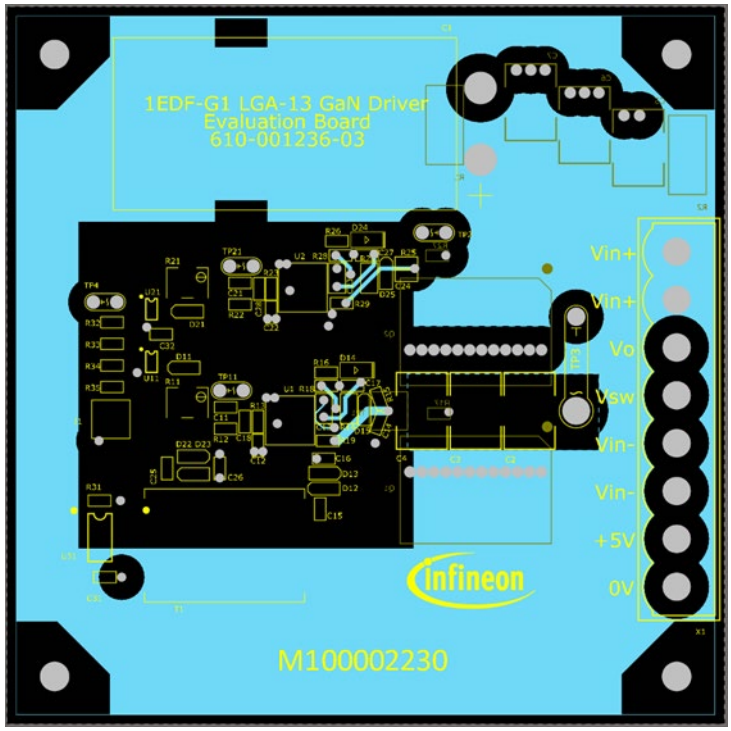

Figure 19 Lower middle copper layer with top and bottom component overlay

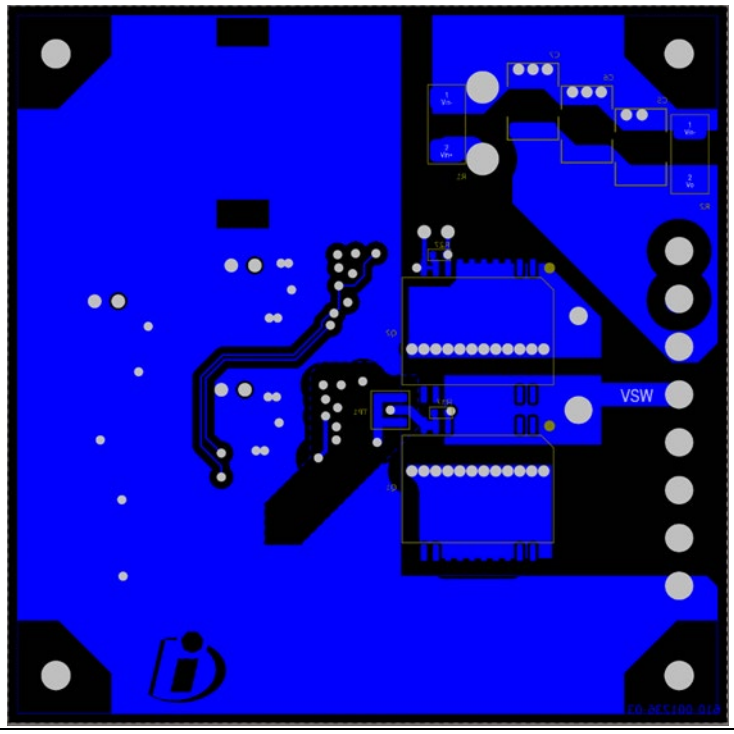

Figure 20 Bottom copper layer with bottom component overlay (viewed from top)

7 Bill of Materials (BoM)

The following table describes all of the components on the PCB:

Table 3 PCB BOM

Designator	Description
C1	CAP ALUM 100 UF 20% 450 V 18D 35L 7.5P
C2, C3, C4, C5, C6, C7	CAP 1uF 450 V X7T 2220
C11, C18, C21, C2	CAP CER 330 PF 16 V C0G/NP0 0603
C12, C22	CAP CER 0.022 UF 25 V X7R 0603
C13, C23	CAP CER 0.1 UF 25 V X7R 0805
C14, C24	CAP CER 3000 PF 25 V NP0 0603
C15, C16, C25, C26, C32	CAP CER 0.1 UF 25 V X7R 0603
C17, C27	CAP CER 1000 PF 16 V C0G/NP0 0603
C31	CAP CER 1 UF 16 V X7R 0603
D11, D12, D13, D15, D21, D22, D23, D25	DIODE SCHOTTKY 30 V 200MA SOD323
D14, D24	LED GREEN CLEAR 0805 SMD
J1	CONN MMCX JACK STR 50 OHM SMD
Q1, Q2	Infineon IGOT60R070D1 CoolGaN™ transistor
R1, R2	RES SMD 499K OHM 1% 1W 2512
R11, R21	TRIMMER 1k OHM 0.125W SMD
R12, R15, R22, R25	RES SMD 470 OHM 1% 1/10 W 0603
R13, R23	RES SMD 100K OHM 1% 1/10 W 0603
R14, R24	RES SMD 10 OHM 1% 1/8W 0805
R16, R26	RES SMD 2.2K OHM 1% 1/10 W 0603
R17, R27	RES SMD 10K OHM 1% 1/10 W 0603
R18, R28	RES SMD 3.3 OHM 1% 1/10 W 0603
R19, R29	RES SMD 1 OHM 1% 1/10 W 0603
R31	RES 33K OHM 1% 1/10 W 0603
R32, R33, R34, R35	RES SMD 200 OHM 1% 1/10 W 0603
T1	Transformer (see section 3.2.1 for additional detail)
TP1	CONN MMCX JACK STR 50 OHM SMD
TP2, TP3, TP4, TP11, TP21	PCB built-in thru-hole test point pair
U1, U2	Infineon EiceDRIVER™ 1EDF5673K GaN driver
U11	74AHCT1G08 IC GATE AND 1CH 2-INP SOT-353
U21	74AHCT1G04 IC SINGLE INVERTER GATE SOT353
U31	MAX256 IC DVR H-BRIDGE 3W 8-SOIC
X1	8-Position pluggable terminal block

Heatsinks for Q1 and Q2 are provided in the kit (Adafruit Industries LLC 3082)

Revision history

Document version	Date of release	Description of changes

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