IFX24401

Low Dropout Voltage Regulator

IFX24401TEV50
IFX24401ELV50

Data Sheet

Rev. 1.02, 2009-12-10

Standard Power

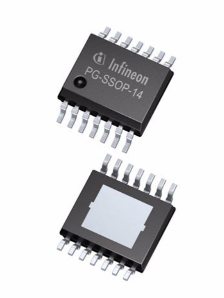
Low Dropout Voltage Regulator **IFX24401**

1 Overview

Features

- Output voltage 5 V ±2%
- Ultra low current consumption: 20 µA (typ.)
- 300 mA current capability
- Enable input
- Very low-drop voltage
- Short circuit protection
- Overtemperature protection
- Low Dropout Voltage, 250mV (typ.)
- High Input Voltage 45 V
- Temperature Range -40 °C ≤ T_j ≤ 125 °C
- Green Product (RoHS compliant)

PG-TO252-5



PG-SSOP-14

Applications

- Battery powered devices (e.g. Handheld GPS)
- Portable Radios
- HDTV Televisions
- Game Consoles
- Network Routers

For automotive and transportation applications, please refer to the Infineon TLE and TLF voltage regulator series.

Functional Description

The IFX24401 is a monolithic integrated low-drop voltage regulator for load currents up to 300 mA. The output voltage is regulated to $V_{Q,nom}$ = 5.0 V with an accuracy of ±2%. A sophisticated design allows stable operation with low ESR ceramic output capacitors down to 470 nF. The device is designed for the harsh environments. Therefore it is protected against overload, short circuit and overtemperature conditions. Due to its ultra low stand-by current consumption of 20 µA (typ.) the IFX24401 is ideal for use in battery powered applications. The regulator can be shut down via an Enable input which further reduces the current consumption to 5 µA (typ.). An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage.

Type	Package	Marking
IFX24401TEV50	PG-TO252-5	2440150
IFX24401ELV50	PG-SSOP-14	24401V50

2 Block Diagram

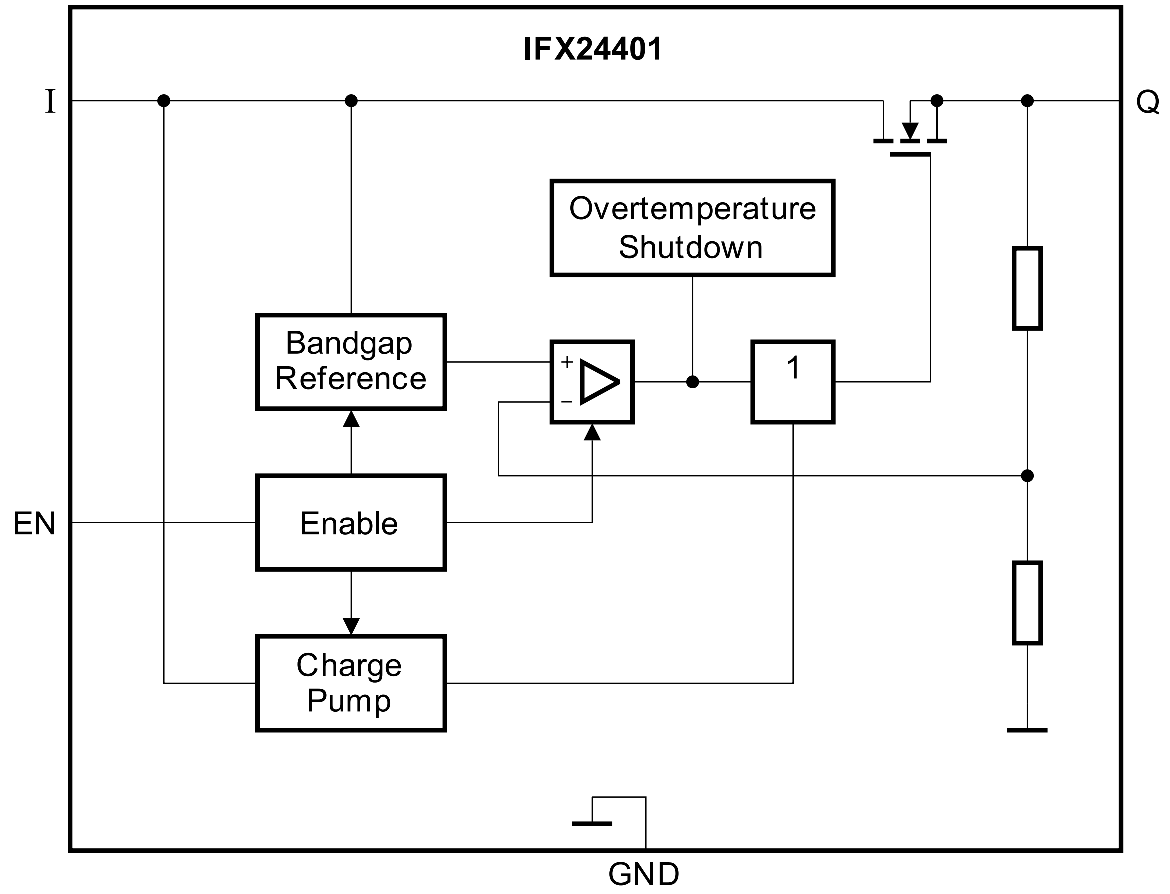


Figure 1 Block Diagram

3 Pin Configuration

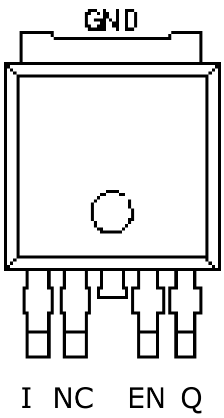


Figure 2 Pin Configuration PG-TO252-5 (top view)

3.1 Pin Definitions and Functions (PG-TO252-5)

Pin	Symbol	Function
1	I	**Input** Connect ceramic capcitor between I and GND
2	N.C.	**No Connect** May be open or connected to GND
3	GND	**Ground** Internally connected to heat slug
4	EN	**Enable Input** Low signal level disables the regulator. Pull-down resistor is integrated.
5	Q	**Output** Place capacitor between Q pin and GND. Capacitor placement should be close to pin. Refer to capacitance and ESR requirements in **“Functional Range” on Page 6**
Heat Slug	--	**Heat Slug** Connect to board GND and heatsink

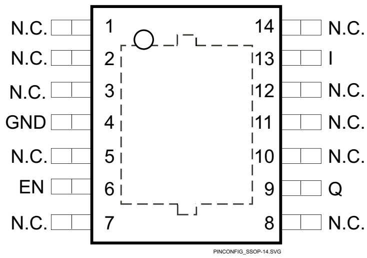


Figure 3 Pin Configuration PG-SSOP-14 (top view)

3.2 Pin Definitions and Functions (PG-SSOP-14)

Pin	Symbol	Function
1,2,3,5,7	N.C.	**No Connect** May be open or connected to GND
4	GND	**Ground**
6	EN	**Enable Input** Low signal level disables the regulator. Pull-down resistor is integrated.
8,10,11,12,14	N.C.	**No Connect** May be open or connected to GND
9	Q	**Output** Place capacitor between Q pin and GND. Capacitor placement should be close to pin. Refer to capacitance and ESR requirements in **"Functional Range" on Page 6**
13	I	**Input** Connect ceramic capcitor between I and GND
Pad		**Exposed Pad** Connect to board GND and heatsink

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1]
T_j = -40 °C to 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Input I					
Voltage	V_I	-0.3	45	V	–
Current	I_I	-1	–	mA	–
Enable EN					
Voltage	V_{EN}	-0.3	45	V	Observe current limit $I_{EN,max}$[2]
Current	I_{EN}	-1	1	mA	–
Output Q					
Voltage	V_Q	-0.3	5.5	V	–
Voltage	V_Q	-0.3	6.2	V	t < 10 s[3]
Current	I_Q	-1	–	mA	–
Temperature					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) Not subject to production test, specified by design.
2) External resistor required to keep current below absolute maximum rating when voltages ≥ 5.5 V are applied.
3) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.5	42	V	–
Junction temperature	T_j	-40	125	°C	–
Output Capacitor	C_Q	470	–	nF	[1]
	ESR (C_Q)	–	10	Ω	f = 10 kHz

1) The minimum output capacitance requirement is applicable for a worst case capacitor tolerance of 30%

Note: In the operating range, the functions given in the circuit description are fulfilled.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Value			Unit	Conditions
			Min.	Typ.	Max.		
IFX24401TEV50 (PG-TO252-5,)							
4.3.1	Junction to Case[1]	R_{thJC}	–	4	–	K/W	measured to pin 5
4.3.2	Junction to Ambient[1]	R_{thJA}	–	115	–	K/W	Footprint only[2]
4.3.3			–	57	–	K/W	300mm^2 heatsink area on PCB[2]
4.3.4			–	42	–	K/W	600mm^2 heatsink area on PCB[2]
IFX24401ELV50 (PG-SSOP-14)							
4.3.5	Junction to Case[1]	R_{thJC}	–	7	–	K/W	measured to pin 5
4.3.6	Junction to Ambient[1]	R_{thJA}	–	120	–	K/W	Footprint only[2]
4.3.7			–	59	–	K/W	300mm^2 heatsink area on PCB[2]
4.3.8			–	49	–	K/W	600mm^2 heatsink area on PCB[2]

1) not subject to production test, specified by design

2) EIA/JESD 52_2, FR4, 80 × 80 × 1.5 mm; 35µ Cu, 5µ Sn

Table 1 Electrical Characteristics

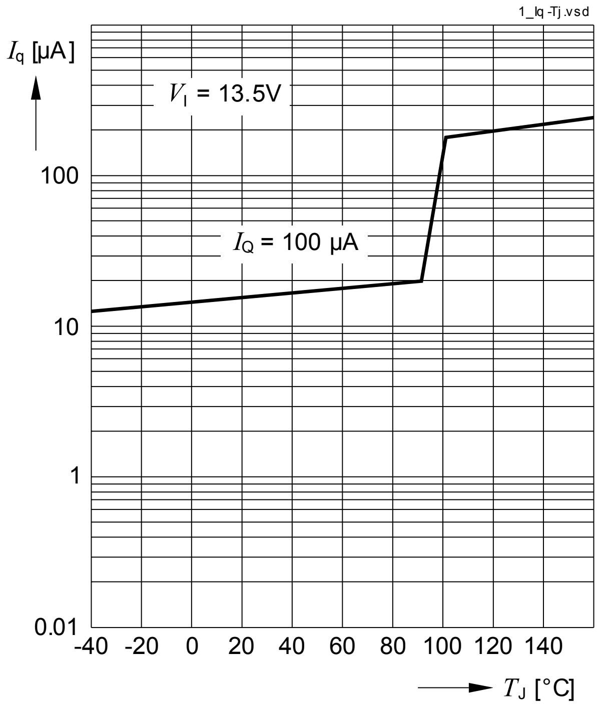
V_I = 13.5 V; V_{EN} = 5 V; -40 °C < T_j < 125 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Output Q						
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q < 300 mA; 6 V < V_I < 16 V
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q < 100 mA; 6 V < V_I < 40 V
Output current limit	$I_{Q,LIM}$	320	–	–	mA	[1]
Output current limit	$I_{Q,LIM}$	–	–	800	mA	V_Q = 0V
Current consumption; $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.1 mA; T_j = 25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	40	µA	I_Q = 0.1 mA; $T_j \leq$ 80 °C
Quiescent current; Disabled	I_q	–	5	9	µA	V_{EN} = 0 V; T_j < 80 °C
Drop voltage	V_{dr}	–	250	500	mV	I_Q = 200 mA; $V_{dr} = V_I - V_Q$ [1]
Load regulation	$\Delta V_{Q, lo}$	-40	15	40	mV	I_Q = 5 mA to 250 mA
Line regulation	$\Delta V_{Q, li}$	-20	5	20	mV	V_I = 10V to 32 V; I_Q = 5 mA
Power supply ripple rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Temperature output voltage drift	dV_Q/dT	–	0.5	–	mV/K	–
Enable Input EN						
Turn-on Voltage	$V_{EN\ ON}$	3.1	–	–	V	$V_Q \geq$ 4.9 V
Turn-off Voltage	$V_{EN\ OFF}$	–	–	0.8	V	$V_Q \leq$ 0.3 V
H-input current	$I_{EN\ ON}$	–	3	4	µA	V_{EN} = 5 V
L-input current	$I_{EN\ OFF}$	–	0.5	1	µA	V_{EN} = 0 V; T_j < 80 °C

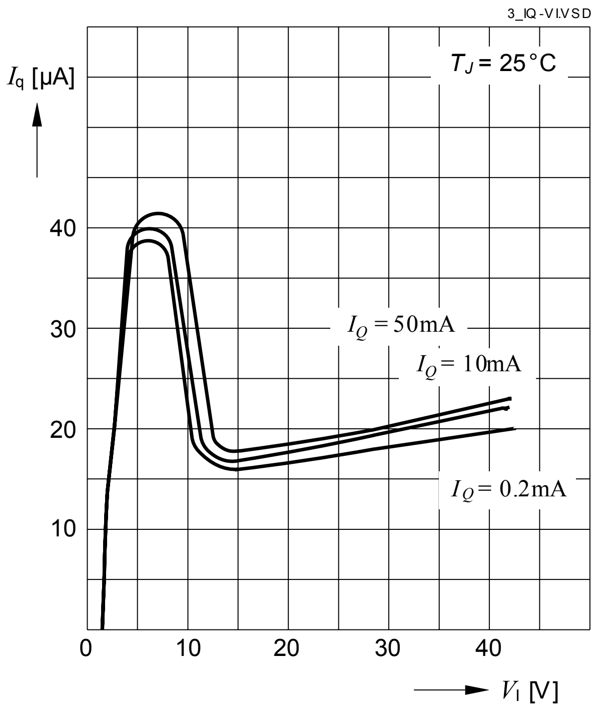
1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

5 Typical Performance Characteristics

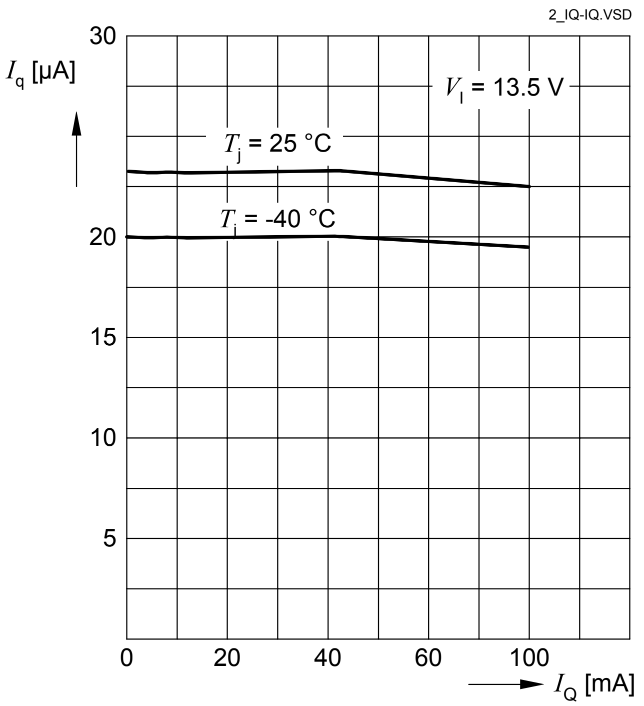
Current Consumption I_q versus Junction Temperature T_J



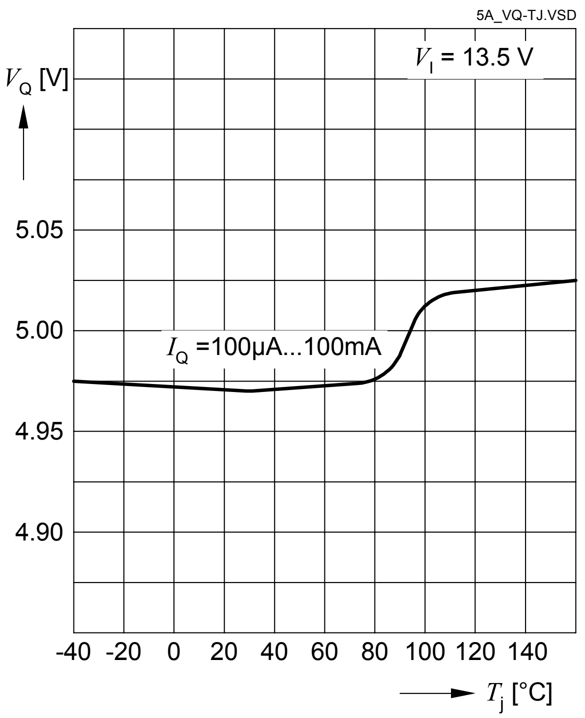
Current Consumption I_q versus Input Voltage V_Q



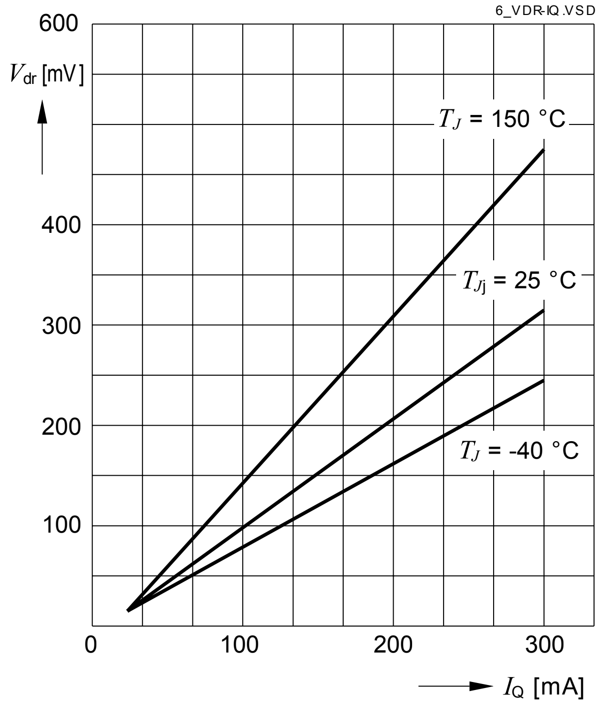
Current Consumption I_q versus Output Current I_Q



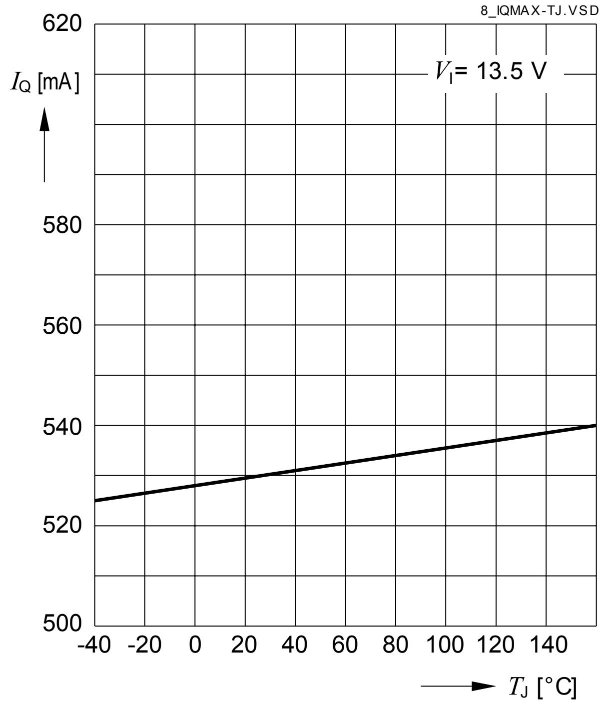
Output Voltage V_Q versus Junction Temperature T_J



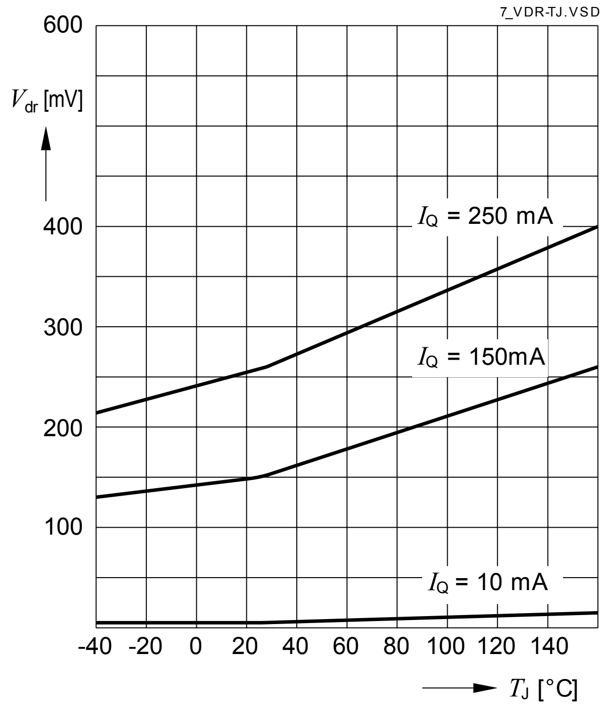
Dropout Voltage V_{dr} versus Output Current I_Q



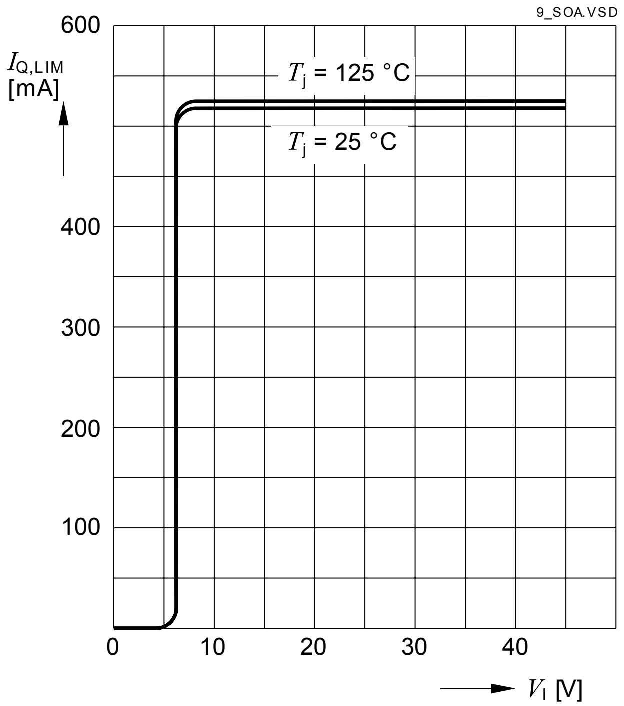
Maximum Output Current I_Q versus Junction Temperature T_j



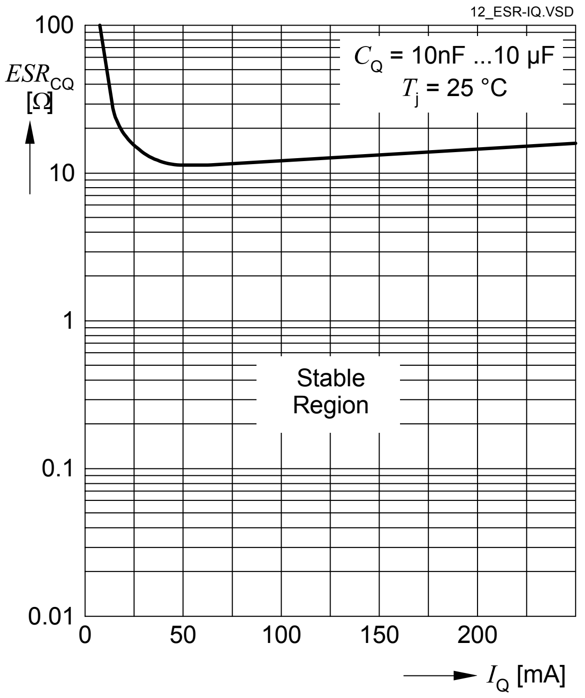
Dropout Voltage V_{dr} versus Junction Temperature



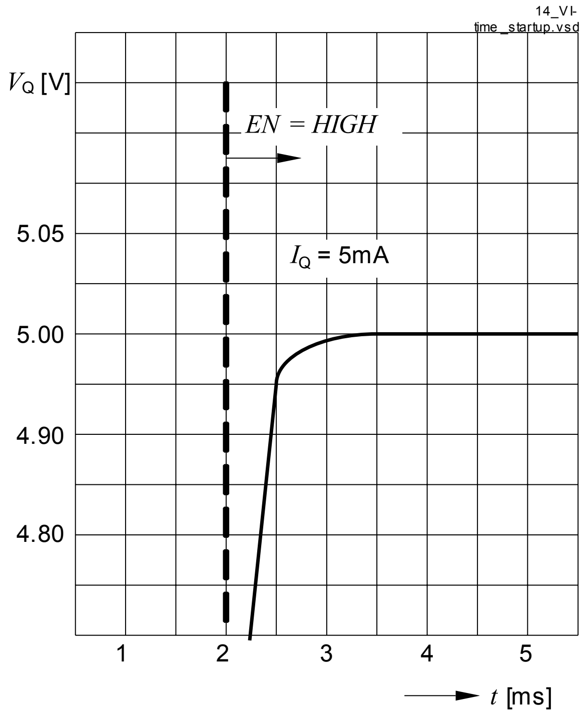
Maximum Output Current I_Q versus Input Voltage V_I



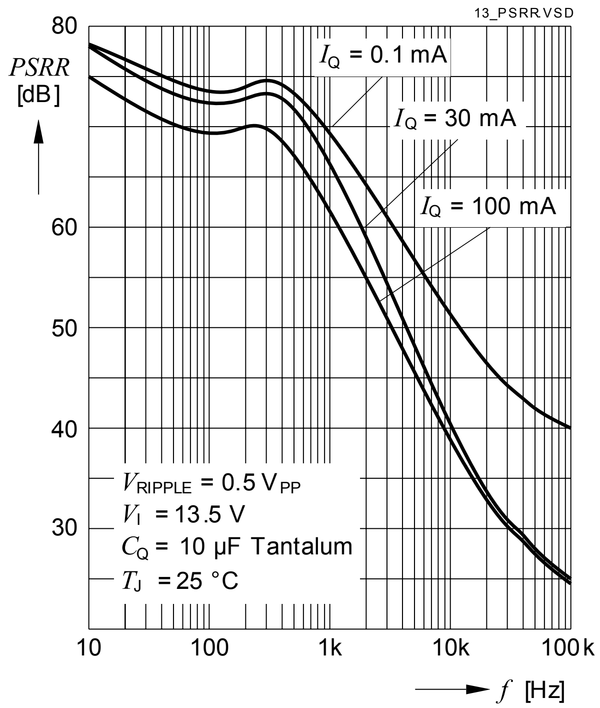
Region of Stability



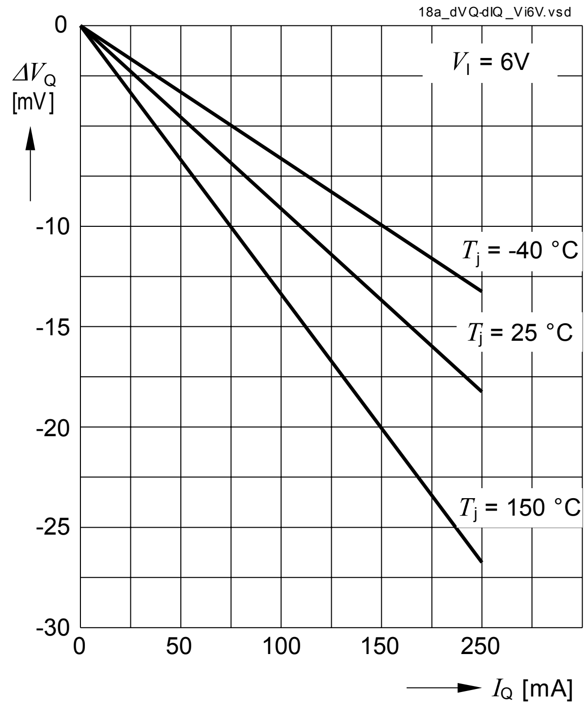
Output Voltage V_Q Start-up behavior



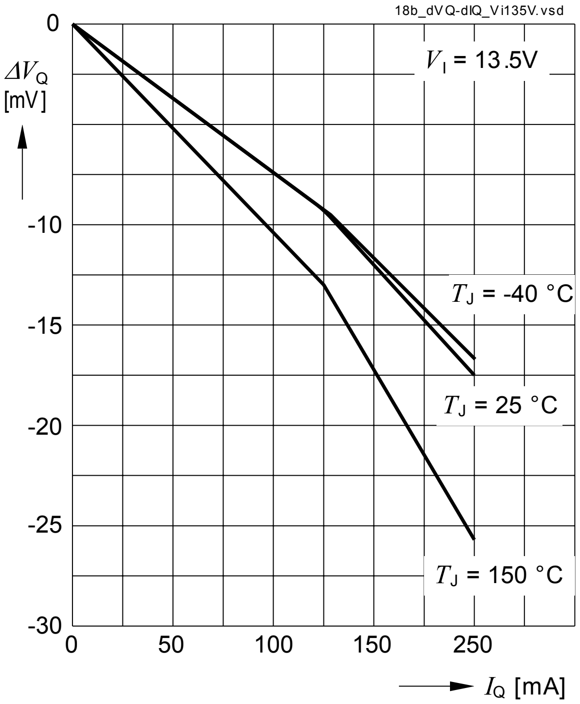
Power Supply Ripple Rejection PSRR versus Frequency f



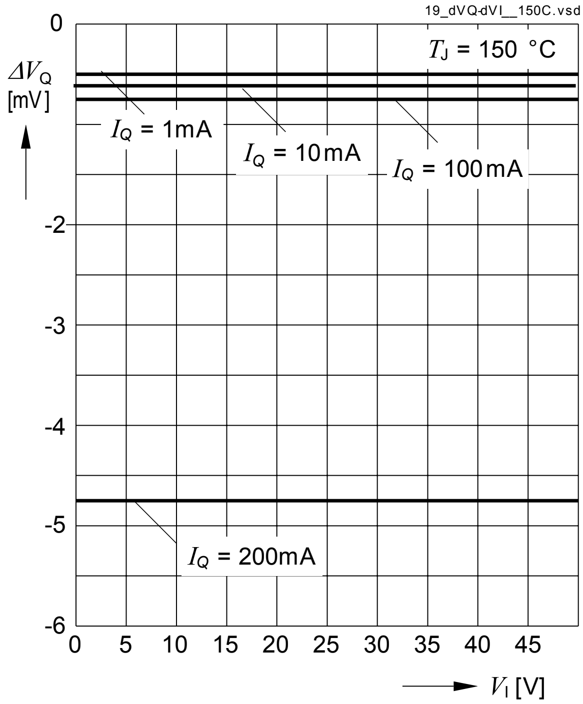
Load Regulation ΔV_Q versus Output Current Change ΔI_Q



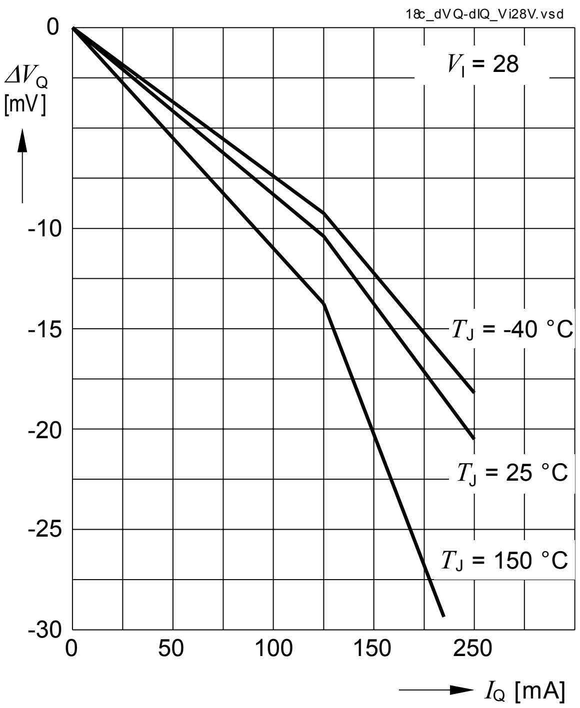
Load Regulation ΔV_Q versus Output Current Change dI_Q



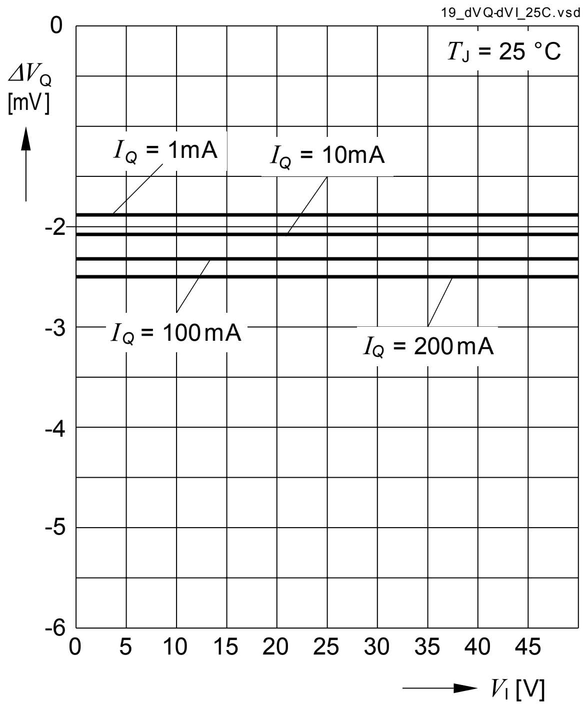
Line Regulation ΔV_Q versus Input Voltage Changed V_I



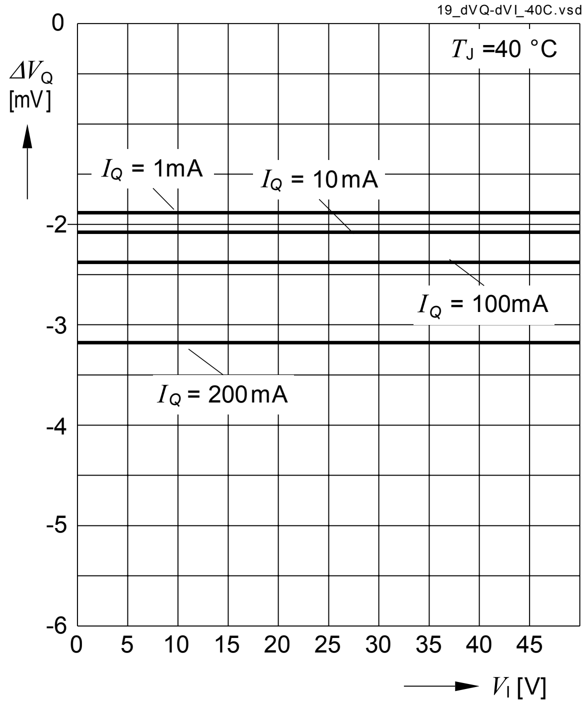
Load Regulation ΔV_Q versus Output Current Change ΔI_Q



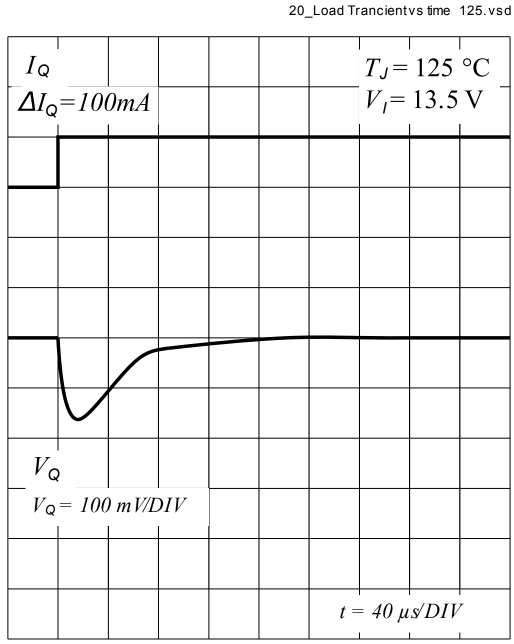
Line Regulation ΔV_Q versus Input Voltage Changed V_I



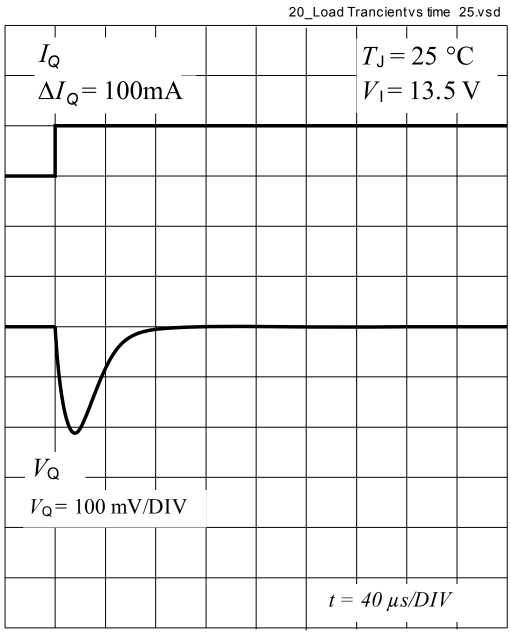
Line Regulation ΔV_Q versus Input Voltage Change V_I



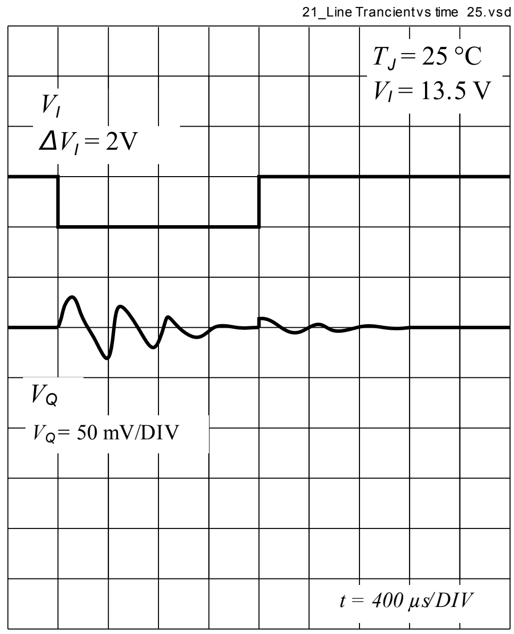
Load Transient Response Peak Voltage ΔV_Q



Load Transient Response Peak Voltage ΔV_Q

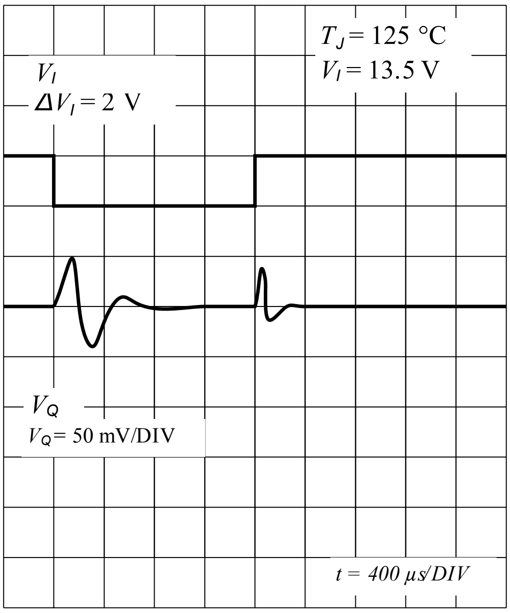


Line Transient Response Peak Voltage ΔV_Q

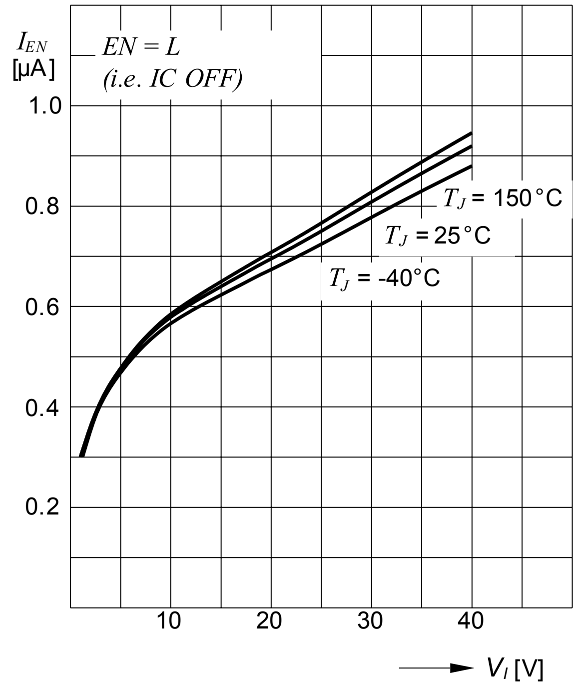


Line Transient Response Peak Voltage ΔV_Q

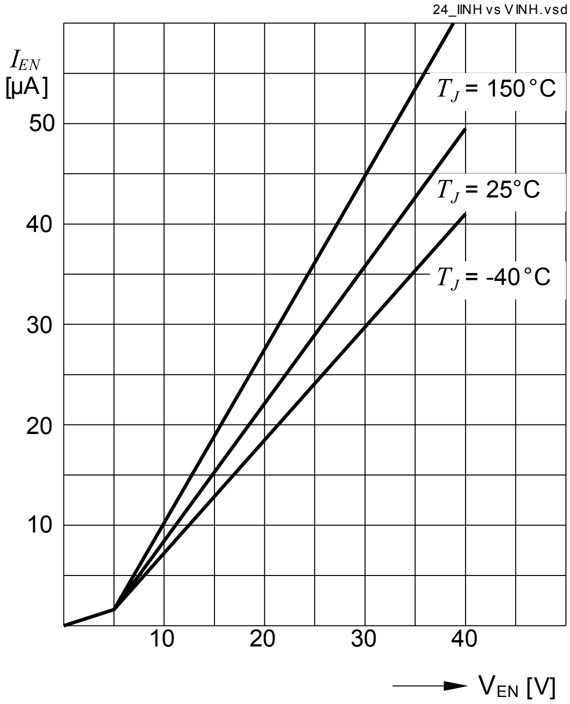
I



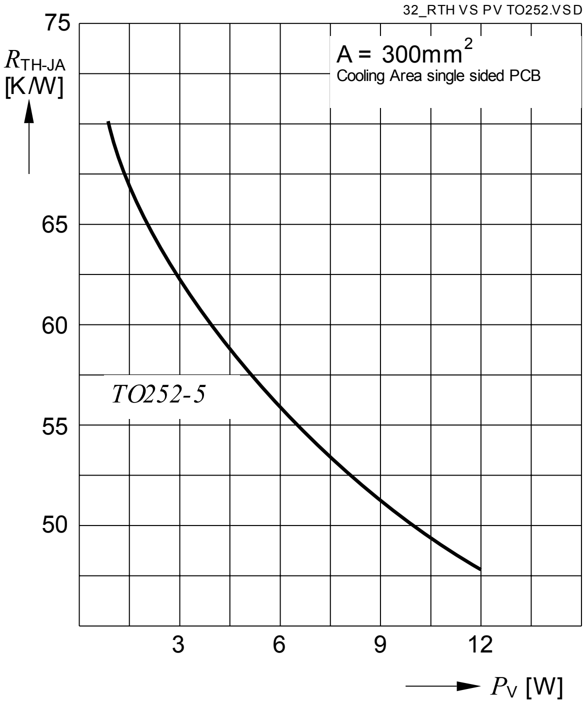
Enabled Input Current I_{EN} versus Input Voltage V_I , EN=Off



Enabled Input Current I_{EN} versus Enabled Input Voltage V_{EN}



Thermal Resistance Junction-Ambient R_{THJA} versus Power Dissipation P_V



6 Application Information

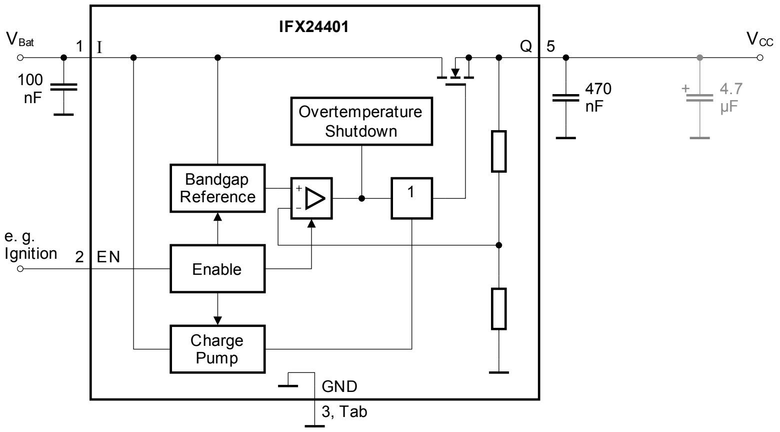


Figure 4 Application Diagram

Input, Output

An input capacitor is necessary for damping line influences. A resistor of approx. 1 Ω in series with C_I, can damp the LC of the input inductivity and the input capacitor.

The IFX24401 requires a ceramic output capacitor of at least 470 nF. In order to damp influences resulting from load current surges it is recommended to add an additional electrolytic capacitor of 4.7 µF to 47 µF at the output as shown in **Figure 4**.

Additionally a buffer capacitor C_B of > 10µF should be used for the output to suppress influences from load surges to the voltage levels. This one can either be an aluminum electrolytic capacitor or a tantalum capacitor following the application requirements.

A general recommendation is to keep the drop over the equivalent serial resistor (ESR) together with the discharge of the blocking capacitor below the allowed Headroom of the Application to be supplied (e.g. typ. dV_Q = 350mV).

Since the regulator output current roughly rises linearly with time the discharge of the capacitor can be calculated as follows:

$dVC_B = dI_Q*dt/C_B$

The drop across the ESR calculates as:

$dV_{ESR} = dI*ESR$

To prevent a reset the following relationship must be fullfilled:

$dV_C + dV_{ESR} < V_{RH} = 350mV$

Example: Assuming a load current change of dI_Q = 100mA, a blocking capacitor of C_B = 22µF and a typical regulator reaction time under normal operating conditions of dt ~ 25µs and for special dynamic load conditions, such as load step from very low base load, a reaction time of dt ~ 75µs.

$dV_C = dI_Q*dt/C_B$ = 100mA * 25µs/22µF = 113mV

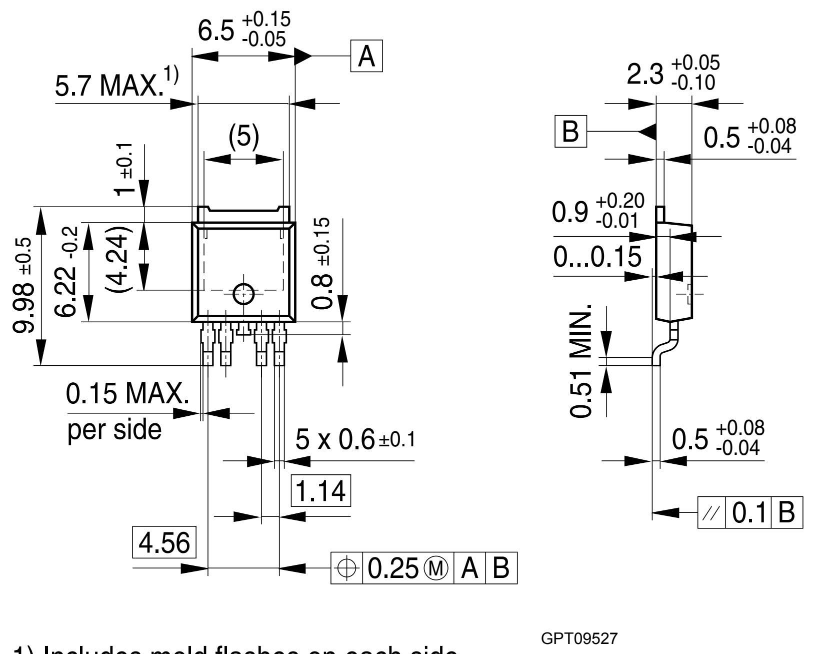
So for the ESR we can allow

$dV_{ESR} = V_{RH2} - dV_C$ = 350mV - 113mV = 236mV

The permissible ESR becomes:

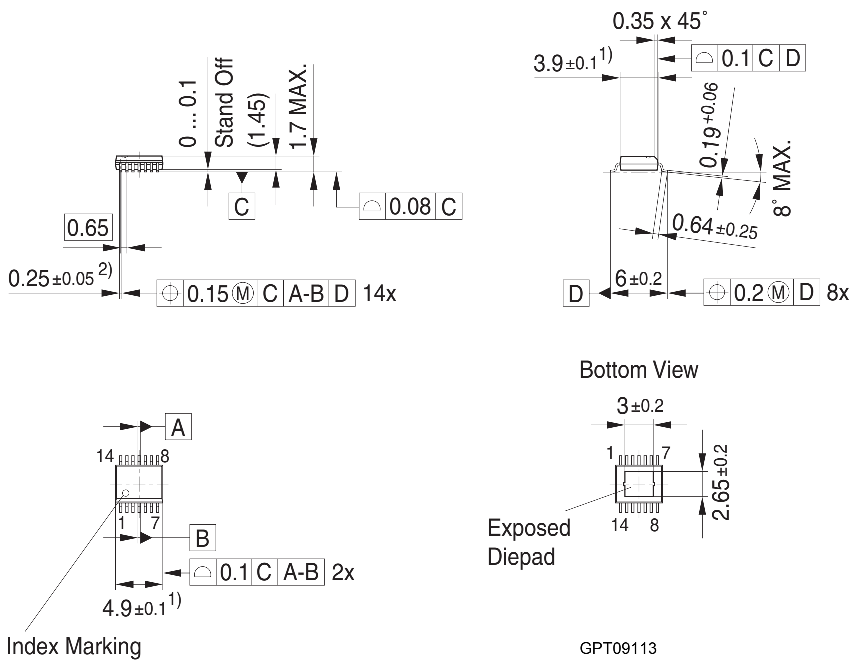
$ESR = dV_{ESR} / dI_Q$ = 236mV/100mA = 2.36Ohm

7 Package Outlines



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 5 PG-TO252-5



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

PG-SSOP-14-1,-2,-3-PO V02

Figure 6 PG-SSOP-14

8 Revision History

Revision	Date	Changes
1.02	2009-12-10	Corrections to pin assignment
1.01	2009-10-19	Coverpage changed Overview page: Inserted reference statement to TLE/TLF series.
1.0	2009-04-28	Initial Release

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