

## Features

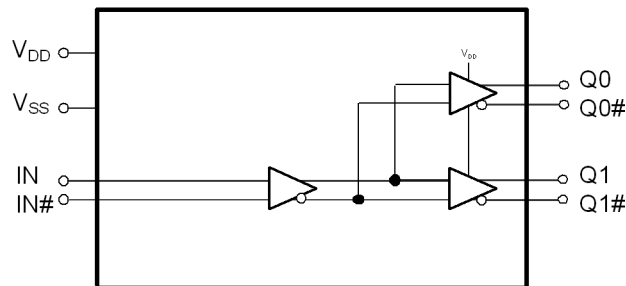
- One differential (LVPECL, LVDS, HCSL, or CML) input pair distributed to two LVPECL output pairs
- Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input
- 20-ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.15-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- 8-pin SOIC or 8-pin TSSOP package
- 2.5-V or 3.3-V operating voltage <sup>[1]</sup>
- Commercial and industrial operating temperature range

## Functional Description

The CY2DP1502 is an ultra-low noise, low-skew, low-propagation delay 1:2 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

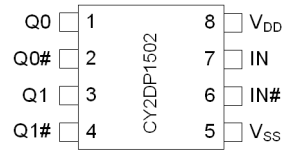
1. Input AC-coupling capacitors are required for voltage-translation applications.

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## Pinouts

Figure 1. 8-pin SOIC and 8-pin TSSOP pinout



## Pin Definitions

Pin Number	Pin Name	Pin Type	Description
1, 3	Q(0:1)	Output	LVPECL output clocks
2, 4	Q(0:1)#	Output	LVPECL complementary output clocks
5	V <sub>SS</sub>	Power	Ground
6	IN#	Input	Differential (LVPECL, LVDS, HCSL, or CML) complementary input clock
7	IN	Input	Differential (LVPECL, LVDS, HCSL, or CML) input clock
8	V <sub>DD</sub>	Power	Power supply

## Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply voltage	Nonfunctional	-0.5	4.6	V
$V_{IN}^{[2]}$	Input voltage, relative to $V_{SS}$	Nonfunctional	-0.5	lesser of 4.0 or $V_{DD} + 0.4$	V
$V_{OUT}^{[2]}$	DC output or I/O voltage, relative to $V_{SS}$	Nonfunctional	-0.5	lesser of 4.0 or $V_{DD} + 0.4$	V
$T_S$	Storage temperature	Nonfunctional	-55	150	°C
$ESD_{HBM}$	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	-	V
$L_U$	Latch-up	Meets or exceeds JEDEC Spec JESD78B IC Latch-up Test	-	-	
UL-94	Flammability rating	At 1/8 in		V-0	
MSL	Moisture sensitivity level	-		3	

## Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
$T_A$	Ambient operating temperature	Commercial	0	70	°C
		Industrial	-40	85	°C
$t_{PU}$	Power ramp time	Power-up time for $V_{DD}$ to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

**Note**

2. The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## DC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Max	Unit
$I_{DD}$	Operating supply current	All LVPECL outputs floating (internal $I_{DD}$ )	–	45	mA
$V_{IH}$	Input high voltage, differential inputs IN and IN#		–	$V_{DD} + 0.3$	V
$V_{IL}$	Input low voltage, differential inputs IN and IN#		–0.3	–	V
$V_{ID\_LVDS}^{[3]}$	LVDS input differential amplitude	See Figure 2 on page 8	0.4	0.8	V
$V_{ID\_LVPECL}^{[3]}$	LVPECL/CML/HCSL input differential amplitude	See Figure 2 on page 8	0.4	1.0	V
$V_{ICM}$	Input common mode voltage	See Figure 2 on page 8	0.2	$V_{DD} - 0.2$	V
$I_{IH}$	Input high current, differential inputs IN and IN#	Input = $V_{DD}^{[4]}$	–	150	$\mu\text{A}$
$I_{IL}$	Input low current, differential inputs IN and IN#	Input = $V_{SS}^{[4]}$	–150	–	$\mu\text{A}$
$V_{OH}$	LVPECL output high voltage	Terminated with $50\ \Omega$ to $V_{DD} - 2.0$ <sup>[5]</sup>	$V_{DD} - 1.20$	$V_{DD} - 0.70$	V
$V_{OL}$	LVPECL output low voltage	Terminated with $50\ \Omega$ to $V_{DD} - 2.0$ <sup>[5]</sup>	$V_{DD} - 2.0$	$V_{DD} - 1.63$	V
$C_{IN}$	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	8-pin SOIC	8-pin TSSOP	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	133	162	$^\circ\text{C/W}$
$\theta_{JC}$	Thermal resistance (junction to case)		44	29	$^\circ\text{C/W}$

### Notes

- $V_{ID}$  minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with  $V_{ID}$  minimum of greater than 200 mV.
- Positive current flows into the input pin, negative current flows out of the input pin.
- Refer to Figure 3 on page 8.
- These parameters are guaranteed by design and are not tested.

## AC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
$F_{IN}$	Input frequency	Differential Input	DC	–	1.5	GHz
		Single-ended CMOS Input <sup>[7]</sup>	DC	–	250	MHz
$F_{OUT}$	Output frequency	$F_{OUT} = F_{IN}$ , Differential Input	DC	–	1.5	GHz
		$F_{OUT} = F_{IN}$ , Single-ended CMOS Input <sup>[7]</sup>	DC	–	250	MHz
$V_{PP}$	LVPECL differential output voltage peak to peak, single-ended, terminated with $50\ \Omega$ to $V_{DD} - 2.0$ <sup>[8]</sup>	$F_{out} = \text{DC to } 150\text{ MHz}$	600	–	–	mV
		$F_{out} = >150\text{ MHz to } 1.5\text{ GHz}$	400	–	–	mV
$t_{PD}$ <sup>[9]</sup>	Propagation delay differential input pair to differential output pair	Input rise/fall time $< 1.5\text{ ns}$ (20% to 80%)	–	–	480	ps
$t_{ODC}$ <sup>[10]</sup>	Output duty cycle	50% duty cycle at input, Frequency range up to 1 GHz, Differential input	48	–	52	%
		50% duty cycle at input, Frequency range up to 250MHz, Single-ended CMOS input <sup>[7]</sup>	45	–	55	%
$t_{SK1}$ <sup>[11]</sup>	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	20	ps
$t_{SK1D}$ <sup>[11]</sup>	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
$PN_{ADD}$	Additive RMS phase noise, 156.25-MHz input, Rise/fall time $< 150\text{ ps}$ (20% to 80%), $V_{ID} > 400\text{ mV}$ or Input Swing = $3.0\text{ V}$ <sup>[7]</sup>	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–145	dBc/Hz
		Offset = 10 MHz	–	–	–153	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz

### Notes

7. Refer to Application Information on page 10.
8. Refer to Figure 3 on page 8.
9. Refer to Figure 4 on page 8.
10. Refer to Figure 5 on page 8.
11. Refer to Figure 6 on page 9.

**AC Electrical Specifications** (continued)

 $(V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

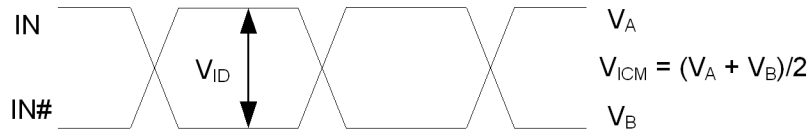
Parameter	Description	Condition	Min	Typ	Max	Unit
$t_{JIT}^{[12]}$	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400\text{ mV}$	–	–	0.15	ps
		156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V <sup>[13]</sup>	–	–	0.15	ps
$t_R, t_F^{[14]}$	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing ( $V_{OL}$ to $V_{OH}$ ) Input rise/fall time < 1.5 ns (20% to 80%)	–	–	250	ps

**Notes**

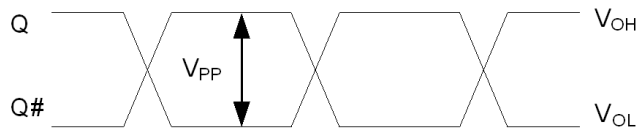
12. Refer to Figure 7 on page 9.  
 13. Refer to Application Information on page 10.  
 14. Refer to Figure 8 on page 9.

## Switching Waveforms

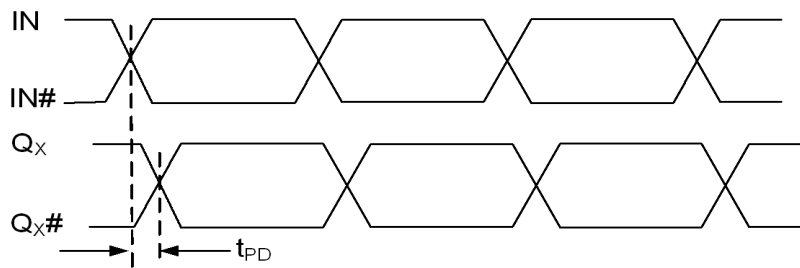
**Figure 2. Input Differential and Common Mode Voltages**



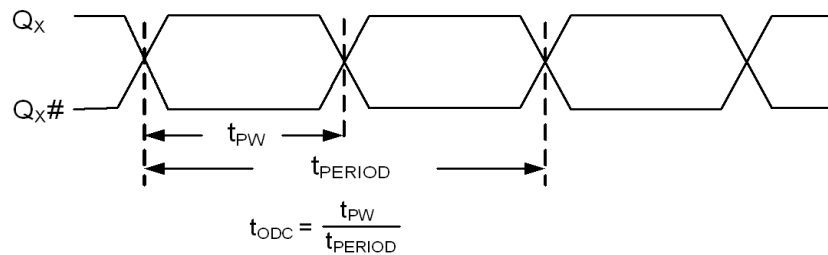
**Figure 3. Output Differential Voltage**



**Figure 4. Input to Any Output Pair Propagation Delay**



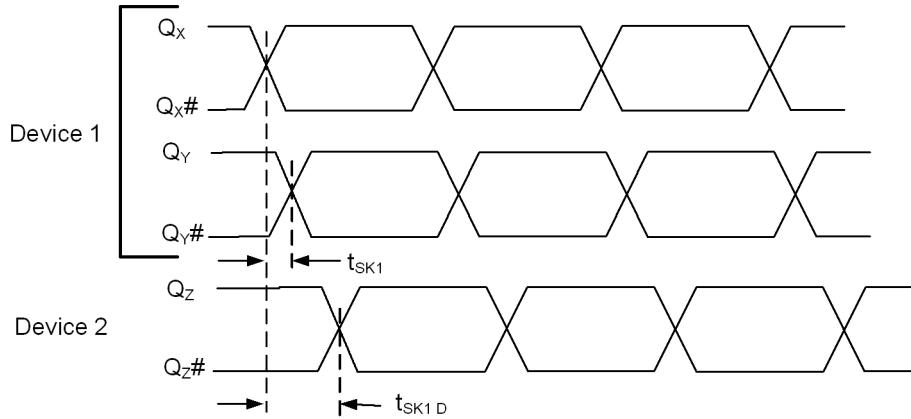
**Figure 5. Output Duty Cycle**



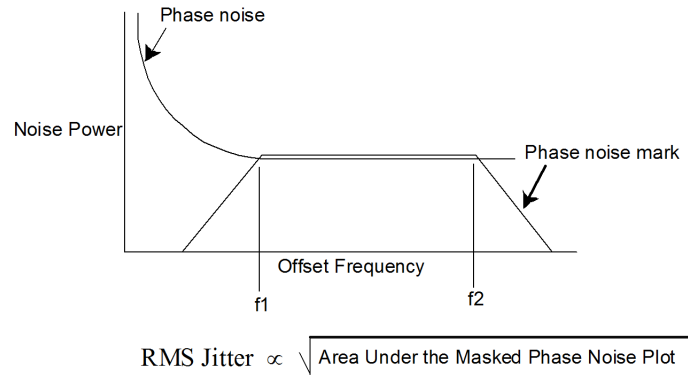


**Switching Waveforms** (continued)

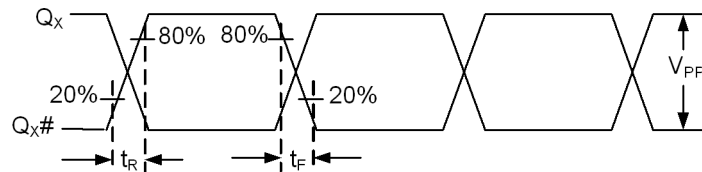
**Figure 6. Output-to-Output and Device-to-Device Skew**



**Figure 7. RMS Phase Jitter**



**Figure 8. Output Rise/Fall Time**



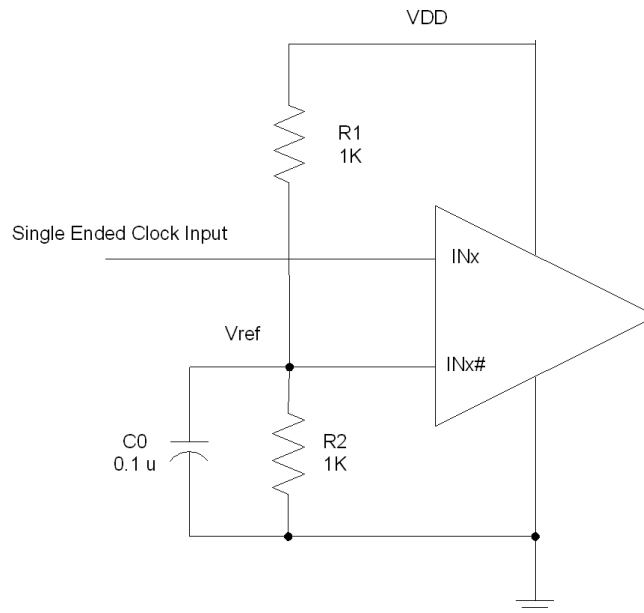
### Application Information

CY2DP1502 can be used with a single ended CMOS input by biasing the Complementary Input Clock (INx#). “True” input pins (INx) of differential input pair can be fed with a single ended CMOS input signal. The “complementary” input pin (INx#) of the same differential input pair can be biased with Vref.

Figure 9 shows the schematic which can be used to give single ended CMOS input to the CY2DP1502.

The reference voltage  $V_{ref} = VDD/2$  is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and  $VDD = 3.3$  V,  $V_{ref}$  should be 1.25 V and  $R2/R1 = 0.609$ .

**Figure 9. Application Example**

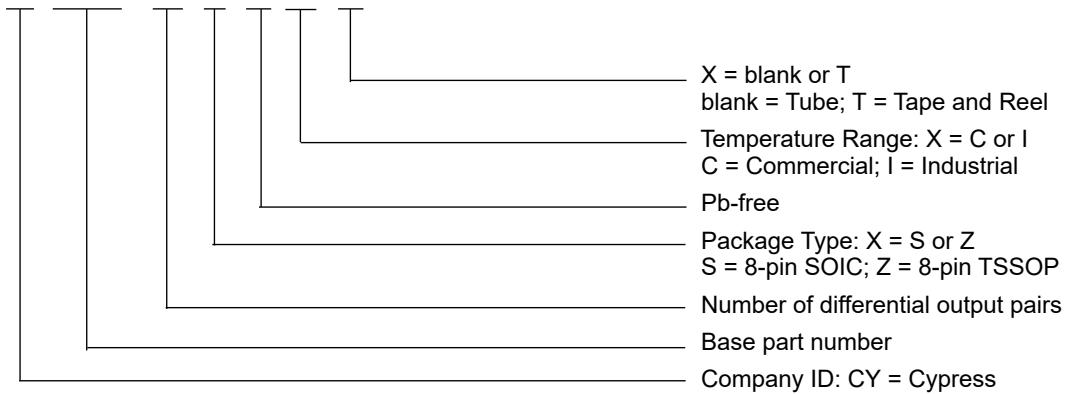


### Ordering Information

Part Number	Type	Production Flow
<b>Pb-free</b>		
CY2DP1502SXI	8-pin SOIC	Industrial, -40 °C to 85 °C
CY2DP1502SXIT	8-pin SOIC – Tape and Reel	Industrial, -40 °C to 85 °C
CY2DP1502ZXI	8-pin TSSOP	Industrial, -40 °C to 85 °C
CY2DP1502ZXIT	8-pin TSSOP – Tape and Reel	Industrial, -40 °C to 85 °C

### Ordering Code Definitions

CY 2DP15 02 X X X X

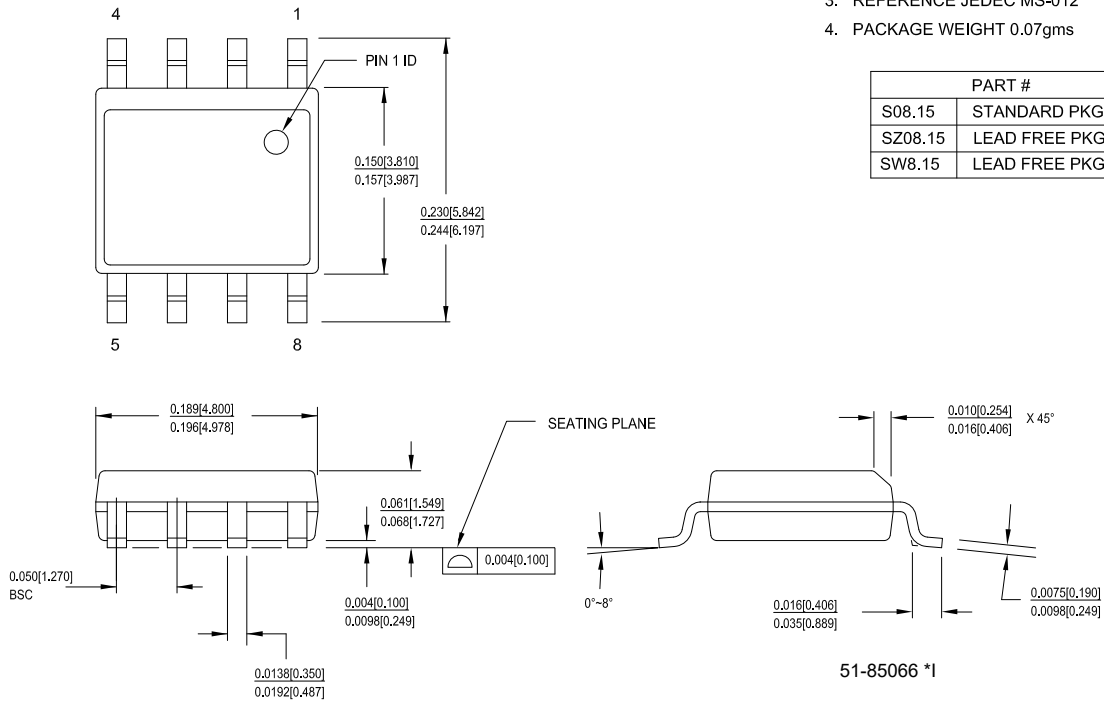


Package Diagrams

Figure 10. 8-pin SOIC (150 Mils) S08.15/SZ08.15 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

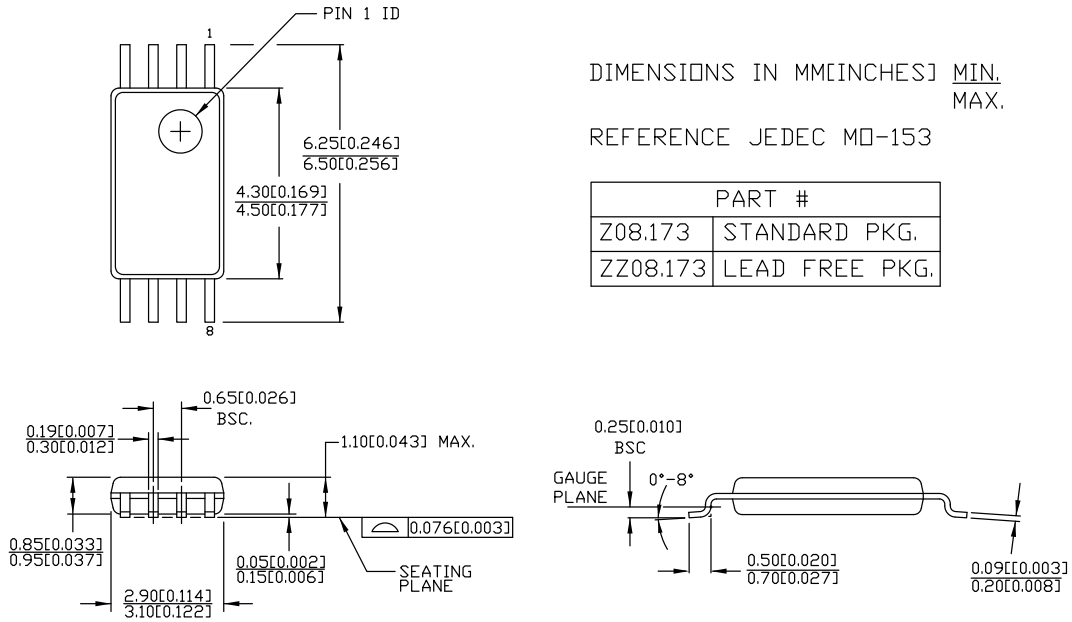
PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 \*1

Package Diagrams (continued)

Figure 11. 8-pin TSSOP 4.40 mm Body Z08.173/ZZ08.173 Package Outline, 51-85093



DIMENSIONS IN MM[INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.

51-85093 \*E

## Acronyms

Acronym	Description
ESD	electrostatic discharge
HBM	Human Body Model
HCSL	high-speed current steering logic
JEDEC	Joint Electron Devices Engineering Council
LVDS	low-voltage differential signal
LVC MOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LV TTL	low-voltage transistor-transistor logic
RMS	root mean square
TSSOP	thin shrunk small outline package

## Document Conventions

### Units of Measure

Symbol	Units of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kΩ	kilohm
MHz	megahertz
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

**Document History Page**

Document Title: CY2DP1502, 1:2 LVPECL Fanout Buffer Document Number: 001-56308				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2782891	CXQ	10/09/2009	New data sheet.
*A	2838916	CXQ	01/05/2010	<p>Changed status from Advance to Preliminary.</p> <p>Updated <b>Features</b>:            Replaced “0.34 ps Maximum Additive RMS Phase Jitter” with “0.25 ps Maximum Additive RMS Phase Jitter”.</p> <p>Updated <b>Operating Conditions</b>:            Added <math>t_{PU}</math> parameter and its details.</p> <p>Updated <b>DC Electrical Specifications</b>:            Changed minimum value of <math>V_{OH}</math> parameter from “<math>V_{DD} - 1.15 V</math>” to “<math>V_{DD} - 1.20 V</math>”.            Changed maximum value of <math>V_{OH}</math> parameter from “<math>V_{DD} - 0.75 V</math>” to “<math>V_{DD} - 0.70 V</math>”.            Removed <math>V_{OD}</math> parameter and its details.            Added <math>R_P</math> parameter and its details.            Added details in “Test Condition” column corresponding to <math>C_{IN}</math> parameter.</p> <p>Updated <b>AC Electrical Specifications</b>:            Updated details in “Parameter” column (Changed letter case and some names of parameters to be consistent with EROS).            Added <math>V_{PP}</math> parameter and its details.            Changed maximum value of <math>t_{JIT}</math> parameter from 0.34 ps to 0.25 ps.            Updated maximum values of <math>PN_{ADD}</math> parameter (Lowered all values by 3 dB).            Updated details in “Condition” column of <math>t_R</math>, <math>t_F</math> parameter (Added “Input rise/fall time &lt; 1.5 ns (20% to 80%)”).</p> <p>Updated <b>Switching Waveforms</b>:            No change in figures (Changed letter case and some names of timing parameters in all figures to be consistent with EROS).</p>
*B	3011766	CXQ	08/20/2010	<p>Updated <b>Features</b>:            Replaced “0.25 ps Maximum Additive RMS Phase Jitter” with “0.11 ps Maximum Additive RMS Phase Jitter”.</p> <p>Updated <b>Functional Description</b>:            Updated description.</p> <p>Updated <b>Logic Block Diagram</b>:            Changed <math>R_P</math> for differential inputs from 100 k<math>\Omega</math> to 150 k<math>\Omega</math>.</p> <p>Updated <b>DC Electrical Specifications</b>:            Added 1.0 V in “Max” column corresponding to <math>V_{ID}</math> parameter.            Added Note 4 and referred the same note in “Test Condition” column of <math>I_{IH}</math> and <math>I_{IL}</math> parameters.            Changed minimum value of <math>R_P</math> parameter from 60 k<math>\Omega</math> to 90 k<math>\Omega</math>.            Changed maximum value of <math>R_P</math> parameter from 140 k<math>\Omega</math> to 210 k<math>\Omega</math>.</p> <p>Updated <b>AC Electrical Specifications</b>:            Added “Frequency range up to 1 GHz” in “Test Condition” column corresponding to <math>t_{ODC}</math> parameter.            Updated maximum values of <math>PN_{ADD}</math> parameter.            Changed maximum value of <math>t_{JIT}</math> parameter from 0.25 ps to 0.11 ps.</p> <p>Updated <b>Ordering Information</b>:            No change in part numbers.            Added <b>Ordering Code Definitions</b>.            Updated <b>Package Diagrams</b>:            spec 51-85066 – Changed revision from *C to *D.            spec 51-85093 – Changed revision from *B to *C.            Added <b>Acronyms and Units of Measure</b>.</p>
*C	3017258	CXQ	08/27/2010	<p>Updated <b>AC Electrical Specifications</b>:            Updated <b>Figure 8</b>.</p>

Document History Page (continued)

Document Title: CY2DP1502, 1:2 LVPECL Fanout Buffer Document Number: 001-56308				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*D	3100234	CXQ	11/18/2010	Updated <a href="#">Absolute Maximum Ratings</a> : Changed maximum value of $V_{IN}$ parameter from 4.0 V to "lesser of 4.0 or $V_{DD} + 0.4$ ". Changed maximum value of $V_{OUT}$ parameter from 4.0 V to "lesser of 4.0 or $V_{DD} + 0.4$ ". Removed minimum value of LU parameter. Added "Meets or exceeds JEDEC Spec JESD78B IC Latch-up Test" under "Min" and "Max" columns of LU parameter. Updated <a href="#">DC Electrical Specifications</a> : Removed $R_p$ parameter and its details. Replaced "Measured at 1 MHz" with "Measured at 10 MHz" in "Condition" column corresponding to $C_{IN}$ parameter. Updated <a href="#">AC Electrical Specifications</a> : Updated maximum values of $PN_{ADD}$ parameter corresponding to Conditions "Offset = 1 MHz", "Offset = 10 MHz", and "Offset = 20 MHz". Changed maximum value of $t_{JIT}$ parameter from 0.11 ps to 0.15 ps.
*E	3137726	CXQ	01/13/2011	Changed status from Preliminary to Final. Updated <a href="#">Logic Block Diagram</a> (Removed resistors on IN/IN#).
*F	3137726	CXQ	01/13/2011	Minor change: Post to external web.
*G	3234654	VED	04/19/2011	Minor change: Revision was not updated in footer in previous revision and updated in this version. Description of Changed was not updated in previous revision and updated in this revision.
*H	3308039	CXQ	07/11/2011	Updated <a href="#">Features</a> : Replaced "One low-voltage positive emitter-coupled logic (LVPECL) input pair distributed to two LVPECL output pairs" with "One differential (LVPECL, LVDS, or CML) input pair distributed to two LVPECL output pairs". Updated <a href="#">Pin Definitions</a> : Updated details in "Description" column corresponding to pin 6 and 7. Updated <a href="#">DC Electrical Specifications</a> : Replaced "LVPECL inputs" with "differential inputs" in "Description" column corresponding to $V_{IH}$ , $V_{IL}$ , $I_{IH}$ and $I_{IL}$ parameters. Removed $V_{ID}$ parameter and its details. Added $V_{ID\_LVDS}$ and $V_{ID\_LVPECL}$ parameters and their details. Updated <a href="#">Package Diagrams</a> : spec 51-85066 – Changed revision from *D to *E.
*I	3395868	PURU	10/05/2011	Updated <a href="#">Features</a> : Replaced "One differential (LVPECL, LVDS, or CML) input pair distributed to two LVPECL output pairs" with "One differential (LVPECL, LVDS, HCSL, or CML) input pair distributed to two LVPECL output pairs". Updated <a href="#">Pin Definitions</a> : Updated details in "Description" column corresponding to pin 6 and 7. Updated <a href="#">DC Electrical Specifications</a> : Replaced "LVPECL/CML input differential amplitude" with "LVPECL/CML/HCSL input differential amplitude" in "Description" column corresponding to $V_{ID\_LVPECL}$ parameter. Changed minimum value of $V_{ICM}$ parameter from 0.5 V to 0.2 V.



Document History Page (continued)

Document Title: CY2DP1502, 1:2 LVPECL Fanout Buffer Document Number: 001-56308				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*J	3799048	PURU	12/05/2012	<p>Updated <b>Features</b>: Added "Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input".</p> <p>Updated <b>AC Electrical Specifications</b>: Added Condition "Single Ended CMOS Input" and added corresponding values (Minimum value = DC, Maximum value = 250 MHz) for F<sub>IN</sub> parameter. Added Condition "Single Ended CMOS Input" and added corresponding values (Minimum value = DC, Maximum value = 250 MHz) for F<sub>OUT</sub> parameter. Added Note 7 and referred the same note in "Single-ended CMOS Input" in "Condition" column of F<sub>IN</sub> and F<sub>OUT</sub> parameters. Replaced "Propagation delay input pair to output pair" with "Propagation delay differential input pair to differential output pair" in "Description" column of t<sub>PD</sub> parameter. Added Condition "Single Ended CMOS Input" and added corresponding values (Minimum value = 45%, Maximum value = 55%) for t<sub>ODC</sub> parameter. Replaced "Additive RMS phase noise, 156.25-MHz input, Rise/fall time &lt; 150 ps (20% to 80%), V<sub>ID</sub> &gt; 400 mV" with "Additive RMS phase noise, 156.25-MHz input, Rise/fall time &lt; 150 ps (20% to 80%), V<sub>ID</sub> &gt; 400 mV or Input Swing = 3.0 V<sup>[7]</sup>" in "Description" column of PN<sub>ADD</sub> parameter. Added Condition "156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time &lt; 150 ps (20% to 80%), Input Swing = 3.0 V<sup>[13]</sup>" and added corresponding values (Maximum value = 0.15 ps) for t<sub>JIT</sub> parameter. Added Note 13 and referred the same note in "Input Swing = 3.0 V" in "Condition" column of t<sub>JIT</sub> parameter. Added <b>Application Information</b>. Updated <b>Package Diagrams</b>: spec 51-85093 – Changed revision from *C to *D. Updated to new template.</p>
*K	3882598	PURU	01/24/2013	<p>No technical updates. Completing Sunset Review.</p>
*L	4587249	PURU	12/04/2014	<p>Updated <b>Functional Description</b>: Added "For a complete list of related documentation, <a href="#">click here.</a>" at the end. Updated <b>Ordering Information</b>: Updated part numbers. Updated <b>Package Diagrams</b>: spec 51-85066 – Changed revision from *E to *F. spec 51-85093 – Changed revision from *D to *E. Completing Sunset Review.</p>
*M	5272915	PSR	05/16/2016	<p>Added <b>Thermal Resistance</b>. Updated <b>Package Diagrams</b>: spec 51-85066 – Changed revision from *F to *H. Updated to new template.</p>
*N	6079539	PAWK	02/23/2018	<p>Updated <b>Package Diagrams</b>: spec 51-85066 – Changed revision from *H to *I. Updated to new template. Completing Sunset Review.</p>

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