

# BTS5236-2GS

Smart High-Side Power Switch

PROFET

Two Channels, 50 m $\Omega$

Automotive Power



Never stop thinking

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## Smart High-Side Power Switch PROFET

**BTS5236-2GS**



### Product Summary

The BTS5236-2GS is a dual channel high-side power switch in PG-DSO-14-32 package providing embedded protective functions.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The device is monolithically integrated in Smart SIPMOS technology.

#### PG-DSO-14-32



|  |               |              |
|--|---------------|--------------|
| Operating voltage                          | $V_{bb(on)}$  | 4.5 ... 28 V |
| Over voltage protection                    | $V_{bb(AZ)}$  | 41 V         |
| On-State resistance                        | $R_{DS(ON)}$  | 50 mΩ        |
| Nominal load current (one channel active)  | $I_{L(nom)}$  | 3.2 A        |
| Current limitation                         | $I_{L(LIM)}$  | 23 A         |
| Current limitation repetitive              | $I_{L(SCr)}$  | 6 A          |
| Standby current for whole device with load | $I_{bb(OFF)}$ | 2.5 μA       |

### Basic Features

- Green product (RoHS Compliant)
- Very low standby current
- 3.3 V and 5 V compatible logic pins
- Improved electromagnetic compatibility (EMC)
- Stable behavior at under voltage
- Logic ground independent from load ground
- Secure load turn-off while logic ground disconnected
- Optimized inverse current capability
- AEC qualified

| Type        | Package      | Marking     |
|-------------|--------------|-------------|
| BTS5236-2GS | PG-DSO-14-32 | BTS5236-2GS |

## **Protective Functions**

- Reverse battery protection without external components
- Short circuit protection
- Overload protection
- Multi-step current limitation
- Thermal shutdown with restart
- Thermal restart at reduced current limitation
- Over voltage protection without external resistor
- Loss of ground protection
- Electrostatic discharge protection (ESD)

## **Diagnostic Functions**

- Enhanced IntelliSense signal for each channel
- Enable function for diagnosis pins (IS1 and IS2)
- Proportional load current sense signal by current source
- High accuracy of current sense signal at wide load current range
- Open load detection in ON-state by load current sense
- Over load (current limitation) diagnosis in ON-state, signalling by voltage source
- Latched over temperature diagnosis in ON-state, signalling by voltage source
- Open load detection in OFF-state, signalling by voltage source

## **Applications**

- $\mu$ C compatible high-side power switch with diagnostic feedback for 12 V grounded loads
- Suitable for automotive and industrial applications
- All types of resistive, inductive and capacitive loads
- Suitable for loads with high inrush currents, such as lamps
- Suitable for loads with low currents, such as LEDs
- Replaces electromechanical relays, fuses and discrete circuits

## 1 Overview

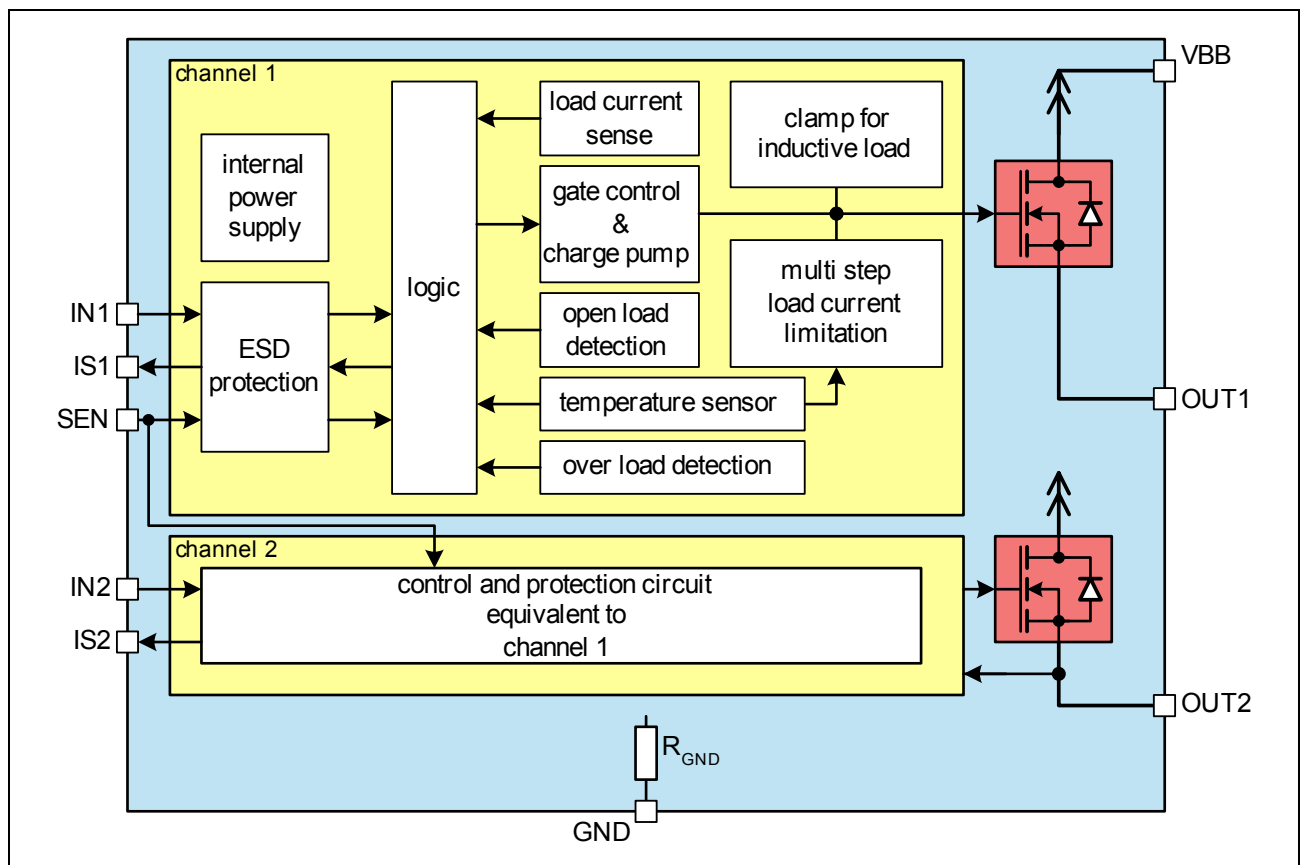
The BTS5236-2GS is a dual channel high-side power switch (two times 50mΩ) in PG-DSO-14-32 package providing embedded protective functions.

The Enhanced IntelliSense pins IS1 and IS2 provide a sophisticated diagnostic feedback signal including current sense function, over load and over temperature alerts in ON-state and open load alert in OFF-state. The diagnosis signals can be switched on and off by the sense enable pin SEN.

An integrated ground resistor as well as integrated resistors at each input pin (IN1, IN2, SEN) reduce external components to a minimum.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart SIPMOS technology.

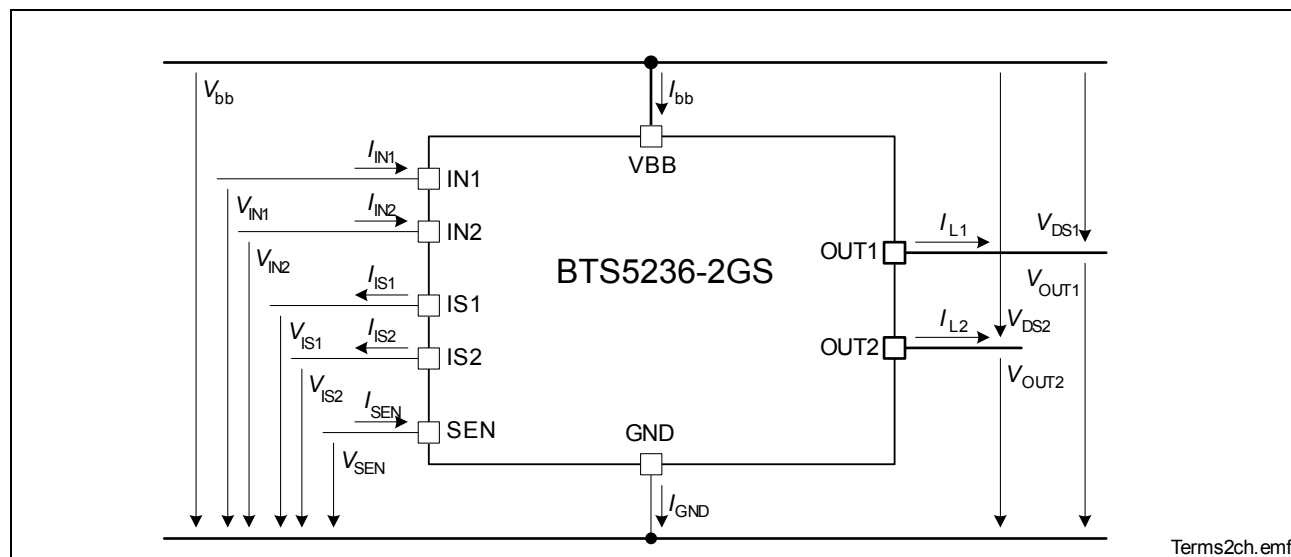
### 1.1 Block Diagram



**Figure 1** Block Diagram

### 1.2 Terms

Following figure shows all terms used in this datasheet.

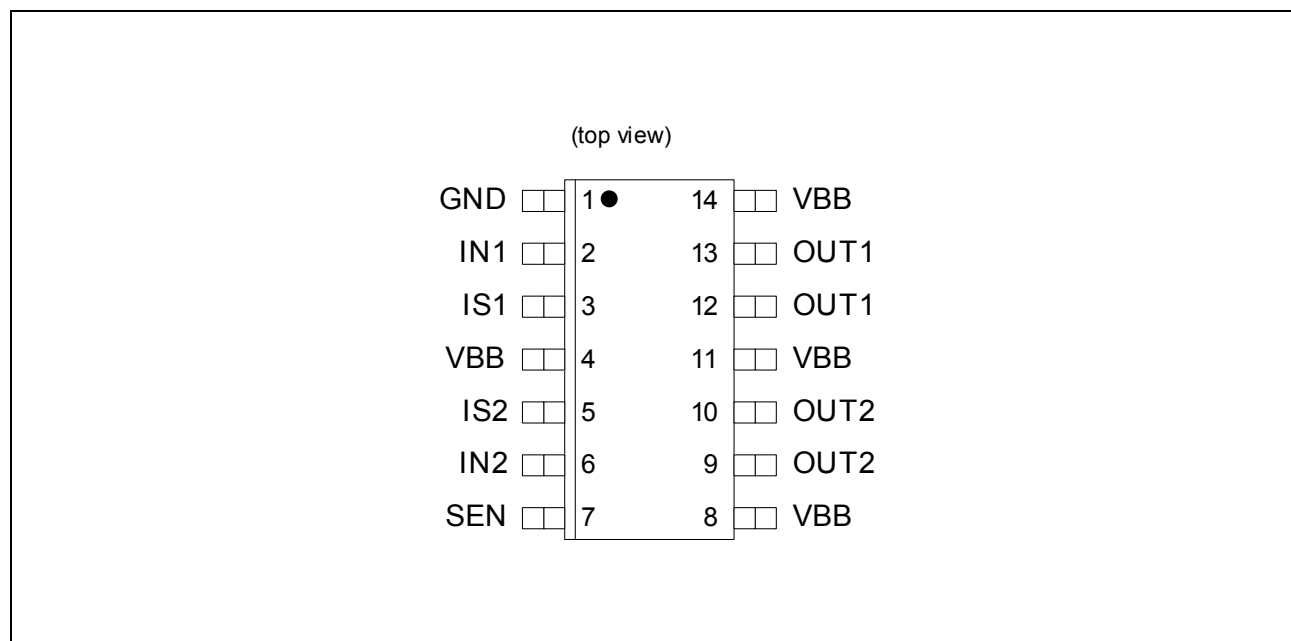


**Figure 2 Terms**

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately.

## 2 Pin Configuration

### 2.1 Pin Assignment BTS5236-2GS



**Figure 3 Pin Configuration PG-DSO-14-32**

### 2.2 Pin Definitions and Functions

| Pin          | Symbol             | I/O | Function  |
|--------------|--------------------|-----|---|
| 2            | IN1                | I   | Input signal for channel 1  |
| 6            | IN2                | I   | Input signal for channel 2  |
| 3            | IS1                | O   | Diagnosis output signal channel 1                                     |
| 5            | IS2                | O   | Diagnosis output signal channel 2                                     |
| 7            | SEN                | I   | Sense Enable input for channel 1&2                                    |
| 12, 13       | OUT1 <sup>1)</sup> | O   | Protected high-side power output channel 1                            |
| 9, 10        | OUT2 <sup>1)</sup> | O   | Protected high-side power output channel 2                            |
| 1            | GND                | –   | Ground connection   |
| 4, 8, 11, 14 | VBB <sup>2)</sup>  | –   | Positive power supply for logic supply as well as output power supply |

1) All output pins of each channel have to be connected

2) All VBB pins have to be connected

### 3 Electrical Characteristics

#### 3.1 Maximum Ratings

Stresses above the ones listed here may affect device reliability or may cause permanent damage to the device.

Unless otherwise specified:

$$T_j = 25\text{ }^{\circ}\text{C}$$

| Pos. | Parameter | Symbol | Limit Values |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|-----------------|
|      |           |        | min.         | max. |      |                 |

##### Supply Voltage

|       |   |              |     |    |   |   |
|-------|---|--------------|-----|----|---|---|
| 3.1.1 | Supply voltage  | $V_{bb}$     | -16 | 28 | V |   |
| 3.1.2 | Supply voltage for full short circuit protection (single pulse)<br>( $T_{j(0)} = -40\text{ }^{\circ}\text{C} \dots 150\text{ }^{\circ}\text{C}$ ) | $V_{bb(SC)}$ | 0   | 28 | V | $L = 8\text{ }\mu\text{H}$ ,<br>$R = 0.2\text{ }\Omega$ <sup>1)</sup> |
| 3.1.3 | Voltage at power transistor   | $V_{DS}$     |     | 52 | V |   |
| 3.1.4 | Supply Voltage for Load Dump protection   | $V_{bb(LD)}$ |     | 41 | V | $R_l = 2\text{ }\Omega$ <sup>2)</sup><br>$R_L = 6.8\text{ }\Omega$    |

##### Power Stages

|       |   |           |  |              |    |  |
|-------|---|-----------|--|--------------|----|--|
| 3.1.5 | Load current                            | $I_L$     |  | $I_{L(LIM)}$ | A  | <sup>3)</sup>  |
| 3.1.6 | Maximum energy dissipation single pulse | $E_{AS}$  |  | 110          | mJ | $V_{bb} = 13.5\text{V}$<br>$I_L(0) = 2\text{ A}$ <sup>4)</sup><br>$T_j(0) = 150\text{ }^{\circ}\text{C}$ |
| 3.1.7 | Power dissipation (DC)                  | $P_{tot}$ |  | 1.1          | W  | $T_a = 85\text{ }^{\circ}\text{C}$ <sup>5)</sup><br>$T_j \leq 150\text{ }^{\circ}\text{C}$               |

##### Logic Pins

|        |                                  |           |              |     |    |                       |
|--------|----------------------------------|-----------|--------------|-----|----|-----------------------|
| 3.1.8  | Voltage at input pin             | $V_{IN}$  | -5<br>-16    | 10  | V  | $t \leq 2\text{ min}$ |
| 3.1.9  | Current through input pin        | $I_{IN}$  | -2.0<br>-8.0 | 2.0 | mA | $t \leq 2\text{ min}$ |
| 3.1.10 | Voltage at sense enable pin      | $V_{SEN}$ | -5<br>-16    | 10  | V  | $t \leq 2\text{ min}$ |
| 3.1.11 | Current through sense enable pin | $I_{SEN}$ | -2.0<br>-8.0 | 2.0 | mA | $t \leq 2\text{ min}$ |
| 3.1.12 | Current through sense pin        | $I_{IS}$  | -25          | 10  | mA |                       |



### Electrical Characteristics

Unless otherwise specified:

$$T_j = 25\text{ }^{\circ}\text{C}$$

| Pos. | Parameter | Symbol | Limit Values |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|-----------------|
|      |           |        | min.         | max. |      |                 |

#### Temperatures

|        |  |                  |     |     |                    |  |
|--------|--|------------------|-----|-----|--------------------|--|
| 3.1.13 | Junction Temperature                         | $T_j$            | -40 | 150 | $^{\circ}\text{C}$ |  |
| 3.1.14 | Dynamic temperature increase while switching | $\Delta T_j$     | -   | 60  | $^{\circ}\text{C}$ |  |
| 3.1.15 | Storage Temperature                          | $T_{\text{stg}}$ | -55 | 150 | $^{\circ}\text{C}$ |  |

#### ESD Susceptibility

|        |                        |                  |    |   |    |                                 |
|--------|------------------------|------------------|----|---|----|---------------------------------|
| 3.1.16 | ESD susceptibility HBM | $V_{\text{ESD}}$ |    |   | kV | according to EIA/JESD 22-A 114B |
|        | IN, SEN                |                  | -1 | 1 |    |                                 |
|        | IS                     |                  | -2 | 2 |    |                                 |
|        | OUT                    |                  | -4 | 4 |    |                                 |

- 1)  $R$  and  $L$  describe the complete circuit impedance including line, contact and generator impedances.
- 2) Load Dump is specified in ISO 7637,  $R_i$  is the internal resistance of the Load Dump pulse generator.
- 3) Current limitation is a protection feature. Operation in current limitation is considered as "outside" normal operating range. Protection features are not designed for continuous repetitive operation.
- 4) Pulse shape represents inductive switch off:  $I_L(t) = I_L(0) * (1 - t / t_{\text{pulse}})$ ;  $0 < t < t_{\text{pulse}}$ .
- 5) Device mounted on PCB (50 mm × 50 mm × 1.5mm epoxy, FR4) with 6 cm<sup>2</sup> copper heatsinking area (one layer, 70 μm thick) for  $V_{\text{bb}}$  connection. PCB is vertical without blown air.

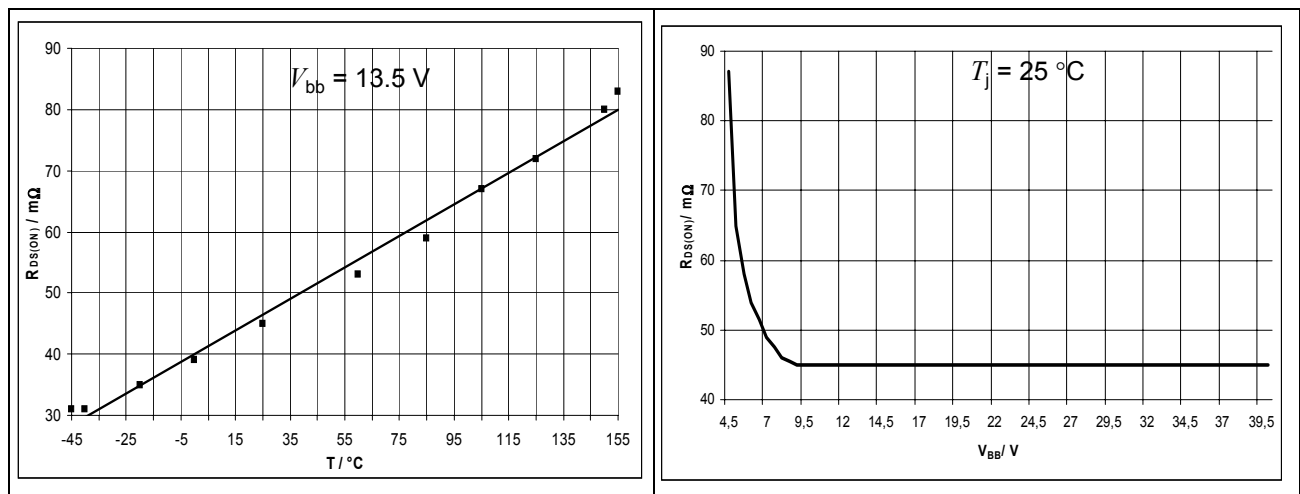
## 4 Block Description and Electrical Characteristics

### 4.1 Power Stages

The power stages are built by N-channel vertical power MOSFETs (DMOS) with charge pumps.

#### 4.1.1 Output On-State Resistance

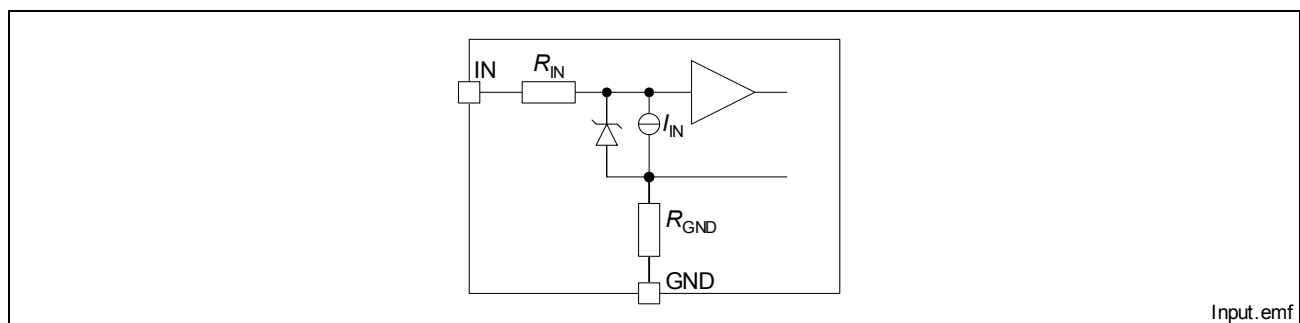
The on-state resistance  $R_{DS(ON)}$  depends on the supply voltage as well as the junction temperature  $T_j$ . **Figure 4** shows that dependencies for the typical on-state resistance. The behavior in reverse polarity mode is described in **Section 4.2.2**.



**Figure 4** Typical On-State Resistance

#### 4.1.2 Input Circuit

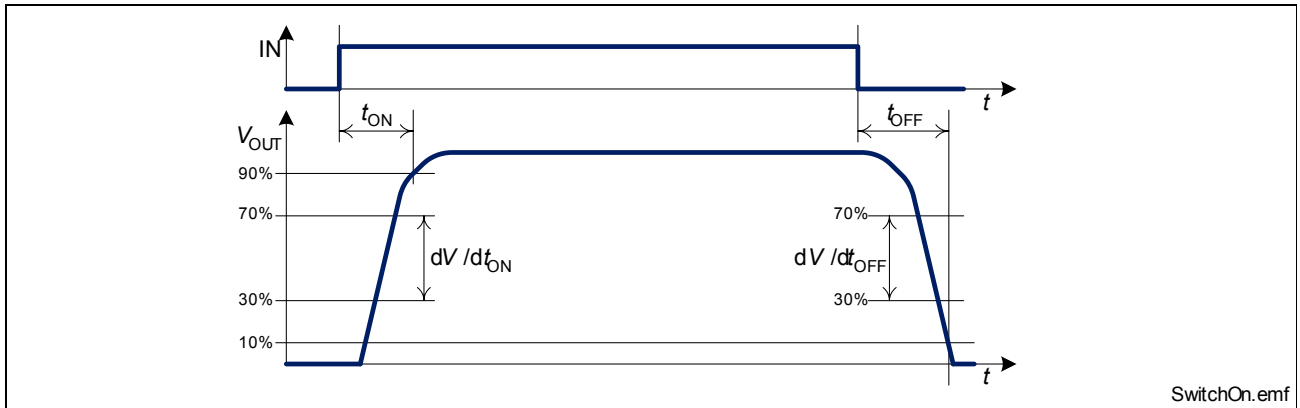
**Figure 5** shows the input circuit of the BTS5236-2GS. There is an integrated input resistor that makes external components obsolete. The current sink to ground ensures that the device switches off in case of open input pin. The zener diode protects the input circuit against ESD pulses.



**Figure 5** Input Circuit (IN1 and IN2)

## Block Description and Electrical Characteristics

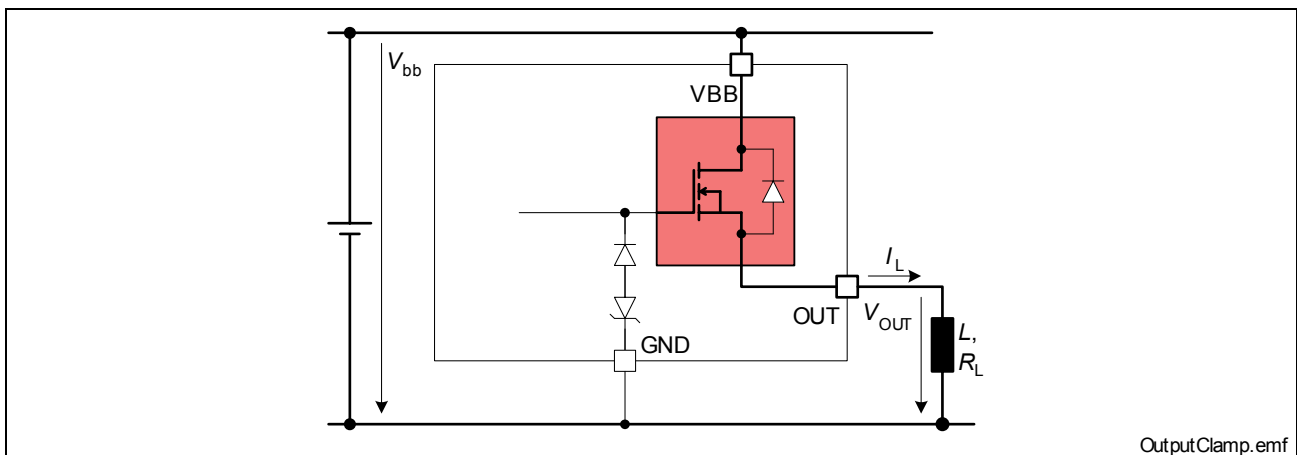
A high signal at the input pin causes the power DMOS to switch on with a dedicated slope, which is optimized in terms of EMC emission.



**Figure 6** Switching a Load (resistive)

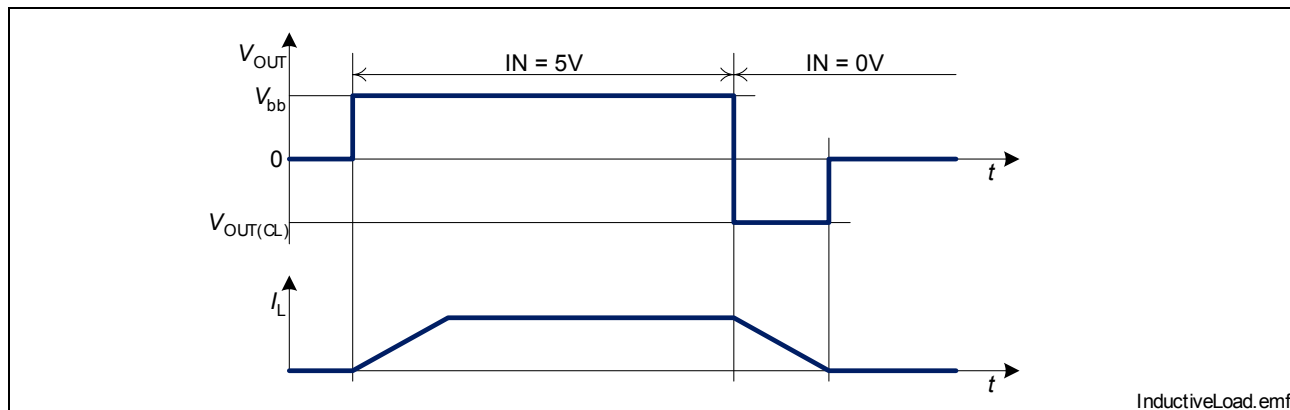
### 4.1.3 Inductive Output Clamp

When switching off inductive loads with high-side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current.



**Figure 7** Output Clamp (OUT1 and OUT2)

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps that negative output voltage at a certain level ( $V_{OUT(CL)}$ ). See [Figure 7](#) and [Figure 8](#) for details. Nevertheless, the maximum allowed load inductance is limited.



**Figure 8** Switching an Inductance

### Maximum Load Inductance

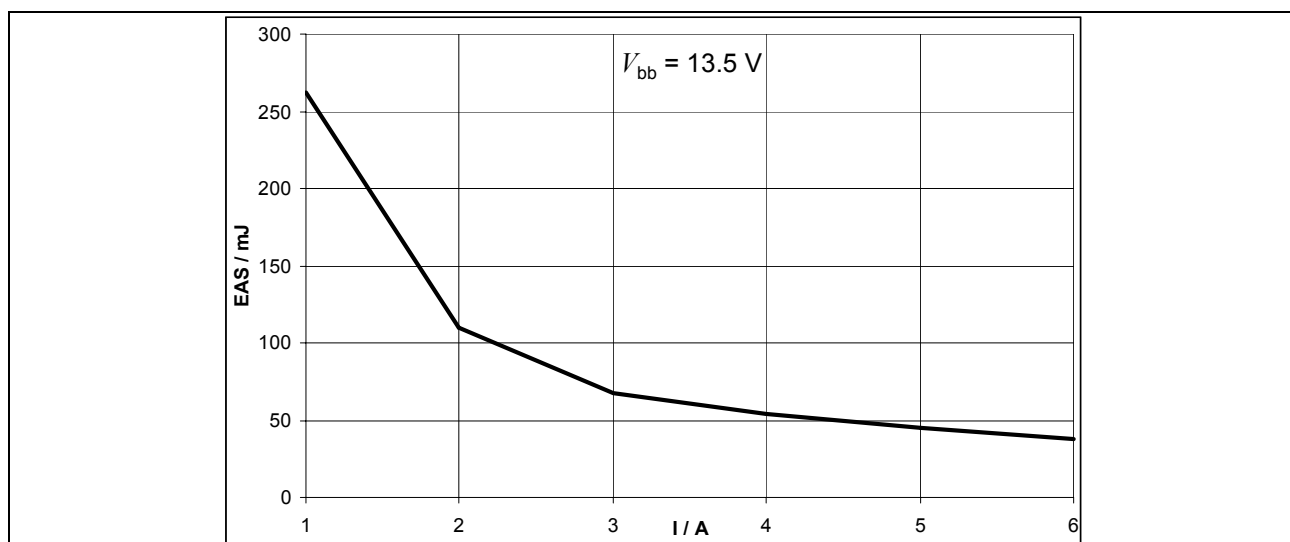
While demagnetization of inductive loads, energy has to be dissipated in the BTS5236-2GS. This energy can be calculated with following equation:

$$E = (V_{bb} - V_{OUT(CL)}) \cdot \left[ \frac{V_{OUT(CL)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{OUT(CL)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

This equation simplifies under the assumption of  $R_L = 0$ :

$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{bb}}{V_{OUT(CL)}} \right) \quad (2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See [Figure 9](#) for the maximum allowed energy dissipation.



**Figure 9** Maximum Energy Dissipation Single Pulse,  $T_{j,Start} = 150^\circ\text{C}$

**Block Description and Electrical Characteristics**
**4.1.4 Electrical Characteristics**

Unless otherwise specified:

$V_{bb} = 9\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ , typical values:  $V_{bb} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|------|-----------------|
|      |           |        | min.         | typ. | max. |      |                 |

**General**

|       |  |               |     |            |                  |               |   |
|-------|--|---------------|-----|------------|------------------|---------------|---|
| 4.1.1 | Operating voltage  | $V_{bb}$      | 4.5 |            | 28               | V             | $V_{IN} = 4.5\text{ V}$<br>$R_L = 12\text{ }\Omega$<br>$V_{DS} < 0.5\text{ V}$  |
| 4.1.2 | Operating current<br>one channel active<br>all channels active | $I_{GND}$     |     | 1.8<br>3.6 | 4.0<br>8.0       | mA            | $V_{IN} = 5\text{ V}$   |
| 4.1.3 | Standby current for<br>whole device with<br>load               | $I_{bb(OFF)}$ |     | 1.5        | 2.5<br>2.5<br>15 | $\mu\text{A}$ | $V_{IN} = 0\text{ V}$<br>$V_{SEN} = 0\text{ V}$<br>$T_j = 25\text{ °C}$<br>$T_j = 85\text{ °C}^{1)}$<br>$T_j = 150\text{ °C}$ |

**Output Characteristics**

|       |  |               |     |            |     |               |  |
|-------|--|---------------|-----|------------|-----|---------------|--|
| 4.1.4 | On-State resistance<br>per channel   | $R_{DS(ON)}$  |     | 40<br>80   | 100 | m $\Omega$    | $I_L = 2.5\text{ A}$<br>$T_j = 25\text{ °C}^{1)}$<br>$T_j = 150\text{ °C}$ |
| 4.1.5 | Output voltage drop<br>limitation at small load<br>currents                  | $V_{DS(NL)}$  |     | 40         |     | mV            | $I_L < 0.25\text{ A}$  |
| 4.1.6 | Nominal load current<br>per channel<br>one channel active<br>channels active | $I_{L(nom)}$  |     | 3.2<br>2.3 |     | A             | $T_a = 85\text{ °C}$<br>$T_j \leq 150\text{ °C}^{2) 3)}$                   |
| 4.1.7 | Output clamp   | $V_{OUT(CL)}$ | -24 | -20        | -17 | V             | $I_L = 40\text{ mA}$   |
| 4.1.8 | Output leakage<br>current per channel  | $I_{L(OFF)}$  |     | 0.1        | 6.0 | $\mu\text{A}$ | $V_{IN} = 0\text{ V}$  |
| 4.1.9 | Inverse current<br>capability  | $-I_{L(inv)}$ | -   | 3          | -   | A             | <sup>1)</sup>  |

**Block Description and Electrical Characteristics**

Unless otherwise specified:

$V_{bb} = 9\text{ V}$  to  $16\text{ V}$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ , typical values:  $V_{bb} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|------|-----------------|
|      |           |        | min.         | typ. | max. |      |                 |

**Thermal Resistance**

|        |  |            |  |          |    |     |       |
|--------|--|------------|--|----------|----|-----|-------|
| 4.1.10 | Junction to case   | $R_{thjc}$ |  |          | 45 | K/W | 1)    |
| 4.1.11 | Junction to ambient<br>one channel active<br>all channels active | $R_{thja}$ |  | 67<br>62 |    | K/W | 1) 2) |

**Input Characteristics**

|        |                 |             |      |     |     |               |                         |
|--------|-----------------|-------------|------|-----|-----|---------------|-------------------------|
| 4.1.12 | Input resistor  | $R_{IN}$    | 1.8  | 3.5 | 5.5 | k $\Omega$    |                         |
| 4.1.13 | L-input level   | $V_{IN(L)}$ | -0.3 | -   | 1.0 | V             |                         |
| 4.1.14 | H-input level   | $V_{IN(H)}$ | 2.5  | -   | 5.7 | V             |                         |
| 4.1.15 | L-input current | $I_{IN(L)}$ | 3    | 18  | 75  | $\mu\text{A}$ | $V_{IN} = 0.4\text{ V}$ |
| 4.1.16 | H-input current | $I_{IN(H)}$ | 10   | 38  | 75  | $\mu\text{A}$ | $V_{IN} = 5\text{ V}$   |

**Timings**

|        |                                   |                |     |      |     |                  |  |
|--------|-----------------------------------|----------------|-----|------|-----|------------------|--|
| 4.1.17 | Turn-on time to<br>90% $V_{OUT}$  | $t_{ON}$       | -   | 100  | 250 | $\mu\text{s}$    | $R_L = 12\text{ }\Omega$<br>$V_{bb} = 13.5\text{ V}$ |
| 4.1.18 | Turn-off time to<br>10% $V_{OUT}$ | $t_{OFF}$      | -   | 120  | 250 | $\mu\text{s}$    | $R_L = 12\text{ }\Omega$<br>$V_{bb} = 13.5\text{ V}$ |
| 4.1.19 | slew rate<br>30% to 70% $V_{OUT}$ | $dV/dt_{ON}$   | 0.1 | 0.25 | 0.5 | V/ $\mu\text{s}$ | $R_L = 12\text{ }\Omega$<br>$V_{bb} = 13.5\text{ V}$ |
| 4.1.20 | slew rate<br>70% to 30% $V_{OUT}$ | $-dV/dt_{OFF}$ | 0.1 | 0.25 | 0.5 | V/ $\mu\text{s}$ | $R_L = 12\text{ }\Omega$<br>$V_{bb} = 13.5\text{ V}$ |

1) Not subject to production test, specified by design.

2) Device mounted on PCB (50 mm  $\times$  50 mm  $\times$  1.5mm epoxy, FR4) with 6 cm<sup>2</sup> copper heatsinking area (one layer, 70  $\mu\text{m}$  thick) for  $V_{bb}$  connection. PCB is vertical without blown air.

3) Not subject to production test, parameters are calculated from  $R_{DS(ON)}$  and  $R_{th}$ .

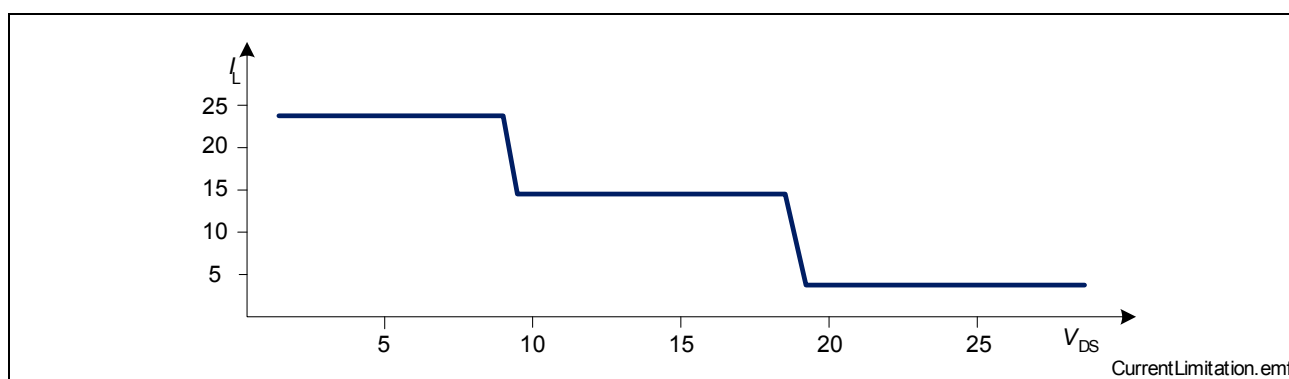
*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.*

## 4.2 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

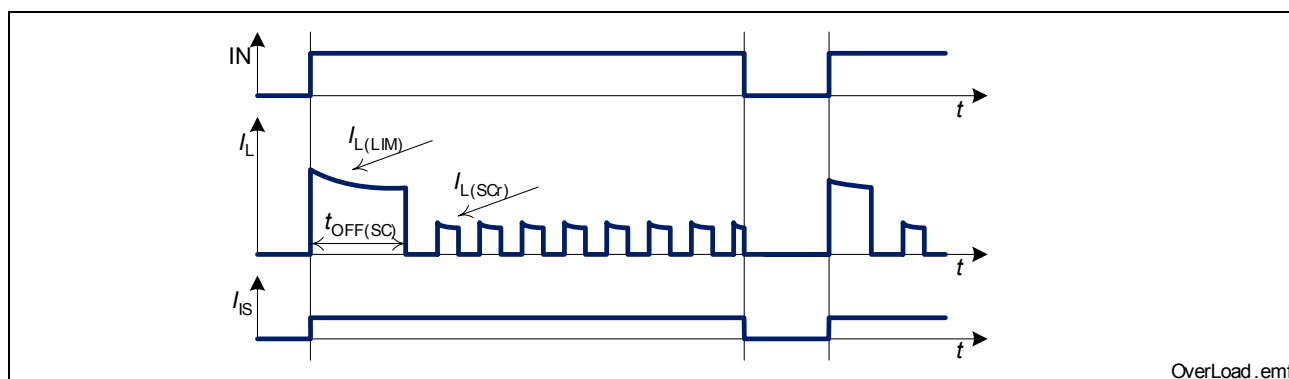
### 4.2.1 Over Load Protection

The load current  $I_{OUT}$  is limited by the device itself in case of over load or short circuit to ground. There are three steps of current limitation which are selected automatically depending on the voltage  $V_{DS}$  across the power DMOS. Please note that the voltage at the OUT pin is  $V_{bb} - V_{DS}$ . Please refer to following figure for details.



**Figure 10 Current Limitation (minimum values)**

Current limitation is realized by increasing the resistance of the device which leads to rapid temperature rise inside. A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. After cooling down with thermal hysteresis, the channel switches on again. Please refer to [Figure 11](#) for details.



**Figure 11 Shut Down by Over Temperature with Current Limitation**

In short circuit condition, the load current is initially limited to  $I_{L(LIM)}$ . After thermal restart, the current limitation level is reduced to  $I_{L(SCr)}$ . The current limitation level is reset to  $I_{L(LIM)}$  by switching off the device ( $V_{IN} = 0$  V).

### 4.2.2 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode causes power dissipation. Additional power is dissipated by the integrated ground resistor. Use following formula for estimation of total power dissipation  $P_{\text{diss(rev)}}$  in reverse polarity mode.

$$P_{\text{diss(rev)}} = \sum_{\text{all channels}} (V_{\text{DS(rev)}} \cdot I_L) + \frac{V_{\text{bb}}^2}{R_{\text{GND}}} \quad (3)$$

The reverse current through the intrinsic body diode has to be limited by the connected load. The current through sense pins IS1 and IS2 has to be limited (please refer to maximum ratings on [Page 8](#)). The current through the ground pin (GND) is limited internally by  $R_{\text{GND}}$ . The over-temperature protection is not active during reverse polarity.

### 4.2.3 Over Voltage Protection

In addition to the output clamp for inductive loads as described in [Section 4.1.3](#), there is a clamp mechanism for over voltage protection. Because of the integrated ground resistor, over voltage protection does not require external components.

As shown in [Figure 12](#), in case of supply voltages greater than  $V_{\text{bb(AZ)}}$ , the power transistor switches on and the voltage across logic part is clamped. As a result, the internal ground potential rises to  $V_{\text{bb}} - V_{\text{bb(AZ)}}$ . Due to the ESD zener diodes, the potential at pin IN1, IN2 and SEN rises almost to that potential, depending on the impedance of the connected circuitry.

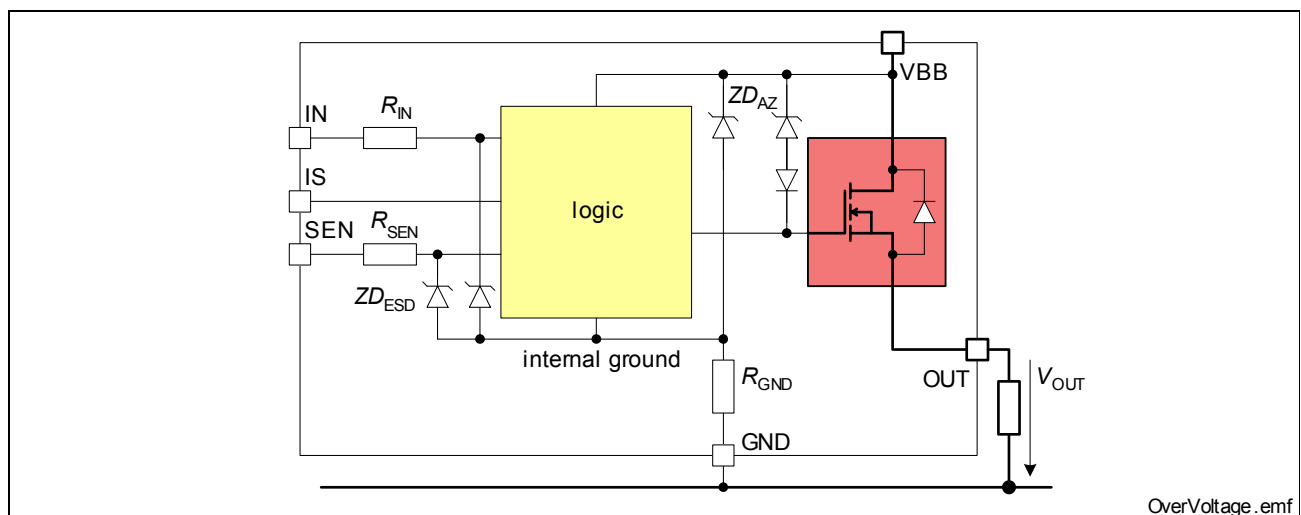


Figure 12 Over Voltage Protection

### 4.2.4 Loss of Ground Protection

In case of complete loss of the device ground connections, but connected load ground, the BTS5236-2GS securely changes to or stays in off state.



## 4.2.5 Electrical Characteristics

Unless otherwise specified:

$V_{bb} = 9\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ , typical values:  $V_{bb} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|------|-----------------|
|      |           |        | min.         | typ. | max. |      |                 |

### Over Load Protection

|       |   |               |     |                   |    |    |                                  |
|-------|---|---------------|-----|-------------------|----|----|----------------------------------|
| 4.2.1 | Load current limitation                     | $I_{L(LIM)}$  | 23  |                   | 42 | A  | $V_{DS} = 7\text{ V}$            |
|       |   |               | 14  |                   | 28 | A  | $V_{DS} = 14\text{ V}$           |
|       |   |               | 3   |                   | 14 | A  | $V_{DS} = 28\text{ V}^{1) 2)}$   |
| 4.2.2 | Repetitive short circuit current limitation | $I_{L(SCr)}$  | -   | 6                 | -  | A  | $T_j = T_{j(SC)}^{2)}$           |
| 4.2.3 | Initial short circuit shut down time        | $t_{OFF(SC)}$ | -   | 0.5               | -  | ms | $T_{jStart} = 25\text{ °C}^{2)}$ |
| 4.2.4 | Thermal shut down temperature               | $T_{j(SC)}$   | 150 | 170 <sup>2)</sup> | -  | °C |                                  |
| 4.2.5 | Thermal hysteresis                          | $\Delta T_j$  | -   | 7                 | -  | K  | <sup>2)</sup>                    |

### Reverse Battery

|       |   |                |   |    |     |    |   |
|-------|---|----------------|---|----|-----|----|---|
| 4.2.6 | Drain-Source diode voltage ( $V_{OUT} > V_{bb}$ ) | $-V_{DS(rev)}$ | - | -  | 900 | mV | $I_L = -3.5\text{ A}$<br>$V_{bb} = -13.5\text{ V}$<br>$T_j = 150\text{ °C}$ |
| 4.2.7 | Reverse current through GND pin                   | $-I_{GND}$     | - | 65 | -   | mA | $V_{bb} = -13.5\text{ V}^{2)}$  |

### Ground Circuit

|       |                                 |           |     |     |     |   |  |
|-------|---------------------------------|-----------|-----|-----|-----|---|--|
| 4.2.8 | Integrated Resistor in GND line | $R_{GND}$ | 115 | 220 | 350 | Ω |  |
|-------|---------------------------------|-----------|-----|-----|-----|---|--|

### Over Voltage

|       |                         |              |    |    |    |   |                        |
|-------|-------------------------|--------------|----|----|----|---|------------------------|
| 4.2.9 | Over voltage protection | $V_{bb(AZ)}$ | 41 | 47 | 53 | V | $I_{bb} = 2\text{ mA}$ |
|-------|-------------------------|--------------|----|----|----|---|------------------------|

### Loss of GND

|        |   |              |   |   |   |    |  |
|--------|---|--------------|---|---|---|----|--|
| 4.2.10 | Output leakage current while GND disconnected | $I_{L(GND)}$ | - | - | 1 | mA | $I_{IN} = 0, I_{SEN} = 0,$<br>$I_{IS} = 0,$<br>$I_{GND} = 0^{2) 3)}$ |
|--------|---|--------------|---|---|---|----|--|

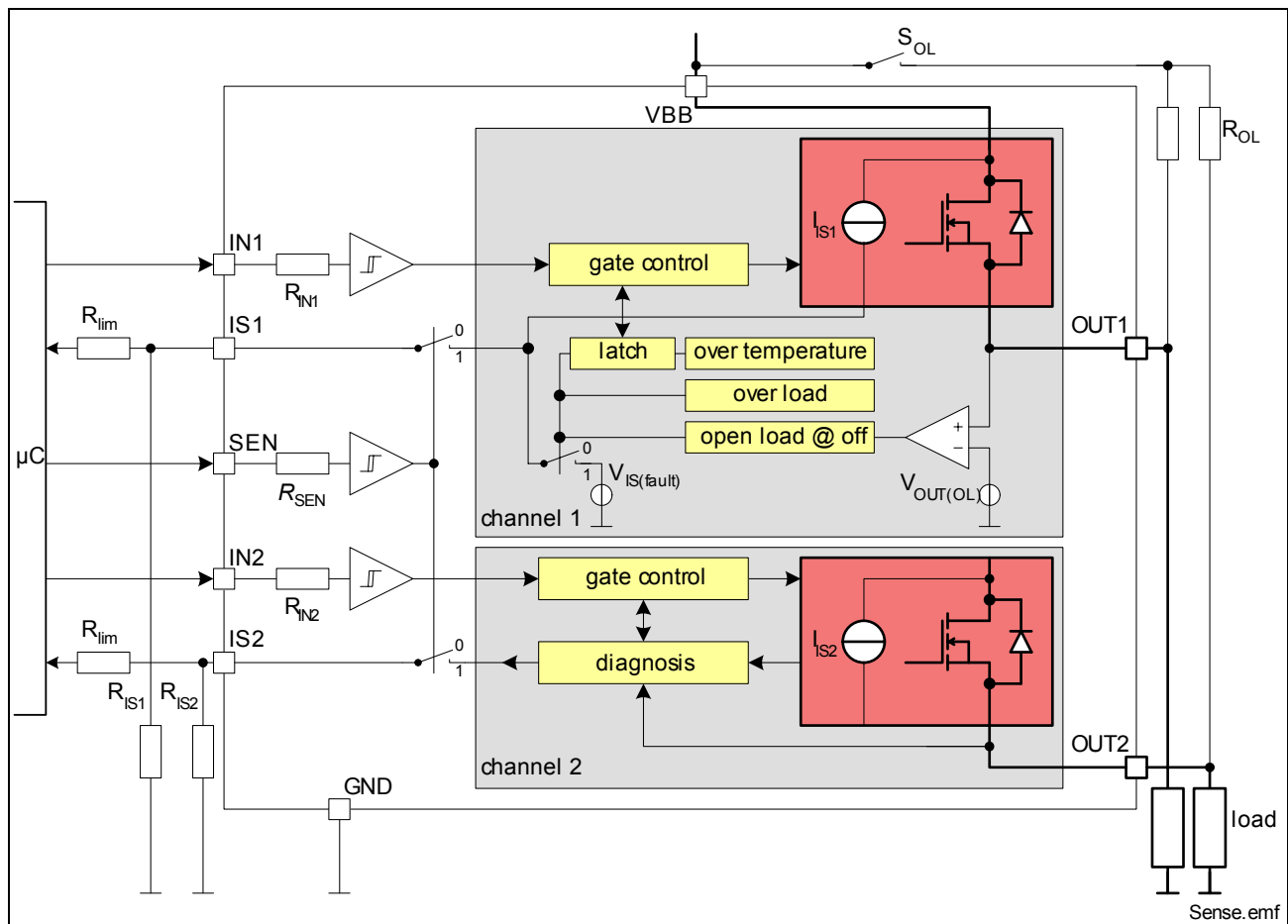
1) Please note that an external forced  $V_{DS}$  must not exceed  $V_{bb} + |V_{OUT(CL)}|$

2) Not subject to production test, specified by design

3) No connection at these pins

### 4.3 Diagnosis

For diagnosis purpose, the BTS5236-2GS provides an Enhanced IntelliSense signal at pins IS1 and IS2. This means in detail, the current sense signal  $I_{IS}$ , a proportional signal to the load current (ratio  $k_{I_{IS}} = I_L / I_{IS}$ ), is provided as long as no failure mode (see [Table 1](#)) occurs. In case of a failure mode, the voltage  $V_{IS(fault)}$  is fed to the diagnosis pin.



**Figure 13 Block Diagram: Diagnosis**

**Table 1 Truth Table<sup>1)</sup>**

| Operation Mode            | Input Level | Output Level                       | Diagnostic Output             |         |
|---------------------------|-------------|------------------------------------|-------------------------------|---------|
|                           |             |                                    | SEN = H                       | SEN = L |
| Normal Operation (OFF)    | L           | GND                                | Z                             | Z       |
| Short Circuit to GND      |             | GND                                | Z                             | Z       |
| Over Temperature          |             | Z                                  | Z                             | Z       |
| Short Circuit to $V_{bb}$ |             | $V_{bb}$                           | $V_{IS} = V_{IS(fault)}$      | Z       |
| Open Load                 |             | $< V_{OUT(OL)}$<br>$> V_{OUT(OL)}$ | Z<br>$V_{IS} = V_{IS(fault)}$ | Z<br>Z  |

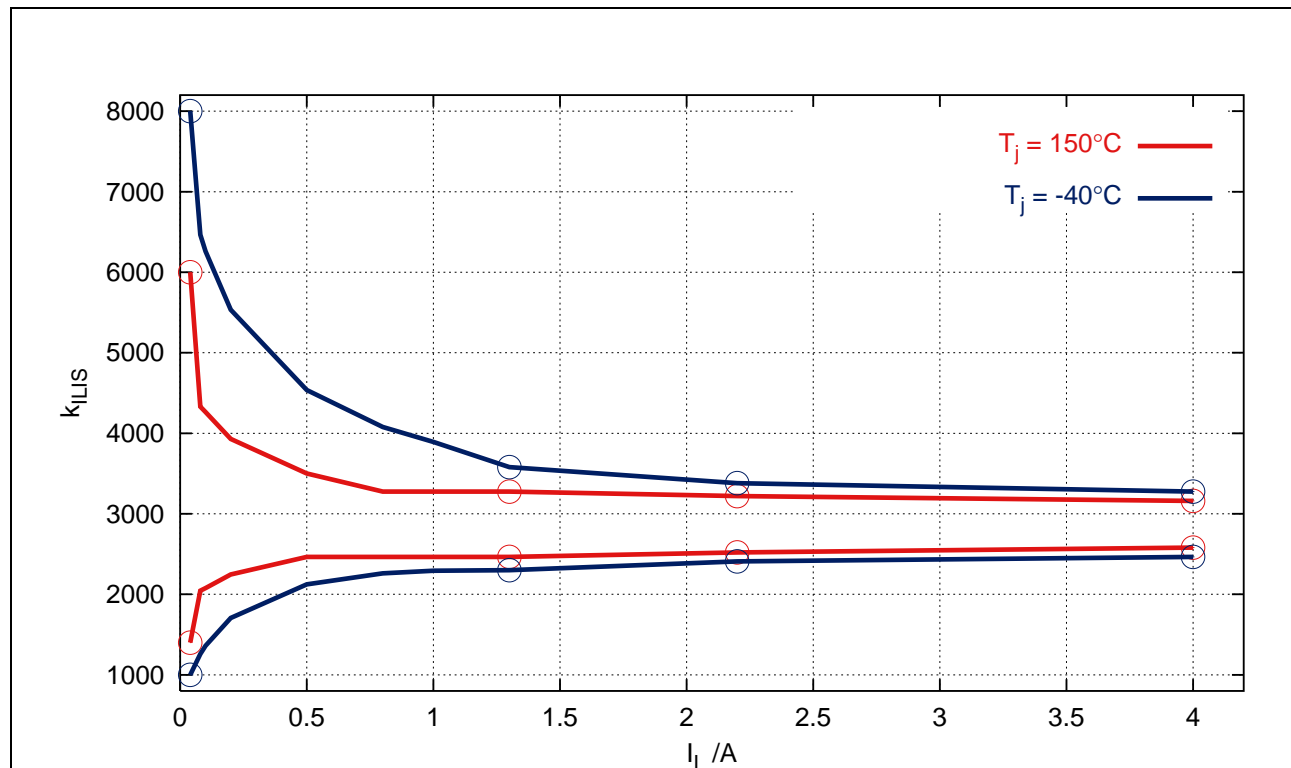
**Table 1 Truth Table<sup>1)</sup> (cont'd)**

| Operation Mode            | Input Level | Output Level  | Diagnostic Output         |         |
|---------------------------|-------------|---------------|---------------------------|---------|
|                           |             |               | SEN = H                   | SEN = L |
| Normal Operation (ON)     | H           | $\sim V_{bb}$ | $I_{IS} = I_L / k_{ILIS}$ | Z       |
| Current Limitation        |             | $< V_{bb}$    | $V_{IS} = V_{IS(fault)}$  | Z       |
| Short Circuit to GND      |             | $\sim GND$    | $V_{IS} = V_{IS(fault)}$  | Z       |
| Over Temperature          |             | Z             | $V_{IS} = V_{IS(fault)}$  | Z       |
| Short Circuit to $V_{bb}$ |             | $V_{bb}$      | $I_{IS} < I_L / k_{ILIS}$ | Z       |
| Open Load                 |             | $V_{bb}$      | Z                         | Z       |

1) L = Low Level, H = High Level, Z = high impedance, potential depends on leakage currents and external circuit

### 4.3.1 ON-State Diagnosis

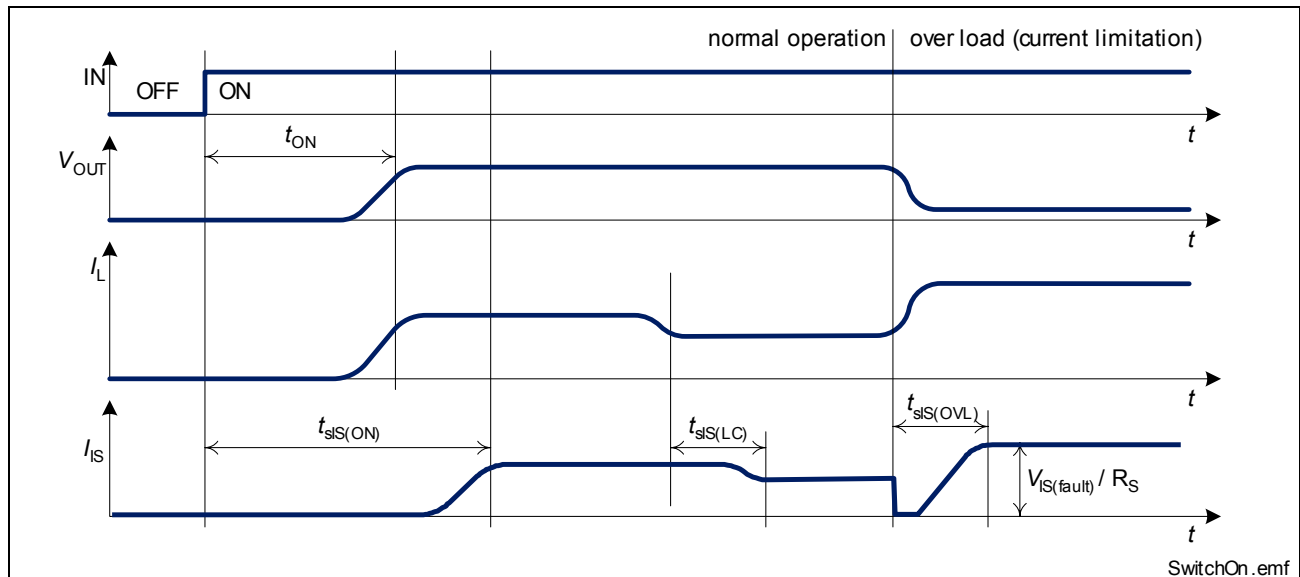
The standard diagnosis signal is a current sense signal proportional to the load current. The accuracy of the ratio ( $k_{ILIS} = I_L / I_{IS}$ ) depends on the temperature. Please refer to following **Figure 14** for details. Usually a resistor  $R_{IS}$  is connected to the current sense pin. It is recommended to use sense resistors  $R_{IS} > 500 \Omega$ . A typical value is 4.7 k $\Omega$ .



**Figure 14 Current sense ratio  $k_{ILIS}$ <sup>1)</sup>**

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Datasheet in **Section 4.3.4** (Position **4.3.6**).

Details about timings between the diagnosis signal  $I_{IS}$  and the output voltage  $V_{OUT}$  and load current  $I_L$  in ON-state can be found in **Figure 15**.

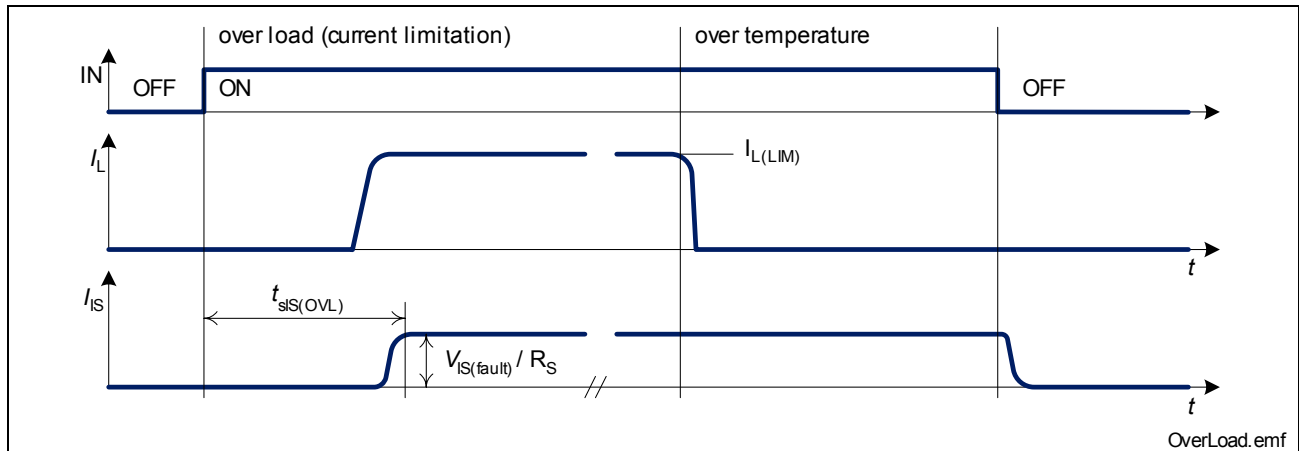


**Figure 15 Timing of Diagnosis Signal in ON-state**

In case of over-load as well as over-temperature, the voltage  $V_{IS(fault)}$  is fed to the diagnosis pins as long as the according input pin is high. This means, even if the overload disappears after the first thermal shutdown or when the device keeps switching on and off in over-load condition (thermal toggling), the diagnosis signal ( $V_{IS(fault)}$ ) is constantly available. Please refer to **Figure 16** for details. Please note, that if the overload disappears before the first thermal shutdown, the diagnosis signal ( $V_{IS(fault)}$ ) may remain for approximately 300  $\mu$ s longer than the duration of the overload.

As a result open load and over load including over temperature can be differentiated in ON-state.

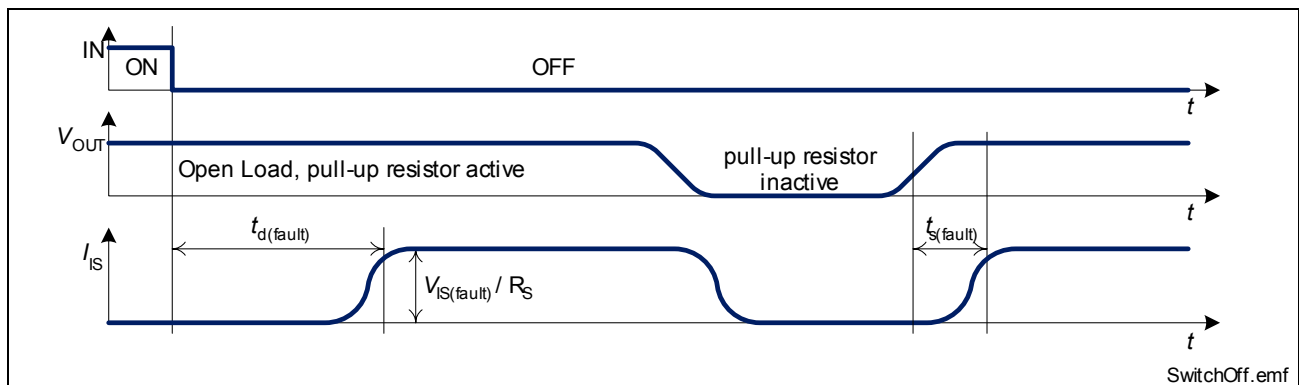
Consideration must be taken in the selection of the sense resistor in order to distinguish nominal currents from the overload/short circuit fault state. A potential of 5 V at the sense pin can be achieved with a big sense resistor even with currents being much smaller than the current limitation.



**Figure 16** Timing of Diagnosis Signal in Over Load Condition

## 4.3.2 OFF-State Diagnosis

Details about timings between the diagnosis signal  $I_{IS}$  and the output voltage  $V_{OUT}$  and load current  $I_L$  in OFF-state can be found in [Figure 17](#). For open load diagnosis in OFF-state an external output pull-up resistor ( $R_{OL}$ ) is necessary.



**Figure 17** Timing of Diagnosis Signal in OFF-state

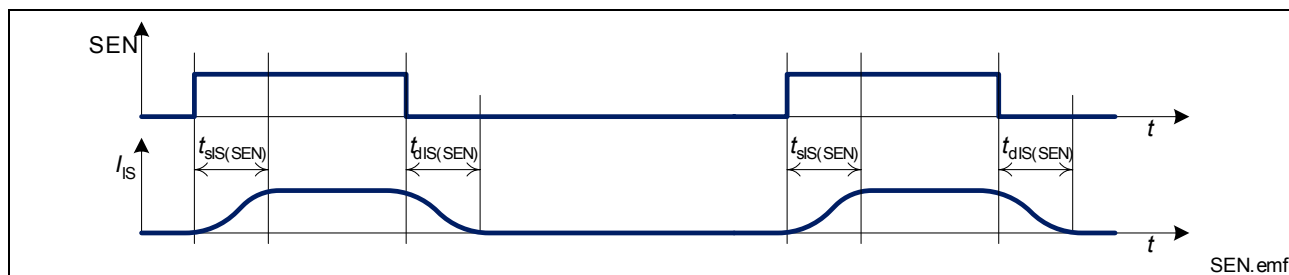
For calculation of the pull-up resistor, just the external leakage current  $I_{leakage}$  and the open load threshold voltage  $V_{OUT(OL)}$  has to be taken into account.

$$R_{OL} = \frac{V_{bb(min)} - V_{OUT(OL,max)}}{I_{leakage}} \quad (4)$$

$I_{leakage}$  defines the leakage current in the complete system e.g. caused by humidity. There is no internal leakage current from out to ground at BTS5236-2GS.  $V_{bb(min)}$  is the minimum supply voltage at which the open load diagnosis in off state must be ensured. To reduce the stand-by current of the system, an open load resistor switch ( $S_{OL}$ ) is recommended.

## 4.3.3 Sense Enable Function

The diagnosis signals have to be switched on by a high signal at sense enable pin (SEN). See [Figure 18](#) for details on the timing between SEN pin and diagnosis signal  $I_{IS}$ . Please note that the diagnosis is disabled, when no signal is provided at pin SEN.



**Figure 18** Timing of Sense Enable Signal

The SEN pin circuit is designed equally to the input pin. Please refer to [Figure 5](#) for details. The resistors  $R_{lim}$  are recommended to limit the current through the sense pins IS1 and IS2 in case of reverse polarity and over voltage. Please refer to maximum ratings on [Page 8](#).

The stand-by current of the BTS5236-2GS is minimized, when both input pins (IN1 and IN2) and the sense enable pin (SEN) are on low level.

### 4.3.4 Electrical Characteristics

Unless otherwise specified:

$V_{bb} = 9\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $V_{SEN} = 5\text{ V}$ ,

typical values:  $V_{bb} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|------|-----------------|
|      |           |        | min.         | typ. | max. |      |                 |

#### General Definition

|       |   |                 |   |   |   |    |   |
|-------|---|-----------------|---|---|---|----|---|
| 4.3.1 | Diagnostics signal in failure mode                    | $V_{IS(fault)}$ | 5 | - | 9 | V  | $V_{IN} = 0\text{ V}$<br>$V_{OUT} = V_{bb}$<br>$I_{IS} = 1\text{ mA}$ |
| 4.3.2 | Diagnostics signal current limitation in failure mode | $I_{IS(LIM)}$   | 3 | - | - | mA | $V_{IN} = 0\text{ V}$<br>$V_{OUT} = V_{bb}$                           |

#### Open Load in OFF-State

|       |   |                |     |     |     |    |  |
|-------|---|----------------|-----|-----|-----|----|--|
| 4.3.3 | Open load detection threshold voltage           | $V_{OUT(OL)}$  | 1.6 | 2.8 | 4.4 | V  |  |
| 4.3.4 | Sense signal invalid after negative input slope | $t_{d(fault)}$ | -   | -   | 1.2 | ms | $V_{IN} = 5\text{ V to }0\text{ V}$<br>$V_{OUT} = V_{bb}$                                  |
| 4.3.5 | Fault signal settling time                      | $t_{s(fault)}$ | -   | -   | 200 | μs | $V_{IN} = 0\text{ V}$<br>$V_{OUT} = 0\text{ V to }> V_{OUT(OL)}$<br>$I_{IS} = 1\text{ mA}$ |

#### Load Current Sense ON-State

|       |                                      |               |      |      |      |    |  |
|-------|--------------------------------------|---------------|------|------|------|----|--|
| 4.3.6 | Current sense ratio                  | $k_{ILIS}$    |      |      |      |    | $V_{IN} = 5\text{ V}$<br>$T_j = -40\text{ °C}$   |
|       | $I_L = 40\text{ mA}$                 |               | 1000 | 4035 | 8000 |    |  |
|       | $I_L = 1.3\text{ A}$                 |               | 2300 | 3050 | 3580 |    |  |
|       | $I_L = 2.2\text{ A}$                 |               | 2410 | 2920 | 3380 |    |  |
|       | $I_L = 4.0\text{ A}$                 |               | 2465 | 2850 | 3275 |    |  |
|       | $I_L = 40\text{ mA}$                 |               | 1400 | 3410 | 6000 |    | $T_j = 150\text{ °C}$                            |
|       | $I_L = 1.3\text{ A}$                 |               | 2465 | 2920 | 3275 |    |  |
|       | $I_L = 2.2\text{ A}$                 |               | 2520 | 2875 | 3220 |    |  |
|       | $I_L = 4.0\text{ A}$                 |               | 2580 | 2870 | 3160 |    |  |
| 4.3.7 | Current sense voltage limitation     | $V_{IS(LIM)}$ | 5.0  | 6.2  | 7.5  | V  | $I_{IS} = 0.5\text{ mA}$<br>$I_L = 3.5\text{ A}$ |
| 4.3.8 | Current sense leakage/offset current | $I_{IS(LH)}$  | -    | -    | 3.5  | μA | $V_{IN} = 5\text{ V}$<br>$I_L = 0\text{ A}$      |

Unless otherwise specified:

$V_{bb} = 9\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $V_{SEN} = 5\text{ V}$ ,

typical values:  $V_{bb} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos.   | Parameter  | Symbol        | Limit Values |      |      | Unit          | Test Conditions   |
|--------|--|---------------|--------------|------|------|---------------|---|
|        |  |               | min.         | typ. | max. |               |   |
| 4.3.9  | Current sense leakage, while diagnosis disabled  | $I_{IS(dis)}$ | -            | -    | 1    | $\mu\text{A}$ | $V_{SEN} = 0\text{ V}$<br>$I_L = 3.5\text{ A}$                      |
| 4.3.10 | Current sense settling time to $I_{IS}$ static $\pm 10\%$ after positive input slope   | $t_{sIS(ON)}$ | -            | -    | 350  | $\mu\text{s}$ | $V_{IN} = 0\text{ V to }5\text{ V}$<br>$I_L = 3.5\text{ A}$<br>1)   |
| 4.3.11 | Current sense settling time to $I_{IS}$ static $\pm 10\%$ after change of load current | $t_{sIS(LC)}$ | -            | -    | 50   | $\mu\text{s}$ | $V_{IN} = 5\text{ V}$<br>$I_L = 3.5\text{ A to }2.2\text{ A}$<br>1) |

#### Over Load in ON-State

|        |  |                |   |   |              |               |   |
|--------|--|----------------|---|---|--------------|---------------|---|
| 4.3.12 | Over load detection current                      | $I_{L(OVL)}$   | 8 | - | $I_{L(LIM)}$ | A             | $V_{IN} = 5\text{ V}$<br>$V_{IS} = V_{IS(fault)}$<br>1)       |
| 4.3.13 | Sense signal settling time in overload condition | $t_{sIS(OVL)}$ | - | - | 200          | $\mu\text{s}$ | $V_{OUT} = 2\text{ V}$<br>$V_{IN} = 0\text{ V to }5\text{ V}$ |

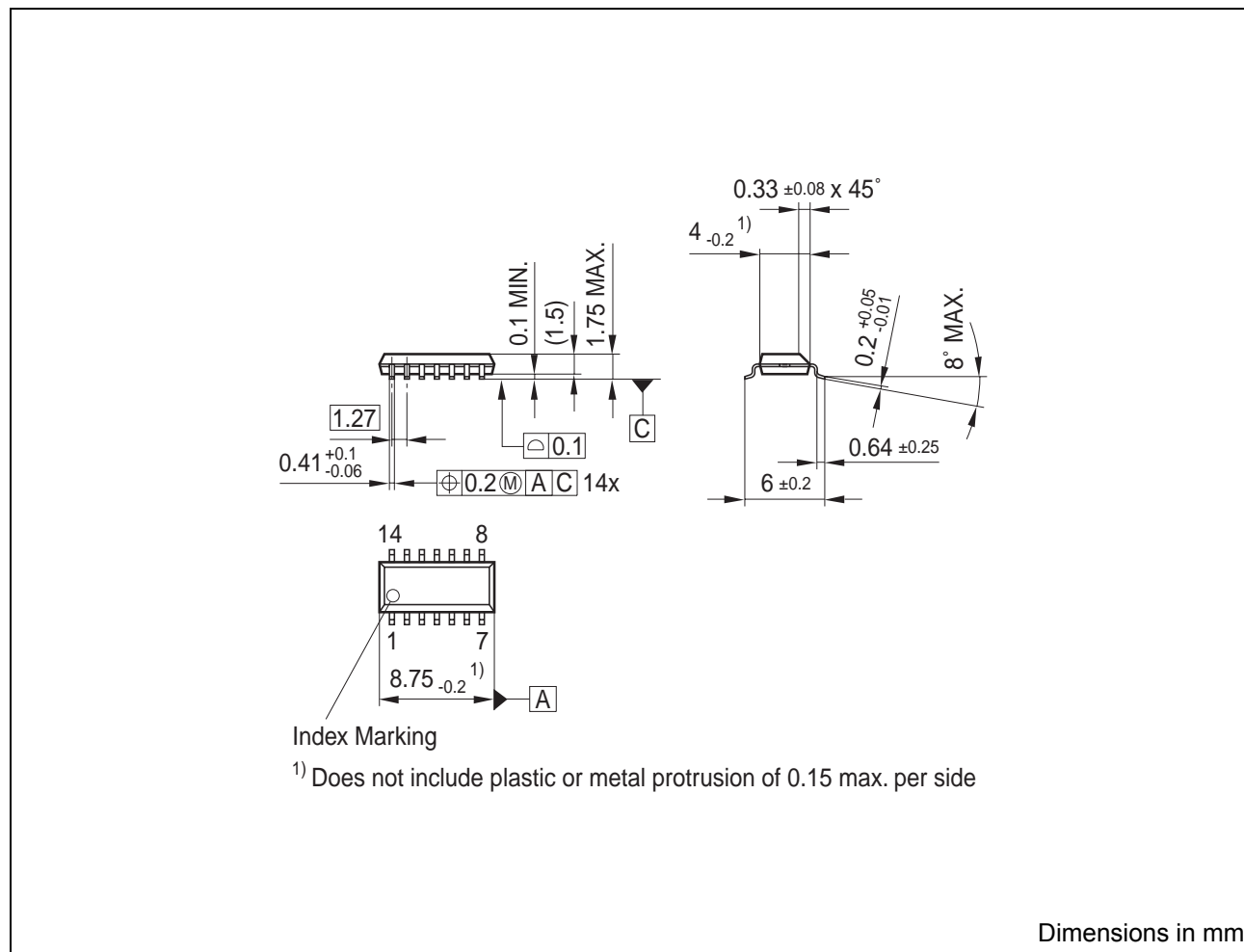
#### Sense Enable

|        |                                 |                |      |     |     |                  |   |
|--------|---------------------------------|----------------|------|-----|-----|------------------|---|
| 4.3.14 | Input resistance                | $R_{SEN}$      | 1.8  | 3.5 | 5.5 | $\text{k}\Omega$ |   |
| 4.3.15 | L-input level                   | $V_{SEN(L)}$   | -0.3 | -   | 1.0 | V                |   |
| 4.3.16 | H-input level                   | $V_{SEN(H)}$   | 2.5  | -   | 5.7 | V                |   |
| 4.3.17 | L-input current                 | $I_{SEN(L)}$   | 3    | 18  | 75  | $\mu\text{A}$    | $V_{SEN} = 0.4\text{ V}$  |
| 4.3.18 | H-input current                 | $I_{SEN(H)}$   | 10   | 38  | 75  | $\mu\text{A}$    | $V_{SEN} = 5\text{ V}$  |
| 4.3.19 | Current sense settling time     | $t_{sIS(SEN)}$ | -    | 3   | 25  | $\mu\text{s}$    | $V_{SEN} = 0\text{ V to }5\text{ V}$<br>$V_{IN} = 0\text{ V}$<br>$V_{OUT} > V_{OUT(OL)}$    |
| 4.3.20 | Current sense deactivation time | $t_{dIS(SEN)}$ | -    | -   | 25  | $\mu\text{s}$    | $V_{SEN} = 5\text{ V to }0\text{ V}$<br>$I_L = 3.5\text{ A}$<br>$R_S = 5\text{ k}\Omega$ 1) |

1) Not subject to production test, specified by design



## 5 Package Outlines BTS5236-2GS



**Figure 19** PG-DSO-14-32 (Plastic Dual Small Outline Package)

## Green Product

To meet the world-wide requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green Products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

## 6 Revision History

| Version | Date     | Changes  |
|---------|----------|--|
| V1.1    | 07-09-07 | Creation of the Data sheet <ul style="list-style-type: none"><li>• insertion of the EAS curves</li><li>• insertion of the Ron vs Temperature and Battery voltage.</li><li>• Adding the test voltage for EAS (3.1.6)</li><li>• Change in the parameter 4.3.11 in the test condition</li></ul> |
|         |          |  |
|         |          |  |
|         |          |  |

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