

900V Cascode GaN FET in TO-247 (source tab)

Description

The TP90H050WS 900V, 50mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

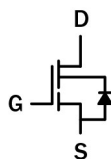
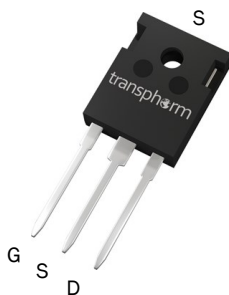
Related Literature

- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0010](#): Paralleling GaN FETs

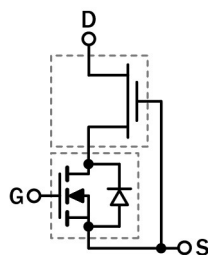
Ordering Information

Part Number	Package	Package Configuration
TP90H050WS	3 lead TO-247	Source

TP90H050WS
TO-247
(top view)



Cascode Schematic Symbol



Cascode Device Structure

Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Intrinsic lifetime tests
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications

V_{DS} (V)	900
$V_{(TR)DSS}$ (V) max	1000
$R_{DS(on)eff}$ (mΩ) max*	63
Q_{RR} (nC) typ	156
Q_G (nC) typ	15

* Reflects both static and dynamic on-resistance; see Figures 18 and 19

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Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise stated. All recommended current levels (I_{DM}) are based on adequate heat sinking, ensuring $T_J=150^{\circ}\text{C}$)

Symbol	Parameter	Limit Value	Unit
I_D	Continuous drain current @ $T_C=25^{\circ}\text{C}$ ^a	34	A
	Continuous drain current @ $T_C=100^{\circ}\text{C}$ ^a	22	A
I_{DM}	Pulsed drain current (pulse width: 10 μs)	150	A
di/dt_{RDMC}	Reverse diode di/dt , repetitive ^b	1600	A/ μs
I_{RDMC1}	Reverse diode switching current, repetitive (dc) ^c	24	A
I_{RDMC2}	Reverse diode switching current, repetitive (ac) ^c	28	A
di/dt_{RDMT}	Reverse diode di/dt , transient ^d	3000	A/ μs
I_{RDMT}	Reverse diode switching current, transient	36	A
$V_{(TR)DSS}$	Transient drain to source voltage ^e	1000	V
V_{GSS}	Gate to source voltage	± 20	V
P_D	Maximum power dissipation @ $T_C=25^{\circ}\text{C}$	119	W
T_C	Operating temperature	Case	-55 to $+150$
T_J		Junction	-55 to $+150$
T_S	Storage temperature	-55 to $+150$	$^{\circ}\text{C}$
T_{SOLD}	Soldering peak temperature ^f	260	$^{\circ}\text{C}$
-	Mounting Torque	80	N cm

Notes:

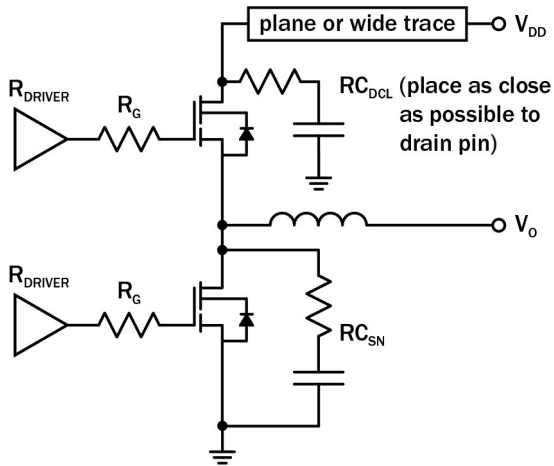
- a. For increased stability at high current operation, see Circuit Implementation on page 3
- b. Continuous switching operation
- c. Definitions: dc = dc to dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
- d. ≤ 300 pulses in 1 second
- e. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$
- f. For 10 sec., 1.6mm from the case

Thermal Resistance

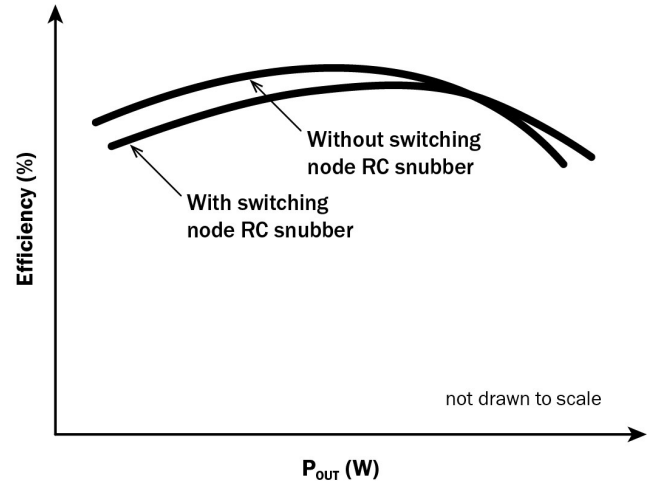
Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1.05	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient	40	$^{\circ}\text{C/W}$

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Circuit Implementation



Simplified Half-bridge Schematic



Efficiency vs Output Power

Recommended gate drive: (0V, 12-14V) with $R_{G(tot)} = 22-30\Omega$, where $R_{G(tot)} = R_G + R_{DRIVER}$

Required DC Link RC Snubber (RC_{DCL}) ^a	Recommended Switching Node RC Snubber (RC_{SN}) ^b
$[10nF + 8\Omega] \times 2$	$100pF + 10\Omega$

Notes:

- RC_{DCL} should be placed as close as possible to the drain pin
- A switching node RC snubber (C, R) is recommended for high switching currents (>70% of I_{RDMC1} or I_{RDMC2})

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Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{(BL)DSS}	Maximum drain-source voltage	900	—	—	V	V _{GS} =0V
V _{GS(th)}	Gate threshold voltage	3.4	3.9	4.4	V	V _{DS} =V _{GS} , I _D =0.7mA
ΔV _{GS(th)} /T _J	Gate threshold voltage temperature coefficient	—	-6.5	—	mV/°C	
R _{DS(on)eff}	Drain-source on-resistance ^a	—	50	63	mΩ	V _{GS} =10V, I _D =22A
		—	105	—		V _{GS} =10V, I _D =22A, T _J =150 °C
I _{DSS}	Drain-to-source leakage current	—	4	40	μA	V _{DS} =900V, V _{GS} =0V
		—	15	—		V _{DS} =900V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V _{GS} =20V
	Gate-to-source reverse leakage current	—	—	-100		V _{GS} =-20V
C _{ISS}	Input capacitance	—	1000	—	pF	V _{GS} =0V, V _{DS} =600V, f=1MHz
C _{OSS}	Output capacitance	—	115	—		
C _{RSS}	Reverse transfer capacitance	—	3.5	—		
C _{O(er)}	Output capacitance, energy related ^b	—	153	—	pF	V _{GS} =0V, V _{DS} =0V to 600V
C _{O(tr)}	Output capacitance, time related ^c	—	260	—		
Q _G	Total gate charge	—	15	—	nC	V _{DS} =600V, V _{GS} =10V, I _D =22A
Q _{GS}	Gate-source charge	—	5	—		
Q _{GD}	Gate-drain charge	—	4.7	—		
Q _{OSS}	Output charge	—	155	—	nC	V _{GS} =0V, V _{DS} =0V to 600V
t _{D(on)}	Turn-on delay	—	48	—	ns	V _{DS} =600V, V _{GS} =10V, I _D =22A R _G =25Ω, 4A driver
t _R	Rise time	—	12	—		
t _{D(off)}	Turn-off delay	—	70	—		
t _F	Fall time	—	12	—		
Reverse Device Characteristics						
I _S	Reverse current	—	—	22	A	V _{GS} =0V, T _C =100 °C, ≤25% duty cycle
V _{SD}	Reverse voltage ^a	—	2.2	2.6	V	V _{GS} =0V, I _S =22A
		—	1.6	1.9		V _{GS} =0V, I _S =11A
t _{RR}	Reverse recovery time	—	53	—	ns	I _S =22A, V _{DD} =600V, di/dt=1000A/μs
Q _{RR}	Reverse recovery charge	—	156	—	nC	

Notes:

- Reflects both static and dynamic on-resistance; dynamic on-resistance test setup and waveform; see Figures 14 and 15 for conditions
- Equivalent capacitance to give same stored energy from 0V to 600V
- Equivalent capacitance to give same charging time from 0V to 600V

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Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

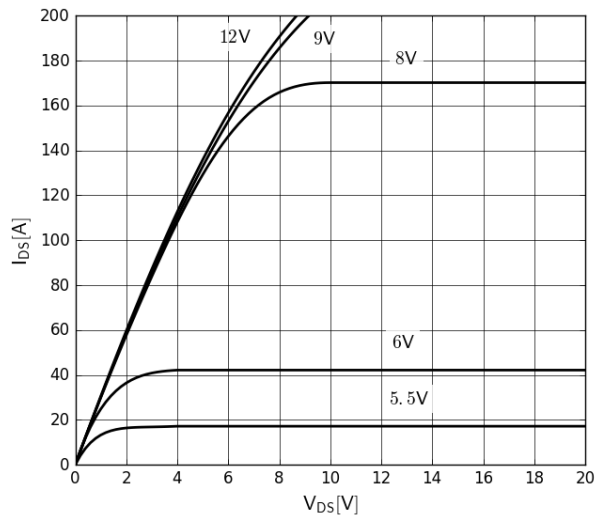


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$
Parameter: V_{GS}

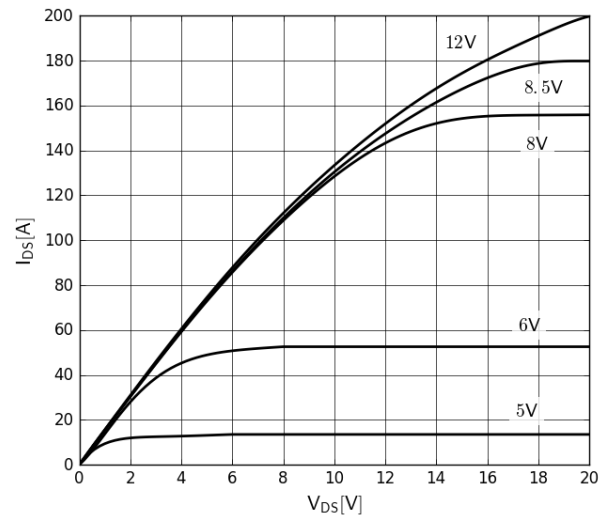


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$
Parameter: V_{GS}

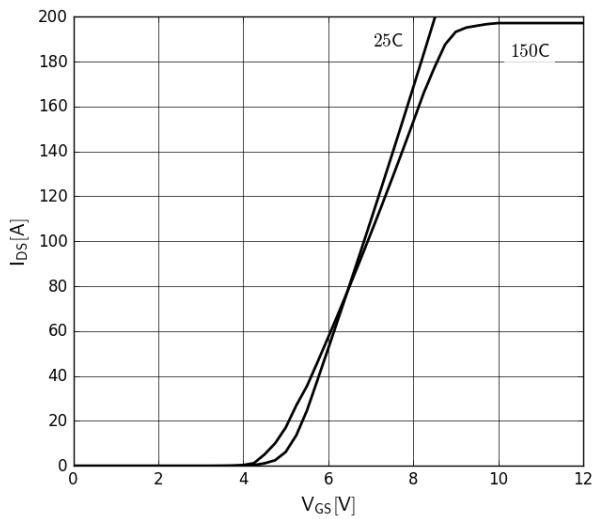


Figure 3. Typical Transfer Characteristics
 $V_{DS}=20\text{V}$, parameter: T_J

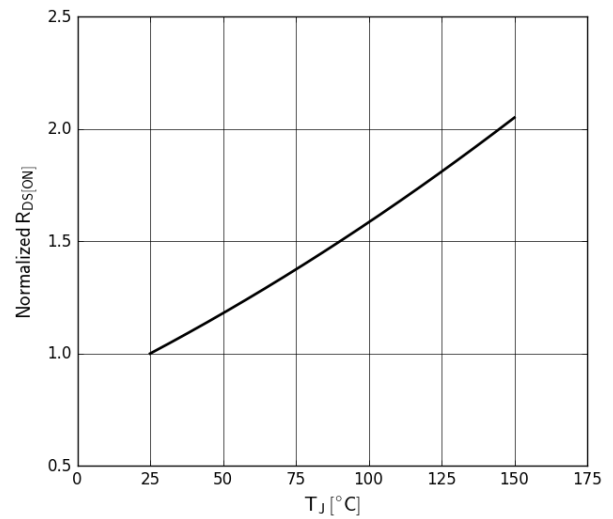


Figure 4. Normalized On-resistance
 $I_D=22\text{A}$, $V_{GS}=8\text{V}$

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Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

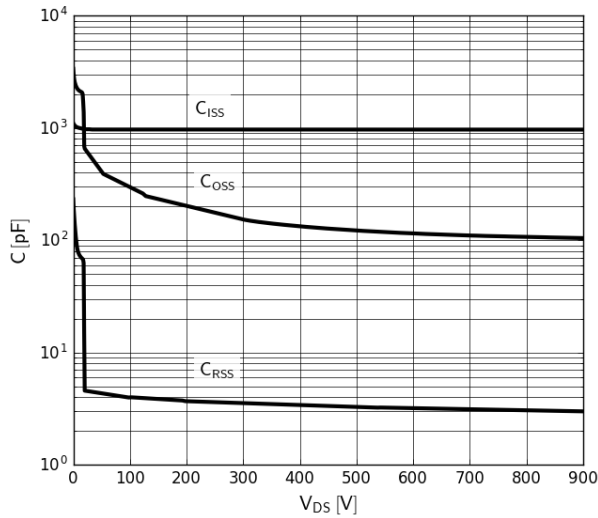


Figure 5. Typical Capacitance
 $V_{GS}=0V$, $f=1\text{MHz}$

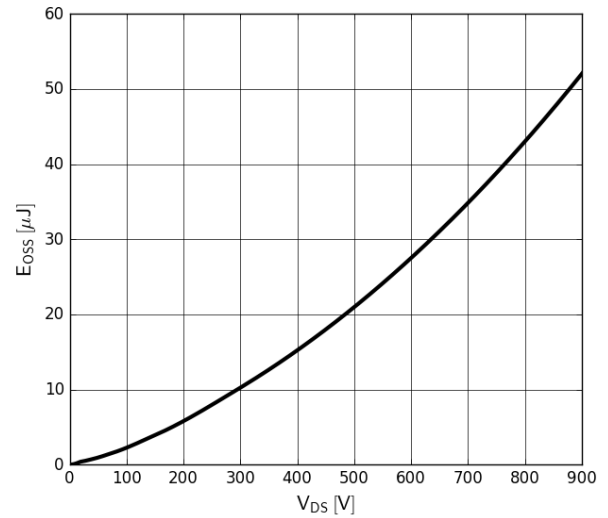


Figure 6. Typical C_{oss} Stored Energy

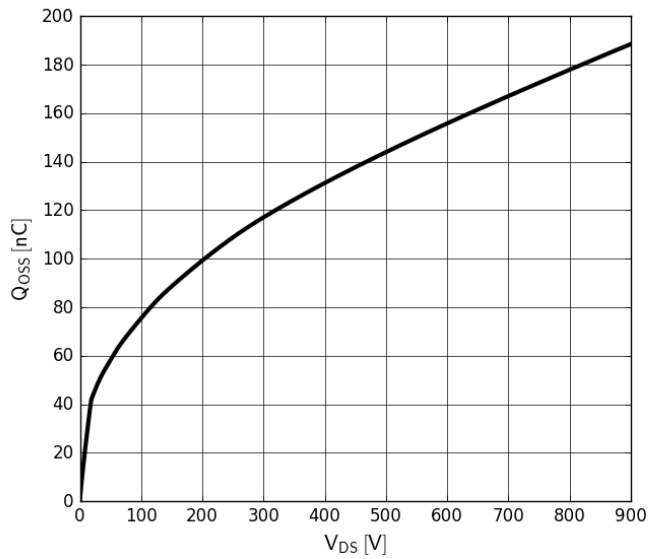


Figure 7. Typical Q_{oss}

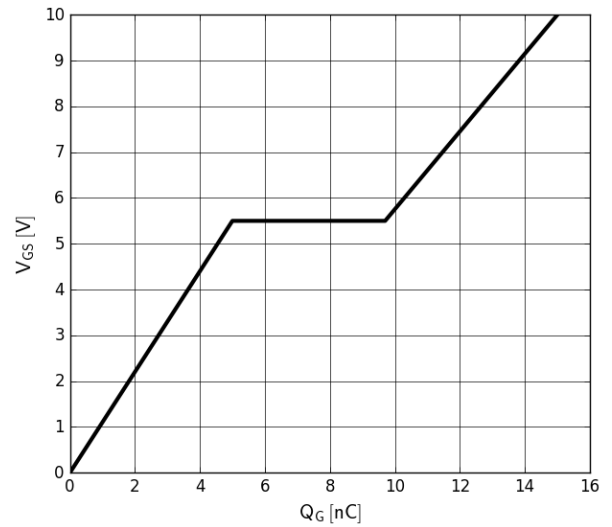


Figure 8. Typical Gate Charge
 $I_{DS}=22A$, $V_{DS}=600V$

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Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

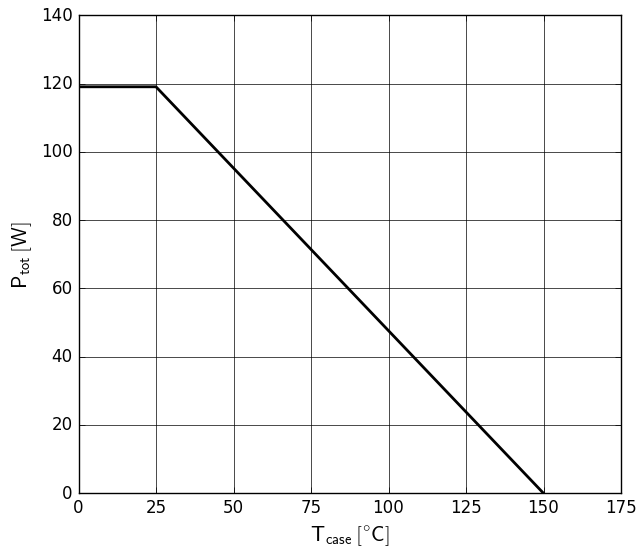


Figure 9. Power Dissipation

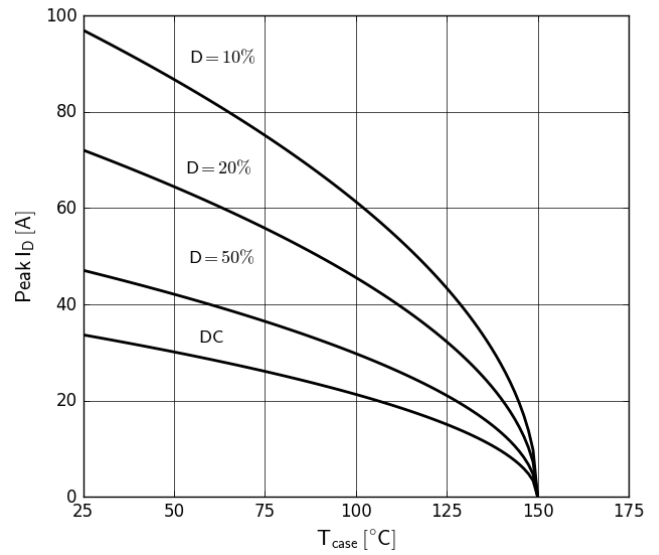


Figure 10. Current Derating
Pulse width $\leq 10\mu\text{s}$, $V_{GS} \geq 10\text{V}$

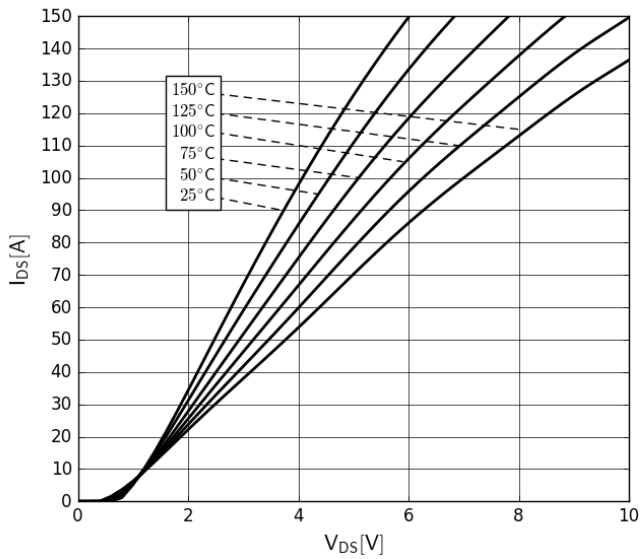


Figure 11. Forward Characteristics of Rev. Diode
 $I_S=f(V_{SD})$, parameter: T_J

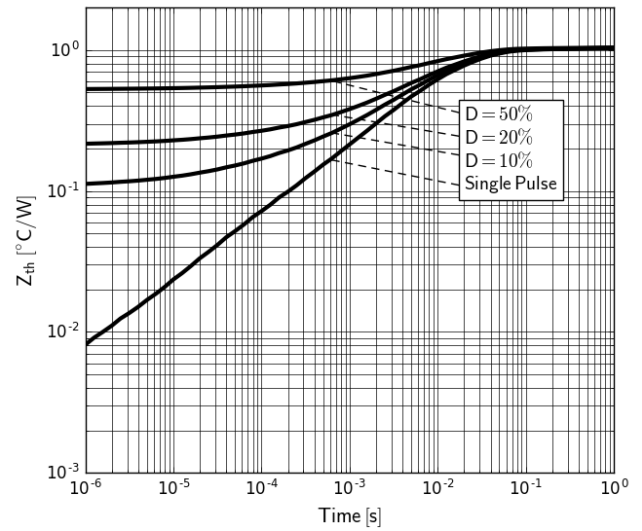


Figure 12. Transient Thermal Resistance

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Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

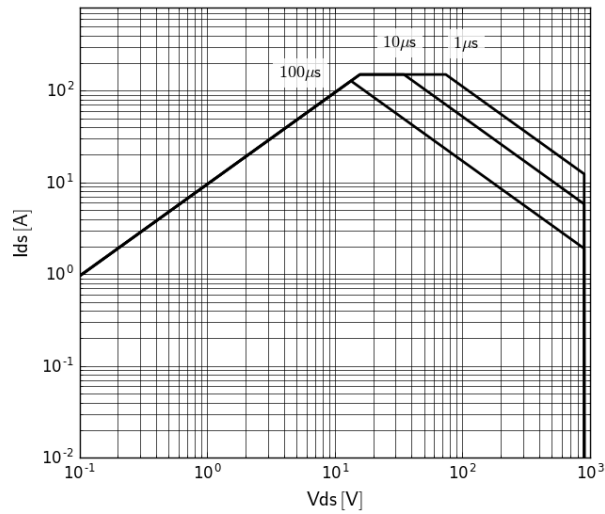


Figure 13. Safe Operating Area $T_c=25^\circ\text{C}$

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Test Circuits and Waveforms

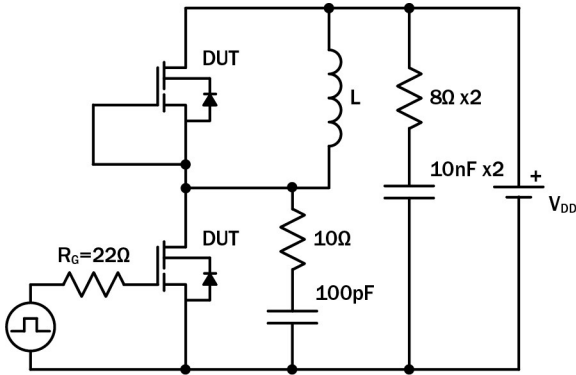


Figure 14. Switching Time Test Circuit
(see Circuit Implementation on page 3
for methods to ensure clean switching)

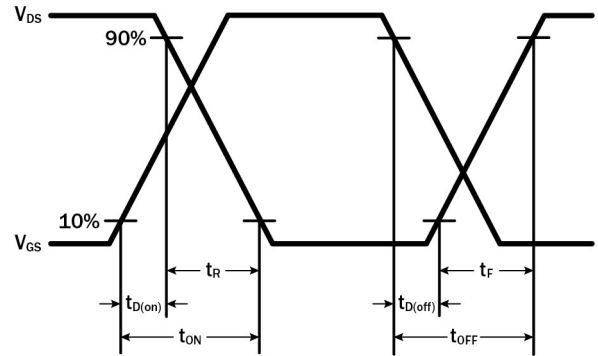


Figure 15. Switching Time Waveform

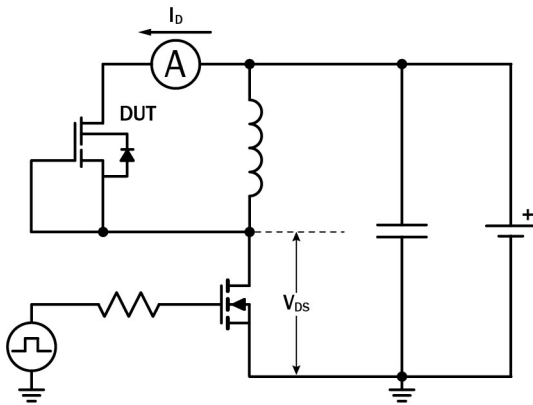


Figure 16. Diode Characteristics Test Circuit

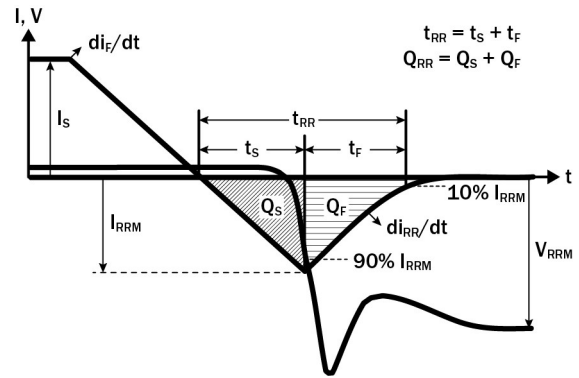


Figure 17. Diode Recovery Waveform

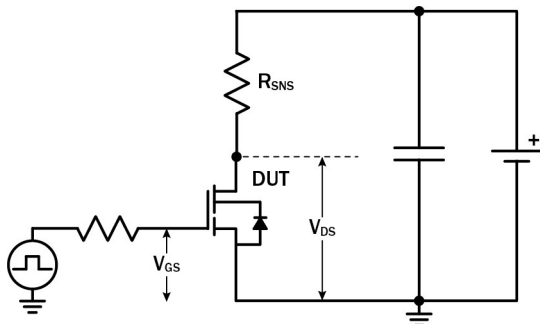


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

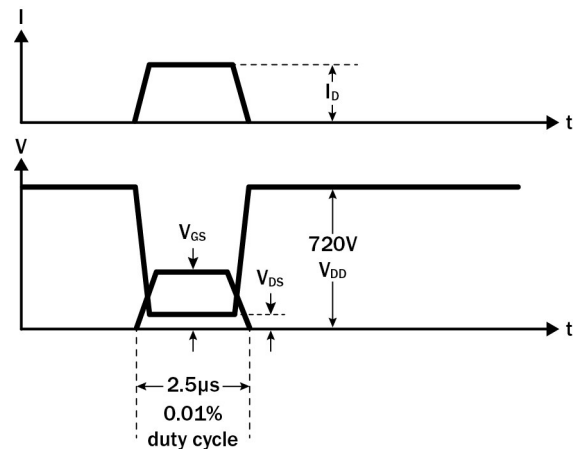


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

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Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003 : Printed Circuit Board Layout and Probing	

GaN Design Resources

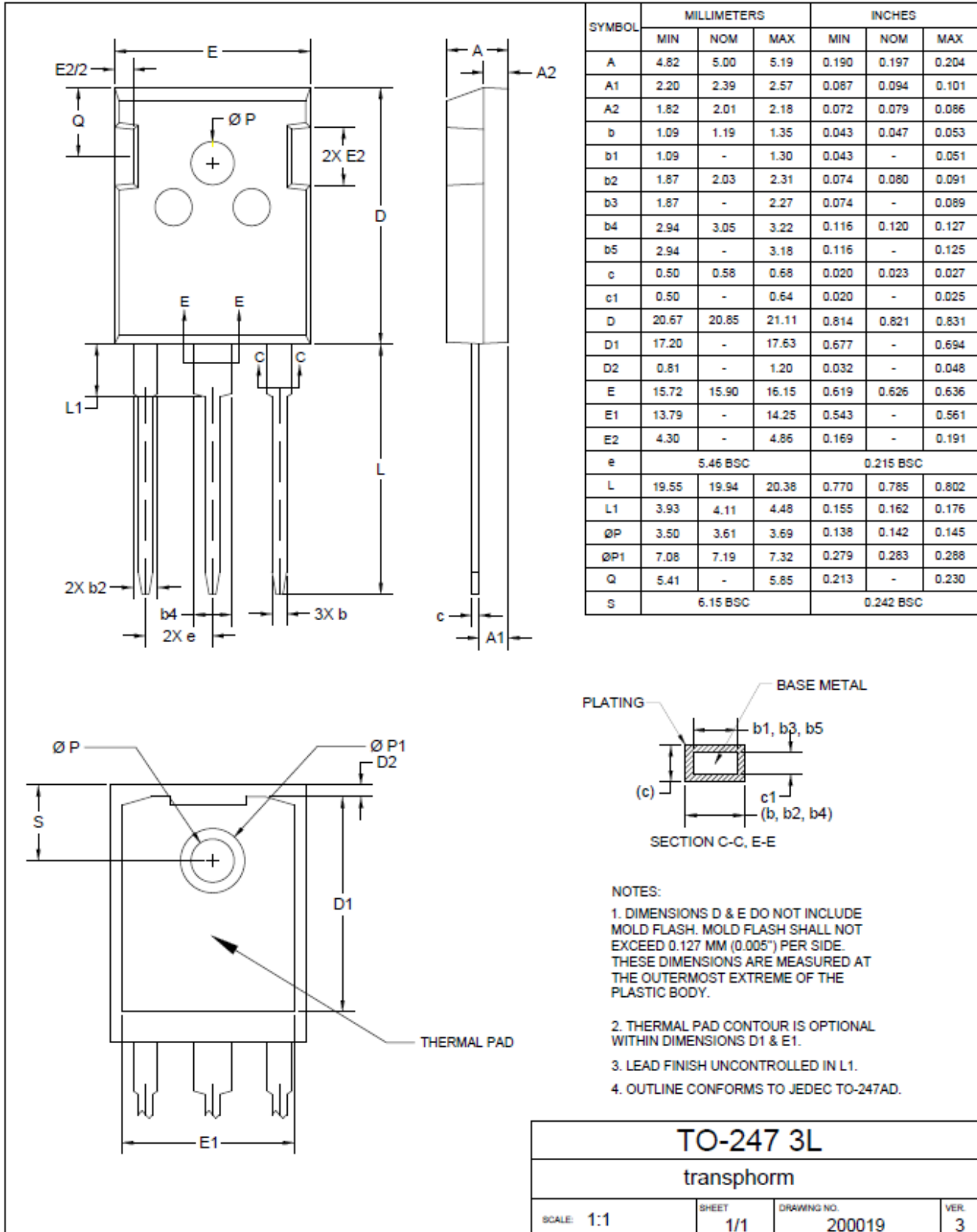
The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

TP90H050WS

Mechanical

3 Lead TO-247 Package



TP90H050WS

Revision History

Version	Date	Change(s)
0.1	10/27/2017	Release preliminary datasheet
0.2	11/20/2018	preliminary datasheet Add max mouting torque
0.3	02/27/2020	preliminary datasheet Updated Qrr Coss Qoss and Qg
1.1	07/07/2020	Datasheet Completed

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