

# 40A Analog MegaDLynx™: Non-Isolated DC-DC Power Modules

4.5V<sub>dc</sub> – 14.4V<sub>dc</sub> input; 0.6V<sub>dc</sub> to 2.0V<sub>dc</sub> output; 40A Output Current

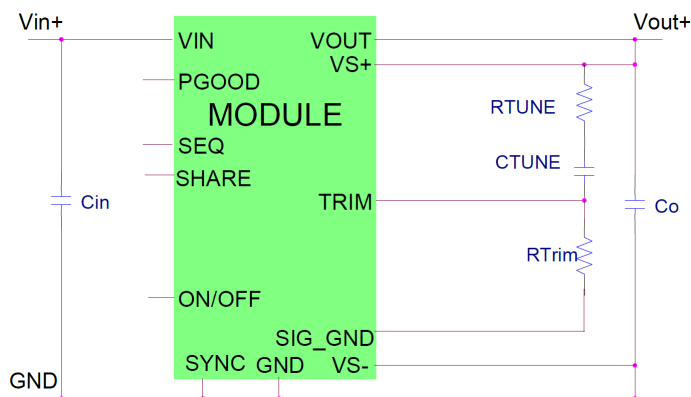
RoHS Compliant

TUNABLE  
LOOP™



## Description

The 40A Analog MegaDLynx™ power modules are non-isolated dc-dc converters that can deliver up to 40A of output current. These modules operate over a wide range of input voltage ( $V_{IN} = 4.5V_{dc} - 14.4V_{dc}$ ) and provide a precisely regulated output voltage from 0.6V<sub>dc</sub> to 2.0V<sub>dc</sub>, programmable via an external resistor. Features include remote On/Off, adjustable output voltage, over current and overtemperature protection. The module also includes the Tunable Loop™ feature that allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.



## Applications

- Industrial equipment
- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment
- Servers and storage applications
- Networking equipment

## Features

- Compliant to RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863.
- Compliant to REACH Directive (EC) No 1907/2006
- Compliant to RoHS EU Directive 2011/65/EU under exemption 7b (Lead solder exemption). Exemption 7b will expire after June 1, 2016 at which time this product will no longer be RoHS compliant (non-Z versions)
- Compliant to IPC-9592 (September 2008), Category 2, Class II
- Compatible in a Pb-free or SnPb reflow environment (Z versions)
- Wide Input voltage range ( $4.5V_{dc}$ - $14.4V_{dc}$ )
- Output voltage programmable from  $0.6V_{dc}$  to  $2.0V_{dc}$  via external resistor.
- Tunable Loop™ to optimize dynamic output voltage response.
- Power Good signal.
- Fixed switching frequency with capability of external synchronization.
- Output overcurrent protection (non-latching).
- Over temperature protection.
- Remote On/Off.
- Ability to sink and source current.
- Cost efficient open frame design.
- Small size: 33.02 mm x 13.46 mm x 10.9 mm (1.3 in x 0.53 in x 0.429 in)
- Wide operating temperature range [-40°C to 105°C (Ruggedized: -D), 85°C(Regular)]
- Ruggedized (-D) version able to withstand high levels of shock and vibration
- ANSI/UL\* 62368-1 and CAN/CSA† C22.2 No. 62368-1 Recognized, DIN VDE‡ 0868-1/A11:2017 (EN62368-1:2014/A11:2017)
- ISO\*\* 9001 and ISO 14001 certified manufacturing facilities

### FOOTNOTES

\* UL is a registered trademark of Underwriters Laboratories, Inc.

† CSA is a registered trademark of Canadian Standards Association.

‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.

\*\* ISO is a registered trademark of the International Organization of Standards

# Technical Specifications

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Symbol	Min	Max	Unit
Input Voltage Continuous	All	$V_{IN}$	-0.3	15	V
Operating Ambient Temperature (see Thermal Considerations section)	All	$T_A$	-40	105	°C
Storage Temperature	All	$T_{stg}$	-55	125	°C

## Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	All	$V_{IN}$	4.5	-	14.4	$V_{dc}$
Maximum Input Current ( $V_{IN} = 4.5V$ to $14V$ , $I_O = I_{O, max}$ )	All	$I_{IN, max}$			24	$A_{dc}$
Input No Load Current ( $V_{IN} = 12V_{dc}$ , $I_O = 0$ , module enabled)	$V_{O, set} = 0.6 V_{dc}$	$I_{IN, no load}$		54.7		mA
	$V_{O, set} = 2V_{dc}$	$I_{IN, no load}$		104		mA
Input Stand-by Current ( $V_{IN} = 12V_{dc}$ , module disabled)	All	$I_{IN, stand-by}$		12.5		mA
Inrush Transient	All	$I^2t$			1	$A^2s$
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, $1\mu H$ source impedance; $V_{IN}=0$ to $14V$ , $I_O = I_{O, max}$ ; see Test configuration)	All			90		$mA_{p-p}$
Input Ripple Rejection (120Hz)	All			-60		dB
Output Voltage Set-point (with 0.1% tolerance for external resistor used to set output voltage)	All	$V_{O, set}$	-1.0		+1.0	$\%V_{O, set}$
Output Voltage (Over all operating input voltage, resistive load, and temperature conditions until end of life)	All	$V_{O, set}$	-3.0	-	+3.0	$\%V_{O, set}$
Adjustment Range (selected by an external resistor) (Some output voltages may not be possible depending on the input voltage – see Feature Descriptions Section)	All	$V_O$	0.6		2.0	$V_{dc}$
Remote Sense Range	All				0.5	$V_{dc}$
Output Regulation Line ( $V_{IN}=V_{IN, min}$ to $V_{IN, max}$ ) Load ( $I_O=I_{O, min}$ to $I_{O, max}$ ) Temperature ( $T_{ref}=T_{A, min}$ to $T_{A, max}$ )	All			-	6	mV
	All			-	10	mV
	All			0.4		$\%V_{O, set}$
Output Ripple and Noise on nominal output ( $V_{IN}=V_{IN, nom}$ and $I_O=I_{O, min}$ to $I_{O, max}$ $C_O = 0.1\mu F$ // $22\mu F$ ceramic capacitors) Peak-to-Peak (5MHz to 20MHz bandwidth) RMS (5MHz to 20MHz bandwidth)						
	All		-	50	100	$mV_{pk-pk}$
	All			20	38	$mV_{rms}$

## Technical Specifications (continued)

### Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
External Capacitance <sup>1</sup> Without the Tunable Loop™ ESR ≥ 1 mΩ	All	C <sub>O, max</sub>	6x47	-	6x47	μF
With the Tunable Loop™ ESR ≥ 0.15 mΩ	All	C <sub>O, max</sub>	6x47	-	7000	μF
ESR ≥ 10 mΩ	All	C <sub>O, max</sub>	6x47	-	8500	μF
Output Current (in either sink or source mode)	All	I <sub>o</sub>	0		40	A <sub>dc</sub>
Output Current Limit Inception (Hiccup Mode) (current limit does not operate in sink mode)	All	I <sub>O, lim</sub>		150		% I <sub>O, max</sub>
Output Short-Circuit Current (V <sub>o</sub> ≤ 250mV) ( Hiccup Mode )	All	I <sub>O, s/c</sub>		2.1		A <sub>rms</sub>
Efficiency V <sub>IN</sub> = 12V <sub>dc</sub> , T <sub>A</sub> = 25°C	V <sub>O, set</sub> = 0.6 V <sub>dc</sub>	η	78.0	81.3		%
	V <sub>O, set</sub> = 1.2 V <sub>dc</sub>	η	84.0	88.5		%
I <sub>o</sub> = I <sub>O, max</sub> , V <sub>O</sub> = V <sub>O, set</sub>	V <sub>O, set</sub> = 1.8 V <sub>dc</sub>	η	85.25	91.5		%
Switching Frequency	All	f <sub>sw</sub>	380	400	420	kHz
Frequency Synchronization	All					
Synchronization Frequency Range	All		350		480	kHz
High-Level Input Voltage	All	V <sub>IH</sub>	2.0			V
Low-Level Input Voltage	All	V <sub>IL</sub>			0.4	V
Input Current, SYNC	All	I <sub>SYNC</sub>			100	nA
Minimum Pulse Width, SYNC	All	t <sub>SYNC</sub>	100			ns
Maximum SYNC rise time	All	t <sub>SYNC_SH</sub>	100			ns

<sup>1</sup> External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

### General Specifications

Parameter	Device	Min	Typ	Max	Unit
Calculated MTBF (I <sub>o</sub> = 0.8 I <sub>O, max</sub> , T <sub>A</sub> = 40°C) Telcordia Issue 2 Method 1 Case 3	All		6,498,438		Hours
Weight		-	11.7 (0.41)	-	g (oz.)

### Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typ	Max	Unit
On/Off Signal Interface (V <sub>IN</sub> = V <sub>IN, min</sub> to V <sub>IN, max</sub> ; open collector or equivalent, Signal referenced to GND) Device with no suffix "4" – Positive Logic (See Ordering Information)						
Logic High (Module ON)						
Input High Current	All	I <sub>IH</sub>		-	10	μA
Input High Voltage	All	V <sub>IH</sub>	3.5	-	V <sub>IN, max</sub>	V
Logic Low (Module OFF)						
Input Low Current	All	I <sub>IL</sub>	-	-	1	mA
Input Low Voltage	All	V <sub>IL</sub>	-0.3	-	0.4	V

## Technical Specifications (continued)

### Feature Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Device Code with no suffix – Negative Logic (See Ordering Information)						
(On/OFF pin is open collector/drain logic input with external pull-up resistor; signal referenced to GND)						
Logic High (Module OFF)						
Input High Current	All	$I_{IH}$	-	-	1	mA
Input High Voltage	All	$V_{IH}$	2	-	$V_{IN,max}$	$V_{dc}$
Logic Low (Module ON)						
Input low Current	All	$I_{IL}$	-	-	10	$\mu A$
Input Low Voltage	All	$V_{IL}$	-0.2	-	0.4	$V_{dc}$
Turn-On Delay and Rise Times						
( $V_{IN}=V_{IN, nom}$ , $I_O=I_{O, max}$ , $V_O$ to within $\pm 1\%$ of steady state)						
Case 1: On/Off input is enabled and then input power is applied (delay from instant at which $V_{IN} = V_{IN,min}$ until $V_O = 10\%$ of $V_{O, set}$ )	All	$T_{delay}$	1.0	1.1	1.7	msec
Case 2: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which $V_{on/off}$ is enabled until $V_O = 10\%$ of $V_{O, set}$ )	All	$T_{delay}$	600	700	1800	$\mu sec$
Output voltage Rise time (time for $V_O$ to rise from 10% of $V_{O, set}$ to 90% of $V_{O, set}$ )	All	$T_{rise}$	1.2	1.5	2.2	msec
Output voltage overshoot ( $T_A = 25^\circ C$ $V_{IN} = V_{IN, min}$ to $V_{IN, max}$ , $I_O = I_{O, min}$ to $I_{O, max}$ ) With or without maximum external capacitance			0	1.5	3.0	% $V_{O, set}$
Over Temperature Protection (See Thermal Considerations section)	All	$T_{ref}$	123	130	137	$^\circ C$
Tracking Accuracy ( $V_{IN, min}$ to $V_{IN, max}$ ; $I_{O, min}$ to $I_{O, max}$ $V_{SEQ} < V_O$ ) (Power-Up: 0.5V/ms) (Power-Down: 0.5V/ms)	All All	$V_{SEQ} - V_O$ $V_{SEQ} - V_O$			100 100	mV mV
Input Undervoltage Lockout						
Turn-on Threshold	All		4.144	4.25	4.407	$V_{dc}$
Turn-off Threshold	All		3.947	3.98	4.163	$V_{dc}$
Hysteresis	All		0.25	0.3	0.35	$V_{dc}$
PGOOD (Power Good)						
Signal Interface Open Drain, $V_{supply} \leq 5V_{DC}$						
Overvoltage threshold for PGOOD ON	All		103	108	113	% $V_{O, set}$
Overvoltage threshold for PGOOD OFF	All		105	110	115	% $V_{O, set}$
Undervoltage threshold for PGOOD ON	All		87	92	97	% $V_{O, set}$
Undervoltage threshold for PGOOD OFF	All		85	90	95	% $V_{O, set}$
Pulldown resistance of PGOOD pin	All				50	$\Omega$
Sink current capability into PGOOD pin	All				5	mA

# Technical Specifications (continued)

## Characteristic Curves

The following figures provide typical characteristics for the 40A Analog MegaDLynx™ at 0.6V<sub>o</sub> and 25°C.

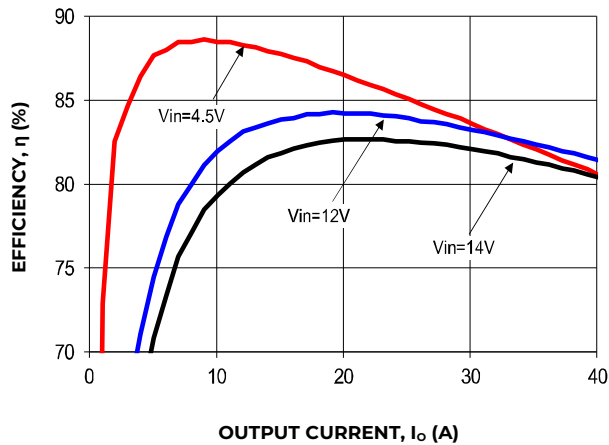


Figure 1. Converter Efficiency versus Output Current.

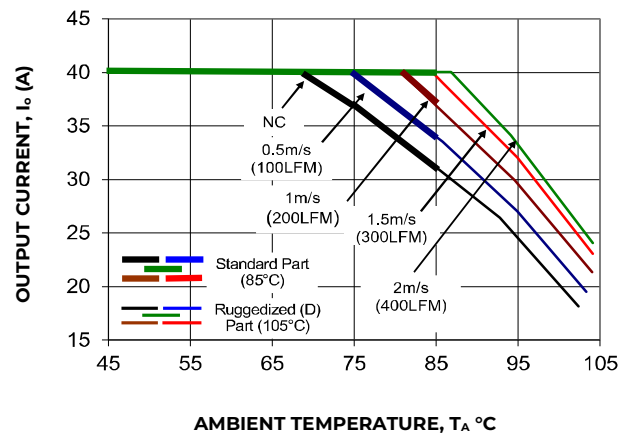


Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

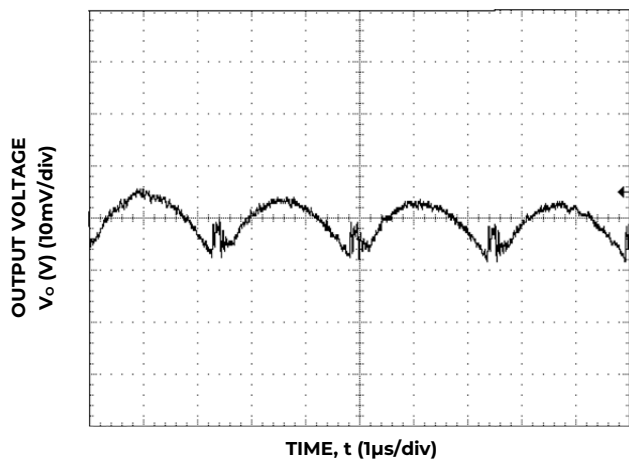


Figure 3. Typical output ripple and noise (C<sub>o</sub>=6x47 μF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

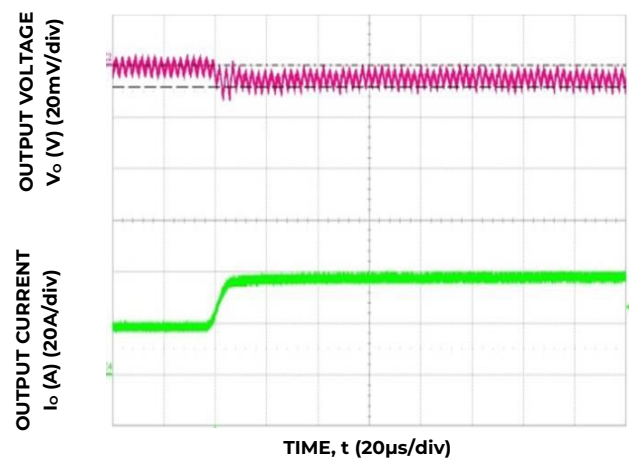


Figure 4. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 12x680μF +6x47μF, C<sub>Tune</sub>=47nF, R<sub>Tune</sub>=180 ohms

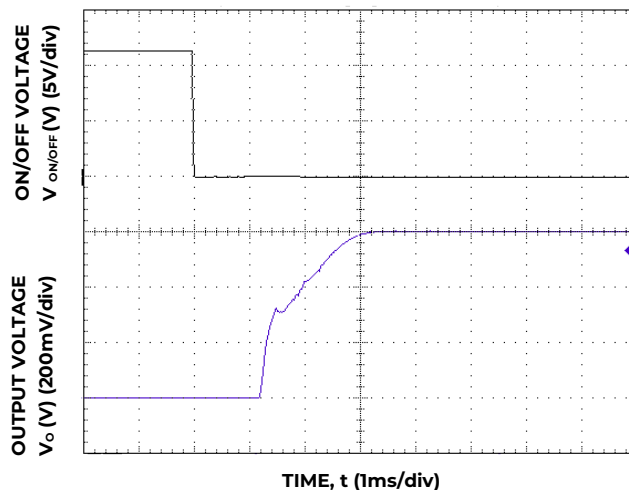


Figure 5. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

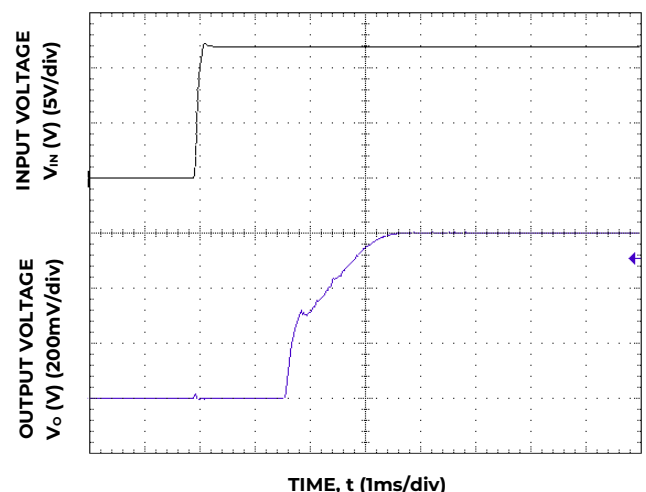


Figure 6. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

## Technical Specifications (continued)

### Characteristic Curves (continued)

The following figures provide typical characteristics for the 40A Analog MegaDLynx™ at 1.2V<sub>o</sub> and 25°C.

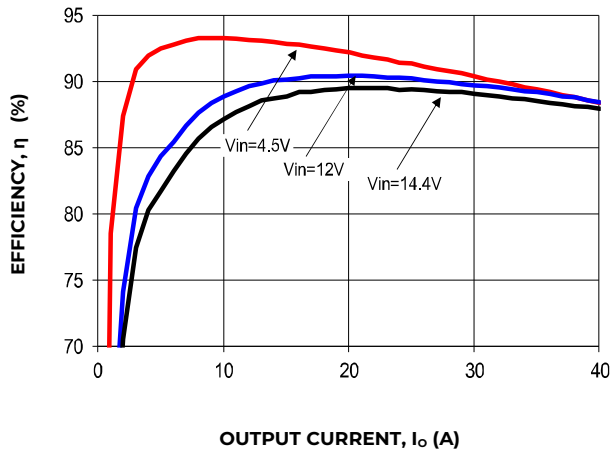


Figure 7. Converter Efficiency versus Output Current.

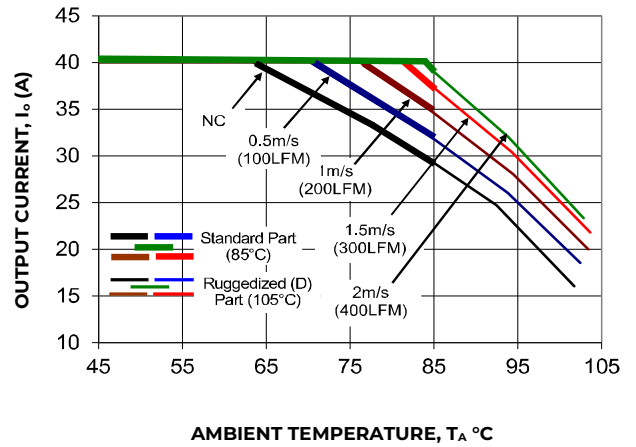


Figure 8. Derating Output Current versus Ambient Temperature and Airflow.

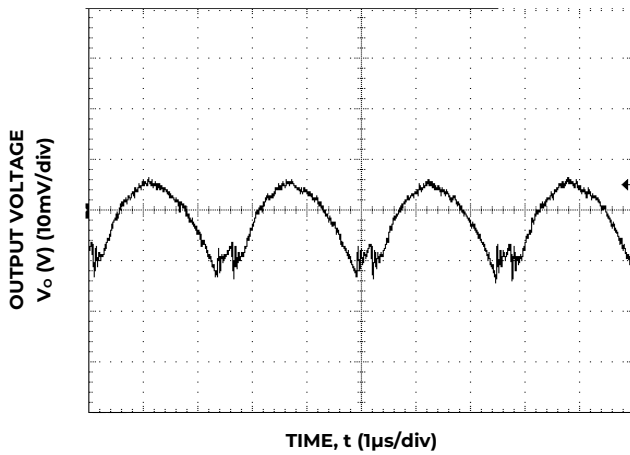


Figure 9. Typical output ripple and noise (C<sub>o</sub>=6x47μF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

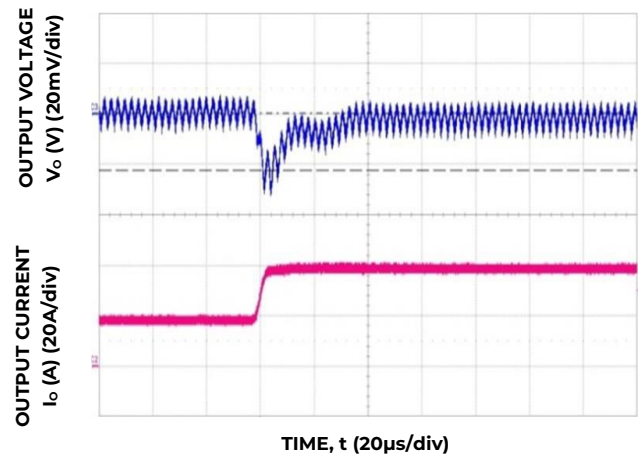


Figure 10. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 6x330μF, C<sub>Tune</sub>=12nF, R<sub>Tune</sub>=200 ohms

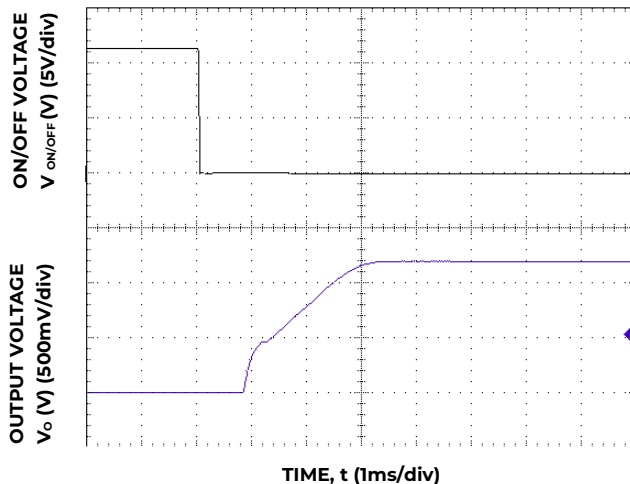


Figure 11. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

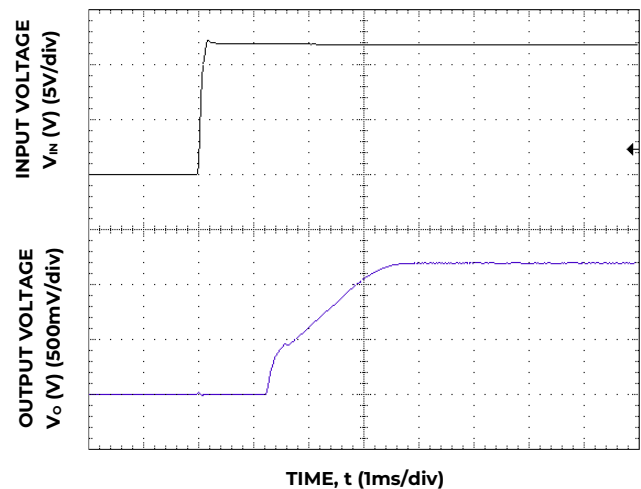


Figure 12. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

## Technical Specifications (continued)

### Characteristic Curves (continued)

The following figures provide typical characteristics for the 40A Analog MegaDlynx™ at 1.8V<sub>o</sub> and 25°C.

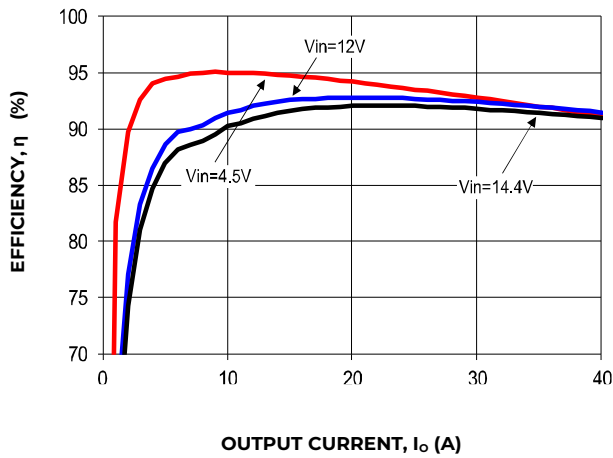


Figure 13 Converter Efficiency versus Output Current.

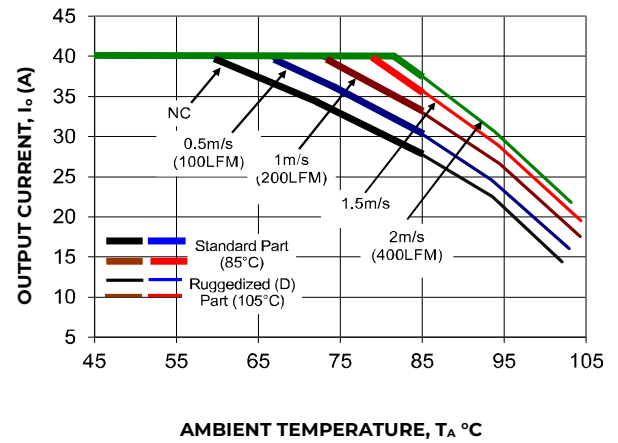


Figure 14. Derating Output Current versus Ambient Temperature and Airflow.

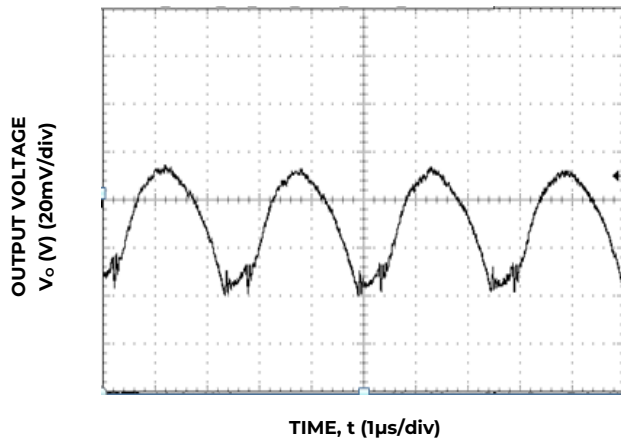


Figure 15. Typical output ripple and noise (C<sub>o</sub>=6x47μF ceramic, V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

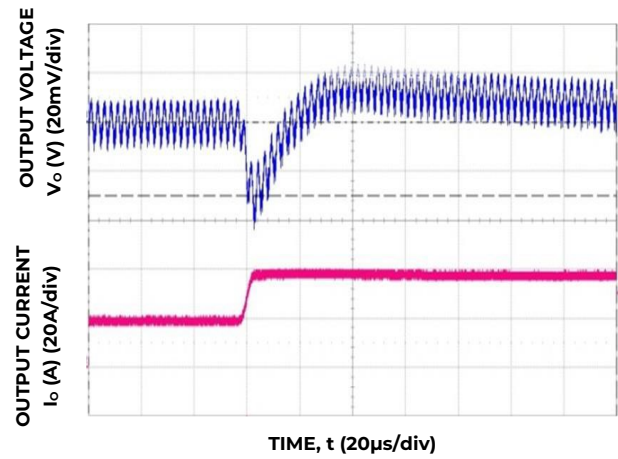


Figure 16. Transient Response to Dynamic Load Change from 50% to 100% at 12V<sub>in</sub>, C<sub>out</sub>= 6x330μF, C<sub>Tune</sub>=5.6nF & R<sub>Tune</sub>=220 ohms.

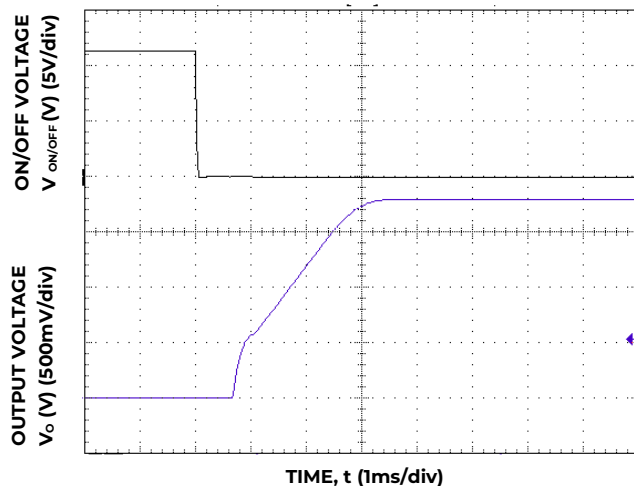


Figure 17. Typical Start-up Using On/Off Voltage (I<sub>o</sub> = I<sub>o,max</sub>).

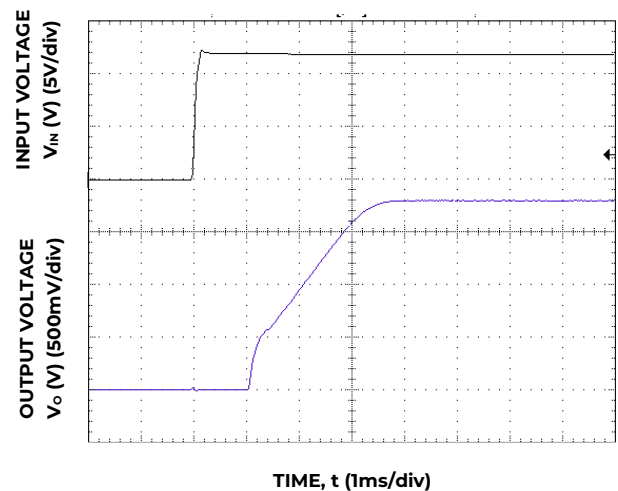


Figure 18. Typical Start-up Using Input Voltage (V<sub>IN</sub> = 12V, I<sub>o</sub> = I<sub>o,max</sub>).

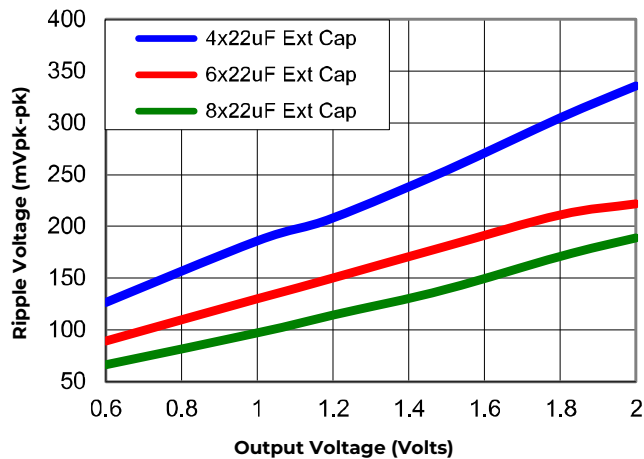
## Technical Specifications (continued)

### Design Considerations

#### Input Filtering

The 40A Analog Mega DLynx™ module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 19 shows the input ripple voltage for various output voltages at 40A of load current with 4x22  $\mu$ F, 6x22  $\mu$ F or 8x22  $\mu$ F ceramic capacitors and an input of 12V.



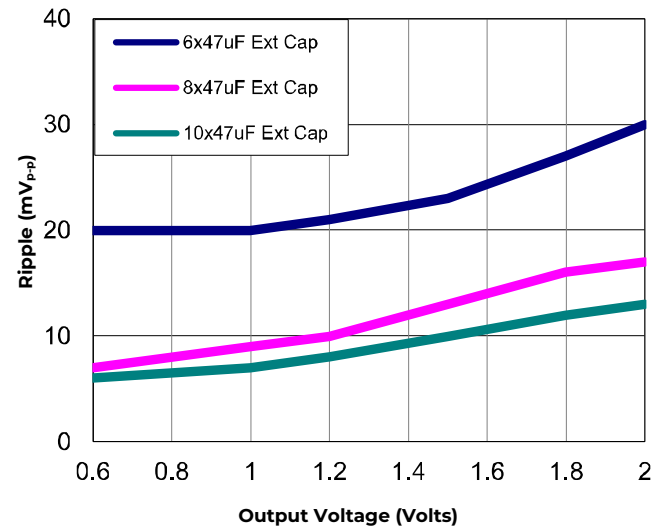
**Figure 19. Input ripple voltage for various output voltages with various external ceramic capacitors at the input (40A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz**

#### Output Filtering

These modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1  $\mu$ F ceramic and 47  $\mu$ F ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figure 20 provides output ripple information for different

external capacitance values at various  $V_o$  and a full load current of 40A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.



**Figure 20. Output ripple voltage for various output voltages with external 6x47  $\mu$ F, 8x47  $\mu$ F or 10x47  $\mu$ F ceramic capacitors at the output (40A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz**

### Safety Considerations

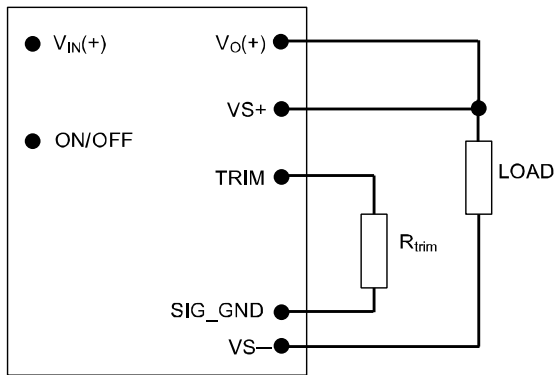
For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL ANSI/UL\* 62368-1 and CAN/CSA+ C22.2 No. 62368-1 Recognized, DIN VDE 0868-1/A11:2017 (EN62368-1:2014/A11:2017).

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast-acting fuse with a maximum rating of 30A, 100V (for example, Little fuse 456 series) in the positive input lead.

## Technical Specifications (continued)

### Analog Feature Descriptions (continued)



**Figure 24. Circuit configuration for programming output voltage using an external resistor.**

**Caution** – Do not connect SIG\_GND to GND elsewhere in the layout

Without an external resistor between Trim and SIG\_GND pins, the output of the module will be 0.6V<sub>dc</sub>. To calculate the value of the trim resistor, R<sub>trim</sub> for a desired output voltage, should be as per the following equation:

$$R_{trim} = \left[ \frac{12}{V_o - 0.6} \right] \text{ k}\Omega$$

R<sub>trim</sub> is the external resistor in kΩ

V<sub>o</sub> is the desired output voltage.

Table 1 provides R<sub>trim</sub> values required for some common output voltages.

V <sub>O, set</sub> (V)	R <sub>trim</sub> (KΩ)
0.6	Open
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10

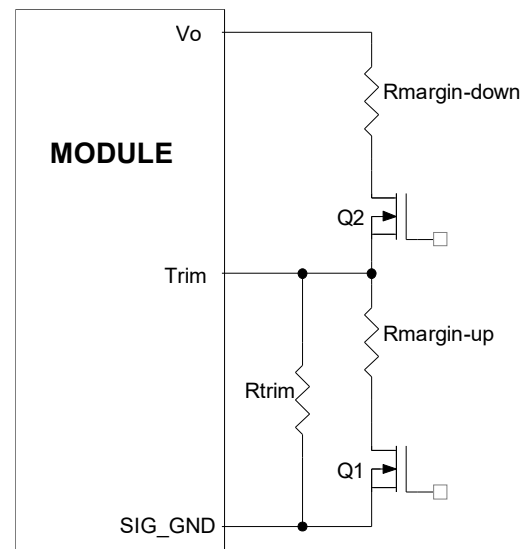
**Table 1**

### Remote Sense

The power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the V<sub>OUT</sub> and GND pins of the module should not exceed 0.5V.

### Analog Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor, R<sub>margin-up</sub>, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, R<sub>margin-down</sub>, from the Trim pin to output pin for margining-down. Figure 25 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at [omnionpower.com](http://omnionpower.com) under the Downloads section, also calculates the values of R<sub>margin-up</sub> and R<sub>margin-down</sub> for a specific output voltage and % margin. Please consult your local OmniOn technical representative for additional details.



**Figure 25. Circuit Configuration for margining Output voltage.**

### Output Voltage Sequencing

The power module includes a sequencing feature, EZSEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig. 26. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.

# Technical Specifications (continued)

## Analog Feature Descriptions

### Remote On/Off

The 40A Analog MegaDLynx™ power modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix “4” – see Ordering Information), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (no device code suffix, see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Figure 21.

For negative logic On/Off modules, the circuit configuration is shown in Figure 22.

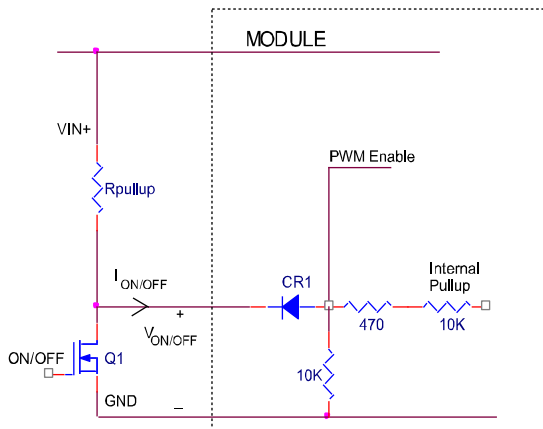


Figure 21. Circuit configuration for using positive On/Off logic.

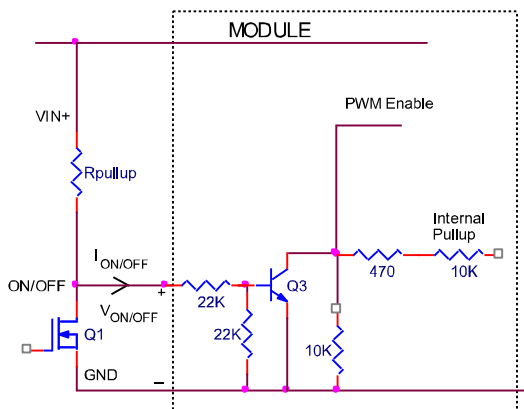


Figure 22. Circuit configuration for using negative On/Off logic.

### Monotonic Start-up and Shutdown

The module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

### Startup into Pre-biased Output

The module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

### Analog Output Voltage Programming

The output voltage of the module is programmable to any voltage from 0.6V<sub>dc</sub> to 2.0V<sub>dc</sub> by connecting a resistor between the Trim and SIG\_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig. 23. The Upper Limit curve shows that for output voltages lower than 0.8V, the input voltage must be lower than the maximum of 14.4V. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 4.5V.

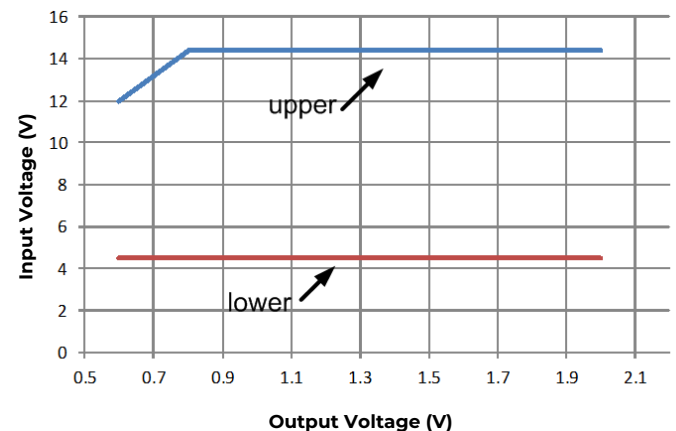


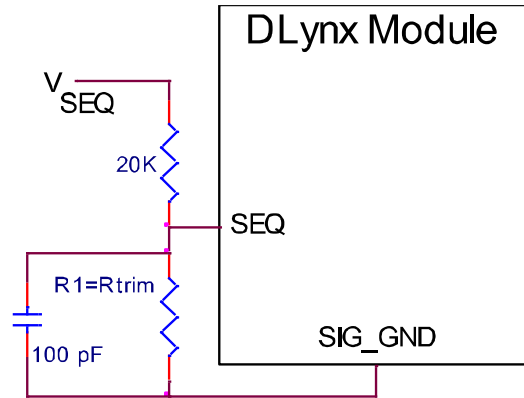
Figure 23. Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

## Technical Specifications (continued)

### Analog Feature Descriptions (continued)

#### Output Voltage Sequencing (continued)

For all DLynx modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.



**Figure 26.** Circuit showing connection of the sequencing signal to the SEQ pin.

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

The module's output can track the SEQ pin signal with slopes of up to 0.5V/msec during power-up or power-down.

To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

#### Overcurrent Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates

normally once the output current is brought back into its specified range.

#### Overtemperature Protection

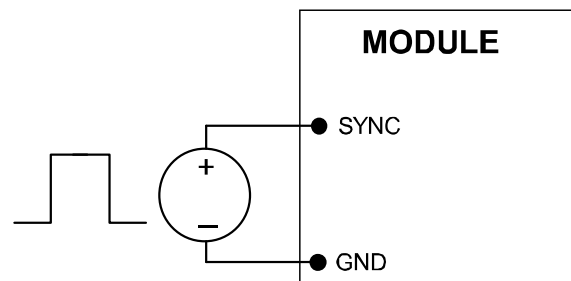
To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of 145°C (typ) is exceeded at the thermal reference point  $T_{ref}$ . Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

#### Input Undervoltage Lockout

At input voltages below the input undervoltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the undervoltage lockout turn-on threshold.

#### Synchronization

The module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module as shown in Fig. 27, with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency. **If synchronization is not being used, connect the SYNC pin to GND.**



**Figure 27.** External source connections to synchronize switching frequency of the module.

#### Active Load Sharing (-P Option)

For additional power requirements, the Mega DLynx™ power module is also equipped with paralleling capability. Up to five modules can be configured in parallel, with active load sharing.

To implement paralleling, the following conditions must be satisfied.

## Technical Specifications (continued)

### Analog Feature Descriptions (continued)

#### Active Load Sharing (-P Option) (continued)

- All modules connected in parallel must be frequency synchronized where they are switching at the same frequency. This is done by using the SYNC function of the module and connecting to an external frequency source. Modules can be interleaved to reduce input ripple/filtering requirements.
- The share pins of all units in parallel must be connected together. The path of these connections should be as direct as possible.
- The remote sense connections to all modules should be made that to the same points for the output, i.e. all VS+ and VS- terminals for all modules are connected to the power bus at the same points.
- For converters operating in parallel, tunable loop components “R<sub>TUNE</sub>” and “C<sub>TUNE</sub>” must be selected to meet the required transient specification. For providing better noise immunity, we recommend that R<sub>TUNE</sub> value to be greater than 300Ω.

Some special considerations apply for design of converters in parallel operation:

- When sizing the number of modules required for parallel operation, take note of the fact that current sharing has some tolerance. In addition, under transient conditions such as a dynamic load change and during startup, all converter output currents will not be equal. To allow for such variation and avoid the likelihood of a converter shutting off due to a current overload, the total capacity of the paralleled system should be no more than 90% of the sum of the individual converters. As an example, for a system of four MegaDLynx™ converters in parallel, the total current drawn should be less than 90% of (3 x 40A), i.e. less than 108 A.
- All modules should be turned ON and OFF together. This is so that all modules come up at the same time avoiding the problem of one converter sourcing current into the other leading to an overcurrent trip condition. To ensure that all modules come up simultaneously, the on/off pins of all paralleled converters should be tied together and the converters enabled and disabled using the on/off pin. Note that this means that converters in parallel cannot be digitally turned ON as that does not ensure that all modules being paralleled turn on at the same time.
- If digital trimming is used to adjust the overall output voltage, the adjustments need to be made in a series of small steps to avoid shutting down the output. Each step should be no more than

20mV for each module. For example, to adjust the overall output voltage in a setup with two modules (A and B) in parallel from 1V to 1.1V, module A would be adjusted from 1.0 to 1.02V followed by module B from 1.0 to 1.02V, then each module in sequence from 1.02 to 1.04V and so on until the final output voltage of 1.1V is reached.

- If the Sequencing function is being used to start-up and shut down modules and the module is being held to 0V by the tracking signal then there may be small deviations on the module output. This is due to controller duty cycle limitations encountered in trying to hold the voltage down near 0V.
- The share bus is not designed for redundant operation and the system will be non-functional upon failure of one of the units when multiple units are in parallel. In particular, if one of the converters shuts down during operation, the other converters may also shut down due to their outputs hitting current limit. In such a situation, unless a coordinated restart is ensured, the system may never properly restart since different converters will try to restart at different times causing an overload condition and subsequent shutdown. This situation can be avoided by having an external output voltage monitor circuit that detects a shutdown condition and forces all converters to shut down and restart together.

When not using the active load share feature, share pins should be left unconnected.

#### Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as over-temperature, overcurrent or loss of regulation occurs that would result in the output voltage going outside the specified thresholds.

The default value of PGOOD ON thresholds are set at ±8% of the nominal Vset value, and PGOOD OFF thresholds are set at ±10% of the nominal Vset. For example, if the nominal voltage (Vset) is set at 1.0V, then the PGOOD ON thresholds will be active anytime the output voltage is between 0.92V and 1.08V, and PGOOD OFF thresholds are active at 0.90V and 1.10V respectively.

The PGOOD terminal can be connected through a pull-up resistor (suggested value 100KΩ) to a source of 5V<sub>DC</sub> or lower.

## Technical Specifications (continued)

### Analog Feature Descriptions (continued)

#### Dual Layout

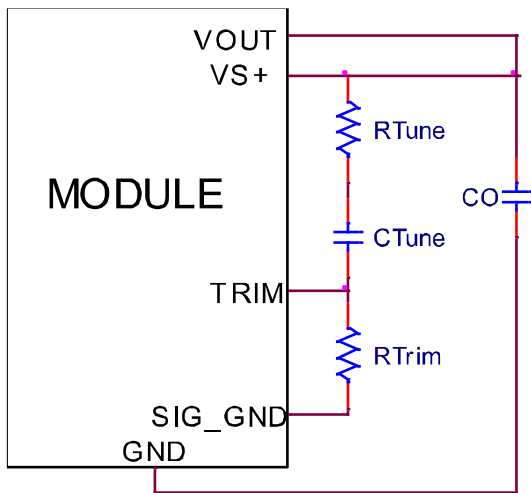
Identical dimensions and pin layout of Analog and Analog MegaDLynx modules permit migration from one to the other without needing to change the layout. In both cases the trim resistor is connected between trim and signal ground.

#### Tunable Loop™

The module has a feature that optimizes transient response of the module called Tunable Loop™.

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the VS+ and TRIM pins of the module, as shown in Fig. 28. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.



**Figure 28.** Circuit diagram showing connection of  $R_{TUNE}$  and  $C_{TUNE}$  to tune the control loop of the module.

Recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  for different output capacitor combinations are given in Table 2. Table 2 shows the recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  for different values of ceramic output capacitors up to 1000 $\mu$ F that might be needed for an application to meet output ripple and noise requirements. Selecting  $R_{TUNE}$  and  $C_{TUNE}$  according to Table 2 will ensure stable operation of the module. In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 20A to 40A step change (50% of full load), with an input voltage of 12V.

Please contact your OmniOn technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values.

$C_o$	6x47 $\mu$ F	8x47 $\mu$ F	10x47 $\mu$ F	12x47 $\mu$ F	20x47 $\mu$ F
$R_{TUNE}$	330 $\Omega$	330 $\Omega$	330 $\Omega$	330 $\Omega$	200 $\Omega$
$C_{TUNE}$	330pF	820pF	1200pF	1500pF	3300pF

**Table 2.** General recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  for  $V_{in}=12V$  and various external ceramic capacitor combinations.

$V_o$	1.8V	1.2V	0.6V
$C_o$	4x47 $\mu$ F + 6x330 $\mu$ F polymer	4x47 $\mu$ F + 11x330 $\mu$ F polymer	4x47 $\mu$ F + 12x680 $\mu$ F polymer
$R_{TUNE}$	220 $\Omega$	200 $\Omega$	180 $\Omega$
$C_{TUNE}$	5600pF	12nF	47nF
$\Delta V$	34mV	22mV	12mV

**Table 3.** Recommended values of  $R_{TUNE}$  and  $C_{TUNE}$  to obtain transient deviation of 2% of  $V_{out}$  for a 20A step load with  $V_{in}=12V$ .

**Note:** The capacitors used in the Tunable Loop tables are 47  $\mu$ F/3 m $\Omega$  ESR ceramic, 330  $\mu$ F/12 m $\Omega$  ESR polymer capacitor and 680 $\mu$ F/12 m $\Omega$  polymer capacitor.

## Technical Specifications (continued)

### Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 29. The preferred airflow direction for the module is in Figure 30.

The thermal reference points,  $T_{ref}$  used in the specifications are also shown in Figure 30. For reliable operation the temperatures at these points should not exceed 130°C. The output power of the module should not exceed the rated power of the module ( $V_{o, set} \times I_{o, max}$ ).

Please refer to the Application Note “Thermal Characterization Process For Open-Frame Board-Mounted Power Modules” for a detailed discussion of thermal aspects including maximum device temperatures.

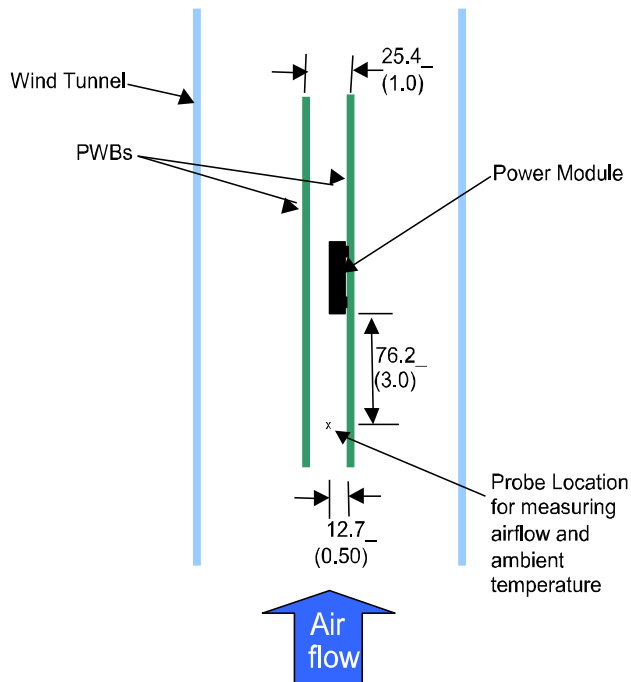


Figure 29. Thermal Test Setup.

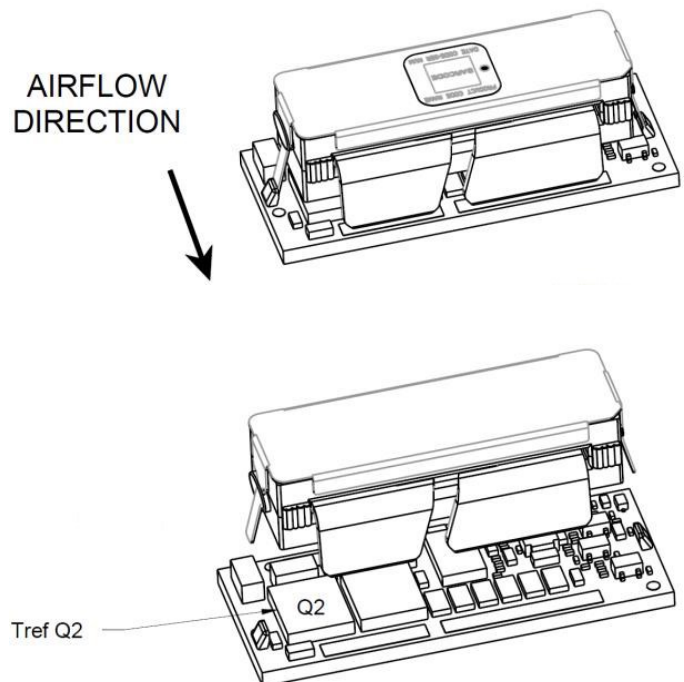


Figure 30. Preferred airflow direction and location of hotspot of the module ( $T_{ref}$ ).

## Technical Specifications (continued)

### Shock and Vibration

The ruggedized (-D version) of the modules are designed to withstand elevated levels of shock and vibration to be able to operate in harsh environments. The ruggedized modules have been successfully tested to the following conditions:

#### Non operating random vibration:

Random vibration tests conducted at 25C, 10 to 2000Hz, for 30 minutes each level, starting from 30Grms (Z axis) and up to 50Grms (Z axis). The units were then subjected to two more tests of 50Grms at 30 minutes each for a total of 90 minutes.

#### Operating shock to 40G per Mil Std. 810G, Method 516.4 Procedure I:

The modules were tested in opposing directions along each of three orthogonal axes, with waveform and amplitude of the shock impulse characteristics as follows:

All shocks were half sine pulses, 11 milliseconds (ms) in duration in all 3 axes.

Units were tested to the Functional Shock Test of MIL-STD-810, Method 516.4, Procedure I - Figure 516.4-4. A shock magnitude of 40G was utilized. The operational units were subjected to three shocks in each direction along three axes for a total of eighteen shocks.

#### Operating vibration per Mil Std 810G, Method 514.5 Procedure I:

The ruggedized (-D version) modules are designed and tested to vibration levels as outlined in MIL-STD-810G, Method 514.5, and Procedure I, using the Power Spectral Density (PSD) profiles as shown in Table 1 and Table 2 for all axes. Full compliance with performance specifications was required during the performance test. No damage was allowed to the module and full compliance to performance specifications was required when the endurance environment was removed. The module was tested per MIL-STD-810, Method 514.5, Procedure I, for functional (performance) and endurance random vibration using the performance and endurance levels shown in Table 4 and Table 5 for all axes. The performance test has been split, with one half accomplished before the endurance test and one half after the endurance test (in each axis). The duration of the performance test was at least 16 minutes total per axis and at least 120 minutes total per axis for the endurance test. The endurance test period was 2 hours minimum per axis.

Frequency (Hz)	PSD Level (G <sup>2</sup> /Hz)	Frequency (Hz)	PSD Level (G <sup>2</sup> /Hz)	Frequency (Hz)	PSD Level (G <sup>2</sup> /Hz)
10	1.14E-03	170	2.54E-03	690	1.03E-03
30	5.96E-03	230	3.70E-03	800	7.29E-03
40	9.53E-04	290	7.99E-04	890	1.00E-03
50	2.08E-03	340	1.12E-02	1070	2.67E-03
90	2.08E-03	370	1.12E-02	1240	1.08E-03
110	7.05E-04	430	8.84E-04	1550	2.54E-03
130	5.00E-03	490	1.54E-03	1780	2.88E-03
140	8.20E-04	560	5.62E-04	2000	5.62E-04

Table 4: Performance Vibration Qualification - All Axes

Frequency (Hz)	PSD Level (G <sup>2</sup> /Hz)	Frequency (Hz)	PSD Level (G <sup>2</sup> /Hz)	Frequency (Hz)	PSD Level (G <sup>2</sup> /Hz)
10	0.00803	170	0.01795	690	0.00727
30	0.04216	230	0.02616	800	0.05155
40	0.00674	290	0.00565	890	0.00709
50	0.01468	340	0.07901	1070	0.01887
90	0.01468	370	0.07901	1240	0.00764
110	0.00498	430	0.00625	1550	0.01795
130	0.03536	490	0.01086	1780	0.02035
140	0.0058	560	0.00398	2000	0.00398

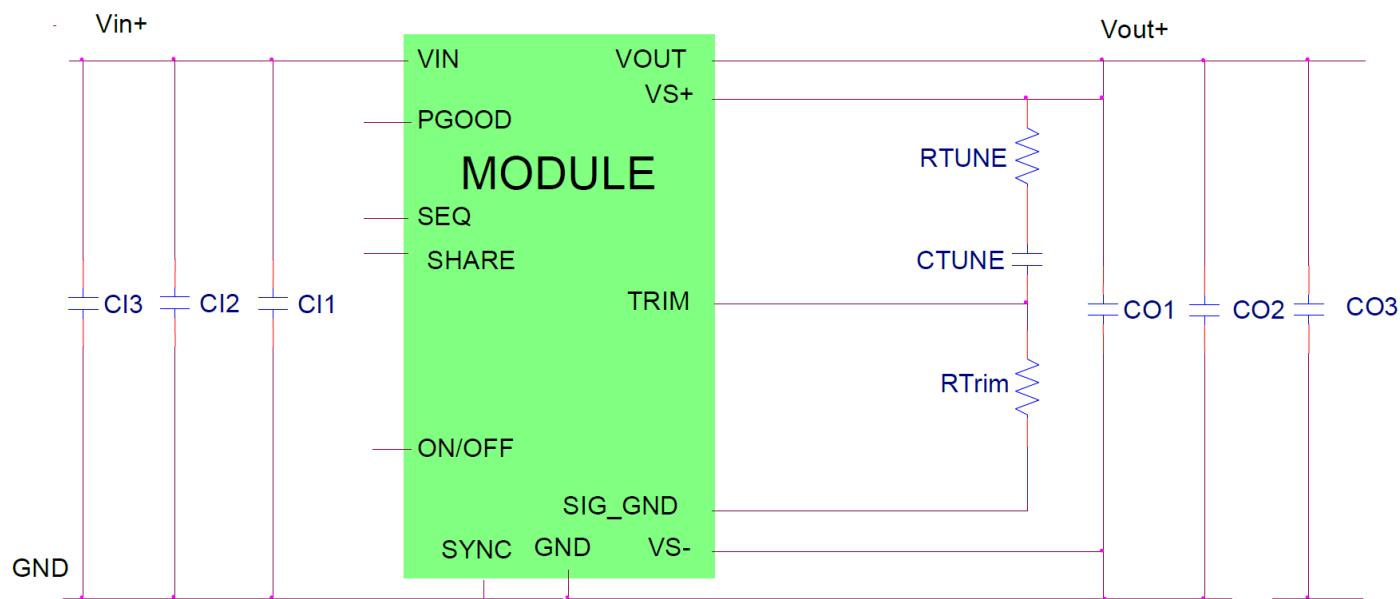
Table 5: Endurance Vibration Qualification - All Axes

## Technical Specifications (continued)

### Example Application Circuit

#### Requirements:

$V_{in}$ :	12V
$V_{out}$ :	1.8V
$I_{out}$ :	30A max., worst case load transient is from 20A to 30A
$\Delta V_{out}$ :	1.5% of $V_{out}$ (27mV) for worst case load transient
$V_{in, ripple}$ :	1.5% of $V_{in}$ (180mV <sub>p-p</sub> )



CI1 Decoupling cap - 1x0.01 $\mu$ F/16V ceramic capacitor (e.g. Murata LLL185R71E103MA01)

CI2 3x22 $\mu$ F/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20)

CI3 470 $\mu$ F/16V bulk electrolytic

CO1 Decoupling cap - 1x0.01 $\mu$ F/16V ceramic capacitor (e.g. Murata LLL185R71E103MA01)

CO2 4 x 47 $\mu$ F/6.3V ceramic capacitor (e.g. Murata GRM31CR60J476ME19)

CO3 6 X330 $\mu$ F/6.3V Polymer (e.g. Sanyo Poscap)

C<sub>Tune</sub> 5600pF ceramic capacitor (can be 1206, 0805 or 0603 size)

R<sub>Tune</sub> 220 ohms SMT resistor (can be 1206, 0805 or 0603 size)

R<sub>Trim</sub> 10k $\Omega$  SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%)

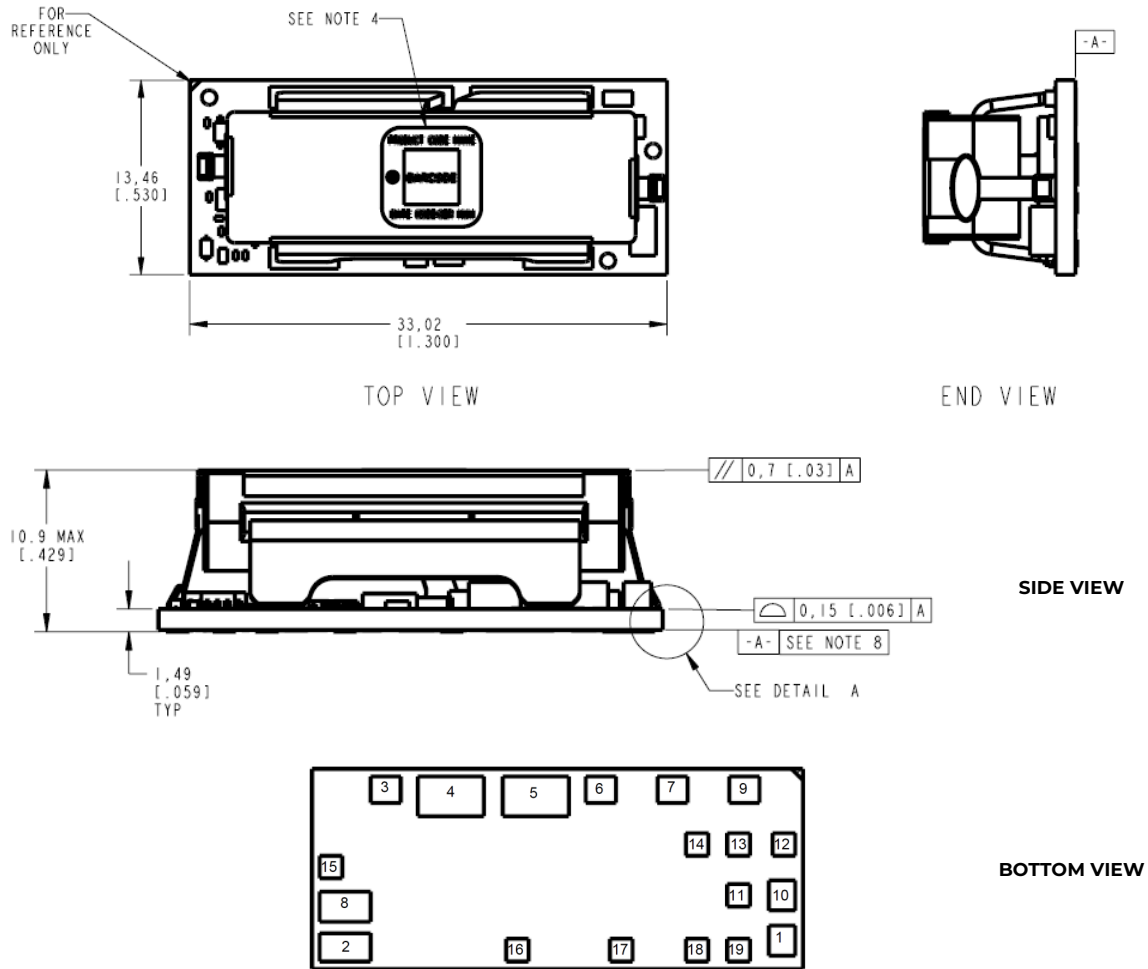
## Technical Specifications (continued)

### Mechanical Outline

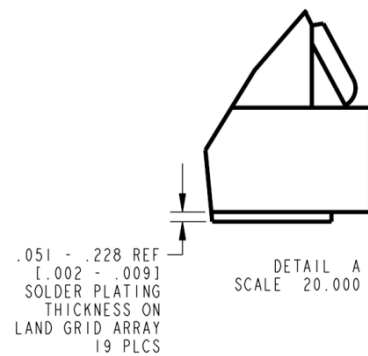
Dimensions are in millimeters and (inches).

**Tolerances:** x.x mm  $\pm 0.5$  mm (x.xx in  $\pm 0.02$  in.) [Unless otherwise indicated]

x.xx mm  $\pm 0.25$  mm (x.xxx in  $\pm 0.010$  in.)



PIN	FUNCTION	PIN	FUNCTION
1	ON/OFF	11	SIG_GND
2	V <sub>IN</sub>	12	VS-
3	SEQ	13	NC
4	GND	14	NC
5	V <sub>OUT</sub>	15	SYNC
6	TRIM	16	PG
7	VS+	17	NC
8	GND	18	NC
9	SHARE	19	NC
10	GND		

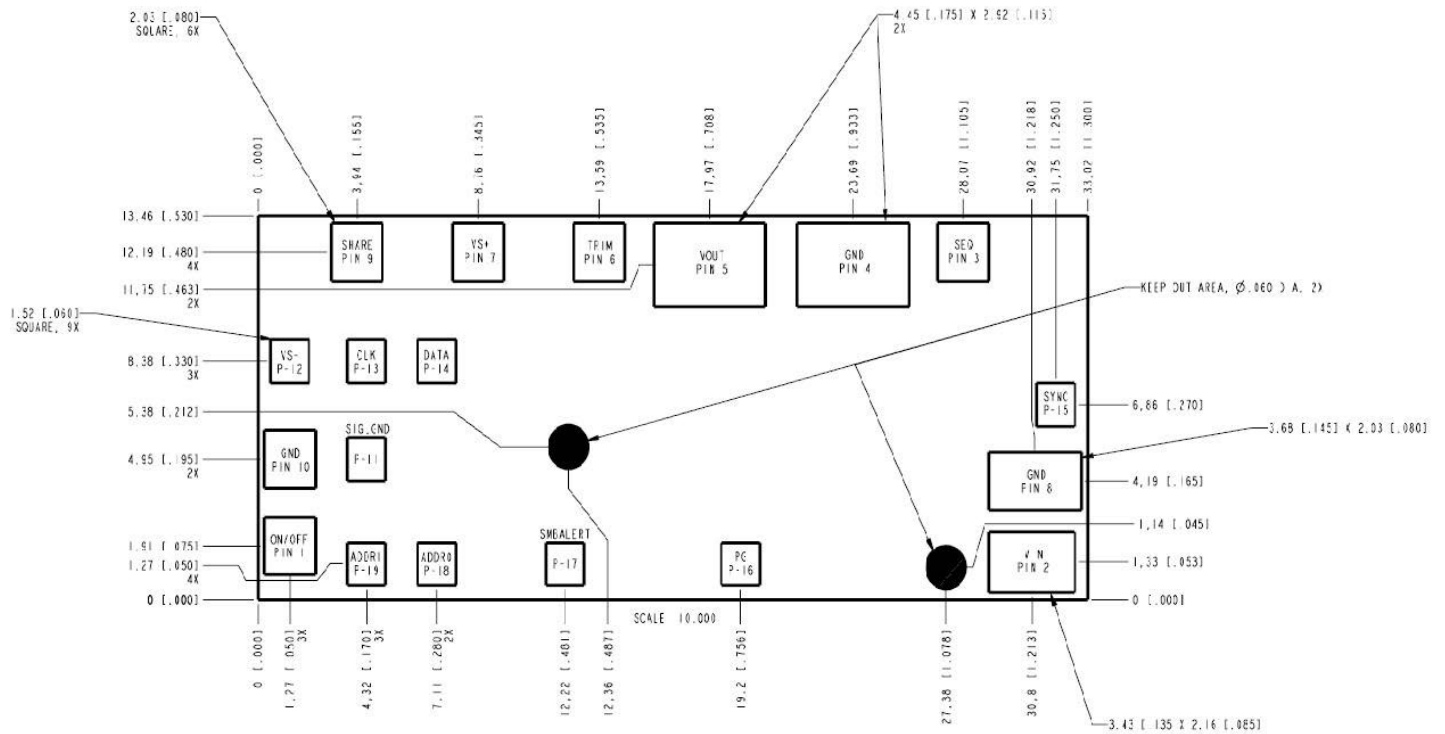


## Technical Specifications (continued)

### Recommended Pad Layout

Dimensions are in millimeters and (inches).

**Tolerances:**    x.x mm  $\pm 0.5$  mm (x.xx in  $\pm 0.02$  in.) [Unless otherwise indicated]  
                       x.xx mm  $\pm 0.25$  mm (x.xxx in  $\pm 0.010$  in.)



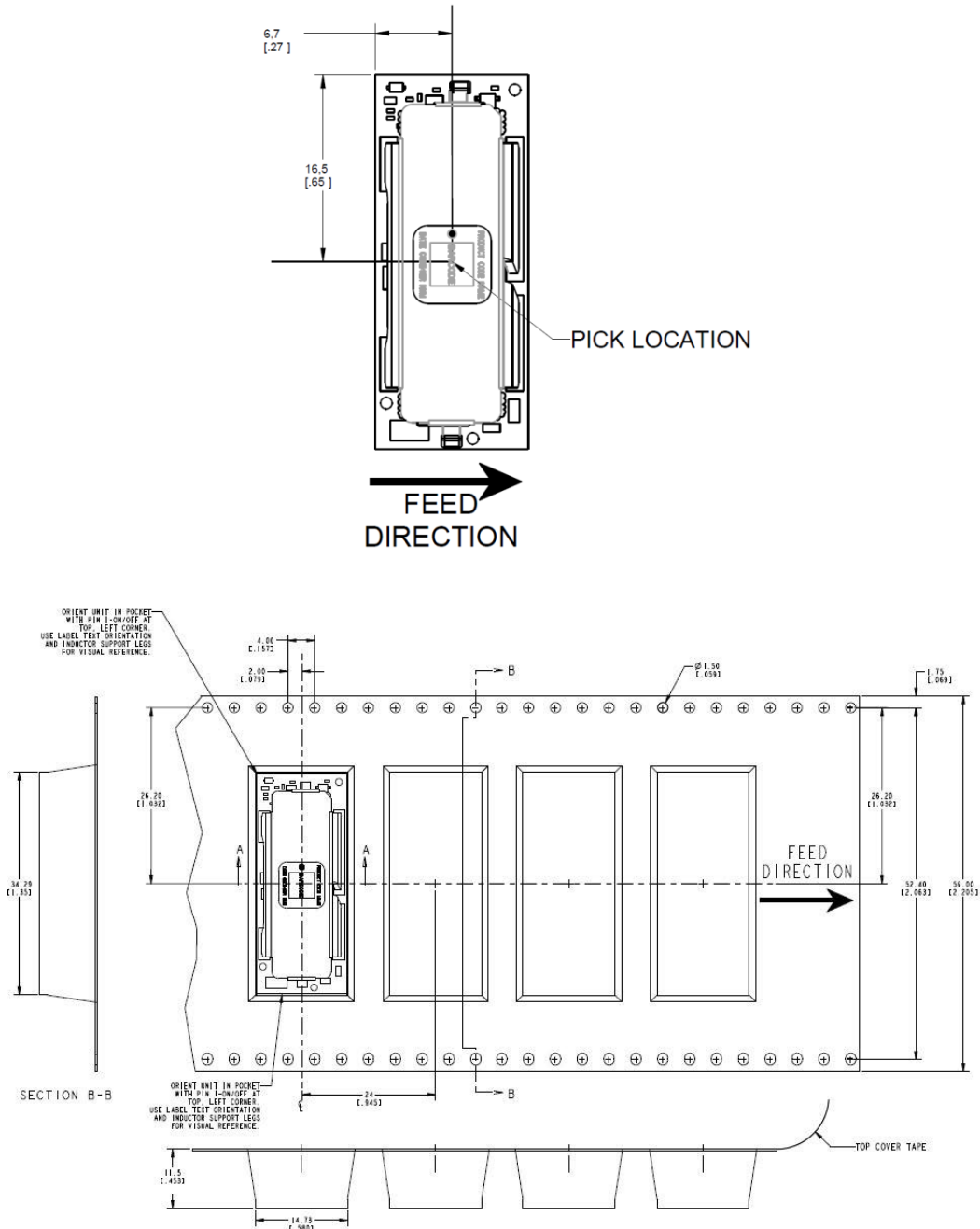
PIN	FUNCTION	PIN	FUNCTION
1	ON/OFF	11	SIG_GND
2	V <sub>IN</sub>	12	VS-
3	SEQ	13	NC
4	GND	14	NC
5	V <sub>OUT</sub>	15	SYNC
6	TRIM	16	PG
7	VS+	17	NC
8	GND	18	NC
9	SHARE	19	NC
10	GND		

## Technical Specifications (continued)

### Packaging Details

The 12V Analog Mega DLynx™ 40A modules are supplied in tape & reel as standard. Modules are shipped in quantities of 140 modules per reel.

All Dimensions are in millimeters and (in inches).



#### Reel Dimensions:

Outside Dimensions: 330.2 mm (13.00)

Inside Dimensions: 177.8 mm (7.00")

Tape Width: 56.00 mm (2.205")

## Technical Specifications (continued)

### Surface Mount Information

#### Pick and Place

The 40A Analog MegaDLynx™ modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

#### Nozzle Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

#### Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

#### Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

#### Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. C (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig. 31. Soldering outside of the recommended profile requires testing to verify results and performance.

#### MSL Rating

The 40A Analog MegaDLynx™ modules have a MSL rating of 2a.

#### Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of  $\leq 30^{\circ}\text{C}$  and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions:  $< 40^{\circ}\text{C}$ ,  $< 90\%$  relative humidity.

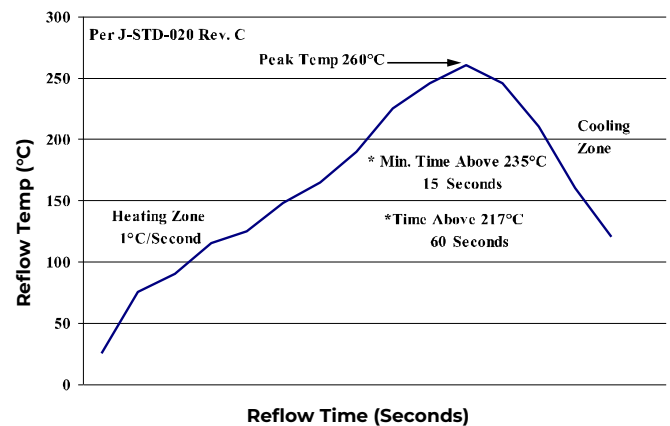


Figure 31. Recommended linear reflow profile using Sn/Ag/Cu solder.

#### Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).

## Technical Specifications (continued)

### Ordering Information

Please contact your OmniOn Sales Representative for pricing, availability and optional features.

Device Code	Input Voltage Range	Output Voltage	Output Current	On/Off Logic	Sequencing	Ordering Codes
MVT040A0X3-SRPHZ	4.5 – 14.4V <sub>dc</sub>	0.6 – 2.0V <sub>dc</sub>	40A	Negative	Yes	CC109159785
MVT040A0X43-SRPHZ	4.5 – 14.4V <sub>dc</sub>	0.6 – 2.0V <sub>dc</sub>	40A	Positive	Yes	CC109159793
MVT040A0X3-SRPHDZ	4.5 – 14.4V <sub>dc</sub>	0.6 – 2.0V <sub>dc</sub>	40A	Negative	Yes	CC150022588

**Table 6. Device Codes**

-Z refers to RoHS compliant parts

Package Identifier	Family	Input voltage range	Output current	Output voltage	On/Off logic	Remote Sense	Options				ROHS Compliance
U	D	T	040A0	X	4	3	-SR	-P	-H	-D	Z
P=Pico U=Micro M=Mega G=Giga	D= Dlynx Digital V = Dlynx Analog.	T=with EZSequence X=without sequencing	40A	X = Programmable output	4 = positive No entry = negative	3 = Remote Sense	S = Surface Mount R = Tape & Reel	Paralleling	2 Extra Ground Pins	D = 105°C operating ambient, 40G operating shock as per MIL Std. 810G,	Z = ROHS

**Table 7. Coding scheme**

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## Change History (excludes grammar & clarifications)

Revision	Date	Description of the change
1.5	03/23/2022	Updated as per template, ROHS
1.6	11/30/2023	Updated as per OmniOn template

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