DATASHEET

CP3000HV54TEZ-FSG(R) Short-form CP High Efficiency Rectifier

Input: 100-120/200-240V_{ac} OR 240/380V_{dc}; Default Output: ±54V_{dc} @3000W; 5/3.3V_{dc} @ 3A

RoHS Compliant

Description

The CP3000HV54TEZ-FSG(R) family of rectifier provides significantly higher power density in a short form factor version of the Compact Power Line of Rectifiers. The fan shall be positioned near the DC output connector in order to reduce the operating temperature around the fan. The unit is configured with dual-redundant, PMBus™ compliant I²C communications busses, positioning the product as a natural choice into high-availability, fault-tolerant, systems that operate off dual-redundant system controllers.

Applications

- 48V_{DC} distributed power architectures
- Routers/ VoIP/Soft and other Telecom Switches
- LAN/WAN/MAN applications
- File servers, Enterprise Networks, Indoor wireless
- SAN/NAS/iSCSI applications

Targeted Countries

Primary: China

Secondary: Argentina, Australia, Brazil, Canada, Chile, Dominican Republic, European Union, Guatemala, Indonesia, Israel, Japan, Laos, South Korea, Malaysia, Mexico, New Zealand, Philippines, Puerto Rico, Saudi Arabia, Singapore, Taiwan, Thailand, USA, Vietnam.

EU Countries

Features

- Efficiency meeting 80plus Titanium requirements
- Compact 1RU form factor with 42.8 W/in³ density
- Constant power down to 52V_{DC}; Constant current while output is lower than 52V_{DC}
- 3000W from nominal 200-240V_{AC} and 180-400V_{DC}
- 1500W from nominal 100 – 120V_{AC}
- Output voltage programmable from 48V – 56V_{DC}
- Standard rear to front airflow (output to input) with reverse (front to rear) airflow option
- 5000m altitude operation
- Front located connector accepts AC or HVDC Inputs
- Hardware selectable HVDC input range (ETSI mode) to compliance ETSI EN300 130-3-1
- ON/OFF control of the main output

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Features (continued)

- Comprehensive input, output and over temperature protection
- Hardware selectable 5V standby @ 3A. Defaulted to 3.3V
- PMBus™ compliant dual I²C serial bus
- Standby output, signals and I²C isolated from main output
- Precision input measurements of power consumption, voltage & current
- Remote firmware upgrade capability, Black Box Diagnostics
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- Redundant, parallel operation with active load sharing
- Internally controlled Variable-speed fan
- Hot insertion/removal (hot plug)
- Two front panel LED indicators
- UL and cUL approved to UL/CSA†62368-1, TUV (EN62368-1), CE§ Mark (for LVD) and CB Report available
- Compliant to RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863
- Compliant to REACH Directive (EC) No 1907/2006

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Technical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings shall cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods shall adversely affect the device reliability.

Parameter	Min	Max	Unit
Input Voltage-Continues - AC Operation	90	290	V_{AC}
- HVDC Operation	180	405	V_{DC}
Operating Ambient Temperature	-10	60	°C
Storage Temperature	-40	85	°C

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, V_o=54V_{DC}, resistive load, and temperature conditions.

INPUT					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Startup Voltage					
Low-line Operation				90	V_{AC}
High-line Operation				185	V_{AC}
HVDC Operation				180	V_{DC}
HVDC Operation (ETSI mode)		250		260	V_{DC}
Operating Voltage Range					
Low-line Configuration		90	100 – 120	140	V_{AC}
High-line Configuration		175	200 – 240	264	V_{AC}
HVDC Operation	V_{INAC}	180	240 – 380	400	V_{DC}
HVDC Operation (ETSI mode)		260	380V	400	V_{DC}
PSU can undergo input interactive change between HVDC and AC					
Voltage Swell (no damage)		300			V_{AC}
Turn OFF Voltage					
AC Operation				86	V_{AC}
HVDC Operation				178	V_{DC}
HVDC Operation (ETSI mode)		247		255	V_{DC}
Hysteresis		5			
Input Over Voltage Protection, OVP, Turn Off Threshold					
AC Operation		285		310	V_{AC}
HVDC Operation		401		421	V_{DC}
HVDC Operation (ETSI mode)		401		421	V_{DC}
Frequency	F_{IN}	47		63	Hz
Operating Current			16.3		
100V_{AC}			14.7		A_{AC}
110V_{AC}			16.7		
200V_{AC}					
240V_{AC}	I_{INAC}		13.9		
180V_{dc}			17.9		A_{DC}
400V_{dc}			7.8		
260Vdc (ETSI mode)			12.1		
Inrush Transient (excluding X-Capacitor) 110V/63Hz/25°C				40	
x-cap impact < 0.1ms. < 75A 230V/50Hz/25°C	I_{INAC}		25	40	A_{PK}
264V/47Hz/60°C				60	
400V_{dc} or 290V_{ac}/55°C				75	
Idle Power	P_{INAC}		9		W

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Technical Specifications (continued)

Electrical Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
(at 240V_{AC}, 25°C) 54V OFF			18		
54V ON @ I_o=0			9/7		
(at 240V_{DC}/380V_{DC}, 25°C) 54V OFF			15/13		
54V ON @ I_o=0					
Leakage Current (300V_{AC}, 60Hz)	I_{INAC}		2.5	3.5	mA
Power Factor (50 – 100% load)	PF	0.98	0.995		
Efficiency, 230VAC @ 25°C (fan driven externally, 5Vaux @ FL)	η	80+ Titanium (except FL)			
At full load (without fan consumption)		94			%
Efficiency, 380V_{DC} @ 25°C, 54V FL, 5Vaux @ FL, At full load (with fan consumption)	η	94	95		%
Holdup time (output ≥ 42V_{DC} @ 54V_{DC} setpoint)220V/50Hz/3000W	T	12			ms
110V/60Hz/1500W		12			ms
Holdup time (output ≥ 42V_{DC} @ 54V_{DC} setpoint) 380V_{DC}/3000W		12			ms
Ride through (at 240V_{AC}, 25°C)	T	1/2	1		cycle
PG# Potential loss of output power[1] (output may decay to 40V_{DC})	PG	3	5		ms
Isolation (per EN62368-1)(consult factory for testing to this requirement) Input-Chassis/Signals	V	1500			V_{AC}
Input – Output		3000			V_{AC}
Output - Chassis		500			V_{DC}

54V_{DC} MAIN OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Output Power Low line input 100 – 175V_{AC}	W	1500			W_{DC}
Brownout input 175 - 200 V_{AC}		2400			
High line input 200 – 264V_{AC}		3000			
HVDC input 180 – 400V_{DC}		3000			
HVDC input 260 – 400V_{DC} (ETSI mode)		3000			
Factory set default set point	V_{OUT}	53.73	54	54.27	V_{DC}
Overall regulation (load, temperature, aging)		-1		+1	%
0 - 45°C LOAD > 2.5A					
> 45°C		-2		+2	
Output Voltage Set Range		48		56	V_{DC}
Output Current -@ 1500W (100 – 120V_{ac}), 54V	I_{Out}			27.8	A_{DC}
@2400W (200 – 240V_{AC}, or HVDC Input) 54V				44.4	
@3000W (200 – 240V_{AC}, or HVDC Input) 54V				55.6	
52~48V				57.7	
Current Share (> 50% FL)		-5		5	%FL
Output Ripple (20MHz bandwidth, load > 1A)RMS (5Hz to 20MHz)	V_{OUT}			100	mV_{rms}
Measured across 10µF electrolytic, 0.1µF ceramic P-P (5Hz to 20MHz)				500	mV_{p-p}
External Bulk Load Capacitance, 54V	C_{OUT}	0		10,000	µF
Turn-On (monotonic 5°C) Delay	T		5		S
Rise Time (from 30-100% of V_{OUT})			100		ms
Output Overshoot	V_{OUT}			2	%
Load Step Response (di/dt =1A/µs $I_{O,START}$ > 2A) ΔI	I_{OUT}			50	%FL
ΔV	V_{OUT}	-3		3	%
ΔI	I_{OUT}			100	%FL
ΔV	V_{OUT}	-5		5	%
Response time	T		4		ms

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Technical Specifications (continued)

Electrical Specifications (continued)

$54V_{DC}$ MAIN OUTPUT					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Overload - Power limit @ high line down to $52V_{DC}$	P_{OUT}		3100		W_{DC}
Power limit @ low line down to $52V_{DC}$	P_{OUT}		1620		W_{DC}
V_{IN} > $175V_{AC}$ or HVDC operation current limit	I_{OUT}		64.5		A_{DC}
90VAC < VIN < 175VAC current limit	I_{OUT}		34		A_{DC}
Hysteresis between ranges	I_{OUT}	5			V_{DC}
Output shutdown	V_{OUT}		44		V_{DC}
System power up	Upon insertion delays shutdown for 20 sec to allow startup				
Overvoltage - Immediate Latched shutdown	V_{OUT}			< 62	V_{DC}
Over-temperature warning (prior to commencement of shutdown)	T		5		°C
Shutdown (below the max device rating being protected)	T		20		°C
Restart attempt Hysteresis (below shutdown level)	T		10		°C
PG# – Power good - normal (Logic HI)	V_{OUT}	40	54	60	V_{DC}
- Asserted[2] (Logic-LO)	V_{OUT}			36	V_{DC}
PG# – Power good - normal (Logic HI) – V_{OUT} within normal regulation	V_{OUT}	-1		1	%
- Asserted[3] (Logic-LO) prior to V_{OUT} < $40V_{DC}$	Time		5-15		ms

$3.3/5V_{DC}$ Auxiliary output[3]					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage Setpoint (configurable by firmware)	V_{OUT}		3.3/5		V_{DC}
Overall Regulation		-5		+5	%
Output Current		0.005		3	A
Captative Load	C_{OUT}			470	µF
Ripple and Noise 20mHz bandwidth	V_{OUT}			200	mV_{p-p}
Ripple and Noise Full bandwidth	V_{OUT}			400	mV_{p-p}
Over-voltage Clamp				7	V_{DC}
Over-current Limit		110		140	%FL

General Specifications

Parameter	**Min**	**Typ**	**Max**	**Units**	**Notes**
Reliability		450,000		Hours	Full load, 25°C ; MTBF per SR232 Reliability protection forelectronic equipment, issue 2, method I, case III,
Service Life		10		Years	Full load, 35°C max ambient, excluding fans
Unpacked Weight		1.92/4.23		Kgs/Lbs	
Packed Weight		2.45/5.4		Kgs/Lbs	

Feature Specifications

Unless otherwise indicated, specifications shall apply overall operating input voltage, resistive load, and temperature conditions. Signals are referenced to LGND unless noted otherwise. Fault, PG#, OTW, and Alert need to be pulled HI through external pull-up resistors. Sink current 5mA

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Technical Specifications (continued)

Feature Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
ON/OFF 54V output OFF	V_{OUT}	1.4	—	5	V_{DC}
54V output ON (should be connected to GND)	V_{OUT}	0	—	0.5	V_{DC}
V_{prog} Margining		48		56	V_{DC}
Voltage control range	$V_{control}$	0		3.3	V_{DC}
Programmed output voltage range	V_{OUT}	48		56	V_{DC}
Voltage adjustment resolution (8-bit A/D)	$V_{control}$		3.3		mV_{DC}
Output configured to $54V_{DC}$	$V_{control}$	3.0		3.3	V_{DC}
Output configured to $48V_{DC}$	$V_{control}$	0		0.1	V_{DC}
Interlock [short pin shorted to V_{OUT}(-) on system side]					
54V output OFF	$V_{control}$	$0.7V_{p-p}$	—	V_{DD}	V_{DC}
54V output ON	$V_{control}$	0	—	0.8	V_{DC}
Module Present [short pin to LGND internally]					
OTW# (Over Temperature Warning) open collector Logic HI- warning	V	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO - normal	V	0	—	0.4	V_{DC}
Fault# open collector Logic HI – normal is present	V	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO - asserted	V	0	—	0.4	V_{DC}
SCL_0, SDA_0, SCL_1, SDA_1 open collector Logic HI - normal	V	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO – pull-down see communications spec	V	0	—	0.3	V_{DC}
Alert# (Alert#_0, Alert#_1) open collector Logic HI - normal	V	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO - asserted	V	0	—	0.4	V_{DC}
PG# Logic HI - open collector normal, output may lose power	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO – asserted	V_{IL}	0	—	0.4	V_{DC}
Aux_set pulled up via 10kΩ to V_{DD} Logic HI - 3.3V output	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO – 5V output	V_{IL}	0	—	0.4	V_{DC}
A2, A1, A0 pulled up via 10kΩ to V_{DD} Logic HI (1) - no connect	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO (0), connected to LGND	V_{IL}	0	—	0.4	V_{DC}
ETSI_set pulled up via 10kΩ to VDD Logic HI (1) - 180~400V_{DC} input	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V_{DC}
Logic LO- ETSI mode: 260~400V_{DC} input	V_{IL}	0	—	0.4	V_{DC}

Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics[4]						
Input Logic High Voltage (CLK, DATA)		V	1.5		3.6	V_{DC}
Input Logic Low Voltage (CLK, DATA)		V	0		0.8	V_{DC}
Input high sourced current (CLK, DATA)		I	0		10	µA
Output Low sink Voltage (CLK, DATA, ALERT#)	I_{OUT}=3.5mA	V			0.4	V_{DC}
Output Low sink current (CLK, DATA, ALERT#)		I	3.5			mA
Output High open drain leakage current (CLK,DATA,ALERT#)	V_{OUT}=3.6V	I	0		10	µA
PMBus Operating frequency range	Slave Mode	FPMB	10		400	kHz

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Technical Specifications (continued)

Digital Interface Specifications (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Measurement System Characteristics						
Clock stretching		$T_{stretch}$			25	ms
I_{OUT} measurement range		I_{rng}	0		80	A_{DC}
I_{OUT} measurement accuracy 25°C		$I_{out(acc)}$	-1.5		+1.5	A_{DC}
I_{OUT} measurement accuracy 0 - 40°C[5]	> 12.8A	$I_{out(acc)}$	-2		+2	% of FL
V_{OUT} measurement range		$V_{out(rng)}$	0		70	V_{DC}
V_{OUT} measurement accuracy[6]		$V_{out(acc)}$	-0.5		+0.5	V_{DC}
Temp measurement range		$T_{emp(rng)}$	0		150	°C
Temp measurement accuracy[7]		$T_{emp(acc)}$	-4		+4	°C
V_{IN} measurement range, AC Input		$V_{in(rng)}$	0		320	V_{AC}
V_{IN} measurement range, HVDC Input		$V_{in(rng)}$	0		410	V_{DC}
V_{IN} measurement accuracy @ 25°C		$V_{in(acc)}$	-4		+4	V_{AC}
I_{IN} measurement range, AC Input		$I_{in(rng)}$	0		30	I_{AC}
I_{IN} measurement range, HVDC Input		$I_{in(rng)}$	0		30	I_{DC}
I_{IN} measurement accuracy - standard measurement @ 25°C		$I_{in(acc)}$	-5		+5	% of FL
P_{IN} measurement range		$P_{in(rng)}$	0		4000	W_{in}
P_{IN} measurement accuracy standard measurement @ 25°C	> 300W < 300W	$P_{in(acc)}$	-5	 50	+5 100	% W
Fan Speed measurement range			0		30k	RPM
Fan Speed measurement accuracy			-10		10	%
Fan speed control range			0		100	%

Environmental Specifications

Parameter	Min	Typ	Max	Units	Notes
Ambient Temperature	-10[8]		50	°C	Air inlet from sea level to 5,000 feet.
Exhaust Air Temperature			25	°C	Maximum allowed internal temperature rise
Storage Temperature	40		85	°C	
Non-operating Altitude			8200/30k	m / ft	
Power Derating with Temperature [9]			2.0	%/°C	50°C to 60°C
Power Derating with Altitude			2.0	C/1000 ft	Above 5000/1524 ft/m to 13000/3962 ft/m
Acoustic noise		55		dbA	Full load
Over Temperature Protection		125/110		°C	Shutdown / restart [internally measured points]
Humidity Operating Storage	5 5		95 95	% %	 Relative humidity, non-condensing
Shock and Vibration acceleration			2.4	Grms	IPC-9592B, Class II

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Technical Specifications (continued)

Environmental Specifications (continued)

EMC				
Parameter	**Criteria**	**Standard**	**Level**	**Test**
AC input/DC input[10]	Conducted emissions	EN55032, FCC Docket 20780 part 15, subpart J Meets EN61000-3-2	A +6dB	0.15 – 30MHz 0 – 2 KHz
	Radiated emissions	EN55032	A +6dB	30 – 10000MHz
Input Immunity (AC and DC)	Line sags and interruptions	EN61000-4-11	B	-30%, 10ms
			B	-60%, 100ms
			B	-100%, 5sec
		Output will stay above 40V_{DC} @ 75% load Sag must be higher than 80V_{rms}.	A	25% line sag for 2 seconds
				1 cycle interruption
	Lightning surge	EN61000-4-5, Level 4, 1.2/50µs – error free	A	4kV, com mode, 2kV diff mode. *cover ETSI EN 300-132-3-1 about 2KV CM/DM surge requirement on 380V_{DC} rated
		ANSI C62.41 - level A3	B	6kV, common & differential
	Fast transients	EN61000-4-4, Level 3	B	5/50ns, 2kV (common mode)
Input Immunity (Ut=380V_{DC} rated)	Voltage variation	ETSI EN 300-132-3-1	A	From Ut to 260V, back to Ut, duration 1 min.
			A	From Ut to 400V, back to Ut, duration 1 min.
			B	From Ut to 410V, back to Ut, duration 1 s.
			B	From Ut to 420V, back to Ut, duration 10ms.
	Voltage dips[11]		A	From Ut to 260V, back to Ut, duration 10ms.
	Voltage interruption		A	From Ut to 0V, back to Ut, duration 10ms. low impedance
			B	From Ut to 0V, back to Ut, duration 1s. High impedance
Enclosure immunity	Conducted RF fields	EN61000-4-6, Level 3	A	130dBµV, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3, Level 3	A	10V/m, 80-1000MHz, 80% AM
		ENV 50140	A	
	ESD	EN61000-4-2, Level 4	B	8kV contact, 15kV air

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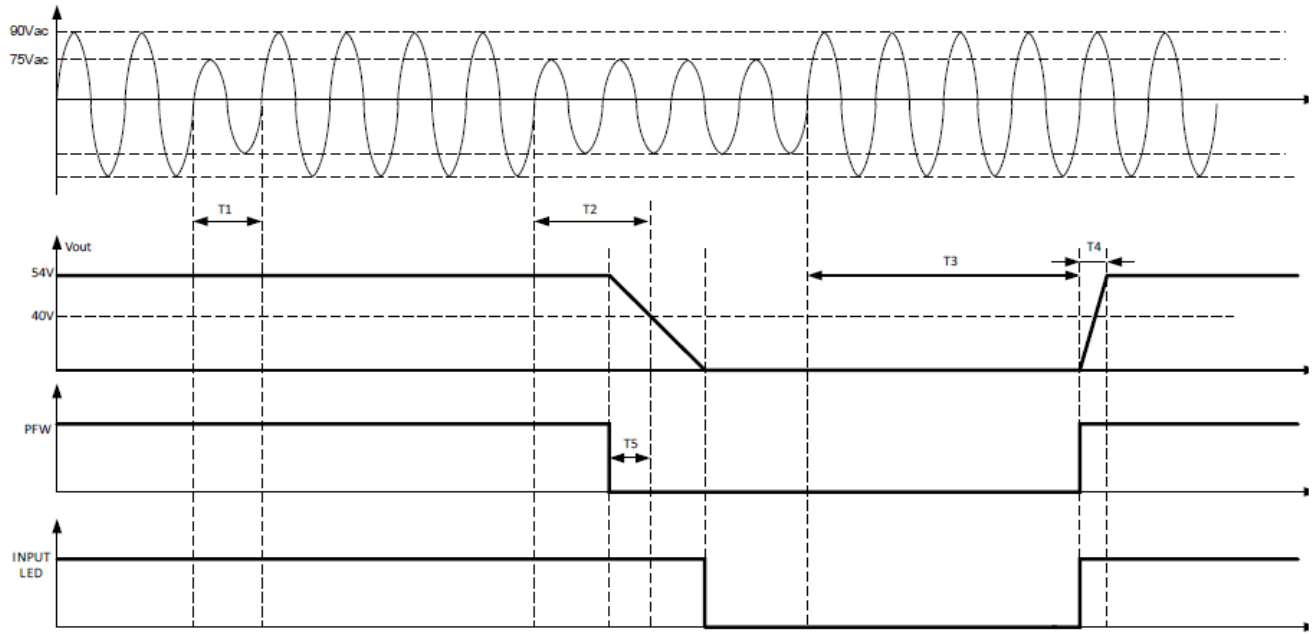
Timing diagrams

Response to AC input fluctuations



T1 – ride through time
T2 – hold up time
T3 – delay time
T4 – rise time
T5 – power fail warning
INPUT LED

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Technical Specifications (continued)

Control and Status

The Rectifier shall provide two means for monitor/control: analog or PMBus™. Details of analog control and the PMBus™ based protocol are provided in this data sheet.

Control hierarchy: Some features, such as output voltage, shall be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (V_{prog}) and a PMBus command, (OPERATION) .

Unless otherwise noted, the signal pin controls the feature until the firmware command is executed. However, once the firmware command has been executed, the signal pin is ignored. In the above example, the rectifier will no longer 'listen' to the V_{prog} pin if the OPERATION command has been executed.

In summary, V_{prog} is utilized for initialized configuration of the output voltage and to change the output voltage when PMBus is not used for that function.

Signal Reference: Unless otherwise noted, all signals are referenced to Logic_GND. See the Signal Definitions Table at the end of this document for further description of all the signals.

Logic_GND is isolated from the main output of the rectifier for PMBus communications. Communications and the 5V/3.3V standby output are not connected to main power return (V_{out} (-)) and shall be tied to the system digital ground point selected by the user.

Logic_GND is capacitively coupled to Chassis_GND inside the rectifier. The maximum voltage differential between Logic_GND and Chassis_GND should be less than $100V_{DC}$.

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > $10V_{DC}$ the Output LED will continue blinking. When output voltage is < $10V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Auto restart: Auto-restart is the default configuration for over- current and over-temperature shutdowns. These features are configured by the PMBus™ fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Restart after a latchoff: PMBus™ fault_response commands shall be configured to direct the rectifier to remain latched off for over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin ON/OFF may be cycled OFF/ON.
2. The unit may be commanded to restart via i^2c cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON input power
5. Changing firmware from latch off to restart.

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to restart.

A successful restart shall clear all alarm registers, set the restarted successful bit of the Status_2 register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers.

Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

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Technical Specifications (continued)

Control and Status (continued)

A synchronous restart shall be implemented by;

1. Issuing a GLOBAL OFF and then ON command
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Control Signals

Device address in I²C mode: Address bits A2, A1, A0 set the specific address of the µP in the rectifier. With these four bits, up to eight (8) rectifiers shall be independently addressed on a single I²C bus. The least significant bit x (LSB) of the address byte is set to either write [0] or read [1]. A write command instructs the rectifier. A read command accesses information from the rectifier.

Device	Address	Address Bit Assignments (Most to Least Significant)							
		7	6	5	4	3	2	1	0
µP	40 – 47	1	0	0	0	A2	A1	A0	R/W
Broadcast	00	0	0	0	0	0	0	0	0
		MSB							LSB

Global Broadcast: This is a powerful command because it instruct all rectifiers to respond simultaneously. A read instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command shall also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth acknowledge bit. To be certain that each rectifier responded to the global instruction, a READ instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Voltage programming (V_{prog}): Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Software voltage programming permanently overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is recycled.

An analog voltage on this signal shall vary the output voltage from $48V_{dc}$ to $56V_{dc}$.

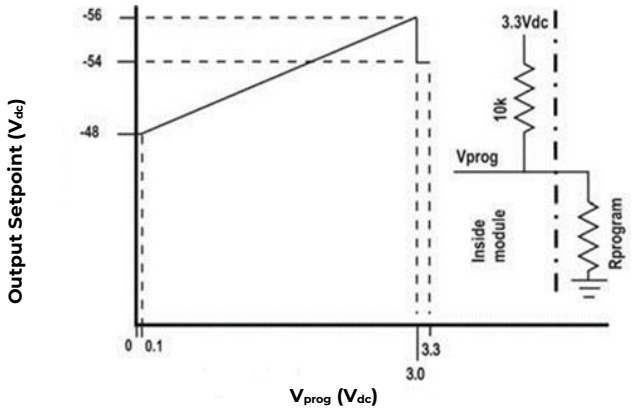

Diagram showing the V_{prog} adjustment.

The V_{prog} pin level should be set by connecting a resistor from the V_{prog} pin to Logic_GND external to the rectifier as shown in the diagram. Programming shall be accomplished either by a resistor as described or by a voltage source injecting a precision voltage level into the V_{prog} pin. Above $3V_{dc}$ the rectifier sets the output to its default state.

Hardware voltage programming controls the output voltage until a software margin command is executed. Software voltage programming (margining) permanently overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is recycled.

When bias power is recycled to the controller the controller restarts into its default configuration, programmed to set the output as instructed by the V_{prog} pin. Again, subsequent software commanded settings permanently override the margin setting. As an example, adding a resistor between V_{prog} and Logic_GND is an effective way of changing the factory set point of the rectifier to whatever voltage level is desired by the user during initial start-up.

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Technical Specifications (continued)

Control Signals (continued)

Load share (Ishare): The power supply compares its internal sourced current to the current requested by the current share pin. If the difference is > 10A, a fault is issued.

ON/OFF: Shall controls the main $54V_{DC}$ output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn ON the rectifier. The rectifier will turn OFF if either the ON/OFF or the Interlock pin is released. This signal is referenced to Logic_GND.

Interlock: This is a shorter pin that shall be utilized for hot-plug applications to ensure that the rectifier turns OFF before the power pins are disengaged. It also ensures that the rectifier turns ON only after the power pins have been engaged. Must be connected to V_OUT (-) for the rectifier to be ON.

Module Present: This signal shall be tied to Logic_GND inside the rectifier. It's intent is to provide a signal to the system that a rectifier is physically present in the slot.

8V_INT: Single wire connection between rectifiers, Provides bias to the secondary processor of an unpowered rectifier.

ETSI_SET: This signal is used to set HVDC input range. Open is set unit to operate with $180\sim400V_{DC}$ rated range; Tied to LGND is set unit to operate with $260\sim400V_{DC}$ rated range to compliance ETSI EN300 -132-3-1. This signal configuration has no effect on AC input operation.

Status Signals

PG# – Power good: This signal is HI when the main output is within regulation and goes LO for the duration listed in this data sheet prior to the output decaying below the listed voltage level.

Fault#: A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires rectifier replacement. These faults may be due to:

- Fan failure
- Over-temperature shutdown
- Over-voltage shutdown
- Internal Rectifier Fault

Over temp warning (OTW#): A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor. If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the rectifier. In its default configuration, the unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

Alert#: A TTL compatible status signal, This signal needs to be pulled HI externally through a resistor.

Power_CAP: This signal is HI when the main output is 3000w and goes LO when the main output is 1400w.

Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus.

All signals are referenced to 'Logic_GND'.

Pull-up resistors: The clock, data, and Alert# lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I²C and SMBus standards.

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Serial Data (SDA): This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Digital Feature Descriptions

PMBus™ compliance: The rectifier is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification shall be obtained from **omnionpower.com**'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

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Digital Feature Descriptions (continued)

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

The Alert# response protocol (ARA) where by the PMBus Master shall inquire who activated the Alert# signal is also supported. This feature is described in more detail later on. Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored shall be saved. (see the Table of Commands for which command parameters shall be saved to non-volatile storage).

Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing an Alert# to the 'host' controller.

If a non-supported read is requested the rectifier will return 0x00h for data.

Data out-of-range: The rectifier validates data settings and sets the data out-of-range bit and Alert# if the data is not within acceptable range.

Master/Slave: The 'host controller' is always the MASTER. Rectifiers are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The 'slave' µController inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier.

Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.

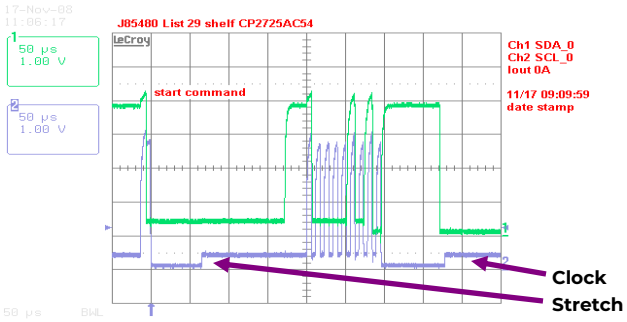

Figure 15. Example waveforms showing clock stretching

I²C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The rectifiers default to the 100kHz clock rate.

Packet Error Checking (PEC): The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the desired command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

Alert#: The rectifier shall issue Alert# driven from either its internal micro controller (µC) or from the I²C bus master selector stage. That is, the Alert# signal of the internal µC funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the rectifier. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The µC driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the rectifier has changed states and the signal will be latched LO until the rectifier receives a 'clear_faults' instruction.

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Technical Specifications (continued)

Digital Feature Descriptions (continued)

The signal will be triggered for any state change, including the following conditions;

- V_{IN} under or over voltage
- V_{out} under or over voltage
- I_{OUT} over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults

Alert#_0 ,the defaulted I²C side in control, is asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled.

The rectifier will re-assert the Alert line if the internal state of the power supply has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the power supply. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

Re-initialization: The I²C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I2C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I²C µController may not recognize a command sent to it.
(i.e. a start condition).

Read back delay: The rectifier issues the Alert# notification as soon as the first state change occurred. During an event a number of different states shall be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the rectifier. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

Successive read backs: Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Global Broadcast: This is a powerful command because it instruct all rectifiers to respond simultaneously. A read instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command shall also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth acknowledge bit. To be certain that each rectifier responded to the global instruction, a READ instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Dual, redundant buses: Two independent I²C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the rectifier. For example, a short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' shall take over control at any time.

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Technical Specifications (continued)

Digital Feature Descriptions (continued)

Conceptually, a Digital Signal Processor (DSP) referenced to $V_{out}(-)$ of the rectifier provides secondary control. A Bidirectional Isolator provides the required isolation between power GND, $V_{out}(-)$ and signal GND (Logic_GND). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I²C lines to two independent system controllers.

The secondary micro controller is designed to default to I²C_0 when powered up. If only a single system controller is utilized, it should be connected to I²C_0. In this case the I²C_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I²C_0 and the other to I²C_1.

At power up the master connected to I²C_0 has control of the bus. See the section on Dual Master Control for further description of this feature.

PMBus™ Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

☐ Master to Slave ▭ Slave to Master

SMBUS annotations;

S – Start , Wr – Write, Sr – re-Start, Rd – Read, Acknowledge, NA – not-acknowledged, P – Stop

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	LSB	A

8	1	8	1	1
MSB	A	PEC	NA	P

Block communications: When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

8	1	8	1	8	1
Byte count = N	A	Data 1	A	Data 2	A

8	1	8	1	8	1	1
.....	A	Data N	A	PEC	A	P

Block read format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte count = N	A	Data 1	A	Data 2	A

8	1	8	1	8	1	1
.....	A	Data N	A	PEC	NA	P

Linear Data Format: The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

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Technical Specifications (continued)

PMBus™ Commands (continued)

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)					Mantissa (M)										

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$V = M * 2^E$

Where: V is the value, M is the 11-bit, two's complement mantissa, E is the 5-bit, two's complement exponent

Standard features

Supported features that are not readable: The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both the CNTL pin, and the OPERATION command, enabling or disabling the output, are supported. Other options are not supported.

Command	Comments
Capability (0x19)	400KHz, ALERT#
PMBus revision (0x98)	1.2

Status and Alarm registers: The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear_faults command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault still persists after the clear_faults is commanded, the register bit annunciating the fault is reset again.

Command	Hex Code	Data Field	Non-Volatile Memory Storage[12] / Default
Operation	0x01	1	Yes/80
Clear_Faults	0x03	0	
Write _Protect	0x10	1	Yes/00
Restore_default_all	0x12	0	
Restore_user_all	0x16	x	
Store_user_code	0x17	1	yes
Restore_user_code	0x18	1	
Vout_mode	0x20	1	
Vout_command	0x21	2	yes
Vin_ON	0x35	2	
Vin_OFF	0x36	2	
Fan_config_1_2	0x3A	1	Yes / 90
Fan_command_1	0x3B	2	
Vout_OV_fault_limit	0x40	2	Yes / 59
Vout_OV_fault_response	0x41	1	No / 80
Vout_OV_warn_limit	0x42	2	Yes / 58.5
Vout_UV_warn_limit	0x43	2	Yes / 45
Vout_UV_fault_limit	0x44	2	Yes / 44
Vout_UV_fault_response	0x45	1	No / C0
Iout_OC_fault_limit	0x46	2	Yes / 59.2
Iout_OC_fault_response[13]	0x47	1	Yes / F8
Iout_OC_LV_fault_limit	0x48	2	Yes/ 36
Iout_OC_warn_limit	0x4A	2	Yes / 57.7
OT_fault_limit	0x4F	2	Yes/120
OT_fault_response[14]	0x50	1	Yes / C0
OT_warn_limit	0x51	2	Yes/115
Vin_OV_fault_limit	0x55	2	No/ 300
Vin_OV_fault_response	0x56	1	No/ C0
Vin_OV_warn_limit	0x57	2	Yes / 295
Vin_UV_warn_limit	0x58	2	Yes / 87.5
Vin_UV_fault_limit	0x59	2	Yes / 80
Vin_UV_fault_response	0x5A	1	No/ C0
Status_byte	0x78	1	
Status_word (+ byte)	0x79	1	
Status_Vout	0x7A	1	
Status_Iout	0x7B	1	
Status_Input	0x7C	1	
Status_temperature	0x7D	1	
Status_CML	0x7E	1	
Status_fans_1_2	0x81	1	
Read_Vin	0x88	2	
Read_Iin	0x89	2	
Read_Vout	0x8B	2	
Read_Iout	0x8C	2	
Read_temp_PFC	0XBD	2	

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Technical Specifications (continued)

PMBus™ Commands (continued)

PMBus™ Command set: (continued)

Command	Hex Code	Data Field	Non-Volatile Memory Storage[15]/ Default
Read_temp_dc_pri	0x8E	2	
Read_temp_dc_sec	0x8F	2	
Read_fan_speed_1	0x90	2	
Read_fan_speed_2	0x91	2	
Read_Pin	0x97	2	
Mfr_ID	0x99	6	
Mfr_model	0x9A	16	
Mfr_revision	0x9B	8	
Mfr_serial	0x9E	16	
Status_summary	0xD0	12	
Status_unit	0xD1	2	
Status_alarm	0xD2	4	
Read_fan_speed	0XD3	7	
Read_input	0xD4	5	
Read_firmware_rev	0xD5	7	
Read_run_timer	0xD6	4	
Status_bus	0xD7	1	
Take_over_bus_control	0xD8		yes
EEPROM Record	0xD9	64	yes
Read_temp_exhaust	0xDA	2	
Read_ temp_inlet	0xDB	2	
Reserved for factory use	0XDC		
Reserved for factory use	0XDD		
Reserved for factory use	0XDE		
Test_Function	0xDF	1	
Upgrade commands			
Password	0xE0	4	
Target_list	0xE1	4	
Compatibility_code	0xE2	16	
Software_version	0xE3	7	
Memory_capability	0xE4	7	
Application_status	0xE5	1	
Boot_loader	0xE6	1	
Data_transfer	0xE7	≤32	
Product comcode	0xE8	11	
Upload_black_box	0xF0	≤32	

Command Descriptions

Operation (0x01) : Turns the 54V output ON or OFF. The default state is ON at power up. Only the following data bytes are supported:

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To RESET the rectifier using this command, command the rectifier OFF, wait at least 2 seconds, and then command the rectifier back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (0x03): Clears all STATUS and FAULT registers and resets the Alert# line of the I²C side in control. The I²C side not in control cannot clear registers in the power supply. This command is always executable.

If a fault still persists after the issuance of the clear_faults command, the specific registers indicating the fault are reset and, the Alert# line is activated again.

WRITE_PROTECT register (0x10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store_user_code command. The default setting of this register is enable_all_writes, write_protect 0x00h. The write_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

Restore_Default_All (0x12): Restores all operating register values and responses to the factory default parameters set in the rectifier. The factory default cannot be changed.

Restore_user_all (0x16): Restores all operating register values and responses to the user default parameters set in the rectifier. The user default can be changed.

Store_user_code (0x17): Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

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Technical Specifications (continued)

Command Descriptions (continued)

Restore_user_code (0x18): Restores the user default setting of a single register.

Vout_mode (0x20): This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data intwo's complement binary format for output voltage related commands, such as Vout_command. These commands have a 16 bit mantissa. The exponent is fixed by the rectifier and is returned by this command

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	xxxxxb

Vout_Command (0x21) : Used to dynamically change the output voltage of the rectifier. This command shall also be used to change the factory programmed default set point of the rectifier by executing a store-user instruction that changes the user default firmware set point.

The default set point shall be overridden by the V_{prog} signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all rectifiers using the Global Address (Broadcast) feature. If only a single rectifier is instructed to change its output, it may attempt to source all the required power which shall cause either a power limit or shutdown condition.

Software programming of output voltage permanently overrides the set point voltage configured by the V_{prog} signal pin. The program no longer looks at the 'V_{prog} pin' and will not respond to any hardware voltage settings. If power is removed from the µController it will reset itself into its default configuration looking at the V_{prog} signal for output voltage control. In many applications, the V_{prog} pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once I^2C communications are established.

To properly hot-plug a rectifier into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the V_{prog} pin. Otherwise, the voltage state of the plugged in rectifier could be significantly different than the powered system.

Programmed voltage range: $48V_{DC}$ – 56 V_{DC}.

A voltage programming example: The task: set the output voltage to $50.45V_{DC}$

The constants for voltage programming are:
m = 400, b and R =0.Multiply the desired set point by the m constant, 50.45 x 400= 20,180. Convert this binary number to its hex equivalent:
20,180b = 4ED4h. Transmit the data LSB first, followed by MSB, 0 x D44Eh.

Vin_ON (0x35): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns ON. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low_line or high_line mode.

Vin_OFF (0x36): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low_line or high_line mode.

Fan_config_1_2 (0x3A) : This command requires that the fan speed be commanded by duty cycle. Both fans must be commanded simultaneously. The tachometer pulses per revolution is not used. Default is duty cycle control.

Fan_command_1 (0x3B): This command instructs the rectifier to increase the speed of both fans above what is internally required. The transmitted data byte represents the hex equivalent of duty cycle in percentage, i.e. 100% = 0 x 64h. The command shall increase or decrease fan speed. An incorrect value will result in a 'data error'.

Sending 00h tells the rectifier to revert back to its internal control.

Fan_command_2 (0x3C): not used in this rectifier. Issuing this command will result in 'invalid command'.

Vout_OV_fault_limit (0x40): Sets the value at which the main output voltage will shut down. The default OV_fault value is set at $59V_{dc}$. This level shall be permanently changed and stored in non-volatile

See Footnote on Page No. 33

Technical Specifications (continued)

Command Descriptions (continued)

Vout_OV_fault_response (0x41): This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

Restart after a latched state: Either of four restart mechanisms is available;

- Hardware pin ON/OFF cycled OFF and then ON.
- Commanded to restart via i²c through the Operation command cycled OFF and then ON.
- Remove and reinsert the unit.
- Cycle AC power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers.

Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart shall be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all rectifiers
- Toggling Off and then ON the ON/OFF signal, if this signal is paralleled among the rectifiers.
- Removing and reapplying input commercial power to the entire system.

The rectifiers should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Vout_OV_warn_limit (0x42): Sets the value at which a warning will be issued that the output voltage is too high. The default OV_warn limit is set at $56V_{dc}$. Exceeding the warning value will set the Alert# signal. This level shall be permanently changed and stored in non-volatile memory.

Vout_UV_warn_limit (0x43): Sets the value at which a warning will be issued that the output voltage is too low. The default UV_warning limit is set at $45V_{dc}$. Reduction below the warning value will set the Alert# signal. This level shall be permanently changed and stored in non-volatile memory.

Vout_UV_fault_limit (0x44): Sets the value at which the rectifier will shut down if the output gets below this level. The default UV_fault limit is set at $44V_{dc}$. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level shall be permanently changed and stored in non-volatile memory.

Vout_UV_fault_response (0x45): Sets the response if the output voltage falls below the UV_fault_limit. The default UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state shall be permanently changed and stored in non-volatile memory.

Iout_OC_fault_limit (0x46): Sets the value at which the rectifier will shut down at High Line. This level shall be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 30A.

Iout_OC_fault_response (0x47): Sets the response if the output overload exceeds the OC_Fault_limit value. The default OC_fault_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The default response state shall be permanently changed and stored in non-volatile memory. The response is the same for both low_line and high_line operations.

Iout_OC_warn_limit (0x4A): Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level at high line. This level shall be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 29A.

OT_fault_limit (0x4F): Sets the value at which the rectifier responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT_fault_response register.

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Technical Specifications (continued)

Command Descriptions (continued)

OT_fault_response (0x50): Sets the response if the output overtemperature exceeds the OT_Fault_limit value. The default OT_fault_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state shall be permanently changed and stored in non-volatile memory.

OT_warn_limit (0x51): Sets the value at which the rectifier issues a warning when the dc-sec temperature sensor exceeds the warn limit.

Vin_OV_fault_limit (0x55): Sets the value at which the rectifier shuts down because the input voltage exceeds the allowable operational limit. The default Vin_OV_fault_limit is set at $300V_{ac}$. This level shall be permanently lowered and stored in non-volatile memory.

Vin_OV_fault_response (0x56): Sets the response if the input voltage level exceeds the Vin_OV_fault_limit value. The default Vin_OV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state shall be permanently changed and stored in non- volatile memory.

Vin_UV_warn_limit (0x58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV_fault_limit is $87.5V_{ac}$. This level shall be permanently raised, but not lowered, and stored in non-volatile memory.

Vin_UV_fault_limit (0x59): Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default Vin_UV_fault_limit is set at 80Vac. This level shall be permanently raised and stored in non-volatile memory

Vin_UV_fault_response (0x5A): Sets the response if the input voltage level falls below the Vin_UV_fault_limit value. The default Vin_UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state shall be permanently changed and stored in non-volatile memory.

STATUS_BYTE (0x78) : Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	Unit is busy	0
6	OUTPUT OFF	0
5	V_{OUT} Overvoltage Fault	0
4	I_{OUT} Overcurrent Fault	0
3	V_{IN} Undervoltage Fault	0
2	Temperature Fault or Warning	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

STATUS_WORD (0x79): Returns status_byte as the low byte and the following high_byte.

Bit Position	Flag	Default Value
7	V_{OUT} Fault or Warning	0
6	I_{OUT} Fault or Warning	0
5	INPUT Fault or Warning	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0
2	FAN Fault or Warning	0
1	OTHER	0
0	UNKNOWN Fault or Warning	0

STATUS_VOUT (0X7A): Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	V_{OUT} OV Fault	0
6	V_{OUT}_OV_WARNING	0
5	VOUT_UV_WARNING	0
4	V_{OUT} UV Fault	0
3 - 0	X	0

STATUS_IOUT (0X7B): Returns one byte of information of output current related faults.

Bit Position	Flag	Default Value
7	I_{OUT} OC Fault	0
6	I_{OUT} OC LV Fault	0
5	I_{OUT} OC Warning	0
4	X	0
3	CURRENT SHARE Fault	0
2	IN POWER LIMITING MODE	0
1-0	X	0

The OC Fault limit sets where current limit is set. The rectifier actually shuts down below the LV fault limit setting.

STATUS_INPUT (0X7C): Returns one byte of information of input voltage related faults.

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Command Descriptions (continued)

Bit Position	Flag	Default Value
7	VIN_OV_Fault	0
6	VIN_OV_Warning	0
5	VIN_UV_ Warning	0
4	VIN_UV_Fault	0
3	Unit OFF for low input voltage	0
2	IIN_OC_Fault	0
1-0	X	0

STATUS_TEMPERATURE (0x7D): Returns one byte of information of temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5-0	X	0

STATUS_CML (0X7E): Returns one byte of information of communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4-2	X	0
1	Other Communication Fault	0
0	X	0

STATUS_fans_1_2 (0X81): Returns one byte of information of fan status.

Bit Position	Flag	Default Value
7	Fan 1 fault	0
6	No Current Function	0
5-4	X	0
3	Fan 1 speed overwritten	0
2	No Current Function	0
1-0	X	0

Read back Descriptions

Single parameter read back: Functions shall be read back one at a time using the read_word_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

1	8	1
Sr	Slave address	Rd	A

8	1	8	1	8	1	1
LSB	A	MSB	A	PEC	No-Ack	P

Read back error: If the µC does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read_fan_speed 1 & 2 (0x90, 0x91): Reading the fan speed is in Direct Mode returning the RPM value of the fan.

1	8	1	8	1
S	Slave address	Wr	A	Command 0x9x	A

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = x	A

8	1	8	1	8	1	8	1	1
Byte_1	A	Byte	A	Byte_x	A	PEC	No-Ack	P

Read_FRU_ID (0x99,0x9A,0x9B,0x9E): Returns FRU information. Must be executed one register at a time.

Mfr_ID (0x99): Manufacturer in ASCII – 5 characters maximum, OmniOn – Critical Power represented as, OmniOn-CP

Mfr_ID (0x9A): Manufacturer model-number in ASCII – 16 characters, for this unit: CP3000AC54TEFSGx

Mfr_revision (0x9B): Total 7 bytes, provides the product series number when the product was manufactured.

Mfr_serial (0x9E): Product serial number includes the manufacturing date, manufacturing location in up to 15 characters. For example:

13KZ51018193xxx, is decoded as;
13 – year of manufacture, 2013
KZ – manufacturing location, in this case Matamoros
51 – week of manufacture
018193xxx – serial #, mfr choice

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Technical Specifications (continued)

Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Mfr_Specific Status and alarm registers: The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of this document, or in batches of two STATUS and two ALARM registers.

Status_summary (0xD0) : This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

1	8	1	8	1
S	Slave address	Wr	A	Command code	A

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 11	A

8	1	8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-3	A	Alarm-2	A

8	1	8	1	8	1
Alarm-1	A	Voltage LSB	A	Voltage LSB	A

8	1	8	1
Current-LSB	A	Current-MSB	A

8	1	8	1
Temperature-LSB	A	Temperature-MSB	A

8	1	1
PEC	No-Ack	P

Status_unit(0xD1): This command shall return the STATUS-2 and STATUS-1 register values using the standard 'read' format

Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4	Power_Capacity [HL = 1]	X
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	X

Status-2

Oring fault: Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the power supply. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus a non-destructive or'ing fault does not trigger a shutdown.

Bit Position	Flag	Default Value
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	No Current Function	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	X

Status-1

Status_alarm (0xD2): This command returns the ALARM-3 - ALARM-1 register values.

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-i2c communications fault	0
3	AC monitor communications fault	0
2	x	0
1	x	0
0	Or'ing fault	0

Alarm-3

See Footnote on Page No. 33

Technical Specifications (continued)

Manufacturer-Specific PMBusTM Commands (continued)

Bit Position	Flag	Default Value
7	FAN_Fault	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	V_o lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

Alarm-2

Power Delivery: If the internal sourced current to the current share current is > 10A, a fault is issued.

Bit Position	Flag	Default Value
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	VOUT_out_of_limits	0
0	VIN_out_of_limits	0

Alarm-1

Read_Fan_speed (0 x D3) : Returns the commanded speed in percent and the measured speed in RPM. If a fan does not exist, or if the command is not supported the unit return 0x00

1	8	1	8	1
S	Slave	Wr	A	Command	A

1	8	1	8	1
Sr	Slave	Rd	A	Byte	A

8	1	8	1	8	1	8	1
Adj%-LSB	A	Adj%-MSB	A	Fan1-LSB	A	Fan1-MSB	A

8	1	8	1	8	1	1
Fan2-LSB	A	Fan2-MSB	A	PEC	NO-Ack	P

Read input string (0xD4): Reads back the input voltage and input power consumed by the rectifier.

1	7	1	8
S	Slave address	Wr	A	Command code 0XD4

1	1	7	1	1
A	Sr	Slave address	Rd	A

8	1	8	1	8	1
Byte count = 5	A	Voltage-LSB	A	Voltage-MSB	A

8	1	8	1	8	1	8	1	1
Power-LSB	A	Power-MSB	A	Input Mode	A	PEC	No-Ack	P

Input mode byte is defined as follows:
Bit0: 1-> AC mode
Bit1: 1-> HVDC mode
Bit2: 1-> HVDC ETSI mode (configured by ETSI set pin)

Read_firmware_rev [0 x D5]: Reads back the firmware revision

1	7	1	1	8	1
S	Slave address	Wr	A	Command code 0XD5	A

1	1	7	1	1	8	1
A	Sr	Slave address	Rd	A	Byte count = 6	A

8	1	8	1
Primary major rev	A	Primary minor rev	A

8	1	8	1
Secondary major rev	A	Secondary minor rev	A

8	1	8	1	8	1	1
I^2c major rev	A	I2c revision	A	PEC	No-Ack	P

Read_run_timer [0 x D6]: This command reads back the recorded operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years of operational state.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0XDE	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 3	A

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Technical Specifications (continued)

Manufacturer-Specific PMBus™ Commands (continued)

8	1	8	1	8	1
Time – LSB	A	Time	A	Time – MSB	A

8	1	1
PEC	No-ack	P

EEPROM record (0xD9): The µC shall contain 64 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0XD9	A

8	1	8	1
Start location	A	Byte count	A

8	1		8	1
first_byte	A	.....	Last - byte	A

8	1	1
PEC	A	P

To read contents from the section

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0XD9	A

8	1	8	1
Memory location	A	Byte count ≤ 32	A

1	7	1	1
Sr	Slave address	Rd	A

8	1		8	1
Byte 1	A	.....	Byte ≤ 32	A

8	1	1
PEC	A	P

LEDS test ON: Will turn-ON simultaneously the front panel LEDs of the Rectifier sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the rectifier being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5-6	reserved	
4	Or'ing test	1=ON, 0=OFF
2-3	reserved	
1	No Current Function	1=ON, 0=OFF
0	LED test	1=ON, 0=OFF

LEDS test OFF: Will turn-OFF simultaneously the four front panel LEDs of the Rectifier.

OR'ing Test: This command shall verify functioning of output OR'ing. At least two paralleled rectifiers are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test shall fail. Only one rectifier should be tested at a time.

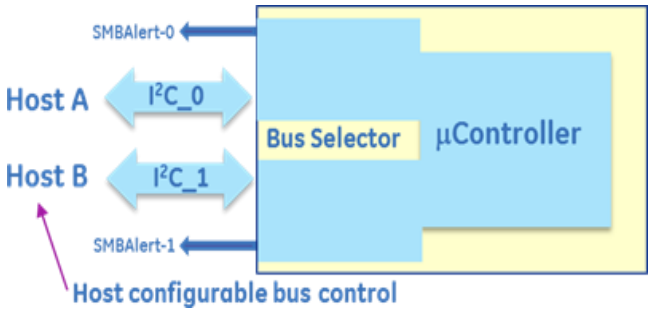
Verifying test completion should be delayed for approximately 30 seconds to allow the rectifier sufficient time to properly execute the test.

Failure of the isolation test is not considered a rectifier FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

Dual Master Control:

Two independent I²C lines and Alert# signals shall provide true communications redundancy allowing two independent controllers to sequentially control the rectifier.

A short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' shall take over control at any time when the bus is idle



Conceptual representation of the dual I²C bus system.

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Technical Specifications (continued)

Dual Master Control: (continued)

The Alert# line exciting the rectifier combines the Alert# functions of rectifier control and dual_bus_control.

Status_bus (0xD7): Bus_Status is a single byte read back. The command shall be executed by either master at any time independent of who has control.

The µC may issue a clock stretch, as it shall for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

Bit position	Flag	Default value
7	Bus 1 command error	0
6	Bus 1 Alert# enabled	0
5	Bus 1 requested control	0
4	Bus 1 has control of the PS	0
3	Bus 0 command error	0
2	Bus 0 Alert# enabled	0
1	Bus 0 requested control	0
0	Bus 0 has control of the PS	0

Command Execution: The master not in control shall issue two commands on the bus, take_over_bus_control and clear_faults

Take_over_Bus_Control(0xD8): This command instructs the internal µC to switch command control over to the 'master' that initiated the request.

Actual transfer is controlled by the I²C selector section of the µC. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by issuing a STOP command. Control shall be transferred at any time if the 'master' being released is executing a read instruction that does not affect the transfer of command control. Note; The µC shall handle read instructions from both busses simultaneously..

The command follows PMBus™ standards and it is not executed until the trailing PEC is validated.

Status Notifications: Once control is transferred both Alert# lines should get asserted by the I²C selector section of the µC. The released 'master' is notified that a STATUS change occurred and he is no longer in control.

The connected 'master' is notified that he is in control and he shall issue commands to the rectifier. Each master must issue a clear_faults command to clear his Alert# signal.

If the Alert# signal was actually triggered by the rectifier and not the I²C selector section of the µC, then only the 'master' in control shall clear the rectifier registers.

Incomplete transmissions should not occur on either bus.

General performance descriptions

Default state: Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state shall be reconfigured by changing non-volatile memory (Store_user_code).

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled rectifiers during power up. If the overload persists beyond the 20 second delay, the rectifier will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > $39V_{DC}$ the Output LED will continue blinking. When output voltage is < $39V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Restart after a latchoff: PMBus™ fault_response commands shall be configured to direct the rectifier to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin ON/OFF may be cycled OFF and then ON.
2. The unit may be commanded to restart via i²c through the Operation command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. 5Changing firmware from latch off to restart.

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Technical Specifications (continued)

General performance descriptions (continued)

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to restart.

A successful restart shall clear all alarm registers, set the restarted successful bit of the Status_2 register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers.

Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart shall be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Auto_restart: Auto-restart is the default configuration for over- current and over-temperature shutdowns. These features are configured by the PMBus™ fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again

Fault Management

The rectifier recognizes that certain transitionary states shall occur before a final state is reached. The STATUS and ALARM registers will not be frozen into a notification state until the final state is reached. Once a final state is reached the Alert# signal is set and the STATUS and ALARM registers will not get reinstated until a clear_faults is issued by the master. The only exception is that additional state changes may be added to the original list if further changes are noted.

The rectifier differentiates between internal faults that are within the rectifier and external faults that the rectifier protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i²c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations shall be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

Input voltage out of range: The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

State Change Definition

A state_change is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a state_change;

- Initial power-up of the system when AC gets turned ON . This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each rectifier to reset the system_interrupt.
- Any changes in the bit pattern of either the PMBus standard STATUS or the mfr_specific STATUS registers should trigger the Alert# signal.

Hot plug procedures

Careful system control is recommended when hot plugging a rectifier into a live system. It takes about 15 seconds for a rectifier to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple rectifiers may respond to specific instructions because the address of the hot plugged rectifier always defaults to xxxx000 (depending on which device is being addressed within the rectifier) until the rectifier configures its address.

The recommended procedure for hot plug is the following: The system controller should be told which rectifier is to be removed. The controller deactivates the power supply via Remote OFF, the DC OK LED will turn off identifying the unit to be removed from the system. The system controller should then poll the MOD_PRES signal to verify when the rectifier is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications shall resume.

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Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the rectifier. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the rectifier is not warranted.

Another example is fan speed monitoring. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a shutdown that would take the rectifier out of service.

Information only alarms: The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- V_{out} out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery
- Stby out of limits
- Communication errors

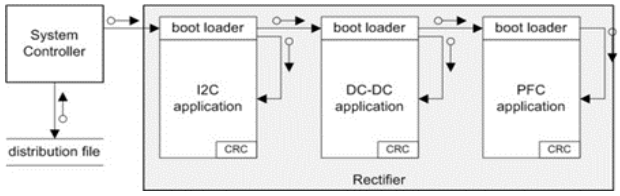
Remote upgrade

This section describes at a high-level the recommended re-programming process for the three internal micro controllers inside the rectifier when the re-programming is implemented in live, running, systems.

The process has been implemented in visual basic by OmniOn Critical Power for controller based systems positioned primarily for the telecommunications industry. OmniOn Critical Power will share its development with customers who are interested to deploy the re-programming capability into their own controllers.

For some customers internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from OmniOn Critical Power. This kit contains a turn-key package with the re-program firmware.

Conceptual Description: The rectifier contains three independent µControllers. The boost (PFC) section is controlled by the primary µController. The secondary DC-DC converter is controlled by the secondary µController, and I^2C communications are being handled by the I^2C Interface µController.



Each of the µControllers contains a boot loader section and an application section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the rectifier.

The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.

The Upgrade Package: This package contains the following files;

- Manifest.txt - The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary. This file contains the version number and the compatibility code of the upgraded program for each of the three processors
- Program.bin - The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file CP3x00AC54TEZ.zip

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Technical Specifications (continued)

Remote upgrade (continued)

- Unzipping the contents shows the following files
  CP3x00AC54TEZ.pfc.bin
  CP3x00AC54TEZ.sec.bin
  manifest.txt
- Opening manifest.txt shows the following
  # Upgrade manifest file
  # Targets: CP3x00AC54TEZ PFC and SEC
  # Date: Tue 01/14/2014 14:25:09.37
  # Notes:
- Program contents
  >p, CP3x00AC54TE _P01, CP3x00AC54TEZ _PFC.bin,1.18
  >s, CP3x00AC54TE _S01, CP3x00AC54TEZ _SEC.bin,1.1

Upgrade Status Indication: The FAULT LED is utilized for indicating the status of the re-programming process. Wink: 0.25 seconds ON, 0.75 seconds OFF

Status	Fault LED	Description
Idle	OFF	Normal state
In boot block	Wink	Application is good
Upgrading	Fast blink	Application is erased or programming in progress
Fault	ON	Erase or re-program Failed

Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

Upgrade procedure

1. Initialization: To execute the re-programming/ upgrade in the system, the rectifier to be re-programmed must first be taken OFF-line prior to executing the upgrade. If the rectifier is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation.
   Note: Make sure that sufficient power is provided by the remaining on-line rectifiers so that system functionality is not jeopardized.
2. Unzip the distribution file
3. Unlock upgrade execution protection by issuing the command below;

Password(0xE0): This command unlocks the upgrade commands feature of the rectifier by sending the characters 'UPGD'.

1	8	1	8	1	8	1
S	Slave address	Wr	A	Cmd – 0xE0	A	Byte count - 4	A

8	1	.....	8	1	8	1	1
Byte 0 - U	A	.....	Byte 4 - D	A	PEC	A	P

4. Obtain a list of upgradable processors (optional)

Target list(0xE1) : This command returns the upgradable processors within the rectifier. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE1	A

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count - n	A

8	1	8	1	8	1	1
Byte 0	A	.....	Byte n	A	PEC	No-Ack	P

Potential target processors are the following:

p – primary (PFC)
s – secondary (DC-DC)
i – I^2C

5. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the rectifier compatibility code of the target processor.

Compatibility code (0xE2): This read command consists of up to 16 characters defining the hardware configuration:

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 16	A	Byte 0	A

	8	1	8	1	1
.....	Byte 15	A	PEC	No-Ack	P

See Footnote on Page No. 33

Technical Specifications (continued)

Remote upgrade (continued)

Where Target-x is an ASCII character pointing to the processor to be updated;

p – primary (PFC)
s – secondary (DC-DC)
i – I^2C

6. Check the software revision number of the target processor in the rectifier and compare it to the revision in the upgrade. If the revision numbers are the same, or the rectifier has a higher revision number then no upgrade is required for the target processor.

Software revision(0xE3): This command returns the software revision of the target.

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE3	A	Target-x	A

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 7	7	Major revision	A

8	1	8	1	8	1	1	1
Minor	A	month	A	Day	A	year[16]	P

8	1	8	1	8	1	1
hrs	A	min	A	PEC	No-Ack	P

7. Verify the capability of each processor

Memory capability (0xE4): Provides the specifics of the capability of the device to be reprogrammed

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 7	A	Max	A

8	1	8	1	8	1	8	1
ET-LSB	A	ET-MSB	A	BT-LSB	A	BT-MSB	A

8	1	8	1	8	1	1
App_CRC_LSB	A	App_CRC_MSB	A	PEC	No-Ack	P

Where the fields definition are shown as below:

Max Bytes	Maximum number of bytes in a data packet
ET	Erase time for entire application space (in mS)
BT	Data packet write execution time (uS)
APP_CRC	Application CRC-16 – returns the applicationCRC-16 calculation. Reading these register values, if the application upload CRC-16 calculation returns an invalid, provides the mismatch information to the host program. (See application status(0xE5) command)

This information should be used by the host processor to determine the max data packet size and add appropriate delays between commands.

8. Verify availability: The Application status command is used to verify the present state of the boot loader.

Application status (0xE5): Returns the Boot Loader's present status

1	8	1	8	1	8	1
S	Slave	Wr	A	Cmd – 0xE5	A	Target-x	A

1	8	1	8	1	8	1	1
Sr	Slave addr	Rd	A	Status	7	PEC	No-Ack	A

Status bits :

0x00 Processor is available	0x10 Reserved
0x01 Application erased	0x20 Reserved
0x02 CRC-16 invalid	0x40 Manages
0x04 Sequence out oforder	downstream µC 0x80 In
0x08 Address out of range	boot loader

Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

9. Issue a Boot Loader command with the enter boot block instruction

Boot loader (0xE6): This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

1	7	7	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE6	A	Target-x	A

8	1	8	1	1
Data	A	PEC	A	P

See Footnote on Page No. 33

Technical Specifications (continued)

Remote upgrade (continued)

Data:

1=enter boot block (software reboot)

2=erase

3=done

4=exit[17] boot block (watchdog reboot)

Note: The target µC field is ignored for enter and exit commands. During this process if the output of the rectifier was not turned OFF the boot loader will turn OFF the output

10. Erase and program each µC using the Boot Loader command, starting with the PFC.
11. Wait at least 1 second after issuing en erase command to allow the µC to complete its task.
12. Use command 0xE5 to verify that the PFC µC is erased. The returned status byte should be 0x81.
13. Use the Data Transfer command to update the application of the target µC.

Data transfer (0xE7): The process starts with uploading data packets with the first sequence number (0x0000).

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE5	A	Target-x	A

8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Byte Count = n	A

8	1	8	1	8	1	1
Byte 0	A	.....	Byte n - 1	A	PEC	A	P

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

1	8	1	8	1
S	Slave	Wr	A	Cmd – 0xE7	A

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 3	A

1	8	8	1	8	1	8	1	1
Seq-LSB	A	Seq-MSB	A	Status	A	PEC	No-Ack	P

The returned Status byte is defined in the Application Status command (0 x E5).

Sequence number validation takes place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

14. Execute a Boot loader command to tell the PFC µC that the transfer is done.

    At the completion signal, the PFC µC should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation.

    Wait for at least 1 second to allow time for the PFC µC to calculate the error checking value.
15. Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.
16. Execute a Boot loader command to exit boot block. Upon receipt of the command the PFC µC will transfer to the uploaded application code.
17. Wait for at least 1 second.
18. Use command 0xE1 to verify that the PFC µC is now in the application code. The returned status data bte should be 0x00.
19. Repeat the program upgrade for the Secondary and I²C µC's, if included in the upgrade package

Product comcode

Although the comcode number is not required for the upgrade process in its present form, it may be useful when upgrading multiple version of the same product in order to differentiate product upgrade requirements.

Product comcode (0xE8):

1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE8	A

See Footnote on Page No. 33

Technical Specifications (continued)

Product comcode (continued)

Product comcode (0xE8): (continued)

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 11	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte 10	A	PEC	No-Ack	P

Error handling: The Boot loader will not start the application if errors occurred during the re-program stage. The controlling program could restart the upgrade process or terminate the upgrade and remove the offending rectifier from service.

Black box

Contents of the black box and more detailed information about the specifics of the feature are described in a separate document. The intent here is to provide a high level summary This feature includes the following;

1. A rolling event Recorder
2. Operational Use Statistics

The rolling event recorder

The purpose of the black box is to provide operational statistics as well as fault retention for diagnostics following either recoverable or non-recoverable fault events. Sufficient memory exists to store up to 5 time-stamped snapshot records (pages) that include the state of the status and alarm registers and numerous internal measurement points within the power supply. Each record is stored into nonvolatile memory at the time when a black box trigger event occurs. Once five records are stored, additional records over-write the oldest record.

The memory locations will be cleared, when the product is shipped from the OmniOn factory.

Operational use statistics

This feature of the black box includes information on the repetition and duration of certain events in order to understand the long-term operational state of the power supply. The events are placed into defined buckets for further analysis. For example; the power supply records how long was the output current provided in certain load ranges.

Accessing the event records

The event records are accessed by uploading the entire contents of the black box of the power supply into a folder assigned by the user. Within the I^2C protocol this upload is accomplished by the upload_black_box (0xF0) command described below. OmniOn provides a Graphical User Interface (GUI) that de-codes the contents of the black box into a set of records that can be reviewed by the user.

Upload black box(0xF0): This command executes the upload from the power supply to a file of the user's choice.

The 100ms delay prior to the restart is mandatory to provide enough time for the power supply to gather the required data from the secondary DSP controller.

1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xF0	A

8	1	8	1
Start address - msb	A	Start address - lsb	A

8	1	
Length = N (≤ 32)	A	..... delay 100ms

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Length ≤ 32	A	Byte 0	A

	8	1	8	1	1
.....	Byte N-1	A	PEC	No-Ack	P

If a transmission error occurs, or if the uC did not receive the data from the DSP, the uC may set the length to 0, issue a PEC and terminate the transmission.

The data array supported by rev 1.3 of the OmniOn Interface Adapter is 32 x 64 comprising 2048 bytes of data

Start Address	0 ..... Byte 31
0000h	
0020h	
0040h	
.	
.	
.	
.	
.	
.	
.	
07E0h	

See Footnote on Page No. 33

Technical Specifications (continued)

Validation: DVT-SIT Test

- DVT-SIT: In order to evaluate current sharing performance, the recommended test set-up for a system, per our default standard, is 4 units in parallel.
- Tests for compliance with ETSI Standards for abnormal input voltage conditions; from ETSI EN 300 132-3-1 V2.1.1 (2011-10), Section 6.

Voltage	Duration	Compliance Criteria on telecommunicationsand datacom (ICT) equipment	Comments
From UT to 260 V,back to UT	1 min	Criteria a) Normal performance	Test of minimum operating voltage at A3 within the normal service voltagerange
From UT to 400 V,back to UT	1 min	Criteria a) Normal performance	Test of minimum operating voltage at A3 within the normal service voltagerange
From UT to 400 V,back to UT	1 s	Criteria b) Temporary loss of function or degradation of performance, automatic recovery to normal performance after the test	Test of voltage rise variation entering abnormal service voltage range
From UT to 420 V,back to UT	10 ms	Criteria b) Temporary loss of function or degradation of performance, automatic recovery to normal performance after the test	Test of voltage rise variation outside abnormal service voltage range

6.1 Voltage Variations

Voltage	Duration	Compliance Criteria on telecommunications and datacom (ICT) equipment	Comments
From UT to 260 V,back to UT	10 ms	Criteria a) Normal performance	Test of minimum operating voltage at A3 within the normal service voltage range

6.2 Voltage Dips

Voltage	Supply Network	Duration	Compliance Criteria on telecommunications and datacom (ICT) equipment	Comments
From UT to 0 V,back to UT	Low Impedance (short circuit)	10 ms	Criteria a) Normal performance	Test of holdup time during faultclearing due to a short-circuit in the system
From UT to 0 V,back to UT	High Impedance (open circuit)	1 s	Criteria b) Temporary loss of function or degradation of performance, automatic recovery to normal performance after the test	Test of automatic recovery after an extended (> 1 s) interruption of the operating voltage at interface A3

6.3 Short interruption

See Footnote on Page No. 33

Technical Specifications (continued)

Validation: DVT-SIT Test (continued)

	Test Condition	LED Indicator		Monitoring Signals		
		LED1 INPUT OK	LED2 (Dual-Color) DC OK / Fault	FAULT#	PG#	OTW#
1	Normal Operation	**Green**	**Green**	High	High	High
2	Out of range INPUT	**Blinking**	OFF	High	High	High
3	No Input[18]	OFF	OFF	High	Low	High
4	OVP	**Green**	**Red**	Low	Low	High
5	Over Current	**Green**	**Blinking**	High	Pulsing	High
6	Over Temp Warning	**Green**	**Green**	High	High	Low
7	Over Temp Fault	**Green**	**Red**	Low	Low	Low
8	Remote OFF[19]	**Green**	OFF	High	Low	High
9	PMBus OFF[20]	**Green**	OFF	High	Low	High

Table 1: Alarm and LED state summary

FOOTNOTES

*UL is a registered trademark of Underwriters Laboratories, Inc..

§ This product is intended for integration into end-user equipment. All CE marking procedures of end-user equipment should be followed. (The CE mark is placed on selected products.)

+ The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

[1] Internal protection circuits may override the PG# signal and may trigger an immediate shutdown.

[2] Asserted state depends on internal operating conditions. Intent is to provide a warning if output power is about to turn OFF.

[3] Aux should be ON prior to the 54VDC output and should turn OFF only if insufficient input voltage exists to provide reliable power.

[4] Clock, Data, and Alert# need to be pulled up to VDD externally.

[5] Below 20% of FL; 10 – 20% of FL: ±0.64A; 5 – 10% of FL: ±0.45A; 2.5 – 5% of FL: ±0.32A.

[6] Above 2.5A of load current

[7] Within 30° of the default warning and fault levels.

[8] Designed to start and work at an ambient as low as -40°C, but may not meet operational limits until above -10°C

[9] Derating begins at 40°C when HVDC input is less than 200V_{DC}, front to rear airflow

[10] Emissions requirements shall be verified using TBD OmniOn shelf. Standalone the additional margin is not required.

[11] Voltage remains above 48V during level A test.

[12] Yes – indicates that the data can be changed by the user

[13] Only latched (0xC0) or hiccup (0xF8) are supported

[14] Only latched (0x80) or hiccup (0xC0) are supported

[15] Yes – indicates that the data can be changed by the user

[16] The threshold commands for Vin limits are available only for AC input. These limits are fixed for HVDC input.

[17] Last two digit

[18] The 'exit boot block' command is only successful if all applications are valid, otherwise, control remains in the boot block

[19] Test condition #2 and #3 had 2 modules plugged in. One module is running and the other one is with no/low AC.

[20] Remote OFF can be accomplished via PMBus Operation command or via Remote ON/OFF pin.

Technical Specifications (continued)

Validation: DVT-SIT Test (continued)

All hardware alarm signals (Fault#, PG#, OTW#) are open drain FETs. These signals need to be pulled HI to either 3.3V or 5V. Maximum sink current 5mA. An active LO signal (< 0.4V_{DC}) state. All signals are referenced to LGND (Logic_GND) unless otherwise stated.

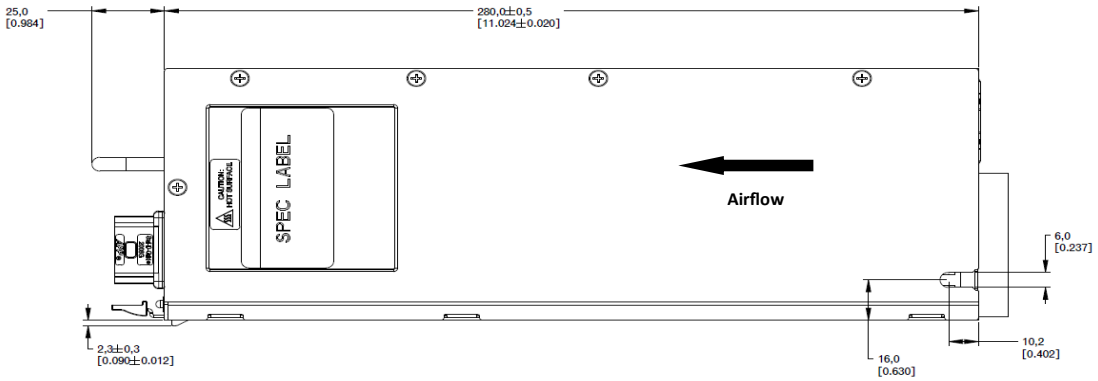
Function	Label	Type	Description
Remote On/Off	ON/OFF	Input	If shorted to LGND main output is ON
Output power monitor	PG#	Output	An open drain FET; Changes to LO @ 5msec before the output decays below 40VDC.
Rectifier Fault	Fault#	Output	An open drain FET; normally HI, changes to active LO during a fault.
Module Present	MOD_PRES	Output	Shorted to LGND inside the rectifier.
Interlock	Interlock	Input	Short pin, controls main output during hot-insertion and extraction. Ref: Vout (-)
Load Power capacity	Power_Cap	Output	Open drain FET; When pulled LO indicates that output power is limited to 1400W
Output voltage margin	Vprog	Input	Changes the set point of the main output.
Over-Temperature Warning	OTW#	Output	Open drain FET; normally HI, changes to LO 5°C prior to thermal shutdown.
I^2C addresses	A2, A1, A0, ETSI_Set	Input	Internal 10kΩ pull ups provided. Tied to LGND for logic LO (0)
HVDC input turn on/off threshold	ETSI_set	Input	Internal 10kΩ pull ups provided. Open to set HVDC input range 180~400V_{DC}; Tied to LGND to set HVDC input range 260~400V_{DC}
Back bias	8V_INT	Bi-direct	Used to back bias the DSP from operating Rectifiers. Ref: V_{out} (-).
Standby power	5V/3.3V	Output	Default set to 3.3V @ 3A
Standby voltage configurator	Aux_set	Input	Pulled up internally. When tied to LGND configures the output to 5V
Current Share	Ishare	Bi-direct	A single wire active-current-share interconnect between modules Ref: V_{out} (-).
I^2C Interrupt	Alert#_0/Alert#_1	Output	Active LO. External pull-up required
I^2C Line 0	SCL_0	Input	PMBus line 0. External pull-up required
I^2C Line 0	SDA_0	Bi-direct	PMBus line 0. External pull-up required
I^2C Line 1	SCL_1	Input	PMBus line 1. External pull-up required
I^2C Line 1	SDA_1	Bi-direct	PMBus line 1. External pull-up required

Table 2: Signal Definitions

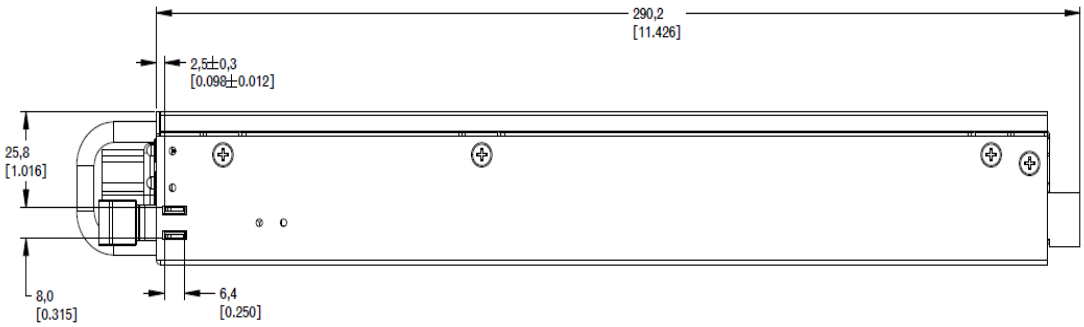
Technical Specifications (continued)

Mechanical Outline

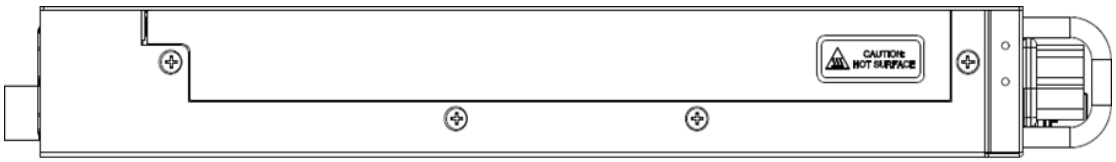
TOP VIEW



RIGHT VIEW

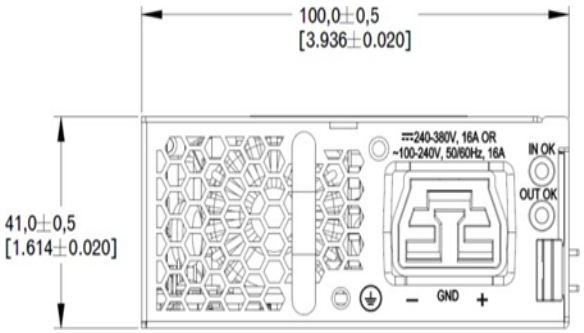


LEFT VIEW

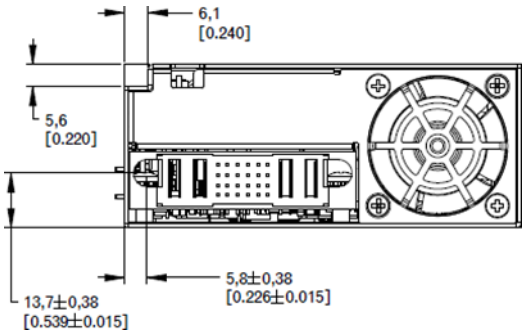


SCALE 2.000

FRONT VIEW



REAR VIEW



Mechanical Outline (continued)

Input Connector: Anderson P/N: 2006G2

Output Connector: TYCO P/N: 2-6450130-9 or FCI Berg P/N: 51720-10202402AALF

Mating connector TYCO P/N: 1-6450160-0 or FCI Berg P/N: 51760-10202402AALF

P4	P3		6	5	4	3	2	1		P2	P1
V_out(-)	V_out(-)	A	Alert_0	Mod_pres	PG#	Aux_set	Power_cap	SCL0	A	V_out(+)	V_out(+)
		B	Alert_1	OTW	ON/OFF	IShare	NC	SCL1	B		
		C	Interlock	Vprog	LGND	I2c_A2	I2c_A1	SDA0	C		
		D	8V_INT	Fault	5V/3.3V	ETSI_set	I2c_A0	SDA1	D		

Notes: 1. Connector is viewed from the rear of the front end

2. Signal pins in red are referenced to LGND (Logic_GND or logic ground), signal pins in black referenced to $V_{out}(-)$.
3. Last to make-first to break short pin
4. Input ground line must be tied to grounding screw if there is no other grounding in the system.

Ordering Information

Please contact your OmniOn Sales Representative for pricing, availability and optional features.

Item	Description	Ordering Codes
CP3000HV54TEZ-FSG	Front AC or HVDC input, 3000W output, 3.3V/5V$_{dc}$ @ 3A, RoHS 6/6, conformal coated. Airflow is rear to front.	150050851
CP3000HV54TEZ-FSGR	Front AC or HVDC input, 3000W output, 3.3V/5V$_{dc}$ @ 3A, RoHS 6/6, conformal coated, Reverse airflow is front to rear.	1600141279A

F-Input on front faceplate, S – Short, G – Global platform, R – Reverse (Front to rear) Airflow

Table 3: Device Codes

Item	Description	Ordering Codes
Anderson 2031KZ3-BK	3 meter Single-Ended “T” Latch Plug Power Cord for AC and HVDC inputs.	4600147059P
Anderson 2031KZ2-BK	2 meter Single-Ended “T” Latch Plug Power Cord for AC and HVDC inputs.	4600158777P
Evaluation Board	CP3000HV54TEZ-FSG(R) Evaluation Board to provide interface between power supply and GUI	7000150557A

Table 4 : Accessories

Contact Us

For more information, call us at
+1-877-546-3243 (US)
+1-972-244-9288 (Int’l)

Change History (excludes grammar & clarifications)

Revision	Date	Description of the change
5.3	11/22/2021	Updated as per template
5.4	11/22/2023	Updated as per OmniOn template

OmniOn Power Inc.
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Plano, TX USA

omnionpower.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

OmniOn Power:

CP3000HV54TEZ-FSGR CONVERTER CP3000HV54TEZ-FSG CONVERTER