CC3500AC52TZL Conduction Cooled, Wide-Output-Range Rectifier

200-277V_{AC} Input; 3725W capable; 42-53V_{DC} Output, 5V_{DC}@10W

Description

The CC3500AC52TZL rectifier has an extremely wide programmable output voltage capability. Featuring high-density, fully enclosed, conduction-cooled packaging, it is designed for minimal space utilization and is highly expandable for future growth. This standard rectifier incorporates both RS485 and dual-redundant I^2C communications busses that allow it to be used in a broad range of applications. Feature-set flexibility makes this rectifier an excellent choice for applications requiring operation over a wide output voltage range.

Applications

Examples applications include, but are not limited to:

- Wide-band power amplifier
- Broadcast systems
- Lasers
- Acoustic-noise-sensitive systems

Features

- Efficiency exceeding 96%
- Compact form factor with 40 W/in^3 density
- 3725W from nominal 200-277V_{AC} up to 40°C case
- Output voltage programmable from 42V – 53V_{DC}
- ON/OFF control of the main output
- Comprehensive input, output and over temp. protection
- PMBus® compliant dual I^2C serial bus and RS485
- Precision measurement reporting such as input power consumption, input/output voltage & current
- Remote firmware upgrade capable
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- Redundant, parallel operation with active load sharing
- Redundant +5V @ 2A Aux power
- Completely enclosed, conduction cooled
- Four front panel LED indicators
- EN/IEC/UL60950-1 2nd edition (CB report)

Technical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess

Parameter	Symbol	Min	Max	Unit
Input Voltage: Continuous	V_{IN}	0	300	V_{AC}
Operating Case Temperature (sink side)[1]	T_C	-5	40	°C
Storage Temperature	T_{STG}	-40	85	°C

Electrical Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, Vo=52V_{DC}, resistive load, and temperature conditions.

INPUT

Parameter	Symbol	Min	Typ	Max	Unit
Startup Voltage High-line Operation	V_{IN}			185	V_{AC}
Operating Voltage Range High-line Configuration	V_{IN}	185[2]	200-277	300	V_{AC}
Voltage Swell (no damage)	V_{IN}	305			V_{AC}
Turn OFF Voltage Turn ON Voltage Hysteresis	V_{IN}	175	 10	 185	V_{AC}
Frequency	F_{IN}	47		66	Hz
Source Impedance (NEC allows 2.5% of source voltage drop inside a building)			0.2		Ω
Operating Current at 185V_{AC} with 3500W at 200V_{AC} with 3725W[3]	I_{IN}			21 20	A_{AC}
Inrush Transient (220VRMS , T_C=25°C, excluding X-Capacitor charging)	I_{IN}		25	40	A_{PK}
Leakage Current (300V_{AC}, 60Hz)	I_{IN}			3.5	mA
Idle Power (at 240V_{AC}, T_C=25°C, 5Vstb 0A) 50V OFF 50V ON @ Io=0	P_{IN}		9 18		W
Power Factor (50 – 100% load)	PF	0.97	0.995		
Efficiency[4], 240V_{AC}, 52V_{DC}, @ T_C=25°C 10% of FL 20% of FL 50% of FL 100% of FL	η	 90 94 96 91			%
Holdup time (52V/3500W, output allowed to decay down to 40V_{DC})	T		10		ms
Ride through (at 240V_{AC}, T_C=25°C, 52V/3500W)	T	1/2	1		cycle
Power Good Warning[5] (main output allowed to decay to 40V_{DC})	PG	3	5		ms
Isolation (per EN60950) (consult factory for testing to this requirement) Input to Chassis & Signals Input to Output	V	1500 3000			V_{AC} V_{AC}

[1] See the derating guidelines under the Environmental Specifications section

[2] 185~200V, 3500W.

[3] 5V $_{STB}$ is 0A

[4] 5V output at 0A load, 50V output 3500W

[5] Internal protection circuits may override the PG signal and may trigger an immediate shutdown. PG should not indicate normal (HI) until the main output is within regulation. PG should be asserted if the main output is about to shut down for any detectible reason.

Technical Specifications (continued)

Electrical Specifications (continued)

MAIN OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Output Power[6] @ high line input 200—300V_{AC}, VO ≥50V_{DC}, T_C ≤40°C @ high line input 185—200V_{AC}, VO ≥50V_{DC}, T_C ≤40°C	W	3725 3500			W_{DC}
Factory set default set point	V_{OUT}		52		V_{DC}
Overall regulation (load, temperature, aging) 0≤T_C≤40°C LOAD > 2.5A	V_{OUT}	-1.5		+1.5	%
Output Voltage Set Range	V_{OUT}	42		53	V_{DC}
Response to a voltage change command	T		400	500	ms
Output Current - T_C≤40°C @200-300VAC, Vo=50/53V_{DC} @185-200VAC, Vo=50/53V_{DC}	I_{OUT}	1 1		74.5/70.3 70/66	A_{DC}
Current Share (> 50% FL, FL is 3500W) V_O > 42V_{DC} V_O < 42V_{DC}	-5 -10			5 10	%FL
Output Ripple (20MHz bandwidth, load > 1A) RMS (5Hz to 20MHz) Peak-to-Peak (5Hz to 20MHz)	V_{OUT}			150 700	mV_{RMS} mV_{P-P}
External Bulk Load Capacitance	C_{OUT}	0		5000	μF
Turn-On (monotonic turn-ON from 30 – 100% of V_{NOM} above 5° C) Delay Rise Time – PMBus mode Rise Time - RS-485 mode[7] Output Overshoot	T V_{OUT}		5 100 5	 2	s ms s %
Load Step Response ($I_{O,START}$ > 2.5A) ΔI[8] ΔV Response Time	I_{OUT} V_{OUT} T		 2.0 2	50	%FL V_{DC} ms
Power limit , high line 200~300Vac (down to 50V_{DC})	P_{OUT}	3725			W
Power limit , high line 185~200Vac (down to 50V_{DC})	P_{OUT}	3500			W
Overvoltage - 200ms delayed shutdown Immediate shutdown	V_{OUT}	>55		<59	V_{DC}
Latched shutdown	Three restart attempts are implemented within a 1 minute window prior to a latched shutdown.				
Over-temperature warning (prior to commencement of shut-down) Shutdown (below the max device rating being protected) Restart attempt Hysteresis (below shutdown level)	T		5 20 10		ºC
Isolation Output to Chassis	V	500			V_{DC}

6 Output power capability is proportional to output voltage setting, see the permissible load boundary
7 Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.
8 di/dt (output current slew rate) 1A/µs.

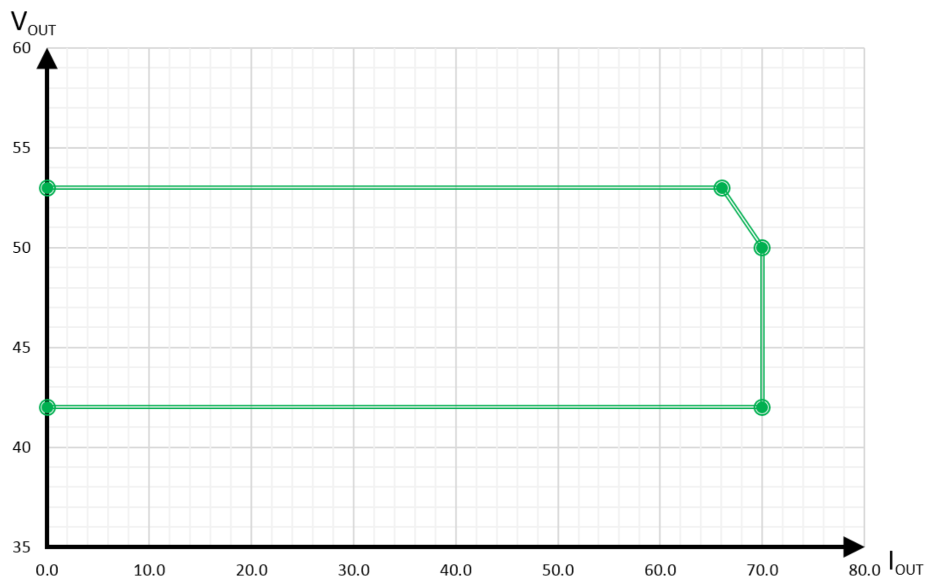
Technical Specifications (continued)

Electrical Specifications (continued)

MAIN OUTPUT

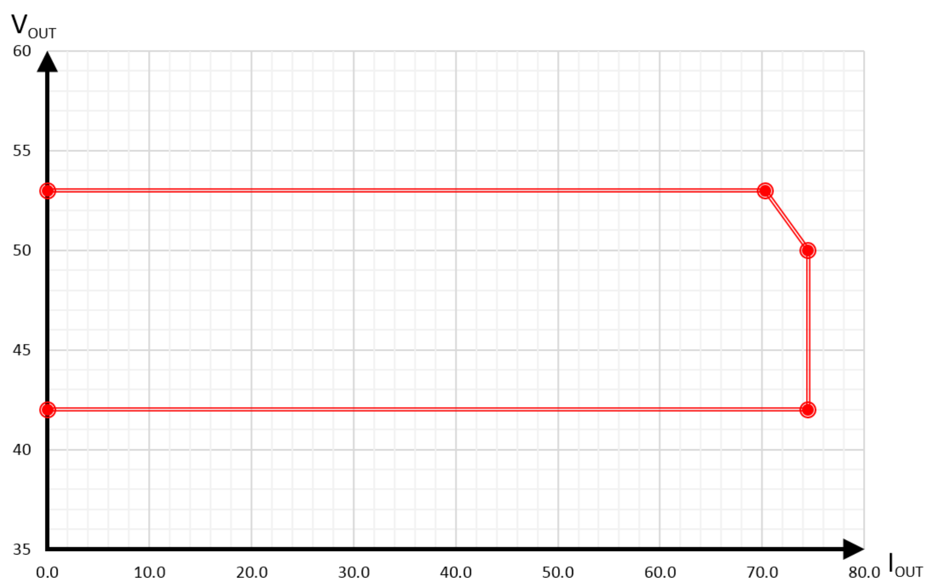
Permissible Load Boundary

185-200V_{AC} input:



Vo (Vdc)	42	44	46	48	49	50	51	52	53
Io (A)	70	70	70	70	70	70	68.6	67.3	66
Po (W)	2940	3080	3220	3360	3430	3500	3500	3500	3500

200-265V_{AC} input:



Vo (Vdc)	42	44	46	48	49	50	51	52	53
Io (A)	74.5	74.5	74.5	74.5	74.5	74.5	73.0	71.6	70.3
Po (W)	3129	3278	3427	3576	3650.5	3725	3725	3725	3725

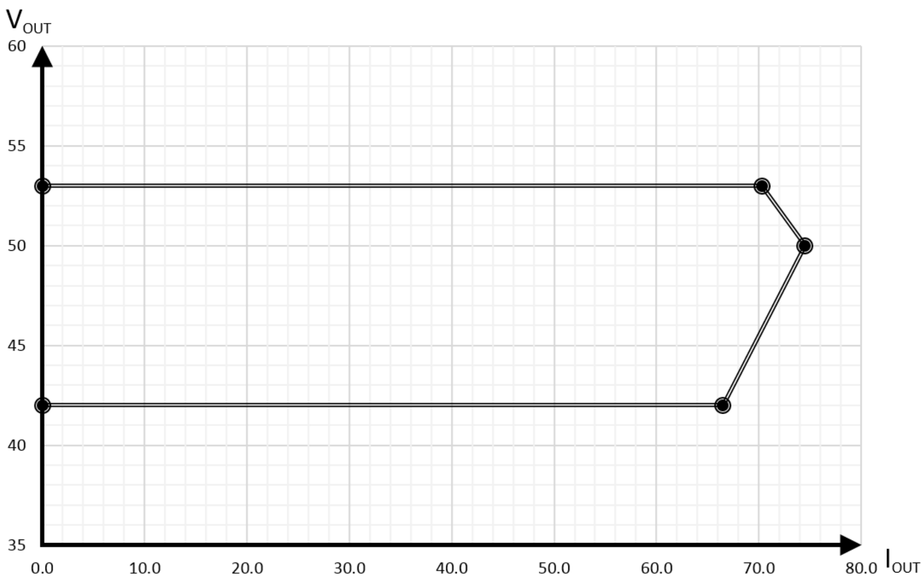
Technical Specifications (continued)

Electrical Specifications (continued)

MAIN OUTPUT

265-300Vac input:

Permissible Load Boundary (continued)



Vo (Vdc)	42	44	46	48	49	50	51	52	53
Io (A)	66.5	68.5	70.5	72.5	73.5	74.5	73.0	71.6	70.3
Po (W)	2793	3014	3243	3480	3601.5	3725	3725	3725	3725

Define Po curve at case temp 40ºC. Ambient temp is less than 30ºC.

The overload current limit threshold is set @ 1~2% above the load envelope shown here.

Contract terms are for supporting all loads inside the load map.

The customer will develop a control interface which maintains the operating voltage and current so as to not exceed the load map.

System power up -Upon insertion the rectifier will delay an overload shutdown for 20 seconds.

$5V_{DC}$ Auxiliary output (return is LGND)

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint	V_{OUT}		5		V_{DC}
Overall Regulation		-3		+3	%
Output Current		0.005		2	A
Ripple and Noise (20mHz bandwidth)			50	100	mV_{P-P}
Over-voltage Clamp				7	V_{DC}
Over-current Limit		110		175	%FL
Isolation LGND to Chassis	V	100			V_{DC}

The $5V_{DC}$ should be ON before availability of the $52V_{DC}$ main output and should turn OFF only if insufficient input voltage exists to provide reliable $5V_{DC}$ power. The PG# signal should have indicated a warning that power would get turned OFF and the $52V_{DC}$ main output should be OFF way before interruption of the $5V_{DC}$ output.

Technical Specifications (continued)

General Specifications

Parameter	Min	Typ	Max	Unit	Notes
Reliability		1,000,00 0		Hours	Full load, T_C=25°C; MTBF per SR232 Reliability protection for electronic equipment, issue 3, method I, case III,
Service Life		10		Years	At 80% load & 40°C cold plate
Unpacked Weight		4.1		Kg	
Packed Weight		4.5		Kg	

Signal Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. Signals are referenced to LGND unless noted otherwise. Fault#, PG#, OTW#, and Alert# need to be pulled HI through external pull-up resistors.

Parameter	Symbol	Min	Typ	Max	Unit
ON/OFF Main output OFF	V_{OUT}	2.4		5	V_{DC}
50V output ON (should be connected to LGND)	V_{OUT}	0		0.4	V_{DC}
Margining (by adjusting Vprog; see "Voltage programming" section)					
Programmed output voltage range	V_{OUT}	42		53	V_{DC}
Linear voltage control range	$V_{CONTROL}$	>0.1		<3.0	V_{DC}
Voltage adjustment resolution (8-bit A/D)	$V_{CONTROL}$		43		mV_{DC}
Output set to $52V_{DC}$	$V_{CONTROL}$	3.0		3.3	V_{DC}
Output set to $42V_{DC}$	$V_{CONTROL}$	0		0.1	V_{DC}
53 – $42V_{DC}$, settling time to new value	T		400	600	ms
Over Temperature Warning (OTW#) Logic HI (temperature normal)	V	2.4		12	V_{DC}
Sink current [note: open collector output FET]	I			5	mA
Logic LO (temperature is too high)	V	0		0.4	V_{DC}
Power Good (PG) Logic HI (temperature normal)	V	2.4		12	V_{DC}
Sink current [note: open collector output FET]	I			5	mA
Logic LO (temperature is too high)	V	0		0.4	V_{DC}
Protocol select Logic HI - Analog/PMBus mode	V_{IH}	2.7		3.5	V_{DC}
Logic – intermediate – RS485 mode	V_{II}	1.0		2.65	V_{DC}
Logic LO – DSP reprogram mode	V_{IL}	0		0.4	V_{DC}
Fault# Logic HI (No fault is present)	V	2.4		12	V_{DC}
Sink current	I			5	mA
Logic LO (Fault is present)	V	0		0.4	V_{DC}
Alert# (Alert#_0, Alert#_1) Logic HI (No Alert - normal)	V	2.4		12	V_{DC}
Sink current [note: open collector output FET]	I			5	mA
Logic LO (Alert# is set)	V	0		0.4	V_{DC}
SCL, SDA (SCL_0/1, SDA_0/1) Logic HI	V	2.1		12	V_{DC}
Sink current [note: open collector output FET]	I			5	mA
Logic LO (Alert# is set)	V	0		0.4	V_{DC}
Interlock	[short pin shorted to V_{OUT} (-) on system side]				
Module Present	[short pin to LGND internally]				

Technical Specifications (continued)

Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics[9]						
Input Logic High Voltage (CLK, DATA)		V	2.1		12	V_{DC}
Input Logic Low Voltage (CLK, DATA)		V	0		0.8	V_{DC}
Input high sourced current (CLK, DATA)		I	0		10	μA
Output Low sink Voltage (CLK, DATA, ALERT#)	I_{OUT}=3.5mA	V			0.4	V_{DC}
Output Low sink current (CLK, DATA, ALERT#)		I	3.5			mA
Output High open drain leakage current (CLK,DATA, ALERT#)	V_{OUT}=3.6V	I	0		10	μA
PMBus Operating frequency range	Slave Mode	FPMB	10		400	kHz
Measurement System Characteristics						
Clock stretching		$T_{STRETCH}$			25	Ms
I_{OUT} measurement range		I_{RNG}	0		80	A_{DC}
I_{OUT} measurement accuracy 25°C	>12.8A <12.8A	$I_{OUR(ACC)}$	-1 5		+1 5	% of FL %
I_{OUT} measurement accuracy 0 - 40°C [10]	>12.8A	$I_{OUR(ACC)}$	-2		+2	% of FL
V_{OUT} measurement range		V_{OUT} (RNG)	0		70	V_{DC}
V_{OUT} measurement accuracy [11]		V_{OUT} (ACC)	-1		+1	%
Temp measurement range		Temp	0		150	ºC
Temp measurement accuracy [12]		Temp	-4		+4	ºC
V_{IN} measurement range		$V_{IN(RNG)}$	0		320	V_{AC}
V_{IN} measurement accuracy @ 25°C	V_{IN}>120V_{AC} V_{IN}<120V_{AC}	$V_{IN(ACC)}$	-1.25 -2		+1.25 2	%
I_{IN} measurement range		$I_{IN(RNG)}$	0		30	I_{AC}
I_{IN} measurement accuracy - standard measurement @ 25°C		$I_{IN(ACC)}$	-4		+4	% of FL
I_{IN} measurement accuracy - improved measurement @ 25°C	>1A ≤1A	$I_{IN(ACC)}$	-2.5 -400		2.5 400	% mA
P_{IN} measurement range		$P_{IN(RNG)}$	0		4000	W_{IN}
P_{IN} measurement accuracy - standard measurement @ 25°C	>350W <350W	$P_{IN(ACC)}$	-5	 35	+5 50	% W
P_{IN} measurement accuracy - improved measurement @ 25°C	>500W 100-500W <100W	$P_{IN(ACC)}$	-1.5 -2.0 -20	1 1.5 15	+1.5 +2.0 20	% % W

[9] Clock, Data, and Alert# need to be pulled up to V_{DD} externally.

[10] Below 20% of FL; 10 – 20% of FL: ±0.64A; 5 – 10% of FL: ±0.45A; 2.5 – 5% of FL: ±0.32A.

[11] Above 2.5A of load current

[12] Within 30° of the default warning and fault levels.

Technical Specifications (continued)

Environmental Specifications

Parameter	Min	Typ	Max	Units	Notes
Operating Case Temperature	-5		40	°C	Measured at the surface that mounted to cold plate and just above the HS_1 and HS2
Storage Temperature	-40		85	°C	
Operating Altitude			5000/16,400	m / ft	
Non-operating Altitude			8200/27,000	m / ft	
Acoustic noise		0		dbA	Full load
Power Derating with Temperature			1	%/°C	40°C-50°C, **derating may not be auto-lunched by rectifier before OTP, customer has to limit the output power accordingly.**
Over Temperature Protection		125/110		°C	Shutdown / restart [internally measured points]
Humidity Operating Storage	 5 5		 95 95	 % %	Relative humidity, non-condensing
Shock and Vibration acceleration			2.4	Grms	IPC-9592B, Class II

EMC (all tested at 3500W/52V_{DC})

Parameter	Measurement	Standard	Level	Test
AC input[13]	Conducted emissions	EN55032, FCC Docket 20780 part 15, subpart J Meets Telcordia GR1089-CORE by a 3dB margin	A +6dB margin	0.15 – 30MHz
	Radiated emissions	EN55032	A +6dB margin	30 – 10000MHz
	Line harmonics	EN61000-3-2 THD	Table 1 5%	0 – 2 kHz 230 Vac, full load, T=25°C

Parameter	Measurement	Standard	Criteria[14]	Test
AC Input Immunity	Line sags and interruptions	EN61000-4-11	B	-30%, 10ms
			B	-60%, 100ms
			B	-100%, 5sec
		Output will stay above 40V_{DC} @ 75% load Sag must be higher than 80Vrms.	A	25% line sag for 2 seconds 1 cycle interruption
	Lightning surge	EN61000-4-5, Level 4, 1.2/50µs – error free	A	4kV, common mode
			A	2kV, differential mode
		ANSI C62.41 - level A3	B	6kV, common & differential
	Fast transients	EN61000-4-4, Level 3	B	5/50ns, 2kV (common mode)
Enclosure immunity	Conducted RF fields	EN61000-4-6, Level 3	A	130dBµV, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3, Level 3	A	10V/m, 80-1000MHz, 80% AM
		ENV 50140	A	
	ESD	EN61000-4-2, Level 4	B	8kV contact, 15kV air

[13] Emissions requirements apply to rectifiers with the "-EC" and "-ES" options (which include filters), not the blind-mate-connector version where an external filter must be added to meet these requirements. External EMI filter reference design is included in this datasheet.

[14] Criteria A: The product must maintain performance within specification limits. Criteria B: Temporary degradation which is self recoverable. Criteria C: Temporary degradation which requires operator intervention.

Technical Specifications (continued)

Characteristic Curves

The following figures provide typical characteristics for the rectifier @25°C, 3500W/52V_{DC}

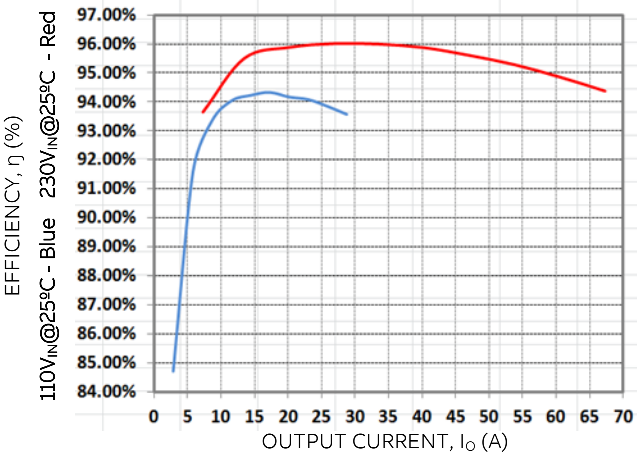


Figure 1. Rectifier Efficiency versus Output Current.

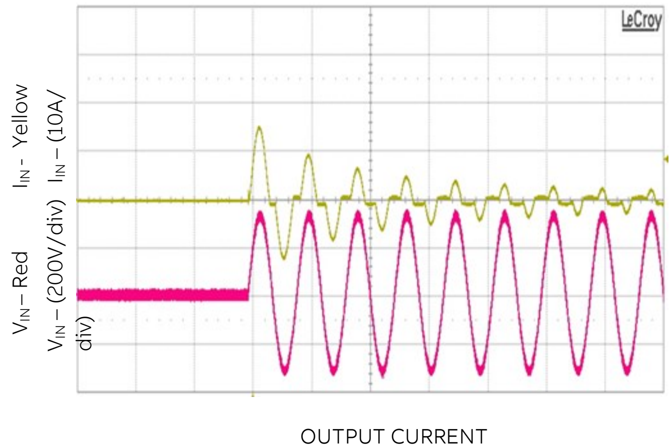


Figure 2. Inrush current V_{IN} = 230V_{AC}, 0°C phase angle

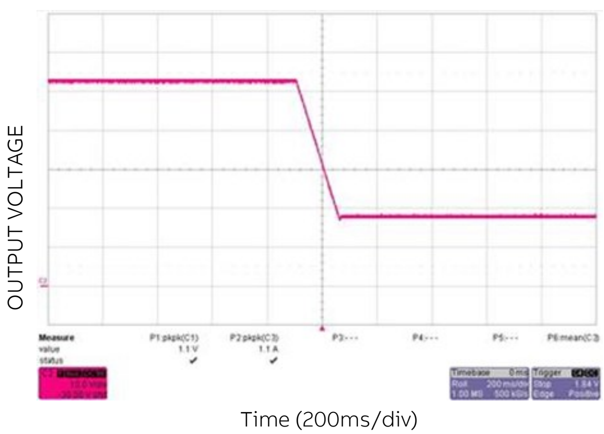


Figure 3. Main output: Output changed from 52V to 18V; commanded via I^{2}C. (For reference)

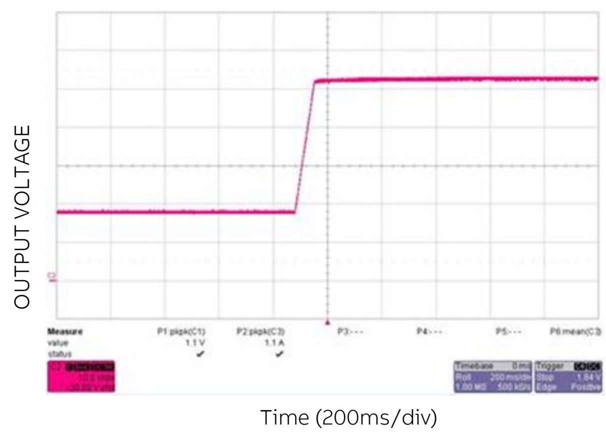


Figure 4. Main output: Output changed from 18V to 52V; commanded via I^{2}C. (For reference)

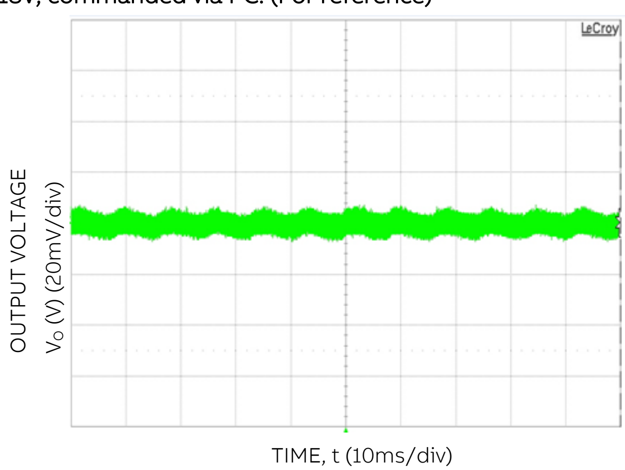


Figure 5. 52V_{DC} output ripple and noise, full load, V_{IN} = 185V_{AC}, 20MHz bandwidth

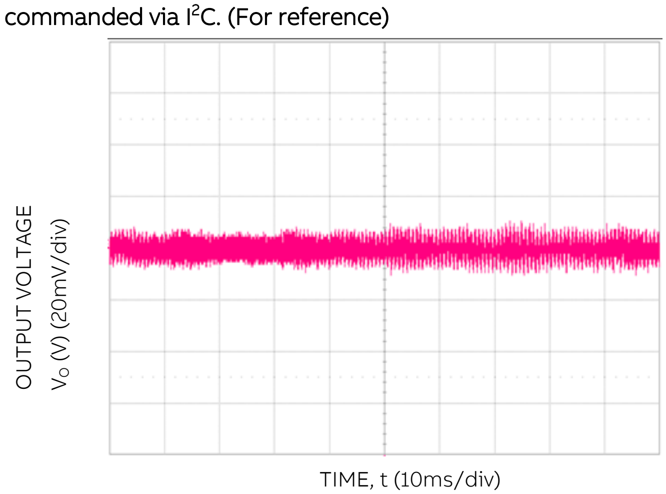


Figure 6. 5V_{DC} output ripple and noise, all full load, V_{IN} = 185V_{AC}, 20MHz bandwidth

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the CC3500AC rectifier @25°C, 3500W

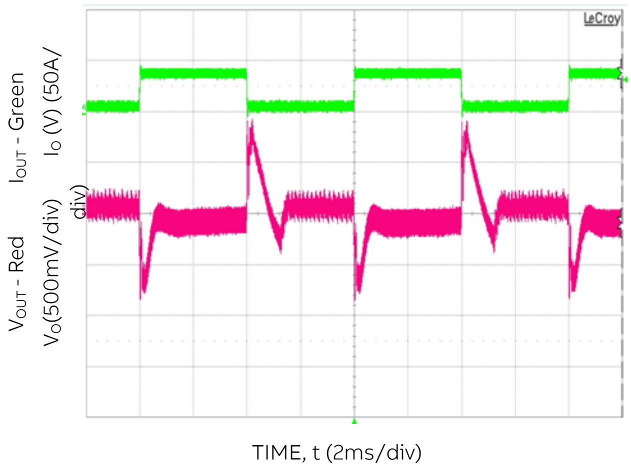


Figure 7. Transient response 52V_{DC} load step 10 – 60%, Slew rate: 1A/µs, V_{IN} = 230V_{AC}

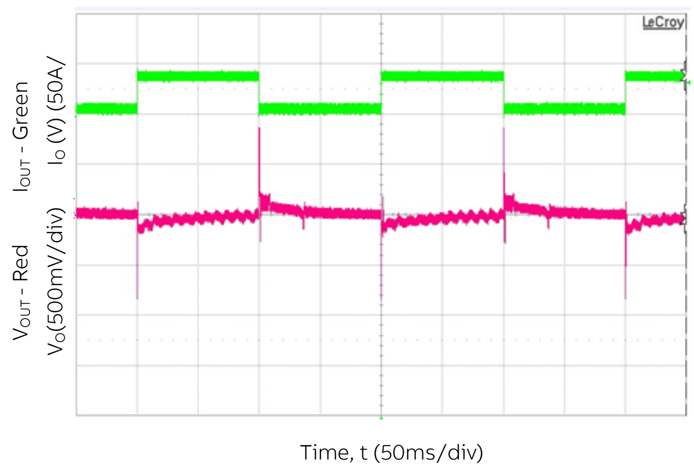


Figure 8. Transient response 52V_{DC} load step 10 – 60%, Slew rate: 1A/µs, V_{IN} = 230V_{AC}

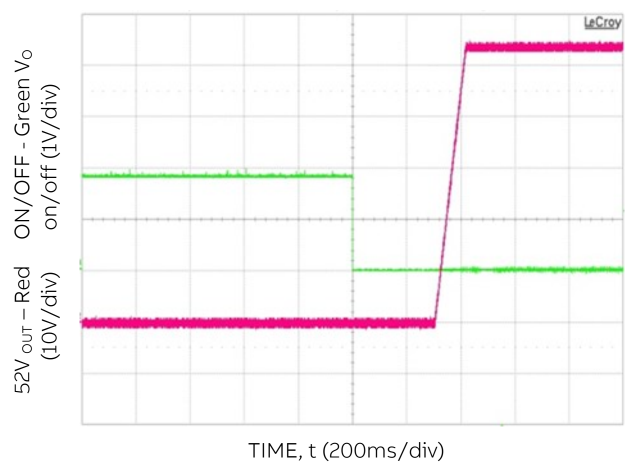


Figure 9. 52V_{DC} soft start delay when ON/OFF is asserted, V_{IN}=230V_{AC} - I²C mode.

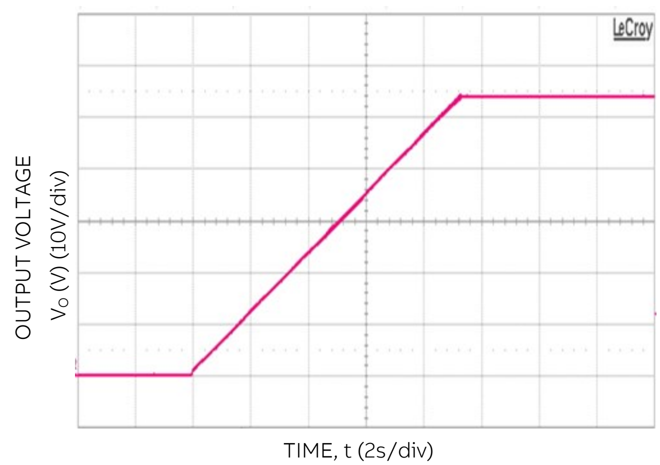


Figure 10. 52V_{DC} soft start, full load, V_{IN} = 230V_{AC} - RS485 mode with 4700µf external capacitance.

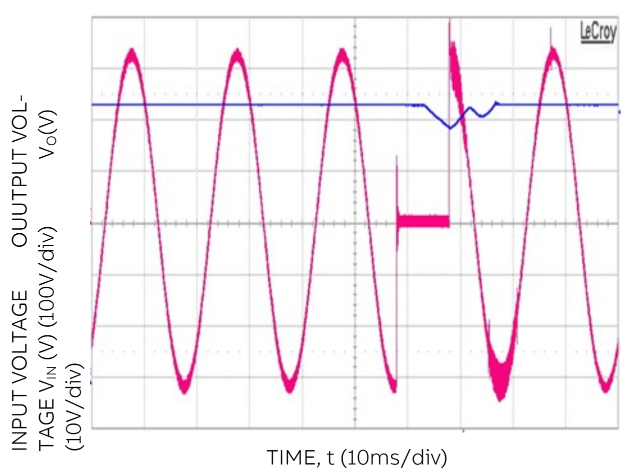


Figure 11. Ride through missing ½ cycle, full load, V_{IN} = 230V_{AC}.

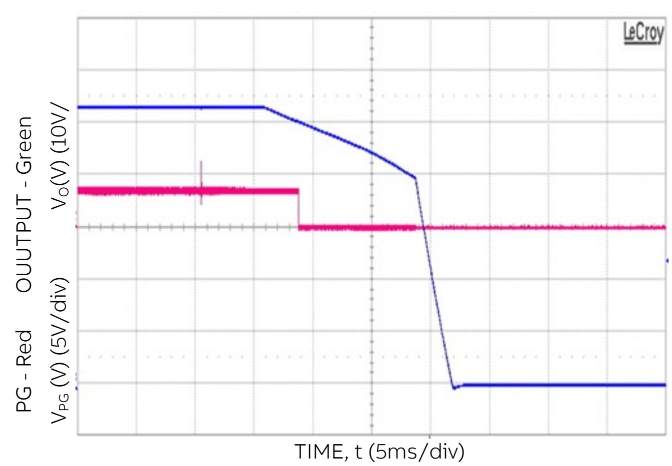


Figure 12. PG# alarmed 10ms prior to Vo < 40V, V_{IN} = 230V_{AC}, Output at Full load

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the CC3500AC rectifier @25°C, 3500W

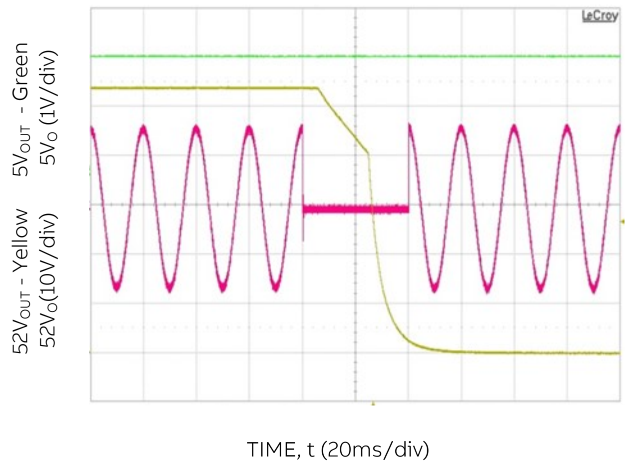


Figure 13. 40ms AC dropout @ full load, V_{IN} = 230V_{AC}.

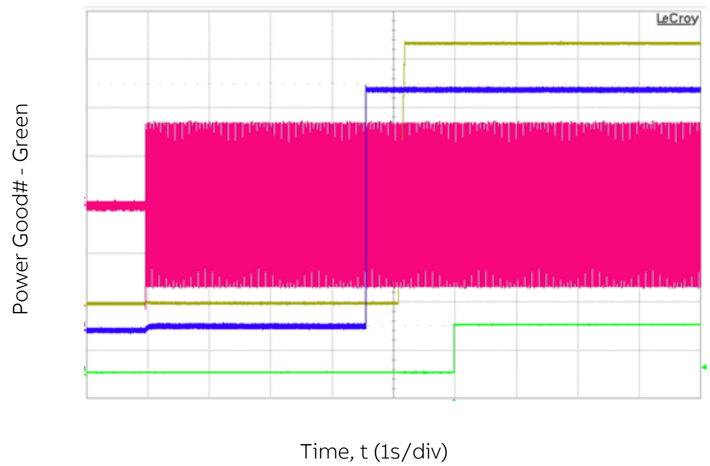


Figure 14. Turn-ON at full load V_{IN} = 230V_{AC}.

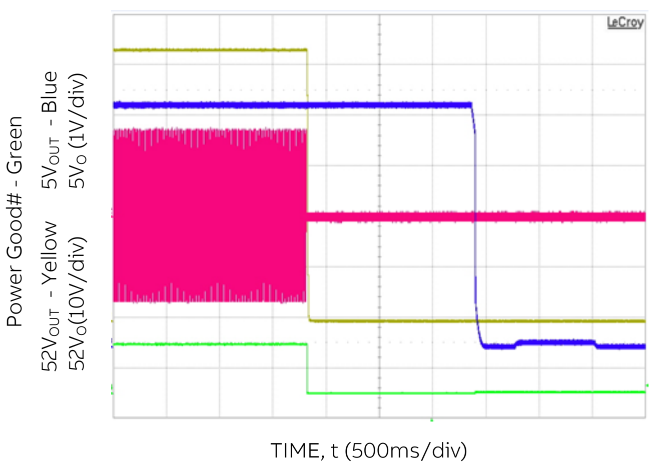


Figure 15. Turn-OFF at full load, V_{IN}=230V_{AC}

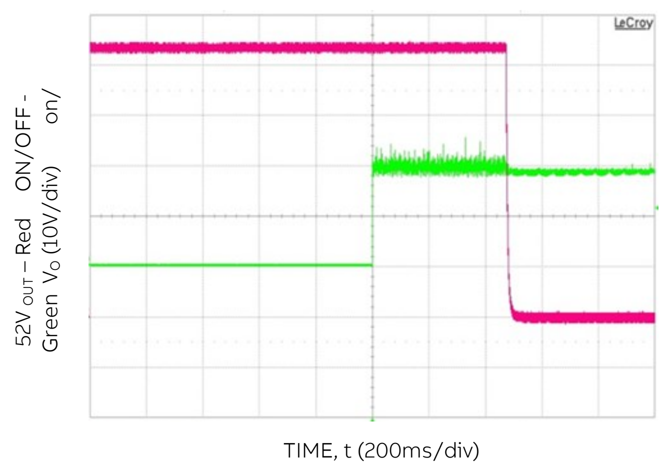


Figure 16. 52V_{DC} turn-OFF delay when ON/OFF is di-asserted, V_{IN}=230V_{AC} - I^{2}C mode.

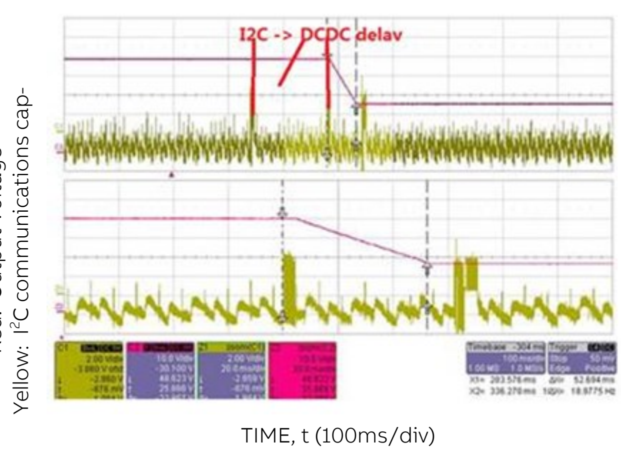


Figure 17: Time delay from sending the I^{2}C command and executing the output voltage change.

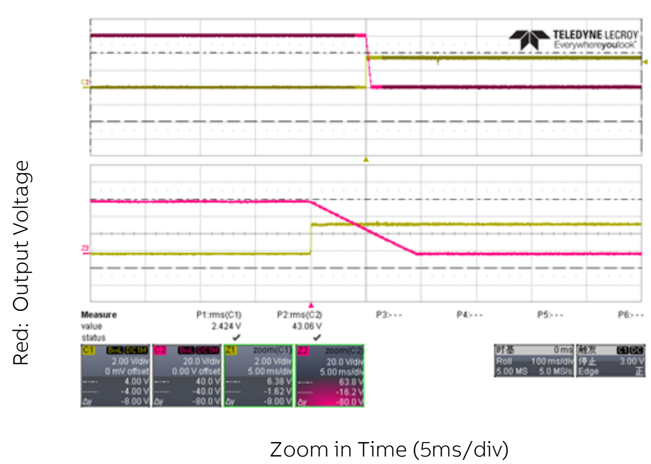
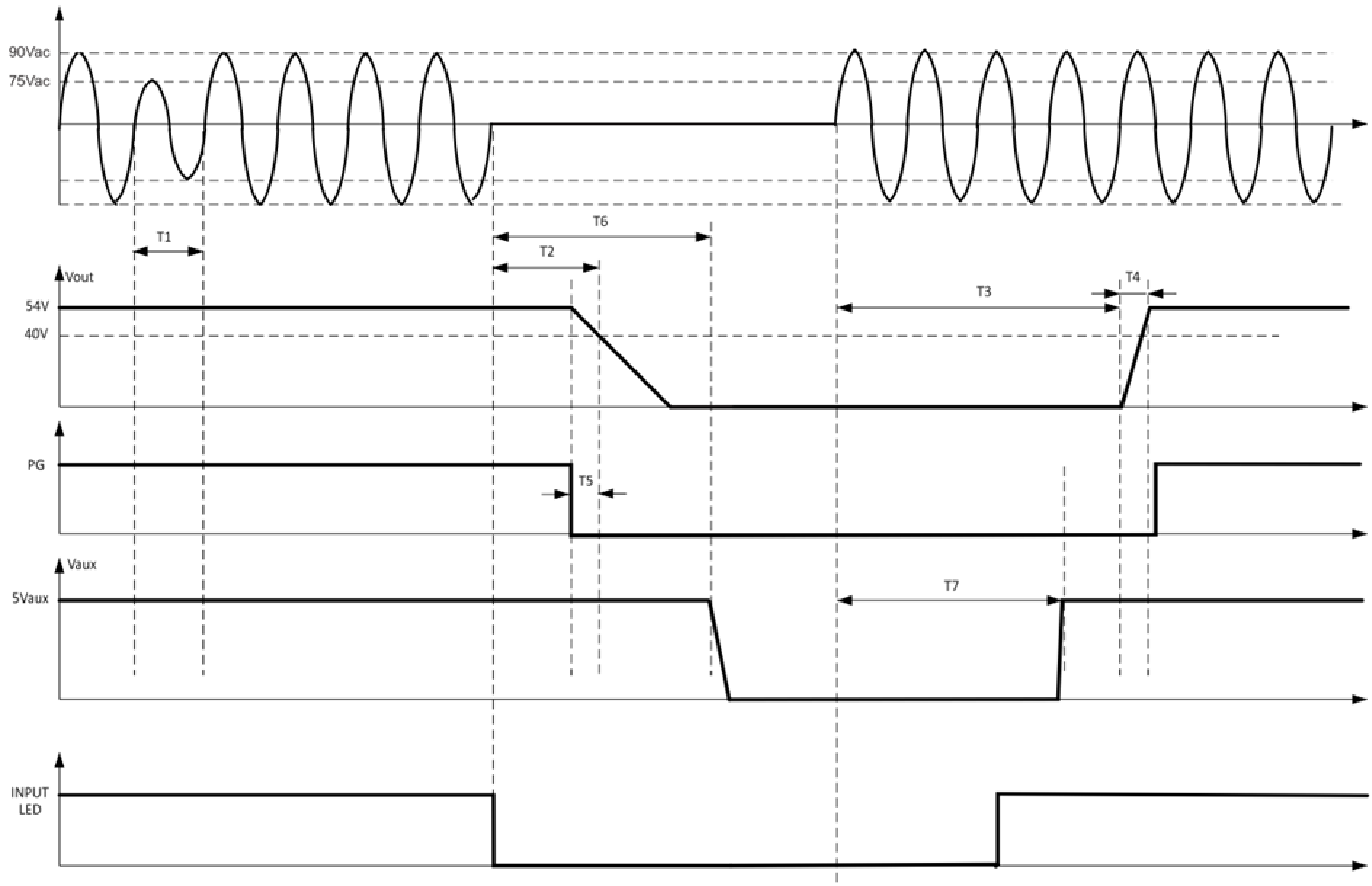


Figure 12. PG# alarmed 10ms prior to Vo < 40V, V_{IN} = 230V_{AC}, Output at Full load

Technical Specifications (continued)

Timing Diagrams

Response to input fluctuations



T1 – ride through time – 0.5 to 1 cycles [10 – 20ms] V_{OUT} remains within regulation – load dependent

T2 – hold up time - 15ms – V_{OUT} stays above $40V_{DC}$

T3 – delay time – 10s – from when the AC returns within regulation to when the output starts rising in I^2C mode

T4 – rise time - 120ms – the time it takes for V_{OUT} to rise from 10% to 90% of regulation in I^2C mode

T5 – power good warning – 3ms – the time between assertion of the PG signal and the output decaying below $40V_{DC}$.

T6 – hold up time of the $5V_{AUX}$ output @ full load – 1s – from the time AC input failed

T7 – rise time of the $5V_{AUX}$ output - 3.65ms – $5V_{AUX}$ is available at least 450ms before the main output is within regulation

Blinking of the input/AC LED – $V_{IN} < 80V_{AC}$ (the low transitioned signal represents blinking of the input LED.

Technical Specifications (continued)

Control and Status

The Rectifier provides three means for monitor/control: analog, PMBus, or the ABB Galaxy-based RS485 protocol.

Details of analog control and the PMBus based protocol are provided in this data sheet. ABB will provide separate application notes on the Galaxy RS485 based protocol for users to interface to the rectifier. Contact your local ABB representative for details.

Control hierarchy: Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (Vprog) and firmware (Vout_command, 0x21).

Using output voltage as an example, the Vprog signal pin voltage level sets the output voltage if its value is between 0.1 and 3.0V_{DC} (see the "Voltage programming" section). When the programming signal Vprog is either a no-connect (0V) or > 3V_{DC}, the output voltage is set at the default value of 52V_{DC}.

The signal pin controls the corresponding feature until the firmware command is executed. Once the firmware command has been executed, the signal pin is ignored until input power is removed and reapplied, which resets control to the signal pin. In the above example, the rectifier will no longer 'listen' to the Vprog pin after Vout_command has been executed, as long as input power is applied without interruption.

In summary, hardware signals such as Vprog are utilized for setting the initial default value and for varying the value until firmware based control takes over. Once firmware control is executed, hardware based control is relinquished so the processor can clearly decide who has control.

Analog controls: Details of analog controls are provided in this data sheet under Feature Specifications.

Signal Reference: Unless otherwise noted, all signals are referenced to LGND ("Logic Ground"). See the Signal Definitions Table at the end of this document for further description of all the signals.

LGND is isolated from the main output of the rectifier for PMBus communications. Communications and the 5V standby output are not connected to main power return (Vout(-)) and can be tied to the system digital ground point selected by the user. (Note that RS485 communications is referenced to Vout(-), main power return of the rectifier).

LGND is capacitively coupled to Earth Ground inside the rectifier where Earth Ground is also wired to the metal case). The maximum voltage differential between LGND and Earth Ground should be less than 100V_{DC}.

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > 10V_{DC} the Output LED will continue blinking.
When output voltage is < 10V_{DC}, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Auto restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the PMBus fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Restart after a latchoff: PMBus fault_response commands can be configured to direct the rectifier to remain latched off for over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin **ON/OFF** may be cycled OFF and then ON.
2. The unit may be commanded to restart via i2c through the *Operation* command by cycling the output OFF followed by ON.

Technical Specifications (continued)

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

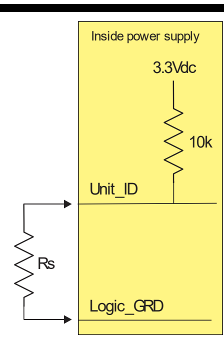
Control Signals

Protocol: This signal pin defines the communications mode setting of the rectifier. Two different states can be configured: State #1 is "Analog/PMBus" mode (I^2C) for which the protocol pin should be left a no-connect. State #2 is the RS485 mode for which a resistor value between 1kΩ and 5kΩ should be present between this pin and Vout (-).

Device address in I^2C mode: Address bits A3, A2, A1, A0 set the specific address of the µP in the rectifier. With these four bits, up to sixteen (16) rectifiers can be independently addressed on a single I^2C bus. These four bits are configured by two signal pins,

Device	Address	Address Bit Assignments (Most to Least Significant)							
		7	6	5	4	3	2	1	0
µP	40 – 4F	1	0	0	A3	A2	A1	A0	R/W
Broadcast	00	0	0	0	0	0	0	0	0
ARA	C	0	0	0	1	1	0	0	1
		MSB							LSB

A voltage divider between 3.3V and LGND configures Unit_ID. Internally a 10kΩ resistor is pulled up to 3.3VDC. A pull down resistor Rs needs to be connected between pin Unit_ID and LGND.

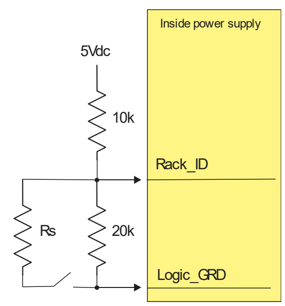


Unit_ID and Rack_ID. The least significant bit x (LSB) of the address byte is set to either <u>write [0]</u> or *read [1]*. A *write* command instructs the rectifier. A *read* command accesses information from the rectifier.

Unit_ID: Up to 10 different units are selectable.

Unit_ID	Voltage level	R_S (± 0.1%)
Invalid	3.30	
1	3.00	100k
2	2.67	45.3k
3	2.34	24.9k
4	2.01	15.4k
5	1.68	10.5k
6	1.35	7.15k
7	1.02	4.99k
8	0.69	2.49k
9	0.36	1.27k
10	0	0

A voltage divider between $5V_{DC}$ and LGND configures Rack_ID. The 10k-20kΩ divider sets the initial voltage level to $3.3V_{DC}$. A switch between each R_S value changes the Rack_ID level according to the table below.



Rack_ID	Voltage level	R_S (± 0.1%)
1	3.3	open
2	2.8	35.2k
3	2.3	15k
4	1.8	8k
5	1.4	4.99k
6	1	2.87k
7	0.5	1.27k
8	0	0

Rack_ID: Up to 8 different combinations are selectable.

Technical Specifications (continued)

Configuration of the A3 – A0 bits: The rectifier will determine the configured address based on the Unit_ID and Rack_ID voltage levels as follows (the

		Unit_ID				
		1	2	3	4	5
Rack_ID	1	0000	0001	0010	0011	
	2	0100	0101	0110	0111	
	3	1000	1001	1010	1011	
	4	1100	1101	1110	1111	
	5					
	6	0000	0001	0010	0011	0100
	7	0101	0110	0111	1000	1001
	8	1010	1011	1100	1101	1110

order is A3 – A0):

		Unit_ID				
		6	7	8	9	10
Rack_ID	1	0000	0001			
	2	0010	0011			
	3	0100	0101			
	4	0110	0111	0000	0001	0010
	5	1000	1001	0011	0100	0101
	6	1010	1011	0110	0111	1000
	7	1100	1101	1001	1010	1011
	8	1110	1111	1100	1101	1110

Unit x Rack: 4 x 4 and 5 x 3

Unit x Rack: 2 x 8 and 3 x 5

Address detection: The **Slot_ID** pin must be connected to **Vout(-)** in order to deliver output power. This connection provides a second interlock feature. This connection may be a short circuit or any resistance up to 100 kohm, to allow addressing in RS485 mode as described below.

Device address in RS485 mode: The address in RS485 mode is divided into three components; Bay_ID, Slot_ID and Shelf_ID

Bay_ID: The Unit_ID definition in I^2C mode becomes the bay id in RS485 mode.

Slot	Resistor	Voltage	Slot	Resistor	Voltage
invalid	none	3.3V	6	7.15k	1.35V
1	100k	3V	7	4.99k	1.02V
2	45.3k	2.67V	8	2.49k	0.69V
3	24.9k	2.34V	9	1.27k	0.36V
4	15.4k	2.01V	10	0	0
5	10.5k	1.68V			

Slot_ID: Up to 10 different rectifiers could be positioned across a 19" shelf if the rectifiers are located vertically within the shelf. The resistor below needs to be placed between Slot_ID and Vout (-). Internal pull-up to 3.3V is 10kΩ.

In the -EC & -ES versions, a 100 kΩ resistor is installed internally to enable the output & indicate slot no. 1. To indicate another slot number, an external

Shelf	V_{MIN}	V_{NOM}	V_{MAX}
1	2.3	2.5	2.7
2	4.7	5.0	5.3
3	7.4	7.5	7.6
4	9.5	10.0	10.5
5	11.8	12.5	13.2
6	14.2	15.0	15.8
7	16.6	17.5	18.4
8	19	20.0	21
9	21.3	22.5	23.6
10	23.8	25.0	26.3

resistor should be connected so the parallel combination is the resistance shown in the table above.

Shelf_ID: When placed horizontally up to 10 shelves can be stacked on top of each other in a fully configured rack. The shelf will generate the precision voltage level tabulated below referenced to Vout (-).

Technical Specifications (continued)

Global Broadcast: This is a powerful command because it instruct all rectifiers to respond simultaneously. A ***read*** instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth *acknowledge* bit. To be certain that each rectifier responded to the global instruction, a *READ* instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Alert Response Address (ARA): This feature enables the 'master' to rapidly determine which 'slave' rectifier triggered the Alert# signal without having to poll each rectifier one at a time. During normal operation the rectifier activates (pulls down LO) the Alert# signal line indicating that it needs attention when a 'state' change occurs. The master can determine who pulled the 'alert' line by sending out the

1	8	1		8	1	8	1	1
S	ARA address	Rd	A	My address	A	PEC	A	P

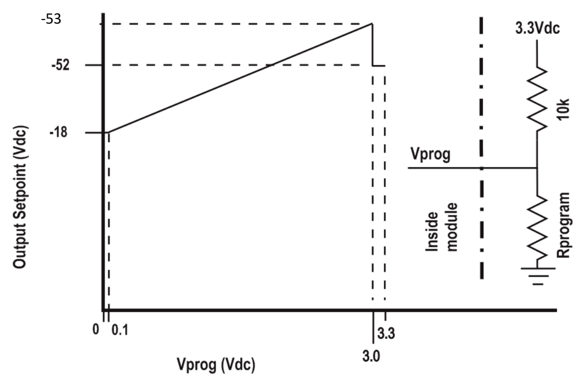
alert-response-address, address 12b, with a 'read' instruction. If the rectifier triggered the 'alert' it should respond back with its address. The instruction takes the form below;
If during the ARA response multiple rectifiers send out their addresses, then the actual address received by the master is the lowest address from the combinations of those rectifiers that responded.

The 'my address' field contains the address of the rectifier in the 7 most significant bits (msb) of the byte. The lsb of the byte is a don't care, it could be a 0 or a 1. For more information refer to the SMBus specification

The µC needs to read the actual **my address** data byte that is sent back to the master. If the **my address** data byte agrees with the address of this unit, then, and only then, the µC needs to clear (de-assert) its Alert# signal. Thus, the rectifier whose address has been sent out gets de-asserted from the joint Alert# line.

If the Alert# line is still asserted, the host should send out an ARA request again and find out who else asserted Alert#. This process needs to continue until the Alert# is released which is a clear indication that all rectifiers that asserted Alert# have had their status states read back.

Voltage programming (V_{prog}): Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Then software voltage programming overrides the hardware margin setting and the rectifier no longer listens to any hardware margin setti[...]
ex[...]
th[...]
U[...]
vo[...] ly
fr[...]
en[...] et
to[...]
o[...]



Factory default setting driven by Vprog

For the blind-mate rectifier option, the Vprog pin level can be set by an external resistor divider between an external voltage source and LGND as shown in the figure above, or by a precision voltage source connected between Vprog and LGND.

When bias power to the controller is recycled, the controller restarts into its default configuration, programmed to set the output voltage as instructed by the V_{prog} pin. Again, subsequent software commanded settings permanently override the "Vout Adjust" setting.

Before enabling a hot-plugged rectifier, the output voltage should be set to a safe level—no higher than the bus voltage, to avoid a transient or possible

Technical Specifications (continued)

Load share (Ishare): This is a single wire analog signal that is generated and acted upon automatically by rectifiers connected in parallel. Ishare pins should be connected to each other for rectifiers, if active current share among the rectifiers is desired. No resistors or capacitors should get connected to this pin.

ON/OFF: Controls the main $52V_{DC}$ output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn **ON** the rectifier. The rectifier will turn **OFF** if either the **ON/OFF** or the **Interlock** pin is released. This signal is referenced to LGND. Note that in RS485 mode the ON/OFF pin is ignored.

Interlock: This is a pin utilized for main power on/off in RS485 mode.

In RS485 mode, open this pin turns OFF main power output. connected to V_OUT (-) for the rectifier to be ON.

When open to turn off output, LED shows in standby mode. And RS485 communication is still active.

In I2C mode, this pin is ignored.

Module Present: This signal is tied to LGND inside the rectifier. It's intent is to provide a signal to the system that a rectifier is physically present in the slot.

8V_INT: Single wire connection between rectifiers, Provides bias to the DSP of an unpowered rectifier.

Status Signals

Power Good Warning (PG#): This signal is HI when the main output is being delivered and goes LO if the main output is about to decay below regulation. Note that should a catastrophic failure occur, the signal may not be fast enough to provide a meaningful warning. PG# also pulses at a 1ms duty cycle if the unit is in overload.

Fault#: A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires rectifier replacement. These faults may be due to:

- Over-temperature shutdown
- Over-voltage shutdown
- Internal Rectifier Fault

Over temp warning (OTW#): A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor.

If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the rectifier. In its default configuration, the unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

Serial Bus Communications

The I^2C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I^2C Serial bus.

All signals are referenced to 'LGND'.

Pull-up resistors: The clock, data, and Alert# lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I^2C and SMBus standards.

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across the I^2C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I^2C /SMBus specifications.

Serial Data (SDA): This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I^2C /SMBus specifications.

Technical Specifications (continued)

Digital Feature Descriptions

PMBus compliance: The rectifier is fully compliant to the Power Management Bus (PMBus) rev1.2 requirements. This Specification can be obtained from www.pmbus.org.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

The Alert# response protocol (ARA) whereby the PMBus Master can inquire who activated the Alert# signal is also supported. This feature is described in more detail later on.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

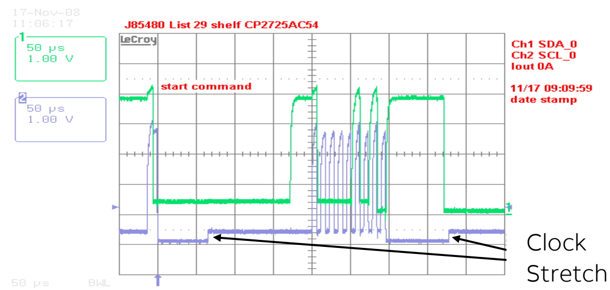
Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing an Alert# to the 'host' controller.

If a non-supported read is requested the rectifier will return 0x00h for data.

Data out-of-range: The rectifier validates data settings and sets the data out-of-range bit and Alert# if the data is not within acceptable range.

Master/Slave: The 'host controller' is always the Master. Rectifiers are always Slaves. Slaves cannot initiate communications or toggle the Clock. Slaves also must respond expeditiously at the command of the Master as required by the clock pulses generated by the Master.

Clock stretching: The 'slave' µController inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.



The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier. Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.

Figure 15. Example waveforms showing clock stretching.

I²C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The rectifiers default to the 100kHz clock rate.

Packet Error Checking (PEC): The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the desired command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

Alert#: The rectifier can issue Alert# driven from either its internal micro controller (µC) or from the I²C bus master selector stage. That is, the Alert# signal of the internal µC funnels through the master selector stage that buffers the Alert# signal and splits the

Technical Specifications (continued)

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOUT over current
- Over Temperature warning or fault
- Communication error
- PEC error
- Invalid command
- Internal faults
- Both Alert#_0 and -1 are asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled

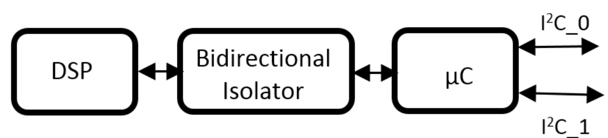
The rectifier will re-assert the Alert line if the internal state of the rectifier has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the rectifier. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

Re-initialization: The I^2C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I^2C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I^2C µController may not recognize a command sent to it. (i.e. a start condition).

Read back delay: The rectifier issues the Alert# notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the rectifier. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

Successive read backs: Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Dual, redundant buses: Two independent I^2C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the rectifier. For example, a short or an open connection in one of the I^2C lines does not affect communications capability on the other I^2C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time.



Conceptually a Digital Signal Processor (DSP) referenced to Vout(-) of the rectifier provides secondary control. A Bidirectional Isolator provides the required isolation between power ground, Vout(-) and signal/logic ground (LGND). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I2C lines to two independent system controllers.

The secondary micro controller is designed to default to I2C_0 when powered up. If only a single system controller is utilized, it should be connected to I2C_0. In this case the I2C_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I2C_0 and the other to I2C_1.

At power up the master connected to I2C_0 has control of the bus. See the section on Dual Master Control for further description of this feature.

Technical Specifications (continued)

PMBus Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

Master to Slave   Slave to Master

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1	1	8	1
	Slave Address	Rd	A	LSB	

8	1	8	1	1
MSB	A	PEC	NA	P

Block communications: When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1
Byte count = N	A	Data 1	A	Data 2	A

Block write format:

8	1	8	1	8	1	1
……….	A	Data N	A	PEC	A	P

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

Block write format:

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
……….	A	Data N	A	PEC	NA	P

Linear Data Format: The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=-9 constant exponent.

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)					Mantissa (M)										

The Linear Data Format is a two byte value with an 11 -bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^E$$

Where: V is the value, M is the 11-bit, two's complement mantissa, *E* is the 5-bit, two's complement exponent

Technical Specifications (continued)

Standard features

Supported features that are not readable: The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both the CNTL pin, and the OPERATION command, enabling or disabling the output, are supported. Other options are not supported.
Capability (0x19)	400KHz, ALERT#
PMBus revision (0x98)	1.2

Status and Alarm registers: The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear_faults command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault still persists after the clear_faults is commanded, the register bit annunciating the fault is reset again.

Adjustment Ranges

Some of the PMBus commands on the next page enable adjustment of operating parameters within the ranges specified below. If a command is received with a value outside this range, the module does not change the present setting. Instead it uses CML to indicate a communication failure.

Command	Hex Code	Default HL(LL)	Adjustment range Low	Adjustment range High
Vout_command	0x21	52	41	55
Vout_OV_fault_limit	0x40	55	42	55
Vout_OV_warn_limit	0x42	54	42	55
Vout_UV_warn_limit	0x43	40	39	55
Vout_UV_fault_limit	0x44	39	39	55
Iout_OC_fault_limit	0x46	76	0	76
Iout_OC_LV_fault_limit	0x48	39	39	55
Iout_OC_warn_limit	0x4A	75.5	0	75.5
OT_fault_limit	0x4F	110	0	150
OT_warn_limit	0x51	105	0	150
Vin_OV_fault_limit	0x55	300	185	270
Vin_OV_warn_limit	0x57	295	185	265
Vin_UV_warn_limit	0x58	180	180	265
Vin_UV_fault_limit	0x59	175	175	265

Command Descriptions

Commands are listed in numerical order, with a summary table at the end of this section.

Operation (0x01) : Turns the 52V output ON or OFF. The default state is **ON** at power up. Only the following data bytes are supported:

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To **RESET** the rectifier using this command, command the rectifier OFF, wait at least 2 seconds, and then command the rectifier back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (0x03): Clears all STATUS and FAULT registers and resets the Alert# line of the I^2C side in control. The I^2C side not in control cannot clear registers in the rectifier. This command is always executable.

If a fault still persists after the issuance of the clear_faults command, the specific registers indicating the fault first clears but then get set again to indicate that the unit is still in the fault state.

WRITE_PROTECT register (0x10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store_user_code command. The default setting of this register is enable_all_writes, write_protect 0x00h. The write_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write protect	80
Disable all writes except write_protect and OPERATION	40

Restore_Default_All (0x12): Restores all operating register values and responses to the factory default parameters set in the rectifier. The factory default cannot be changed.

Restore_default_code (0x14): Restore only a specific register parameter into the operating register section of the rectifier.

Technical Specifications (continued)

Vout_mode (0x20): This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout_command. These commands have a 16 bit mantissa. The exponent is fixed by the rectifier and is returned by this command.

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	xxxxxb

Vout_Command (0x21) : Used to dynamically change the output voltage of the rectifier. This command can also be used to change the factory programmed default set point of the rectifier by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the Vprog signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all rectifiers using the Global Address (Broadcast) feature. If only a single rectifier is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Digital programming of output voltage overrides the set point voltage configured by the **Vprog** signal pin as long as ac input power is applied continuously. The program no longer looks at the '**Vprog** pin' and will not respond to any hardware voltage settings. If ac input power is removed, the µController is reset to its default configuration, looking at the **Vprog** signal for output voltage control. In many applications, the **Vprog** pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once a Vout_Command is sent.

To properly hot-plug a rectifier into a live backplane, the system generated voltage should match either the factory adjusted firmware level or the voltage level reconfigured by the Vprog pin. Otherwise, the voltage state of the plugged in rectifier could be significantly different than the powered system.

Programmed voltage range: $18V_{DC} – 53V_{DC}$ for FB version; $18V_{DC} – 58V_{DC}$ for FB2 version.

A voltage programming example: The task: set the output voltage to $50.45V_{DC}$

This rectifier supports the linear mode of conversion specified in the PMBus specification. The supported output voltage exponent is documented in the Vout_mode (0x20) command. The exponent for output voltage setting is 2^{-9} (see the PMBus specification for reading this command). Calculate the required voltage setting to be sent; $50.45 \times 2^{9} = 25830$. Convert this decimal number into its hex equivalent: 64E6 and send it across the bus LSB first and then MSB; E664 with the trailing PEC.

Vin_ON (0x35): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns ON. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low_line or high_line mode.

Vin_OFF (0x36): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF.

The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low_line or high_line mode.

Vout_OV_fault_limit (0x40): Sets the value at which the main output voltage will shut down. The default OV_fault value is set at 60Vdc. This level can be permanently changed and stored in non-volatile memory.

Vout_OV_fault_response (0x41): This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

Restart after a latched state: Either of four restart mechanisms is available;

- The hardware pin ON/OFF may be cycled OFF and then ON.

Technical Specifications (continued)

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all rectifiers
- Toggling Off and then ON the ON/OFF signal, if this signal is paralleled among the rectifiers.
- Removing and reapplying input commercial power to the entire system.

The rectifiers should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Vout_OV_warn_limit (0x42): Sets the value at which a warning will be issued that the output voltage is too high. The default OV_warn limit is set at 56Vdc. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_warn_limit (0x43): Sets the value at which a warning will be issued that the output voltage is too low. The default UV_warning limit is set at 41Vdc. Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_limit (0x44): Sets the value at which the rectifier will shut down if the output gets below this level when not in overload (see 0x48 for overload). The default UV_fault limit is set at 36Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

Vout_UV_fault_response (0x45): Sets the response if the output voltage falls below the UV_fault_limit. The default UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

Iout_OC_fault_limit (0x46): Sets the value at which the rectifier will shut down at High Line. This level can be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 30A.

Iout_OC_fault_response (0x47): Sets the response if the output overload exceeds the OC_Fault_limit value. The default OC_fault_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The default response state can be permanently changed and stored in non-volatile memory. The response is the same for both low_line and high_line operations.

Iout_OC_LV_fault_limit (0x48): Sets the value at which the rectifier will shut down when the rectifier is in overload and the output gets below this level. The default fault limit is set at 36Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

Iout_OC_warn_limit (0x4A): Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level at high line. This level can be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 29A.

OT_fault_limit (0x4F): Sets the value at which the rectifier responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT_fault_response register.

OT_fault_response (0x50): Sets the response if the output overtemperature exceeds the OT_Fault_limit value. The default OT_fault_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

OT_warn_limit (0x51): Sets the value at which the rectifier issues a warning when the dc-sec temperature sensor exceeds the warn limit.

Technical Specifications (continued)

Vin_UV_warn_limit (0x58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV_fault_limit is 90Vac. This level can be permanently raised, but not lowered, and stored in non-volatile memory.

Vin_UV_fault_limit (0x59): Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default Vin_UV_fault_limit is set at 85Vac. This level can be permanently raised and stored in non-volatile memory

Vin_UV_fault_response (0x5A): Sets the response if the input voltage level falls below the Vin_UV_fault_limit value. The default Vin_UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory

STATUS_BYTE (0x78) : Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	Unit is busy	0
6	OUTPUT OFF	0
5	VOUT Overvoltage Fault	0
4	IOUT Overcurrent Fault	0
3	VIN Undervoltage Fault	0
2	Temperature Fault or Warning	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

STATUS_WORD (0x79): Returns status_byte as the low byte and the following high_byte.

Bit Position	Flag	Default Value
7	VOUT Fault or Warning	0
6	IOUT Fault or Warning	0
5	INPUT Fault or Warning	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0
2	N/A	0
1	OTHER	0
0	UNKNOWN Fault or Warning	0

STATUS_VOUT (0X7A): Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	VOUT_OV_WARNING	0
5	VOUT_UV_WARNING	0
4	VOUT UV Fault	0
3 - 0	X	0

STATUS_IOUT (0X7B): Returns one byte of information of output current related faults.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	IOUT OC LV Fault	0
5	IOUT OC Warning	0
4	X	0
3	CURRENT SHARE Fault	0
2	IN POWER LIMITING MODE	0
1 - 0	X	0

Bit Position	Flag	Default Value
7	VIN_OV_Fault	0
6	VIN_OV_Warning	0
5	VIN_UV_ Warning	0
4	VIN_UV_Fault	0
3	Unit OFF for low input voltage	0
2	IIN_OC_Fault	0
1 - 0	X	0

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5 - 0	X	0

The OC Fault limit sets where current limit is set. The

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4 - 2	X	0
1	Other Communication Fault	0
0	X	0

rectifier actually shuts down below the LV fault limit

Read back Descriptions

Single parameter read back: Functions can be read back one at a time using the read_word_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

1	8		1	8	1	
S	Slave address	Wr	A	Command Code	A	
1	8		1			
Sr	Slave address	Rd	A			
8	1	8	1	8	1	1
LSB	A	MSB	A	PEC	No-Ack	P

Read back error: If the µC does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read_FRU_ID (0x99,0x9A,0x9B,0x9E): Returns FRU information. Must be executed one register at a time.

1	8		1	8	1			
S	Slave address	Wr	A	Command 0x9x	A			
1	8		1	8	1			
Sr	Slave address	Rd	A	Byte count = x	A			
8	1	8	1	8	1	8	1	1
Byte_1	A	Byte	A	Byte_x	A	PEC	No-Ack	P

Mfr_ID (0x99): Manufacturer in ASCII – 6 characters maximum,

ABB – ABB Power Electronics represented as,

ABB-PE

Mfr_model (0x9A): Manufacturer model-number in ASCII – 16 characters, for this unit: CC3500AC52TZL

Mfr_revision (0x9B): Total 8 bytes, this is the product series taking the form X:YZ. Each byte is in ASCII format. The series number is read from left to right, scanned from the series number bar code on the power supply. Unused characters are filled at the end with null

Mfr_serial (0x9E): Product serial number includes the manufacturing date, manufacturing location in up to 16 characters. For example:

13KZ51018193xxx, is decoded as;
13 – year of manufacture, 2013
KZ – manufacturing location, in this case Matamoros
51 – week of manufacture
018193xxx – serial #, mfr choice

Manufacturer-Specific PMBus Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Mfr_Specific Status and alarm registers: The content and partitioning of these registers is significantly different than the standard register set in the PMBus specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of

1	8		1	8	1		
S	Slave address	Wr	A	Command Code	A		
1	8		1	8	1		
Sr	Slave address	Rd	A	Byte count = 11	A		
8	1	8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-3	A	Alarm-2	A
8	1	8	1	8	1		
Alarm-1	A	Voltage LSB	A	Voltage MSB	A		
8	1	8	1				
Current-LSB	A	Current-MSB	A				
8	1	8	1				
Temperature-LSB	A	Temperature-MSB	A				
8	1	1					
PEC	No-Ack	P					

Technical Specifications (continued)

Status_unit(0xD1): This command returns the STATUS-2 and STATUS-1 register values using the standard 'read' format.

Status-2

Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4		x
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	x

Oring fault: Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the rectifier. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus a non-destructive or'ing fault does not trigger a shutdown.

Status-1

Bit Position	Flag	Default Value
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	Service LED ON	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	x

Status_alarm (0xD2): This command returns the ALARM-3 - ALARM-1 register values.

Alarm-3

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-i2c communications fault	0
3	AC monitor communications fault	0
2	x	0
1	x	0
0	Or'ing fault	0

Alarm-2

Bit Position	Flag	Default Value
7	N/A	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	Vo lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

Alarm-1

Bit Position	Flag	Default Value
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	VOUT_out_of_limits	0
0	VIN_out_of_limits	0

Read input string (0xD4): Reads back the input voltage and input power consumed by the rectifier.

1	7	1	1	8
S	Slave address	Wr	A	Command Code 0xDC

1	1	7	1	1
A	Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte Count = 4	A	Voltage - LSB	A	Voltage - MSB	A

8	1	8	1	8	1	1
Power - LSB	A	Power - MSB	A	PEC	No-Ack	P

Technical Specifications (continued)

Read_firmware_rev [0 x D5]: Reads back the firmware revision of all three µC in the rectifier.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDD	A

1	1	7	1	1	8	1
A	Sr	Slave Address	Rd	A	Byte Count = 6	A

8	1	8	1
Primary major rev	A	Primary minor rev	A

8	1	8	1
Secondary major rev	A	Secondary minor rev	A

8	1	8	1	8	1	1
i2c major rev	A	i2c revision	A	PEC	No-ack	P

Read_run_timer [0 x D6]: This command reads back the recorded operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years of operational state.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDE	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 3	A

8	1	8	1	8	1
Time - LSB	A	Time	A	Time - MSB	A

8	1	1
PEC	No-ack	P

EEPROM record (0xD9): The µC contains 128 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xD9	A

8	1	8	1
Start location	A	Byte count	A

8	1		8	1
first_byte	A	....	last - byte	A

8	1	1
PEC	A	P

1	7	1	1	8	1
S	Slave address	Wr	A	Command 0xD9	A

8	1	8	1
Memory location	A	Byte count ≤ 32	A

1	7	1	1
Sr	Slave address	Rd	A

8	1		8	1
Byte 1	A	....	Byte ≤ 32	A

8	1	1
PEC	No-ack	P

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5 - 6	reserved	
4	Or'ing test	1=ON, 0=OFF
2 - 3	reserved	
1	Service LED	1=ON, 0=OFF
0	LED test	1=ON, 0=OFF

Technical Specifications (continued)

LEDS test ON: Will turn-ON simultaneously the front panel LEDs of the Rectifier sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the rectifier being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

LEDS test OFF: Will turn-OFF simultaneously the four front panel LEDs of the Rectifier.

Service LED ON: Requests the rectifier to *flash*-ON the Service (ok-to-remove) LED. The *flash* sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

Service LED OFF: Requests the rectifier to turn OFF the Service (ok-to-remove) LED.

OR'ing Test: This command verifies functioning of output OR'ing. At least two paralleled rectifiers are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one rectifier should be tested at a time.

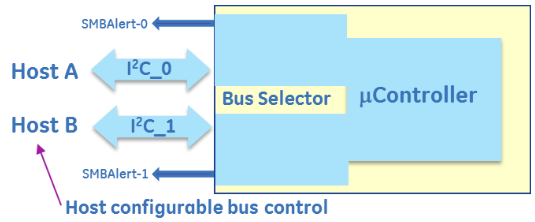
Verifying test completion should be delayed for approximately 30 seconds to allow the rectifier sufficient time to properly execute the test.

Failure of the isolation test is not considered a rectifier FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

Dual Master Control:

Two independent I^2C lines and Alert# signals provide true communications redundancy allowing two independent controllers to sequentially control the rectifier.

A short or an open connection in one of the I^2C lines does not affect communications capability on the other I^2C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time when the bus is idle.



Conceptual representation of the dual I^2C bus system.

The Alert# line exciting the rectifier combines the Alert# functions of rectifier control and du-

Bit Position	Flag	Default Value
7	Bus 1 command error	0
6	Bus 1 Alert# enabled	0
5	Bus 1 requested control	0
4	Bus 1 has control of the PS	0
3	Bus 0 command error	0
2	Bus 0 Alert# enabled	0
1	Bus 0 requested control	0
0	Bus 0 has control of the PS	1

al_bus_control.

Status_bus (0xD7): Bus_Status is a single byte read back. The command can be executed by either master at any time independent of who has control.

The µC may issue a clock stretch, as it can for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

Command Execution: The master not in control can issue two commands on the bus, take_over_bus_control and clear_faults

Take_over_Bus_Control(0xD8): This command instructs the internal µC to switch command control over to the 'master' that initiated the request.

Actual transfer is controlled by the I^2C selector section of the µC. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by issuing a STOP command. Con-

Technical Specifications (continued)

Status Notifications: Once control is transferred both Alert# lines should get asserted by the I^2C selector section of the µC. The released 'master' is notified that a STATUS change occurred and he is no longer in control. The connected 'master' is notified that he is in control and he can issue commands to the rectifier. Each master must issue a clear_faults command to clear his Alert# signal.

If the Alert# signal was actually triggered by the rectifier and not the I^2C selector section of the µC, then only the 'master' in control can clear the rectifier registers.

Incomplete transmissions should not occur on either bus.

General performance descriptions

Default state: Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store_user_code).

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled rectifiers during power up. If the overload persists beyond the 20 second delay, the rectifier will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > $36V_{DC}$ the Output LED will continue blinking.
When output voltage is < $36V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Restart after a latchoff: **PMBus** fault_response commands can be configured to direct the rectifier to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin **ON/OFF** may be cycled OFF and then ON.
2. The unit may be commanded to restart via i2c through the *Operation* command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from **latch off** to **restart.**

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the ***Status_2*** register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch -off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Auto_restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus** fault_response commands
An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Fault Management

Technical Specifications (continued)

The rectifier differentiates between internal faults that are within the rectifier and external faults that the rectifier protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

Input voltage out of range: The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

State Change Definition

A state_change is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a state_change;

- Initial power-up of the system when AC gets turned ON . This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each rectifier to reset the system_interrupt.
- Any changes in the bit pattern of either the PMBus standard STATUS or the mfr_specific STATUS registers should trigger the Alert# signal.

Smart Hot plug

The wide output capability of this rectifier requires special controls when the rectifier gets plugged into a live backplane.

During hot plug the rectifier attempts to configure itself into the bus voltage setting of a working system. When inserted into the system the output of the rectifier will be off.

- Prior to turning ON the main output, the rectifier reads the voltage present on the bus. If the bus voltage is ≥18V the rectifier will check whether Vmargin and the bus voltage are in agreement with each other.
- If there is agreement between Vmargin and the bus voltage, the rectifier will proceed to turn ON its output utilizing the delayed overcurrent shutdown during turn-ON.
- If there is no agreement between Vmargin and the bus voltage, the rectifier recognizes that the bus voltage is being controlled externally. In this case the rectifier will keep its output OFF and will wait for the controller based output voltage command. Once such a command is received from the controller, the rectifier will proceed with normal turn-ON utilizing the delayed overcurrent shutdown.
- The rectifier continues vto monitor Vmargin and the bus voltage. If no command is received from the controller, and if Vmargin and the bus voltage should agree at a later time, then the rectifier will normally turn ON it output utilizing the delayed overcurrent shutdown.
- If the bus voltage is <18V, the rectifier proceeds with normal turn-ON into either its default voltage level or the voltage level commanded externally by Vmargin.

Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the rectifier. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the rectifier is not warranted.

The goal is to identify problems early before a protective shutdown would occur that would take the rectifier out of service.

Information only alarms: The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- V_{out} out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery
- Stby out of limits
- Communication errors

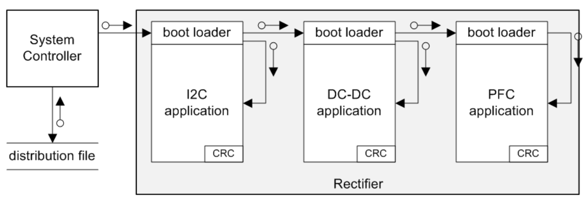
Remote upgrade

This section describes at a high-level the recom-

Technical Specifications (continued)

For some customers internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from ABB Power Electronics. This kit contains a turn-key package with the re-program firmware.

Conceptual Description: The rectifier contains three independent µControllers. The boost (PFC) section is controlled by the primary µController. The secondary DC-DC converter is controlled by the secondary µController, and I^{2}C communications are being handled by the I^{2}C Interface µController.



Each of the µControllers contains a **boot loader** section and an **application** section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the rectifier.

The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.

The Upgrade Package: This package contains the following files;

- **Manifest.txt** - The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary. This file contains the version number and the compatibility code of the upgraded program for each of the three processors

- **Program.bin** - The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file
  CC3x00AC52FB.zip

- Unzipping the contents shows the following files
  CC3x00AC52FB.pfc.bin
  CC3x00AC52FB.sec.bin
  manifest.txt

- Opening manifest.txt shows the following
  # Upgrade manifest file
  # Targets: CC3x00AC52FB PFC and SEC
  # Date: Tue 01/14/2014 14:25:09.37
  # Notes:

Status	Fault LED	Description
Idle	OFF	Normal state
In boot block	Wink	Application is good
Upgrading	Fast blink	Application is erased or programming in progress
Fault	ON	Erase or re-program failed

- Program contents
  >p, CC3x00AC52TE _P01, CC3x00AC52FB _PFC.bin,1.18
  >s, CC3x00AC52TE _S01, CC3x00AC52FB _SEC.bin,1.1

  compatibility code, new program, revision number

Upgrade Status Indication: The FAULT LED is utilized for indicating the status of the re-programming process.

Wink: 0.25 seconds ON, 0.75 seconds OFF
Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

Upgrade procedure

1. Initialization: To execute the re-programming/upgrade in the system, the rectifier to be re-programmed must first be taken OFF-line prior to executing the upgrade. If the rectifier is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation.

   Note: Make sure that sufficient power is provid-

Technical Specifications (continued)

Password(0xE0): This command unlocks the upgrade commands feature of the rectifier by sending the characters ‘UPGD’.

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE0	A	Byte count - 4	A

8	1		8	1	8	1	1
Byte 0 - U	A	…………	Byte 4 - D	A	PEC	A	P

4. Obtain a list of upgradable processors (optional)

1	8		1	8	1
S	Slave addr	Wr	A	Cmd – 0xE1	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count - n	A

8	1		8	1	8	1	1
Byte 0	A	…………	Byte n	A	PEC	No-Ack	P

Target list(0xE1) : This command returns the upgradable processors within the rectifier. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 32	A	Byte 0	A

	8	1	8	1	1
……… ……	Byte 31	A	PEC	No-Ack	P

Potential target processors are the following:

p – primary (PFC)
s – secondary (DC-DC)
i – I^2C

5. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the rectifier compatibility code of the target processor.

Compatibility code (0xE2): This read command consists of up to 32 characters defining the hardware configuration:

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE3	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count=7	A	Major revision	A

8	1	8	1	8	1	8	1
Minor revision	A	month	A	day	A	year	A

8	1	8	1	8	1	1
hrs	A	min	A	PEC	No-Ack	P

Where Target-x is an ASCII character pointing to the processor to be updated;

p – primary (PFC)
s – secondary (DC-DC)
i – I^2C

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count=7	A	Max bytes	A

8	1	8	1	8	1	8	1
ET-LSB	A	ET-MSB	A	BT-LSB	A	BT-MSB	A

8	1	8	1	8	1	1
App_CRC_LSB	A	App_CRC_MSB	A	PEC	No-Ack	P

6. Check the software revision number of the target processor in the rectifier and compare it to the revision in the upgrade. If the revision numbers are the same, or the rectifier has a higher revi-

Technical Specifications (continued)

Max Bytes	Maximum number of bytes in a data packet
ET	Erase time for entire application space (in mS)
BT	Data packet write execution time (uS)
APP_CRC	Application CRC-16 – returns the application CRC-16 calculation. Reading these register values, if the application upload CRC-16 calculation returns an invalid, provides the mismatch information to the host program. (See application status(0xE5) command)

Where the fields definition are shown as below:

This information should be used by the host processor to determine the max data packet size and add appropriate delays between commands.

8. Verify availability: The Application status command is used to verify the present state of the boot loader.

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE5	A	Target-x	A

1	8		1	8	1	8	1	1
Sr	Slave addr	Rd	A	Status	A	PEC	No-Ack	P

Application status (0xE5): Returns the Boot Loader's present status

0x00	Processor is available	0x10	Reserved
0x01	Application erased	0x20	Reserved
0x02	CRC-16 invalid	0x40	Manages downstream µC
0x04	Sequence out of order	0x80	In boot loader
0x08	Address out of range		

Status bits:
Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

9. Issue a Boot Loader command with the *enter boot block* instruction

1	7	7	7	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE6	A	Target-x	A

8	1	8	1	1
Data	A	PEC	A	P

Boot loader (0xE6): This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

Data:

1=enter boot block (software reboot)
2=erase
3=done
4=exit boot block (watchdog reboot)

Note: The target µC field is ignored for enter and exit commands. During this process if the output of the rectifier was not turned OFF the boot loader will turn OFF the output

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xE7	A	Target-x	A

8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Byte Count = n	A

8	1		8	1	8	1	1
Byte 0	A	………....	Byte n-1	A	PEC	A	P

10. Erase and program each µC using the Boot Loader command, starting with the PFC.
11. Wait at least 1 second after issuing en *erase* command to allow the µC to complete its task.
12. Use command 0xE5 to verify that the PFC µC is erased. The returned status byte should be 0x81.

Technical Specifications (continued)

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd - 0xE4	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count = 3	A

1	8	8	1	8	1	8	1	1
Seq-LSB	A	Seq-MSB	A	Status	A	PEC	No-Ack	P

Sequence number validation takes place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

14. Execute a Boot loader command to tell the PFC µC that the transfer is done.

    At the completion signal, the PFC µC should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation.

    Wait for at least 1 second to allow time for the PFC µC to calculate the error checking value.

15. Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.

16. Execute a Boot loader command to exit boot block. Upon receipt of the command the PFC µC will transfer to the uploaded application code.

17. Wait for at least 1 second.

18. Use command 0xE1 to verify that the PFC µC is now in the application code. The returned status data bte should be 0x00.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd - 0xE8	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count = 11	A

8	1		8	1	8	1	1
Byte 0	A	……… ….	Byte 10	A	PEC	No-Ack	P

19. Repeat the program upgrade for the Secondary and I^{2}C µC's, if included in the upgrade package.

Product comcode

Although the comcode number is not required for the upgrade process in its present form, it may be useful when upgrading multiple version of the same product in order to differentiate product upgrade requirements.

Product comcode (0xE8):

Error handling: The Boot loader will not start the application if errors occurred during the re-program stage. The controlling program could restart the upgrade process or terminate the upgrade and remove the offending rectifier from service.

Black box

Contents of the black box and more detailed infor-

Technical Specifications (continued)

Operational use statistics: This feature of the black box includes information on the repetition and duration of certain events in order to understand the long -term operational state of the rectifier. The events are placed into defined buckets for further analysis. For example; the rectifier records how long was the output current provided in certain load ranges.

Accessing the event records: The event records are accessed by uploading the entire contents of the black box of the rectifier into a folder assigned by the user. Within the I^2C protocol this upload is accomplished by the upload_black_box (0xF0) command described below. ABB provides a Graphical User Interface (GUI) that de-codes the contents of the black box into a set of records that can be reviewed by the user.

Upload black box(0xF0): This command executes the upload from the rectifier to a file of the user's choice.

The 100ms delay prior to the restart is mandatory to provide enough time for the rectifier to gather the required data from the secondary DSP controller.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd – 0xF0	A

8	1	8	1
Start address - msb	A	Start address - lsb	A

8	1	
Length = N (≤ 32)	A	……………….. delay 100ms

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Length ≤ 32	A	Byte 0	A

	8	1	8	1	1
…………………………	Byte N-1	A	PEC	No-Ack	P

Start Address	0 .... Byte 31
0000h	
0020h	
0040h	
.	
.	
.	
.	
.	
07E0h	

If a transmission error occurs, or if the uC did not receive the data from the DSP, the uC may set the length to 0, issue a PEC and terminate the transmission.

The data array supported by latest version of the ABB Interface Adapter is 32 x 64 comprising 2048 bytes of data.

Technical Specifications (continued)

PMBus Command Summary

Command	Hex Code	Data Field	Non-Volatile Memory Storage[19] / Default
Operation	0x01	1	Yes/80
Clear_Faults	0x03	-	
Write _Protect	0x10	1	Yes/00
Restore_default_all	0x12	-	
Restore_user_all	0x16	-	
Store_user_code	0x17	1	yes
Restore_user_code	0x18	1	
Vout_mode	0x20	1	
Vout_command	0x21	2	Yes/**
Vin_ON	0x35	2	
Vin_OFF	0x36	2	
Vout_OV_fault_limit	0x40	2	Yes / **
Vout_OV_fault_response	0x41	1	No / 80
Vout_OV_warn_limit	0x42	2	Yes / **
Vout_UV_warn_limit	0x43	2	Yes / **
Vout_UV_fault_limit	0x44	2	Yes / **
Vout_UV_fault_response	0x45	1	No / C0
Iout_OC_fault_limit	0x46	2	Yes / **
Iout_OC_fault_response[16]	0x47	1	Yes / F8
Iout_OC_LV_fault_limit	0x48	2	Yes/ **
Iout_OC_warn_limit	0x4A	2	Yes / **
OT_fault_limit	0x4F	2	Yes/ **
OT_fault_response[17]	0x50	1	Yes / C0
OT_warn_limit	0x51	2	Yes/ **
Vin_OV_fault_limit	0x55	2	No/ **
Vin_OV_fault_response	0x56	1	No/ C0
Vin_OV_warn_limit	0x57	2	Yes / **
Vin_UV_warn_limit[18]	0x58	2	Yes / **
Vin_UV_fault_limit[19]	0x59	2	No / **
Vin_UV_fault_response	0x5A	1	No / C0
Status_byte	0x78	1	
Status_word (+ byte)	0x79	1	
Status_Vout	0x7A	1	
Status_Iout	0x7B	1	
Status_Input	0x7C	1	
Status_temperature	0x7D	1	
Status_CML	0x7E	1	
Read_Vin	0x88	2	
Read_Iin	0x89	2	

Command	Hex Code	Data Field	Non-Volatile Memory Storage[15] / Default
Read_Vout	0x8B	2	
Read_Iout	0x8C	2	
Read_temp_PFC	0x8D	2	
Read_temp_dc_pri	0x8E	2	
Read_temp_dc_sec	0x8F	2	
Read_Pin	0x97	2	
Mfr_ID	0x99	6	
Mfr_model	0x9A	16	
Mfr_revision	0x9B	8	
Mfr_serial	0x9E	16	
Status_summary	0xD0	12	
Status_unit	0xD1	2	
Status_alarm	0xD2	4	
Read_input	0xD4	5	
Read_firmware_rev	0xD5	7	
Read_run_timer	0xD6	4	
Status_bus	0xD7	1	
Take_over_bus_control	0xD8		yes
EEPROM Record	0xD9	128	yes
Read_temp_exhaust	0xDA	2	
Read_ temp_inlet	0xDB	2	
Reserved for factory use	0XDC		
Reserved for factory use	0XDD		
Reserved for factory use	0XDE		
Test_Function	0xDF	1	
Upgrade commands			
Password	0xE0	4	
Target_list	0xE1	4	
Compatibility_code	0xE2	32	
Software_version	0xE3	7	
Memory_capability	0xE4	7	
Application_status	0xE5	1	
Boot_loader	0xE6	1	
Data_transfer	0xE7	≤32	
Product comcode	0xE8	11	
Upload_black_box	0xF0	≤32	

** See "Adjustment Ranges" table on previous page

[15] Yes – new value can be saved permanently using Store_user_code

[16] Only latched (0xC0) or hiccup (0xF8) are supported

[17] Only latched (0x80) or restart (0xC0) are supported

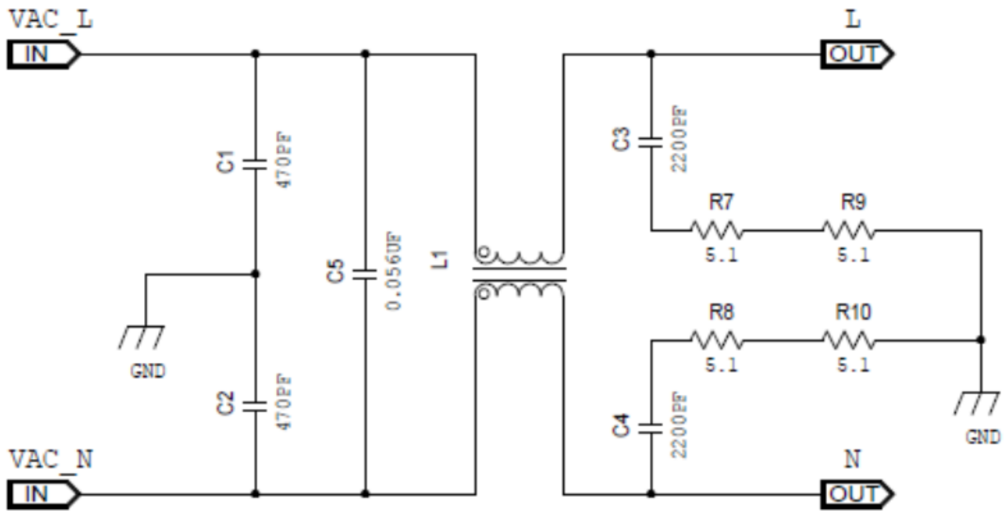
[18] Recovery set at V

[19] Recovery set at V

Technical Specifications (continued)

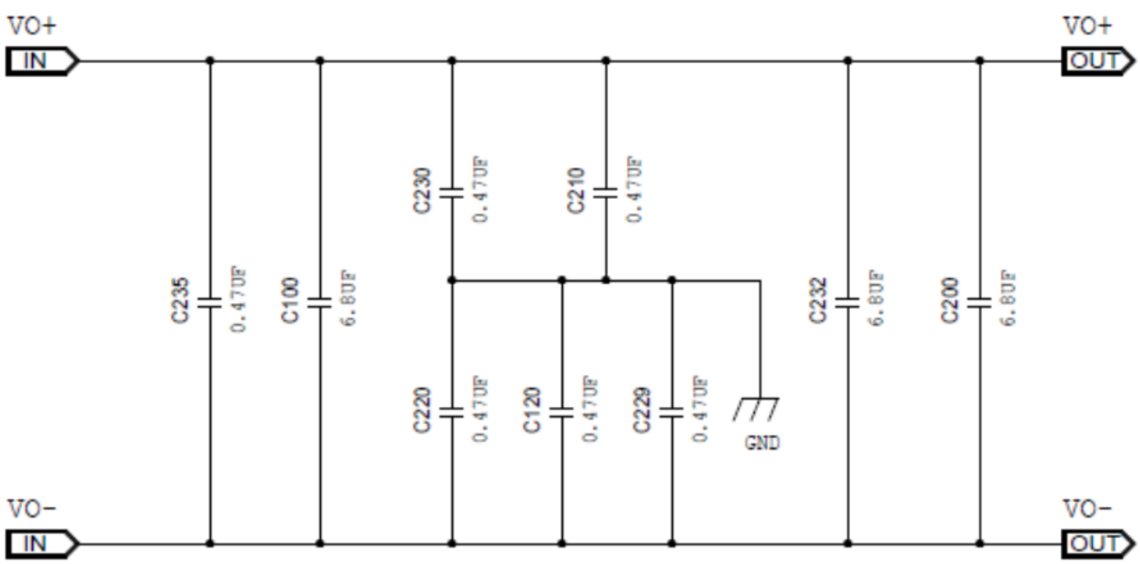
External EMI filter reference design for blind-mate connector version:

Input EMI filter circuit:



L1: 1.35UH,3 TURNS,TWO CORES CSC CK270060

Output EMI filter circuit:



Technical Specifications (continued)

Table 1: Alarm and LED state summary

	Rectifier LED State				Monitoring Signals			
Condition	AC OK Green	DC OK Green	Service Amber	Fault Red	Fault	OTW	PG	Module Present
OK	1	1	0	0	HI	HI	HI	LO
Thermal Alarm (5C before shutdown)	1	1	1	0	HI	LO	HI	LO
Thermal Shutdown	1	0	1	1	LO	LO	LO	LO
Blown AC Fuse in Unit	1	0	0	1	LO	HI	LO	LO
AC Present but not within limits	Blinks	0	0	0	HI	HI	LO	LO
AC not present[1]	0	0	0	0	HI	HI	LO	LO
Boost Stage Failure	1	0	0	1	LO	HI	LO	LO
Over Voltage Latched Shutdown	1	0	0	1	LO	HI	LO	LO
Over Current	1	Blinks	0	0	HI	HI	Pulsing[4]	LO
Non-catastrophic Internal Failure[2]	1	1	0	1	LO	HI	HI	LO
Standby in PMBUS mode(remote)	1	0	0	0	HI	HI	LO	LO
Service Request (PMBus mode)	1	1	Blinks	0	HI	HI	HI	LO
Communications Fault (RS485 mode)	1	1	0	Blinks	HI	HI	HI	LO
Standby in RS485 mode	1	0	0	0	N/A	N/A	N/A	LO

[1] This signal is correct if the rectifier is back biased from other rectifiers in the shelf .
[2] Any detectable fault condition that does not cause a shutting down. For example, ORing FET failure, boost section out of regulation, etc.
[3] Signal transition from HI to LO is output load dependent
[4] Pulsing at a duty cycle of 1ms as long as the unit is in overload.
[5] either by interlock pin or GP command

Table 2: Signal Definitions

Label	Function	Type	Description
5VA	Standby power	Output	5V at 2A provided for external use; return is LGND
8V_INT	Back bias	Bi-direct	Used to back bias the DSP from operating Rectifiers. Ref: Vout (-).
Alert#_0/1	I^2C Interrupt	Output	This signal is pulled to 3.3V via a 10kΩ resistor. Active LO.
Fault#	Rectifier Fault	Output	An open drain FET; normally HI, changes to LO.
Interlock	Interlock	Input	on/off in RS485 mode. Ref: Vout (-).
Ishare	Current Share	Bi-direct	A single wire active-current-share interconnect between rectifiers Ref: Vout (-)
LGND	Logic Ground	Input	Return for all signals unless Vout(-) is indicated in description
MOD_PRES	Module Present	Output	Short pin, see Status and Control description for further information on this signal.
ON/OFF	Output control	Input	If shorted to LGND main output is ON in Analog or PMBus mode.
OTW#	Over-Temperature Warn-ing	Output	Open drain FET; normally HI, changes to LO 5°C prior to thermal shutdown.
PG#	Power Good Warning	Output	Open drain FET; Changes to LO if an imminent loss of the main output may occur.
Protocol	Protocol select	Input	Selects communications mode. No-connect for Analog/PMBus; 1 to 5kΩ for RS485. Ref: Vout (-)
Rack_ID	I^2C address	Input	Second of 2 voltage levels selecting the A3 – A0 bits of the address byte
RS_485+	RS485 Line	Bi-direct	RS485 line +; Ref: Vout(-)
RS_485-	RS485 Line	Bi-direct	RS485 line -; Ref: Vout(-)
SCL_0/1	I^2C Line 0/1	Input	PMBus line 0/1
SDA_0/1	I^2C Line 0/1	Bi-direct	PMBus line 0/1
Shelf_ID	RS485 address	Input	Ref: Vout(-)
Slot_ID	RS485 address	Input	Requires ≤100 kΩ to enable output (internal for -EC & -ES). Ref: Vout(-)
Unit_ID	I^2C address	Input	First of 2 voltage levels selecting the A3 - A0 bits of the address byte
V_OUT(-)	Power output low side	Input	Signal return where indicated in description; 2.5A max on this pin
Vprog	Margining	Input	Changes the set point of the main output

Technical Specifications (continued)

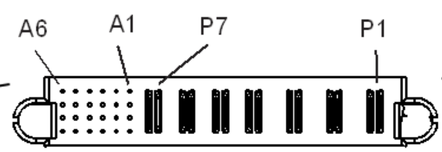
Front Panel LEDs

	Analog Mode	I²C Mode	RS485 Mode
☐ ~	←	**ON:** Input ok **Blinking:** Input out of limits	→
☐ ⎓	←	**ON:** Output ok **Blinking:** Overload	→
☐ ♨ *	**ON:** Over-temperature Warning	**ON:** Over-temperature Warning **Blinking:** Service	**ON:** Over-temperature Warning
☐ !	←	**ON:** Fault →	**ON:** Fault **Blinking:** Not communicating

*Arrow next to "hot" symbol points to the cooling side, where heat should be removed.

Blind-Mate Output Connector: TE: 3-6450832-8, or FCI: 10106262-7006001LF

Mating Connector: right angle PWB mate – all pins: TE – 1-6450872-6, FCI – 10106264-7006001LF;



	SIGNAL						OUTPUT POWER				INPUT POWER		
	6	5	4	3	2	1	P7	P6	P5	P4	P3	P2	P1
A	SCL_0	MOD_PRES	PG#	LOGIC_GRD	RS_485+	Slot_ID							
B	SCL_1	OTW#	Alert#_0	Alert#_1	RS_485-	8V_INT	V_OUT (-)	V_OUT (+)	V_OUT (+)	V_OUT (-)	EARTH (GND)	LINE-2 (Neutral)	LINE-1 (HOT)
C	SDA_0	Vprog	ON/OFF	Rack_ID	Ishare	Protocol							
D	SDA_1	Fault#	5VA	Unit_ID	Interlock	Shelf_ID							

Note: Connector is viewed from the rear positioned inside the rectifier
Signal pins columns 1 and 2 are referenced to V_OUT (–). Slot_ID and Shelf_ID are used only with RS485 communications.
Signal pins columns 3 through 6 are referenced to Logic GRD

(blue)	Last to make-first to break shortest pin
Earth	First make-last to break longest pin implemented in the mating connector

right angle PWB mate except pass-thru input power: TE – 6450874-3, FCI – 10106265-70CB001LF

Technical Specifications (continued)

Appendix

Bus transfer reporting

The events below concentrate on what happens when a clear_faults is issued. The system controller needs to be intelligent enough to inquire the status of the power supply before issuing a clar_faults. Otherwise, it would lose whatever information may be in the status registers.

	operation	Alert#1	Alert#0	status_bus	status_word	status_cml	
1	i2c1-command sent, not in control	1	0	0xC1	0x0000	0x00	
2	i2c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
3	i2c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
4	i2c1 takes over control	1	1	0x74	event1	0x00	
5	i2c1 read system status	1	1	0x74	event1	0x00	controller needs to read status before clearing the registers.
6	i2c1 issues a clear_faults	0	1	0x14	0x0000	0x00	Assuming that the event has cleared
7	i2c0 reads system status	0	1	0x14	0x0000	0x00	the Alert remains because of status_bus, not because of unit fault
8	i2c0 issues clear faults	0	0	0x10	0x0000	0x00	
9	i2c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
10	i2c0 issues clear faults	0	0	0x01	0x0000	0x00	Assuming that the event has cleared
11	i2c1 in control	0	0	0x10	0x0000	0x00	
12	i2c0 takes over control	1	1	0x47	0x0000	0x00	
13	i2c0 issues a clear_faults	1	0	0x41	0x0000	0x00	
14	i2c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
15	i2c1 in control	0	0	0x10	0x0000	0x00	
16	i2c0 issues a command	0	1	0x1C	0x0000	0x00	the command is rejected because i2c0 is not in control
17	i2c0 issues a clear_faults	0	0	0x10	0x0000	0x00	
18	i2c1 issues a bad command	1	0	0x10	0x0002	0x80	
19	i2c1 issues a clear_faults	0	0	0x10	0x0000	0x00	

Rules:
Side in control is the only one that can clear the Status registers.
The side in control cannot clear the alert of the side not in control
A power supply alarm should not set the status_bus registers

Latched status states until cleared

The following bits are sticky until cleared by the customer

Or'ing test failed or passed: I cannot see how it could be otherwise. The customer needs to delete the information (clear_faults) thus indicating that he received the information.

Restarted_ok: this bit has been removed from the requirements. PMBus latched states replace this bit.

Shutdown: must be sticky – it tells the customer that the rectifier output has been turned OFF

OV, UV, OC, input, unknown warnings & faults, CML Errors, Internal or External Fault: must be sticky

OC and OT response registers are in their own confined state. The only way these should change is by commanding the change by the controller. So theoretically they are sticky because a clear_faults should never change them.

The way to look at this is, all fault information is sticky (if the fault still persists after a clear_faults has been issued then the fault state will reassert), all operational state information is not sticky.

Technical Specifications (continued)

Mechanical Outline

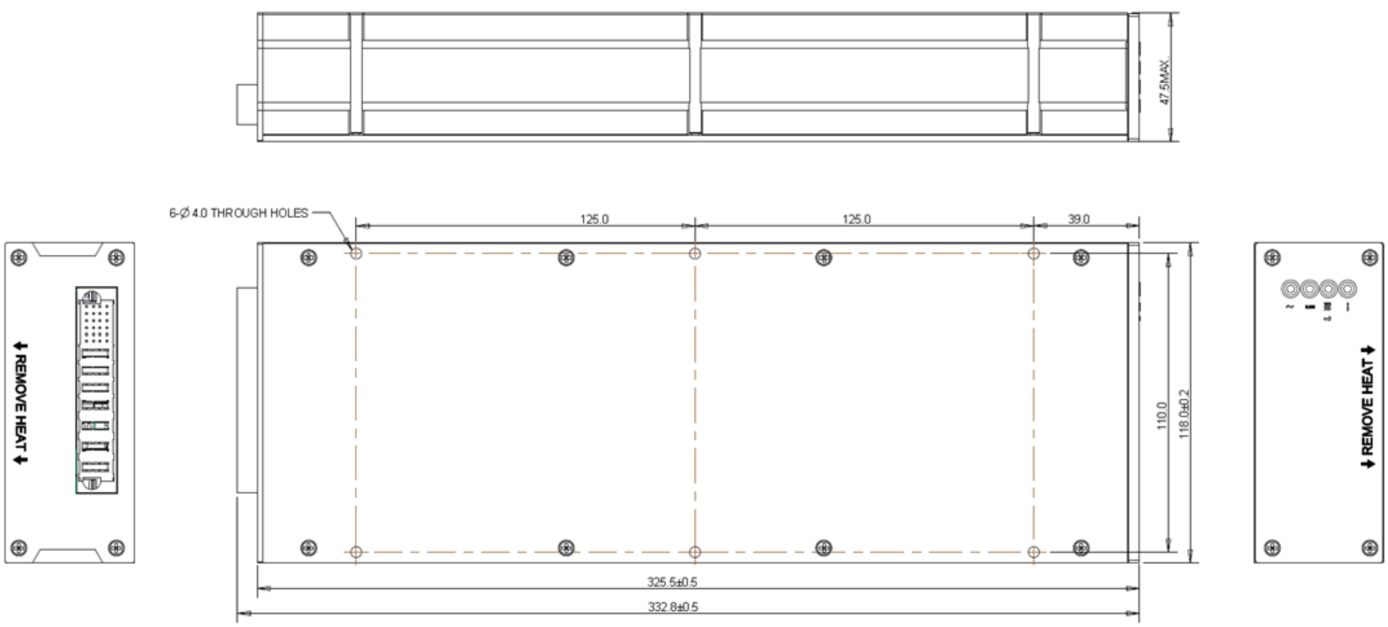
Flatness of cooling surface ±0.25 mm

Rectifier with Blind-Mate Connector

Outer dimensions (including protruding connector): 333 x 118 x 47.5 mm (13.10 x 4.65 x 1.87 in)

"Cooling side" (for heat transfer) is the large surface shown in the bottom row below, (opposite the label; closest to the Fault light (!); farthest from the blind-mate connector).

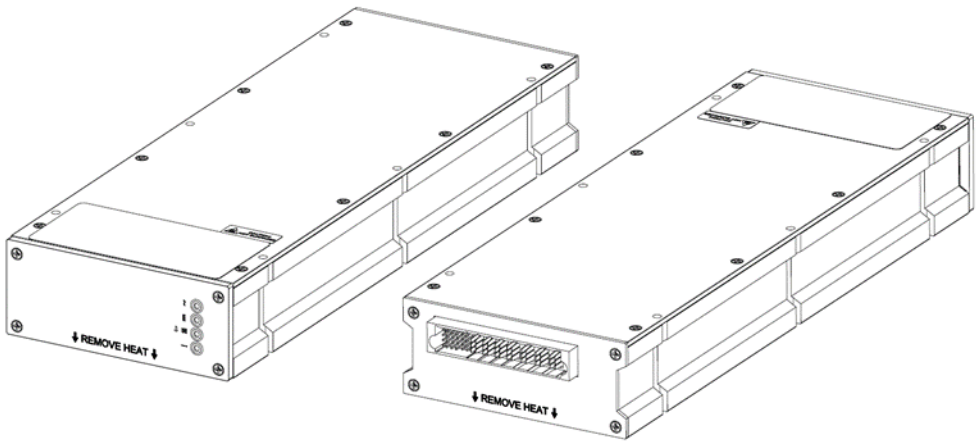
The cooling device (cold plate, warm wall or heat sink) should be placed in good thermal contact with the entire cooling surface by using thermal grease or a thermal interface pad between them.



Technical Specifications (continued)

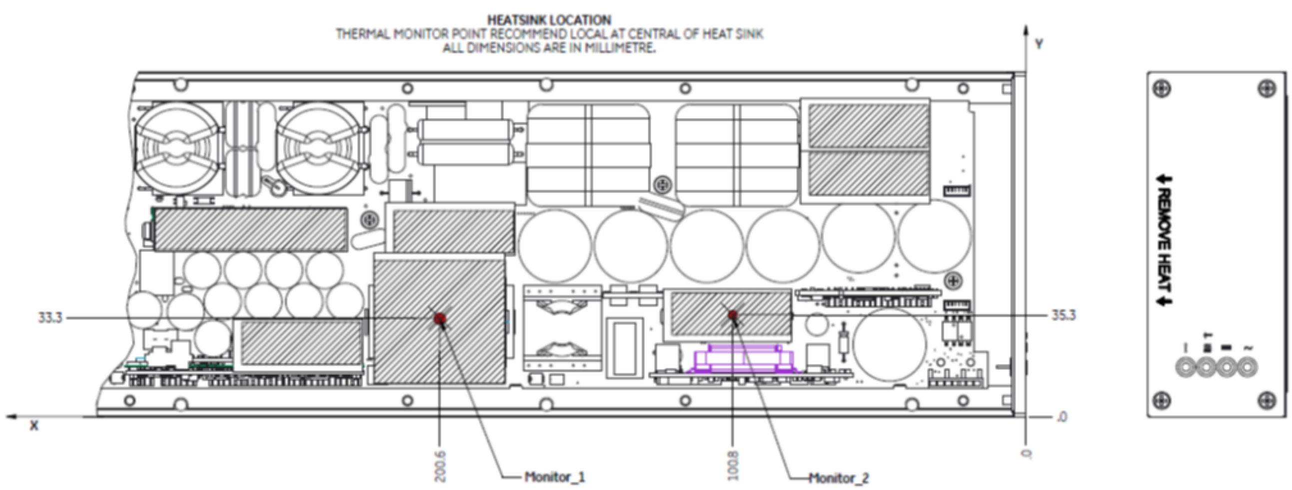
Application Notes:

Be notice that there are “REMOVE HEAT” and “↓” silkscreen on both front and rear panel to show the surface to contact with cold plate/heatsink.



Temperature Monitoring Location

The following graphic shows the heatsink location, and heatsinks are the hot spots, should maintain the surface temperature above these hot spots at the recommended operating temperature or below. normally, the HS_1 (monitor_1) the and the HS_2(monitor_2) are the hottest spot, so can assume these two hot spots surface temperature (cold plate side) as the case temperature.



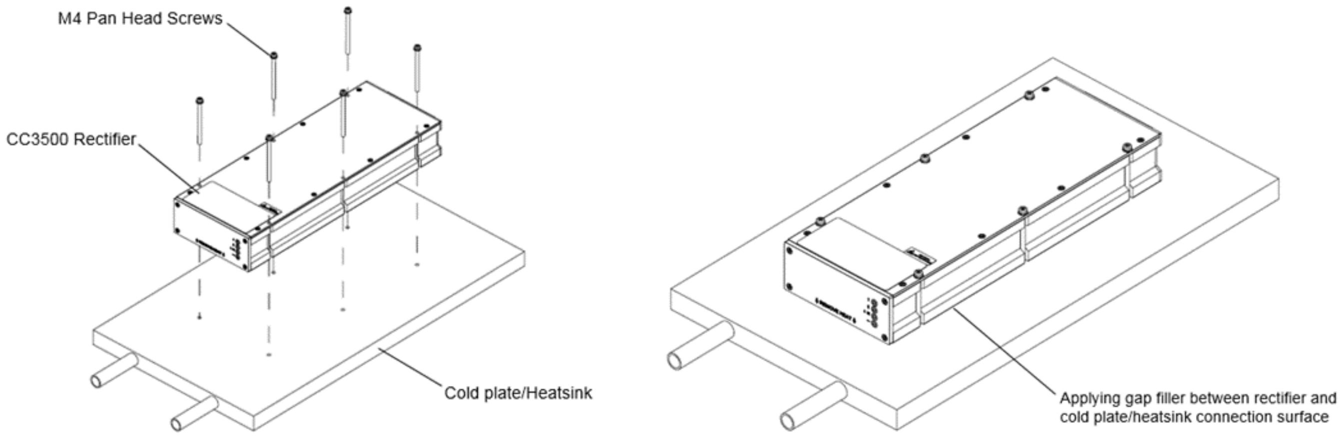
Technical Specifications (continued)

There are 2 options for installing the module with cold plate/Heatsink:

Option 1:

Install the module to the cold plate/heatsink with 6 pcs M4 pan head screw from the module top,

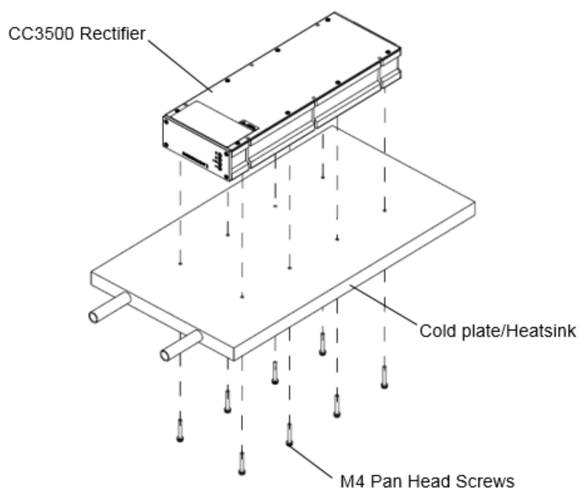
Torque to be 1.5Nm

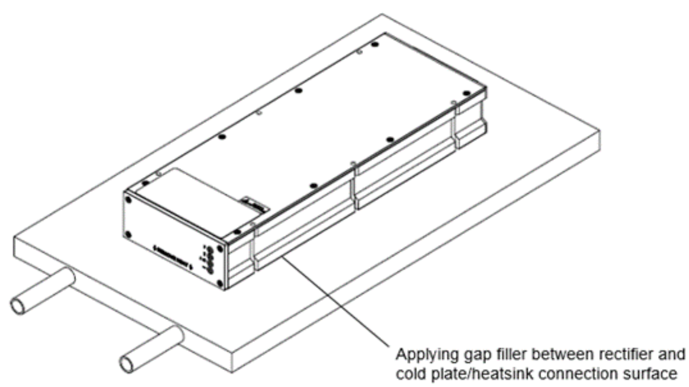


(upon figure as a reference)

Option 2:

Install the module to the cold plate/heatsink with 8 M4 pan head screw from cold plate /heatsink bottom





(upon figure as a reference)

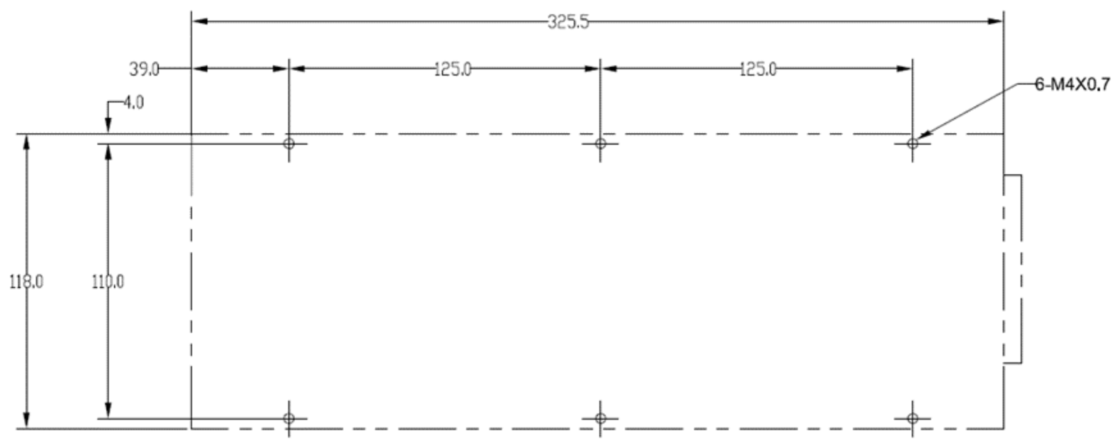
Note:
Apply gap filler, Laird T-putty 504, or other equivalent material, Thermal Conductivity is no less than 1.8 W/mK between the unit and cold plate/heatsink

Amount is 1.15 cubic inch approx. thickness is 0.02inch approx.

Technical Specifications (continued)

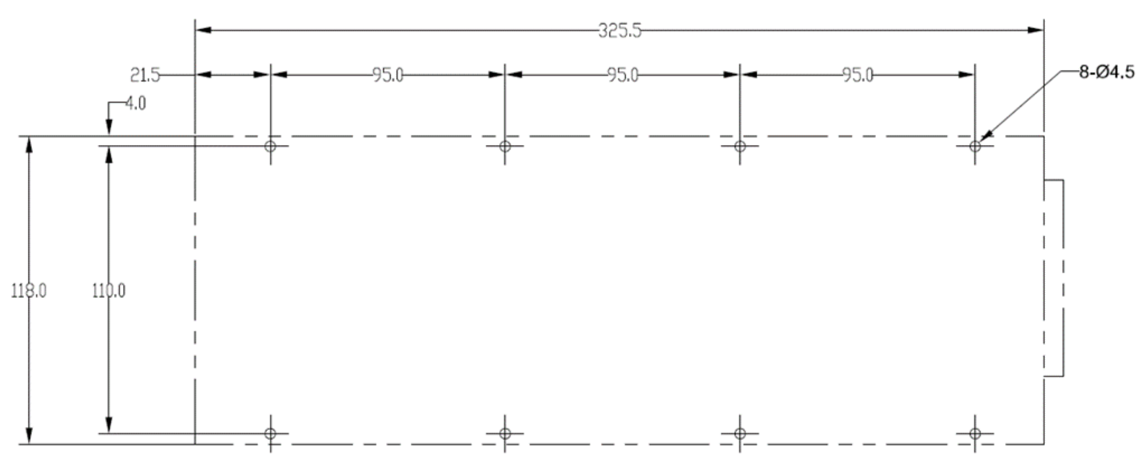
For installation option 1 :

Drill 6 M4X0.7 thread holes on cold plate/heatsink as the following drawing for installing the module.



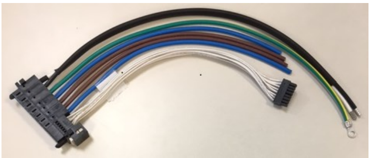
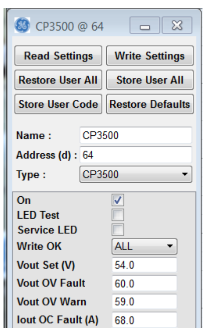
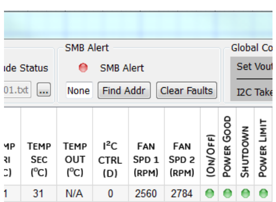
For installation option 2 :

Drill 8 ф4.5mm through holes on cold plate/heatsink as the following drawing for installing the module.



Technical Specifications (continued)

Accessories

Item	Description	Part number
	Single-unit cable assembly that mates with rectifier Blind-Mate connector. (sold as a component; equipment containing this harness requires safety certification),	850045138
	1u_CC3500_interface: Rectifier interface board. This debug tool can be used to evaluate the performance of the rectifier. The input interface is a standard IEC 320 C20 type socket. Outputs are connected via standard 0.25 fast-ons.	150039572
	Isolated Interface Adapter Kit – interface between a USB port and the I^2C connector on the rectifier interface board. Includes a cable set to the PC and to the 1u_CC3500_interface board above.	150036482
 	The site below downloads the ABB Digital Power Insight™ software tools, including the pro_GUI. When the download is complete, icons for the various utilities will appear on the desktop. Click on pro_GUI.exe  to start the program after the download is complete. https://electrification.us.abb.com/publibrary/family/embedded-power/software Graphical User Interface Manual; The GUI download created a directory  In that directory start the DPI_manual.pdf file.	Free download

Technical Specifications (continued)

Ordering Information

Please contact your ABB Sales Representative for pricing, availability and optional features.

Item	Description	Comcode
CC3500AC52TZL	Rectifier with blind-mate connector (short model); V_O range 42-53V, 3725W	1600281282A

Table 4: Device Codes

ABB
601 Shiloh Rd.
Plano, TX USA

Go.ABB/Industrial

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