UMFT4233HPEV Evaluation Module Datasheet

Version 1.0

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1 Introduction

UMFT4233HPEV is a high speed USB Type-C to Multipurpose UART/JTAG/SPI/I2C serial interface evaluation module with two Type-C™ USB PD ports.

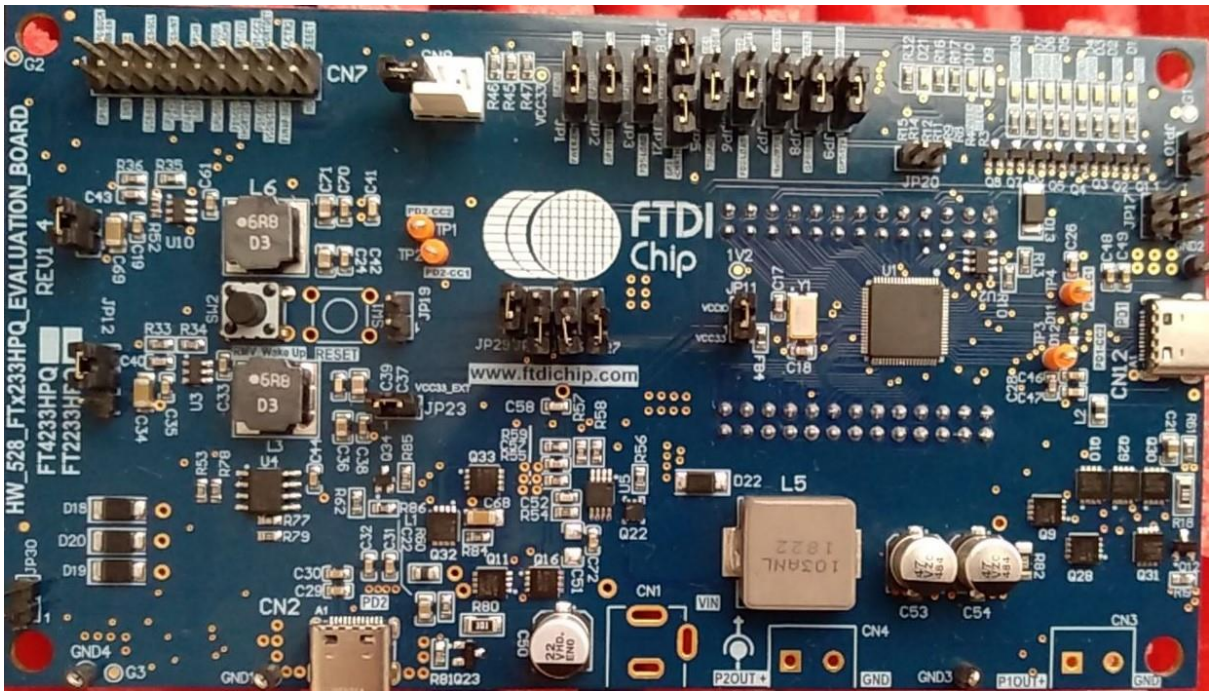


Figure 1 - UMFT4233HPEV Evaluation Board

The module has 138.5mm x 77mm dimensions, with a pair of Type-C power delivery ports incorporated into it. The first of these ports is capable of sink (receiving power) and source (providing power) roles. The second port serves only as a sink. Both of these ports are able to support the 5V, 9V, 12V, 15V and 20V power delivery object (PDO) profiles - as defined in revision 3.0 of the USB Power Delivery specification. These profiles may be configured via an external EEPROM memory, with LED indicators signifying which PDO profile is in use.

While the first port offers USB data transmission plus power delivery, the second port only has power delivery capabilities. A power pass-through function has also been included, with the input power on the second port being passed to the first port. External control of power delivery policy can be achieved using the on-board I2C interface and the GPIO pins. GPIO pins allow adjustment of the voltage regulator and the load switch.

1.1 EVB Features

- Two Type-C™ USB PD ports with,
  - PD1 which is an initial sink port that supports power role swap and USB Data which is USB 2.0 compliant.
  - PD2 which is a sink-only port.
- Supports the self-powered and bus-powered operation.
- Configurable Jumper options to enable/disable pass-through circuit or voltage-dc regulator.
- Supports external control of power delivery policy using the on-board I2C and GPIO pins. Configurable jumper options to connect I2C.
- LED indicators for every GPIO pin and PWREN#, SUSPEND# signals and System Power.
- Test points for all power supply voltages, core voltages, PD VBUS voltages and CC Voltages.
- External EEPROM for configurable options.

2 Typical Applications

- Rapid USB integration into existing electronic systems
- Prototyping platform for USB interface on new system
- USB Bridge with Type-C/PD3.0 (chargers and devices).
- Up to 60W power application delivery via USB PD and/or Type-C port.
- USB to multi-port JTAG, SPI and I2C interfaces
- USB to multi-port asynchronous serial interfaces

2.1 Driver Support

The FT4233HP requires USB drivers (listed below), available free from https://www.ftdichip.com, which are used to make the FT4233HP appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT4233HP through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater
- Android(J2xx)

For driver installation, please refer to the installation guides on our website: https://ftdichip.com/document/installation-guides/.

2.2 USB Bridge Features

For information on USB Bridge features, please refer to FT4233HP Datasheet.

3 Electrical Details

The UMFT4233HPEV Evaluation Board is a 138.5mm by 77mm 4-layered printed circuit board.

The key features are labelled in Figure 2 and Figure 3. Refer to Table 1 for the label description.

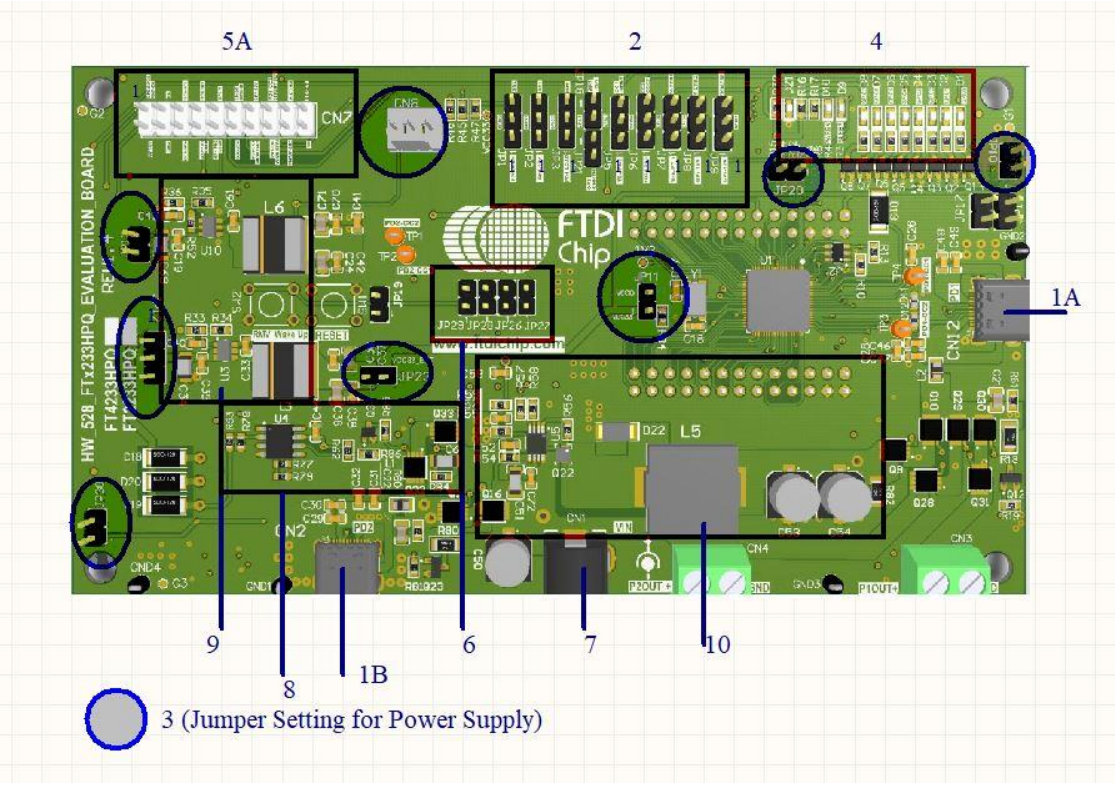


Figure 2 - UMFT4233HPEV Evaluation Board – Top View

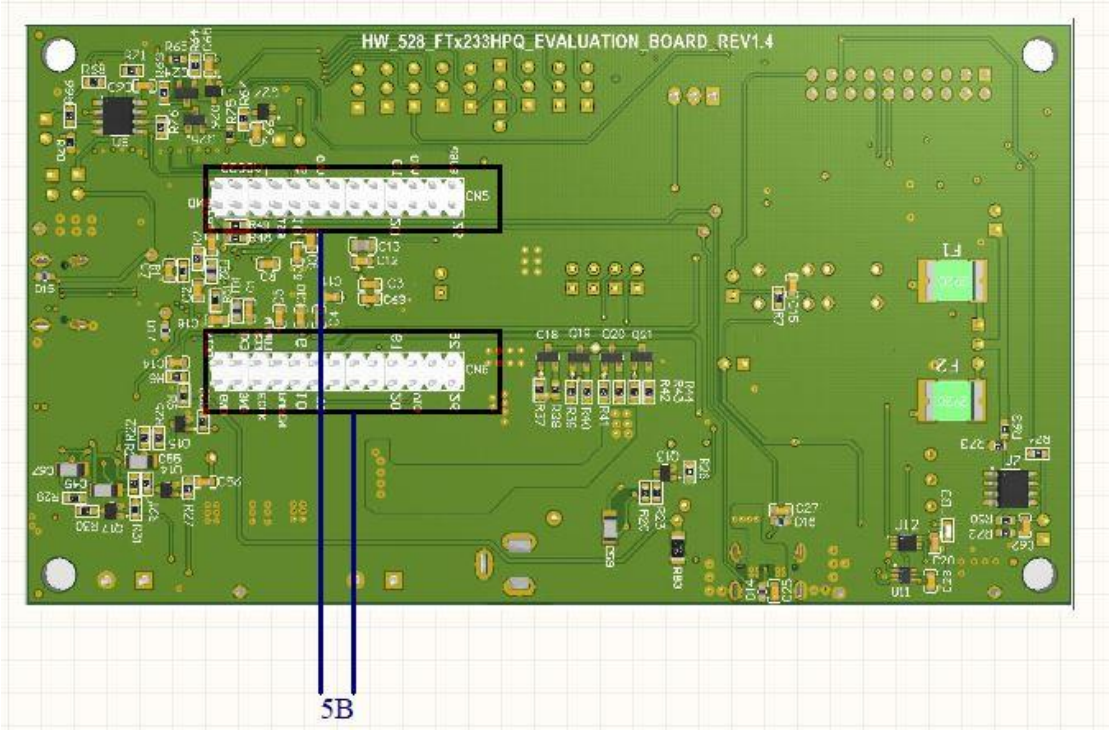


Figure 3 - UMFT4233HPEV Evaluation Board – Bottom View

Label	Description
1A	PD Port 1 for sink or dual role
1B	PD Port 2 for sink only
2	Jumper Setting for GPIOs control of power profile
3	Jumper Setting for Power Supply
4	LEDs indication for the USB and GPIO control of power profile
5A	Functional interface connector for Ext MCU
5B	Connector for 4 channels multipurpose interface
6	Push Button switch and jumper setting for remote wakeup
7	DC power socket (Not mounted)
8	5V detector circuit
9	DC-DC converters for FT4233HPQ and other circuits
10	Voltage Regulator for PD source supply

Table 1 – UMFT4233HPEV Evaluation Board – Electrical Details – Label & Description

3.1 Power

The UMFT4233HPEV Evaluation board provides two power sources:

a) 3.46V for FT4233HPQ and most other circuits on the board.
b) 3.3V for LED drivers

The reason why 3.46V is needed for FT4233HPQ is due to the adding of schottky diode between Vcc_PD/PD1_Vconn and VCC33 to prevent CC leakage during initial attach when the chip is not yet fully powered up. Refer to section 4.6.5 of FT4233HPQ datasheet for more detail.

Both power sources are derived from bus power via PD port1 or port 2. There is also provision of DC plug footprint as an option to obtain power from external power supply or DC power adaptor.

Table 2 shows the jumper pin detail for power configuration.

Jumper pin	Name	Description	Default jumper setting
JP11-1	VCC33	3.46V supply	JP11-1 short to JP11-2
JP11-2	VCCIO	Power to the VCCIO of FT4233HPQ	
JP12-1	PD1_PD2_DCIN_VBUS	sources from PD1_Vbus or PD2_Vbus or DC power adaptor	JP12-1 short to JP12-2
JP12-2	V_SYS_INPUT	Power input to the 3.46V DC to DC converter (U3)	
JP12-3	V_SYS_INPUT_EXT	Sources from external power supply	
JP13-1	V_SYS_INPUT	Power input to the 3.3V DC to DC converter (U10)	JP13-1 short to JP13-2
JP13-2	VIN	Power input to the 3.3V DC to DC converter (U10)	
JP23-1	V3.3	Output from the 3.46V DC to DC converter (U3)	JP23-1 short to JP23-2
JP23-2	VCC33	3.46V supply	
JP10-1	-	Power input to comparator U9	Open
JP10-2	VCC33	3.46V supply	
JP20-1	-	Power input to the PD1 and PD2 external Vconn control circuit	Open
JP20-2	VCC_3V3	3.3V supply	
JP30-1	VCC33	3.46V supply	Open
JP30-2	-	Power input to comparator U7	
CN8-1	VCC_3V3	VCC_3V3 pin	Open
CN8-2	GND	GND pin	Open
CN8-3	VCC33	VCC33 pin	Open

Table 2 - Jumper Pin Details for Power

USB Bus-Powered:

The power configuration for power deriving from the PD ports should be as follows:

JP12 pin1 should be connected to JP12 pin2 –This is to route the power from either PD1 or PD2 to the U3 and U10 DC to DC converter. Refer to Figure 5 in Section Schematics.

JP11 pin 1 should be connected to JP11 pin2 – This is to provide power to VCCIO of FT4233HPQ. Refer to Figure 6 in Section Schematics.

USB Self-Powered:

The power configuration for power deriving from the external DC power should be as follows:

JP12 pin1 should be connected to JP12 pin2 –This is to route the power from DC jack CN1 to the U3 and U10 DC to DC converter. Refer to Figure 5 in Section Schematics.

JP11 pin 1 should be connected to JP11 pin2 – This is to provide power to VCCIO of FT233HPQ. Refer to Figure 6 in Section Schematics.

Precaution: Take note that PD charger shall not be plugged into the PD2 port during Self-powered mode.

3.2 GPIO

The GPIOs from FT4233HPQ are used to control the load switch as well as the voltage regulator on the board in accordance to the PD power profile used during PD negotiation between the charger and the charging device. It can also be allowed external MCU access through an I2C slave interface with jumper setting. Table 3 shows the overview on the jumper configuration of GPIOs.

Jumper Pin	Name	Description	Default jumper setting
JP1-1	GPIO0-BuckPWR-EN	To enable/disable the voltage regulator (U5) and the load switch from voltage to PD1_Vbus (Q9,Q10,Q15)	JP1-1 short to JP1-2
JP1-2	GPIO0	Output from FT4233HPQ	
JP1-3	I2CS-SDA	I2C data (slave)	
JP2-1	GPIO1-9V	To control the resistor divider on the voltage regulator for 9V generation	JP2-1 short to JP2-2
JP2-2	GPIO1	Output from FT4233HPQ	
JP2-3	I2CS-SCL	I2C clock (slave)	
JP3-1	GPIO2-PD1-LOAD	To control the PD1 load switch to route the Vbus from PD1 to the CN3 for monitoring.	JP3-1 short to JP3-2
JP3-2	GPIO2	Output from FT4233HPQ	
JP3-3	I2CS-INT	I2C Interrupt (slave)	
JP5-1	GPIO3-M	To JP18 and JP21	JP5-1 short to JP5-2
JP5-2	GPIO3	Output from FT4233HPQ	
JP5-3	PD1_CC1_SHORTDET	Output from external Vconn short detection circuit	
JP6-1	GPIO4_PD2-LOAD	To control the PD2 load switch to route the Vbus from PD2 to the voltage regulator and pass-through path	JP6-1 short to JP6-2
JP6-2	GPIO4	Output from FT4233HPQ	
JP6-3	PD1_CC2_SHORTDET	Output from external Vconn short detection circuit	
JP7-1	GPIO5-DISCHR	To control the discharge circuit on	JP7-1 short to

		PD1_Vbus	JP7-2
JP7-2	GPIO5	Output from FT4233HPQ	
JP7-3	PD1_EXT_VCON_CTRL1	To enable the external Vconn power for PD1 CC1	
JP8-1	GPIO6-15V	To control the resistor divider on the voltage regulator for 15V generation	JP8-1 short to JP8-2
JP8-2	GPIO6	Output from FT4233HPQ	
JP8-3	PD1_EXT_VCON_CTRL2	To enable the external Vconn power for PD1 CC2	
JP9-1	GPIO7-12V	To control the resistor divider on the voltage regulator for 12V generation	JP9-1 short to JP9-2
JP9-2	GPIO7	Output from FT4233HPQ	
JP9-3	FSWAP_SRC	Output from Fast Role Swap circuit	
JP18-1	GPIO3-CHRTH	To control the load switch to route the negotiated power from PD2 to PD1	JP18-1 short to JP18-2
JP18-2	GPIO3-M	-	
JP19-1	RESET#	Active low reset to FT4233HPQ	Open
JP19-2	RESET	To connector CN7-19	
JP21-1	GPIO3-20V	To control the resistor divider on the voltage regulator for 20V generation	Open
JP21-2	GPIO3-M	-	

Table 3 - Jumper Configuration details for GPIO

3.3 Connectors

Connectors CN5, CN6 and CN7 for functional interface are detailed in Table 4, Table 5 and Table 6.

Connector Pin	Name (FT4233HPQ)	Description
CN5-1	VCC33	To power FT4233HPQ from external source, remove JP23
CN5-2	GND	Ground
CN5-3	VCC33	To power FT4233HPQ
CN5-4	GND	Ground
CN5-5	VCC33	To power FT4233HPQ
CN5-6	GND	Ground
CN5-7	ADBUS0	FT4233HPQ ADBUS0 pin
CN5-8	RESET#	FT4233HPQ RESET# pin
CN5-9	ADBUS2	FT4233HPQ ADBUS2 pin
CN5-10	ADBUS1	FT4233HPQ ADBUS1 pin
CN5-11	VCCIO	To power FT4233HPQ VCCIO from external source, remove JP11
CN5-12	ADBUS3	FT4233HPQ ADBUS3 pin
CN5-13	ADBUS5	FT4233HPQ ADBUS5 pin
CN5-14	ADBUS4	FT4233HPQ ADBUS4 pin
CN5-15	ADBUS7	FT4233HPQ ADBUS7 pin
CN5-16	ADBUS6	FT4233HPQ ADBUS6 pin
CN5-17	BDBUS1	FT4233HPQ BDBUS1 pin
CN5-18	BDBUS0	FT4233HPQ BDBUS0 pin
CN5-19	BDBUS3	FT4233HPQ BDBUS3 pin
CN5-20	BDBUS2	FT4233HPQ BDBUS2 pin
CN5-21	VCCIO	To power FT4233HPQ VCCIO
CN5-22	BDBUS4	FT4233HPQ BDBUS4 pin
CN5-23	BDBUS6	FT4233HPQ BDBUS6 pin
CN5-24	BDBUS5	FT4233HPQ BDBUS5 pin
CN5-25	SUSPEND#	FT4233HPQ SUSPEND# pin
CN5-26	BDBUS7	FT4233HPQ BDBUS7 pin

Table 4 - Connection Pin details of CN5

Connector Pin	Name (FT4233HPQ)	Description
CN6-1	PD1_PD2_DCIN_VBUS_1	Power from PD1/PD2/ext DC
CN6-2	GND	Ground
CN6-3	V_SYS_INPUT_EXT_1	External DC
CN6-4	GND	Ground
CN6-5	EECS	EEPROM Chip Select
CN6-6	EECLK	Clock to EEPROM
CN6-7	EEDATA	EEPROM data I/O
CN6-8	PWREN#	FT4233HPQ PWREN# pin
CN6-9	DDBUS7	FT4233HPQ DDBUS7 pin
CN6-10	DDBUS6	FT4233HPQ DDBUS6 pin
CN6-11	DDBUS5	FT4233HPQ DDBUS5 pin
CN6-12	VCCIO	To power FT4233HPQ VCCIO
CN6-13	DDBUS4	FT4233HPQ DDBUS4 pin
CN6-14	DDBUS3	FT4233HPQ DDBUS3 pin
CN6-15	DDBUS2	FT4233HPQ DDBUS2 pin
CN6-16	DDBUS1	FT4233HPQ DDBUS1 pin
CN6-17	DDBUS0	FT4233HPQ DDBUS0 pin
CN6-18	CDBUS7	FT4233HPQ CDBUS7 pin
CN6-19	CDBUS6	FT4233HPQ CDBUS6 pin
CN6-20	CDBUS5	FT4233HPQ CDBUS5 pin
CN6-21	CDBUS4	FT4233HPQ CDBUS4 pin
CN6-22	VCCIO	To power FT4233HPQ VCCIO from external source, remove JP11
CN6-23	CDBUS3	FT4233HPQ CDBUS3 pin
CN6-24	CDBUS2	FT4233HPQ CDBUS2 pin
CN6-25	CDBUS1	FT4233HPQ CDBUS1 pin
CN6-26	CDBUS0	FT4233HPQ CDBUS0 pin

Table 5 - Connector Pin details of CN6

CN7 connector pin detail is shown in Table 6. This can be either used for debugging or as an interface to an external MCU.

Connector Pin	Name	Description
CN7-1	GPIO0-BUCKPWR-EN	To enable/disable the voltage regulator (U5) and the load switch from voltage to PD1_Vbus (Q9,Q10,Q15)
CN7-2	GPIO1-9V	To control the resistor divider on the voltage regulator for 9V generation
CN7-3	N/A	-
CN7-4	GND	Ground
CN7-5	I2CS-SCL	I2C clock from external MCU
CN7-6	I2CS-SDA	I2C data from external MCU
CN7-7	I2CS-INT	I2C Interrupt from external MCU
CN7-8	GPIO2-PD1-LOAD	To control the PD1 load switch
CN7-9	GPIO3-M	To control the load switch for the pass-through path and resistor divider on the voltage regulator for 20V
CN7-10	GPIO4-PD2-LOAD	To control the PD2 load switch
CN7-11	GPIO5-DISCHR	To control discharge circuit for PD1_VBUS
CN7-12	GPIO6-15V	To control the resistor divider on the voltage regulator for 15V generation
CN7-13	GPIO7-12V	To control the resistor divider on the voltage regulator for 12V generation
CN7-14	PD1_CC1_SHORTDET	Output from external Vconn short detection circuit
CN7-15	PD1_CC2_SHORTDET	Output from external Vconn short detection circuit
CN7-16	PD1_EXT_VCON_CTRL1	To enable the external Vconn power for PD1 CC1
CN7-17	PD1_EXT_VCON_CTRL2	To enable the external Vconn power for PD1 CC2
CN7-18	FSWAP_SRC	Output from Fast Role Swap circuit

CN7-19	RESET	To the reset pin of FT4233HPQ
CN7-20	N/A	-

Table 6 - Connector Pin details of Ext MCU (CN7)

PRECAUTION: Do not plug in any external MCU module to CN7 if operating in internal MCU mode.

3.4 Remote Wakeup

Remote wakeup is achieved by issuing high to low pulse to the following pins of each channel interface of FT4233HPQ through the Push Button switch (SW2). See Figure 4.

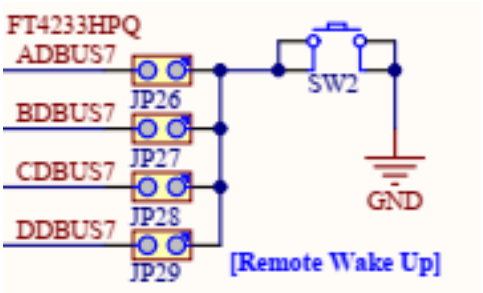


Figure 4 - Remote Wakeup Diagram

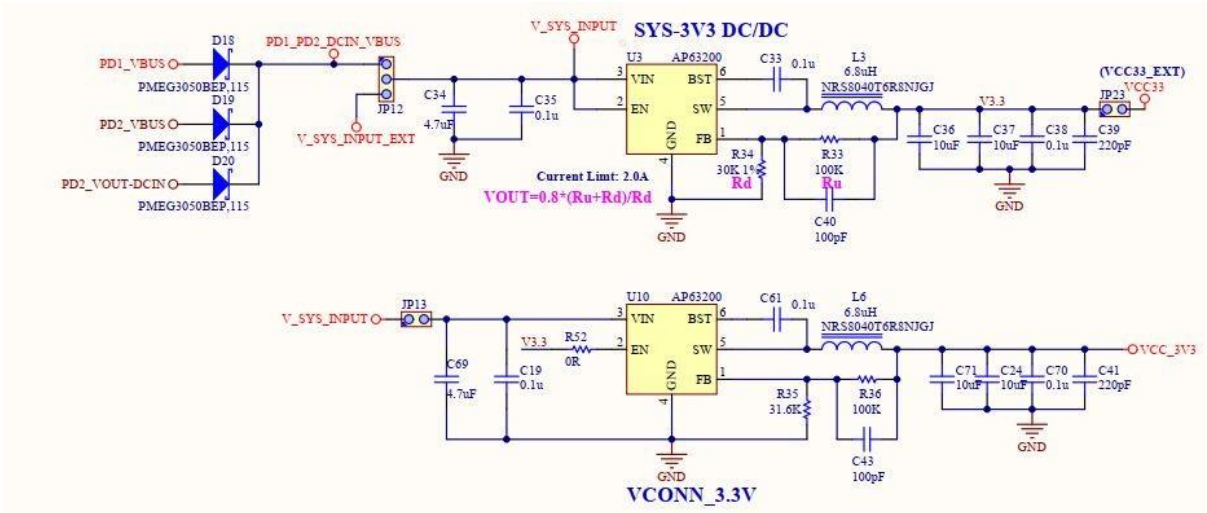
To enable remote wakeup, see Table 7.

FT4233HPQ	Jumper Setting
ADBUS7	Short pin1 to pin2 of JP26
BDBUS7	Short pin1 to pin 2 of JP27
CDBUS7	Short pin1 to pin2 of JP28
DDBUS7	Short pin1 to pin2 of JP29

Table 7 - Jumper Settings for Remote Wakeup

3.5 Schematics

Figure 5 to Figure 10 show the various elements of the schematic.



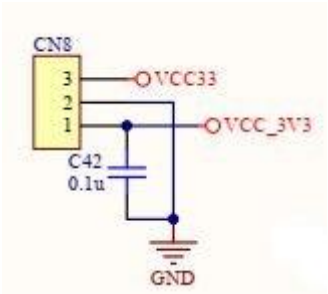


Figure 5 - DC to DC Converter for 3.46V and 3.3V from Vbus or External Power Supply

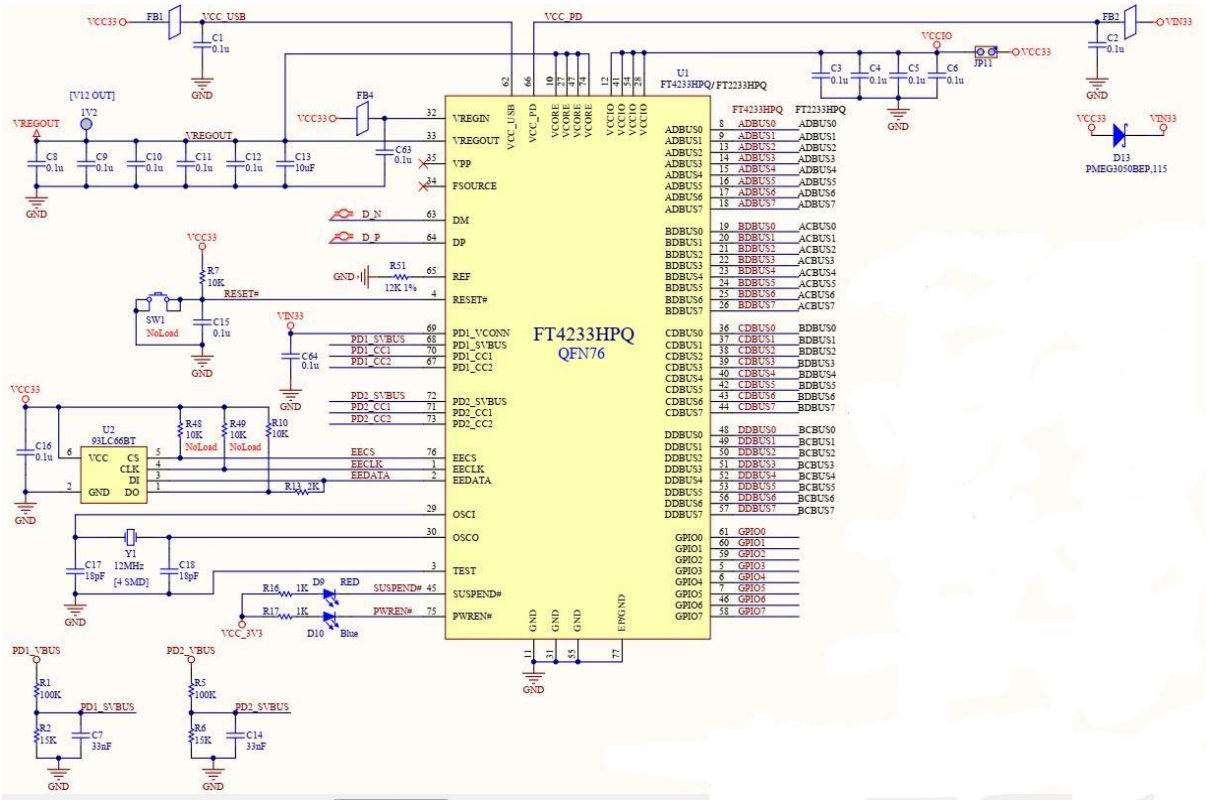


Figure 6 - FT4233HPQ IC

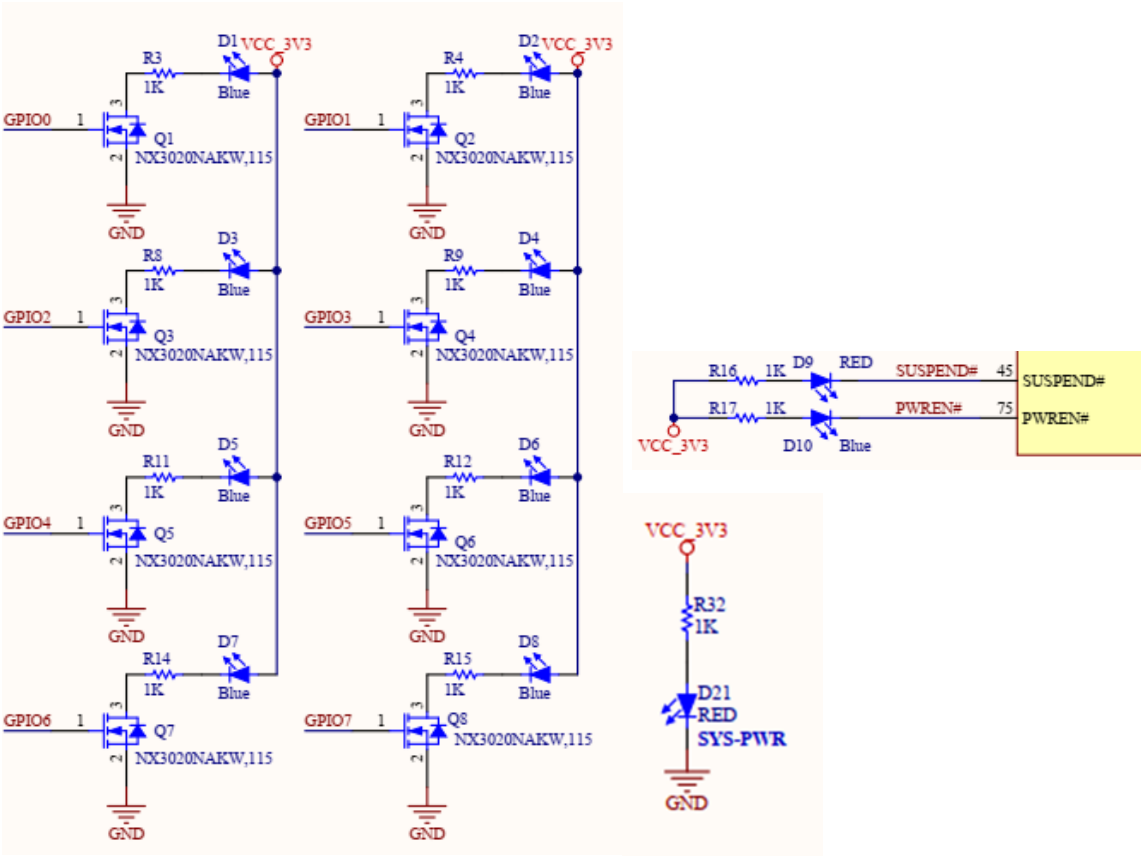
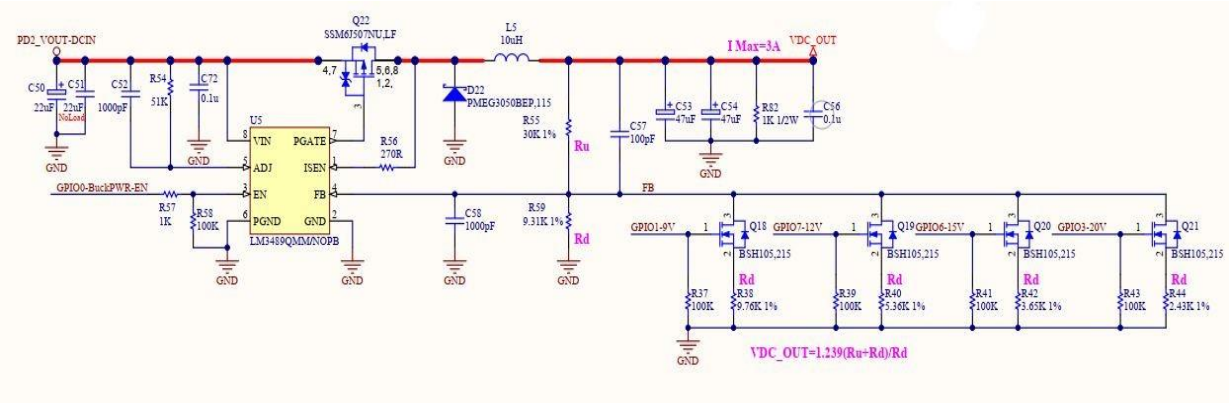


Figure 7 - LED Driver Circuit for Power, GPIO and USB Activity



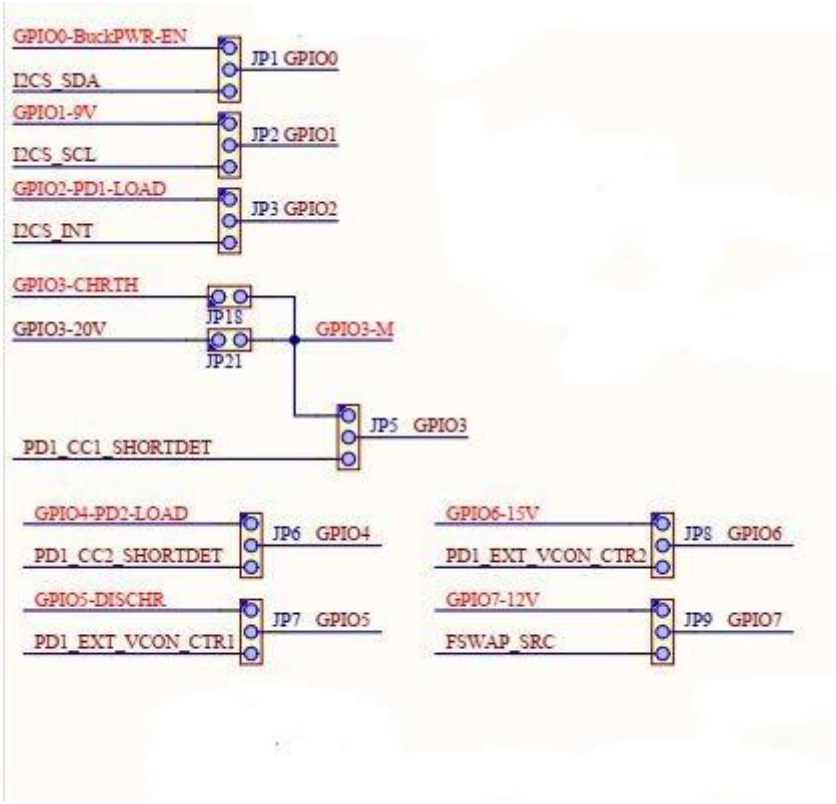


Figure 8 - Voltage Regulator for PD Profile Configurable with GPIOs

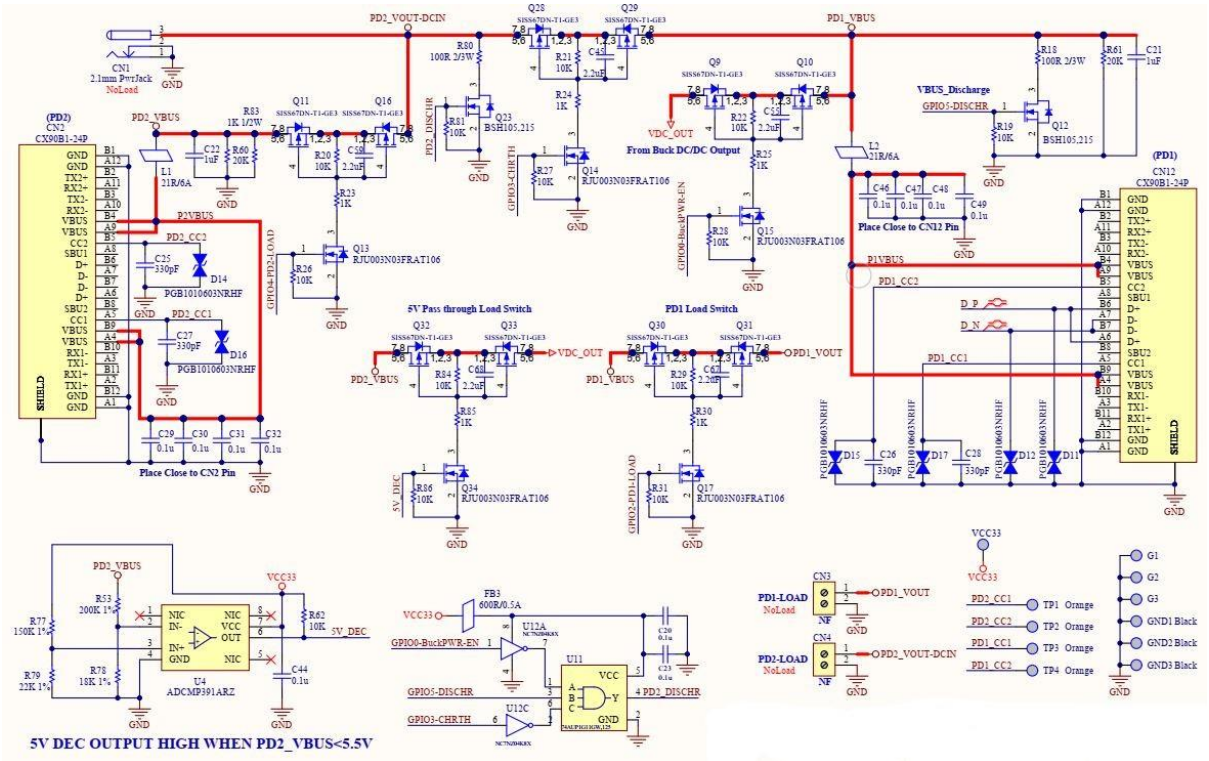


Figure 9 - PD1/PD2 Ports, Load Switches, 5V Detector and PD1/PD2 Discharging Circuit

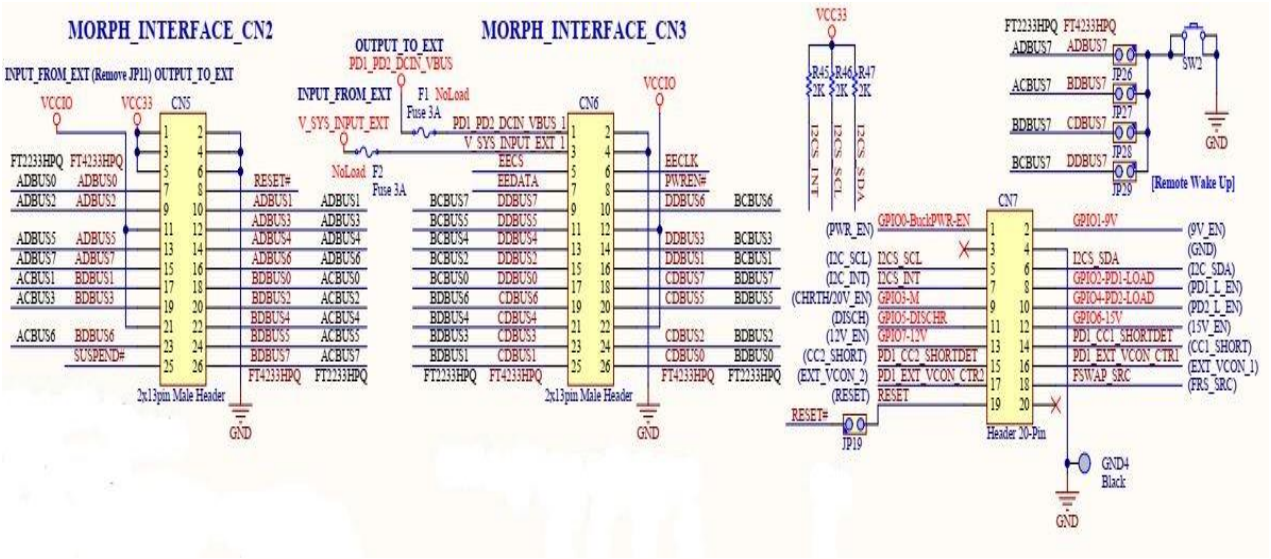


Figure 10 - Interfaces, Connector and Remote Wakeup Button

4 Power Delivery Functional Configuration

4.1 Pass-through

Pass-through is a feature where the input power on PD2 is passed through to PD1 to charge or power the device connected to PD1.

The block diagram in Figure 11 shows a use case in pass-through mode with charger plugged onto PD2 charges the PC that is plugged to PD1. (EEPROM has been programmed to pass-through mode in the factory).

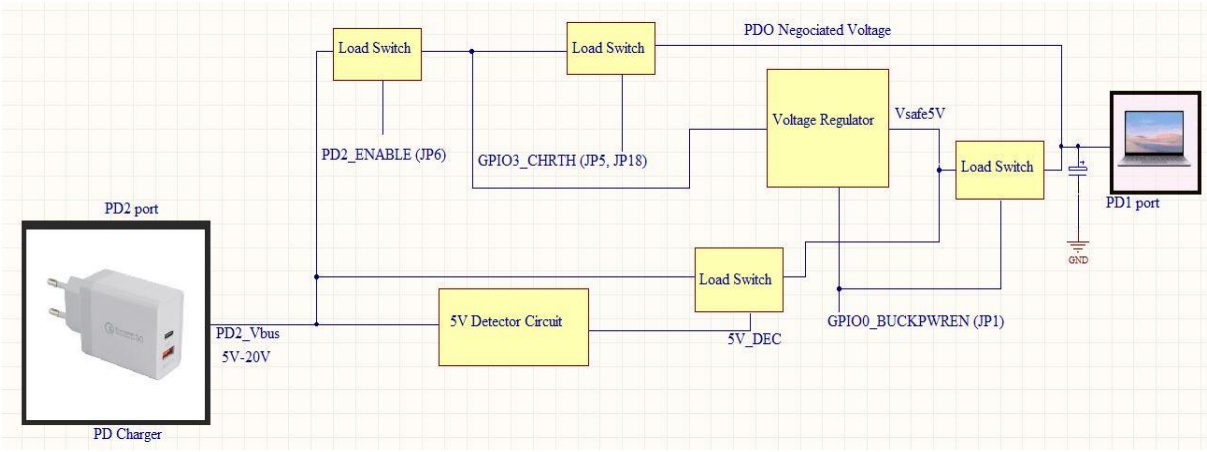


Figure 11 - Pass-through Block Diagram

Pass-through configuration:

Pin 1 of JP1 should be connected to Pin 2 of JP1: This is to enable the voltage regulator to provide the Vsafe5v. It is also enable the load switch (Q9, Q10, and Q15) to route the 5V from voltage regulator to the PD1 Vbus.

Pin 1 of JP6 should be connected to Pin 2 of JP6: This is to enable the PD2 load switch (Q11,Q16, Q13) to route the power from PD2 to the voltage regulator as well as to the input of the GPIO3-CHRTH load switch (Q28 Q29,Q14). Refer to Figure 11.

Pin 1 of JP5 should be connected to pin 2 of JP5. Pin 1 of JP18 should be connected to pin2 of JP18: This is to enable the GPIO3-CHRTH load switch (Q28, Q29, and Q14) to route the negotiated power from PD2 to PD1.

Pin 1 of JP7 should be connected to pin 2 of JP7: This is to control the discharge circuit on PD1 Vbus.

4.2 Dual Role

Dual Role is a feature where the input power from either PD2 or other external DC sources is fed to the voltage regulator where different power supplies can be configured based on the power profile in the FT4233HP external EEPROM to charge the device on PD1.

The block diagram in Figure 12 and Figure 13 shows two use cases in dual role mode where

1) Charger plugs onto PD2 is providing power to the voltage regulator that provide power to device plugged onto PD1 in accordance to the power profiles in the external EEPROM.
2) External DC source plugs onto CN1 providing power to the voltage regulator that provides power to device plugged onto PD1 in accordance to the power profiles in the external EEPROM.

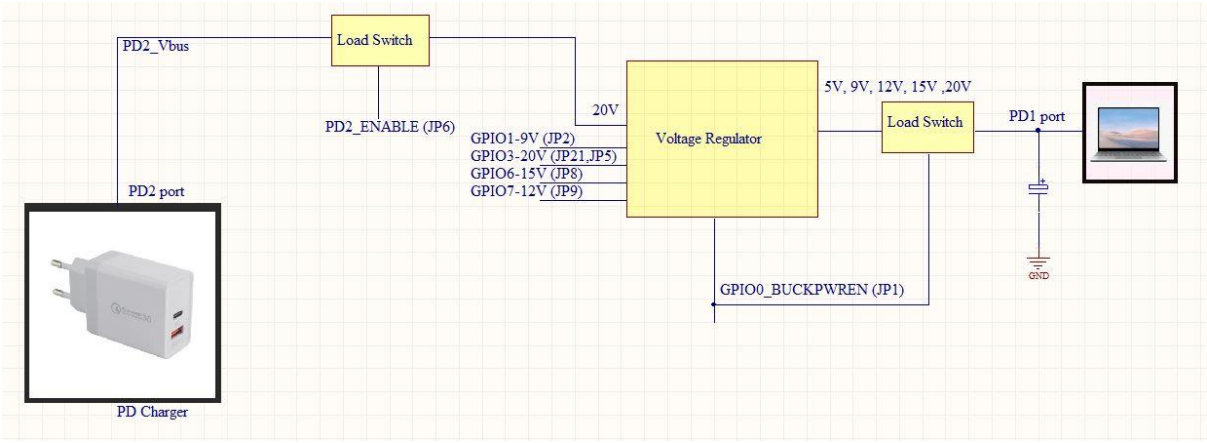


Figure 12 - Dual Role Block Diagram (Charger to PD2 Port)

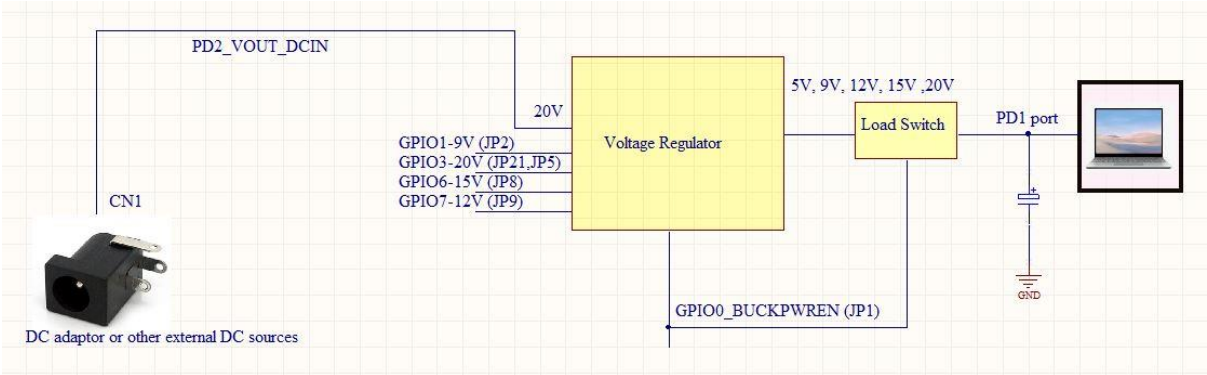


Figure 13 - Dual Role Block Diagram (External DC Source to CN1)

Dual-role configuration

Pin 1 of JP1 should be connected to Pin 2 of JP1: This is to enable the voltage regulator to provide the power. It is also to enable the load switch (Q9, Q10, and Q15) to route the negotiated power from voltage regulator to the PD1 Vbus.

Pin 1 of JP2 should be connected to Pin 2 of JP2: This is to enable the resistor divider in the voltage regulator to provide 9V.

Pin 1 of JP5 should be connected to pin 2 of JP5. Pin 1 of JP21 should be connected to pin2 of JP21: This is to enable the resistor divider in the voltage regulator to provide 20V.

Pin 1 of JP8 should be connected to pin 2 of JP8: This is to control the resistor divider to provide 15V.

Pin 1 of JP9 should be connected to pin 2 of JP9: This is to control the resistor divider to provide 12V.

Pin 1 of JP7 should be connected to pin 2 of JP7: This is to control the discharge circuit on PD1 Vbus.

4.3 Sink

Sink is feature where the PD2 or PD1 can be configured as sink mode when attach to PD charger or other PD devices to provide power to the modules connected to the board. Figure 14 and Figure 15 shows two possible use case of sink configuration.

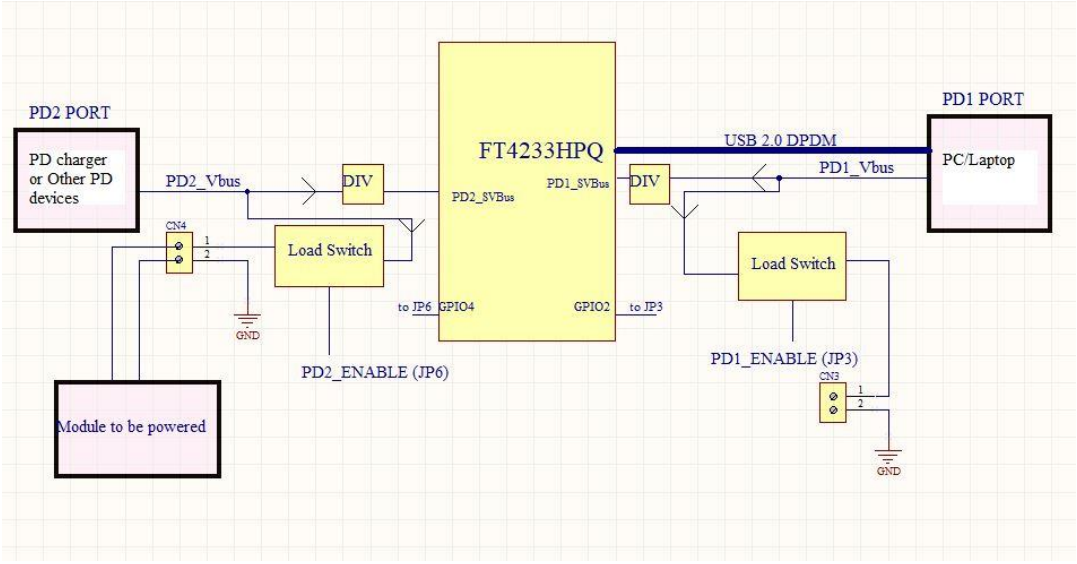


Figure 14 - Sink Block Diagram (PD1 Port as USB to Host PC, PD2 Port Sink Power into the module from Charger)

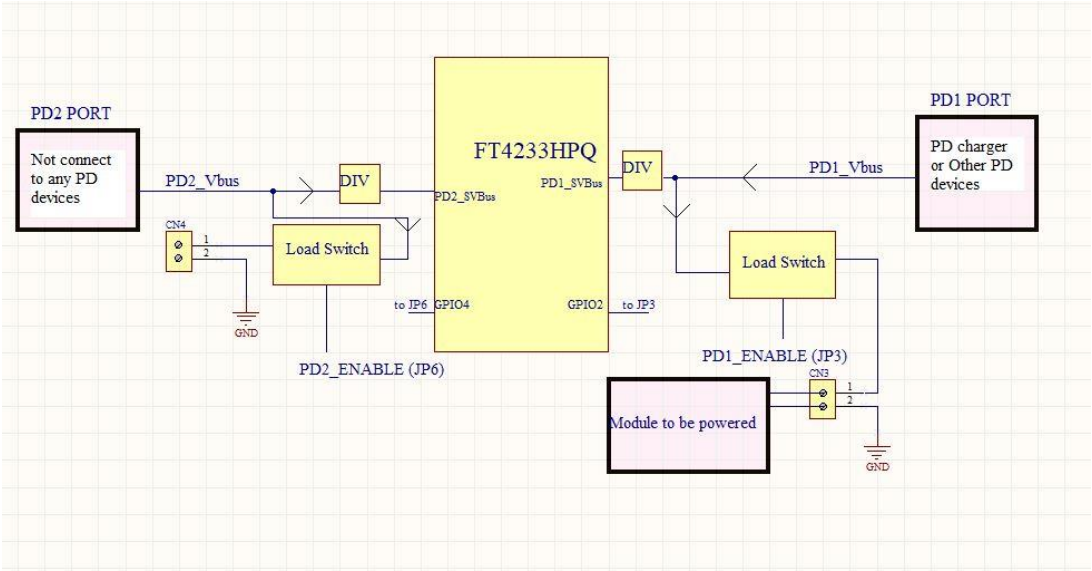


Figure 15 - Sink Block Diagram (PD1 Port Sink Power into the Module from Charger)

Sink Configuration

Pin 1 of JP3 should be connected to Pin 2 of JP3: This is to enable PD1 load switch to route the power from PD1 Vbus to PD1_Vout (CN3) to provide power to external modules or peripheral if required. The PD1 sink power profiles are configurable in EEPROM.

Pin 1 of JP6 should be connected to Pin 2 of JP6: This is to enable the PD2 load switch (Q11, Q16, and Q13) to route the power from PD2 to the PD2_Vbus_DCIN (CN4) to provide power to external modules or peripheral if required. The PD2 sink power profiles are configurable in EEPROM.

5 Mechanical Details

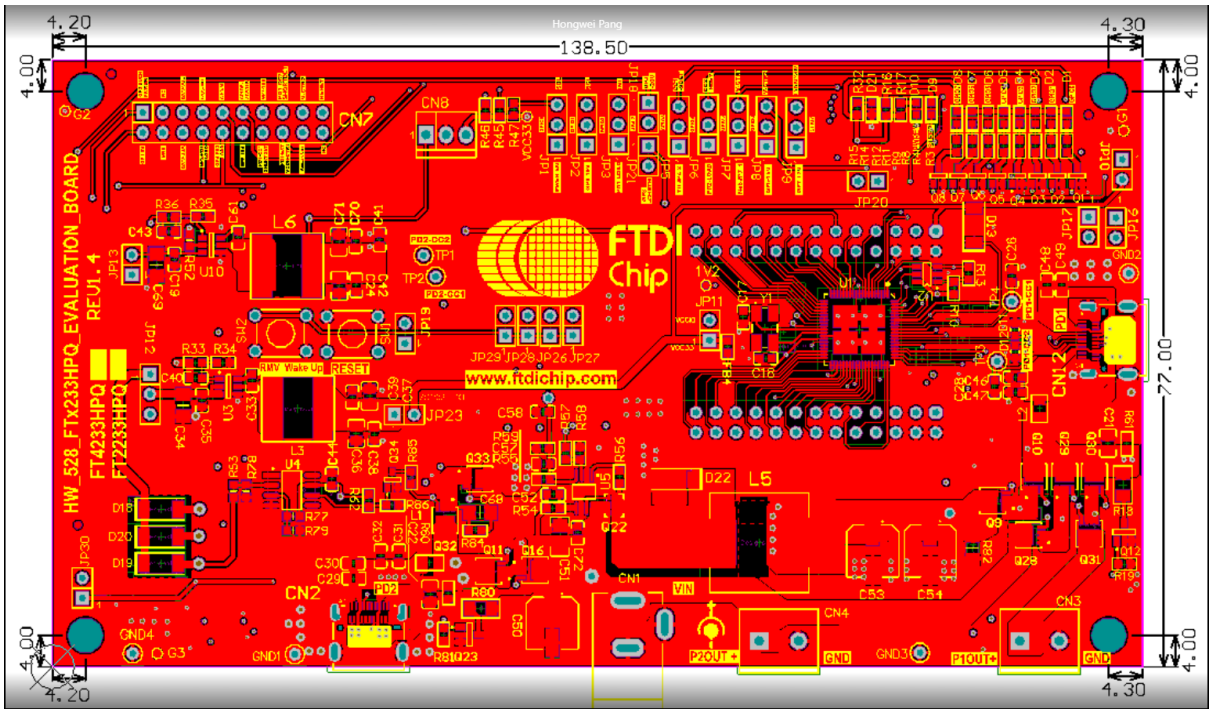


Figure 16 - UMFT4233HPEV Evaluation Board – Mechanical Diagram - Top View

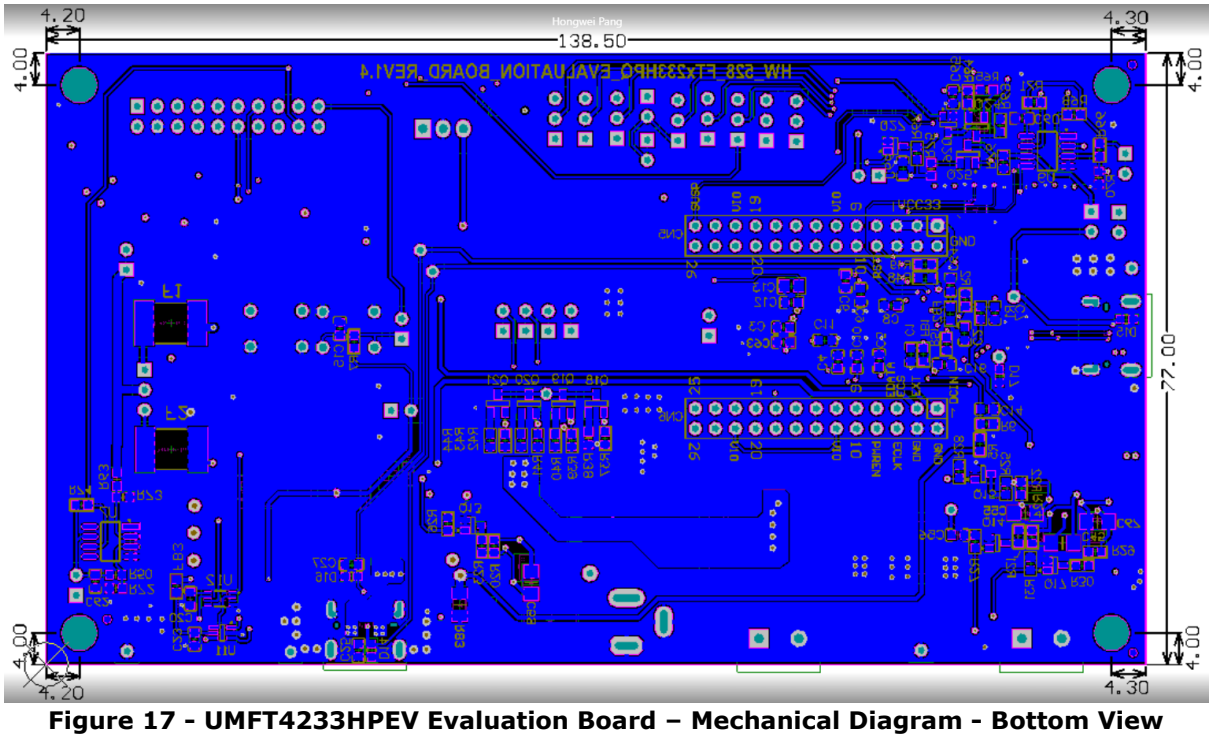


Figure 17 - UMFT4233HPEV Evaluation Board – Mechanical Diagram - Bottom View

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

AN_448 FT4233HP_FT2233HP_FT233HP_Configuration_Guide

AN_449 FT4233HP_FT2233HP_FT233HP_FT4232HP_FT2232HP_FT232HP_DCDC_Power Delivery Application Note

FT4233HP Datasheet

Acronyms and Abbreviations

Terms	Description
EEPROM	Electrically Erasable Programmable Read-Only Memory
GPIO	General Purpose Input Output
PD	Power Delivery
USB	Universal Serial Bus
USB-IF	USB Implementer Forum

Appendix B – List of Tables and Figures

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Appendix C – Revision History

Document Title: UMFT4233HPEV Evaluation Module Datasheet
Document Reference No.: FT_001509
Clearance No.: FTDI#563
Product Page: https://ftdichip.com/product-category/products/
Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	24-11-2021

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