Document Number: AFT18S230S
Rev. 2, 3/2013

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 50 watt RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1880 MHz.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1800 mA, P_{out} = 50 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

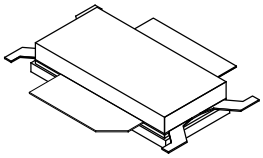
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.9	32.0	7.2	-35.0	-19
1840 MHz	19.1	32.0	7.1	-35.0	-18
1880 MHz	19.0	32.0	6.8	-34.0	-11

Features

- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel. For R5 Tape and Reel option, see p. 12.

AFT18S230SR3

1805-1880 MHz, 50 W AVG., 28 V



NI-780S-6

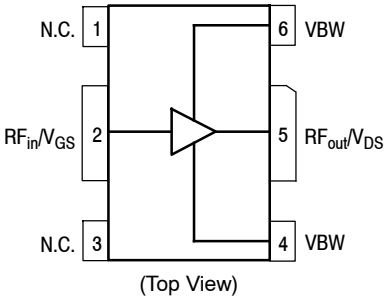


Figure 1. Pin Connections

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ T_C = 25°C when DC current is fed through drain lead, pin 5 Derate above 25°C	CW	253 1.7	W W/°C
CW Operation @ T_C = 25°C when DC current is fed through pin 4 and pin 6 Derate above 25°C	CW	83 0.41	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 50 W CW, 28 Vdc, I_{DQ} = 1800 mA, 1840 MHz Case Temperature 92°C, 160 W CW(4), 28 Vdc, I_{DQ} = 1800 mA, 1840 MHz	$R_{\theta JC}$	 0.41 0.31	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 291 μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1800 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.3	2.8	3.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.9 Adc)	$V_{DS(on)}$	0.1	0.24	0.3	Vdc
Functional Tests (5) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1800 mA, P_{out} = 50 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.0	19.0	21.0	dB
Drain Efficiency	η_D	30.5	32.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.4	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.0	-32.0	dBc
Input Return Loss	IRL	—	-11	-7	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1800 mA, f = 1840 MHz					
VSWR 10:1 at 32 Vdc, 257 W CW[1] Output Power (3 dB Input Overdrive from 230 W CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1800 mA, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	207	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz bandwidth)	Φ	—	7.6	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	90	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 50 W Avg.	G_F	—	0.35	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) [1]	ΔP1dB	—	0.37	—	dB/°C

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

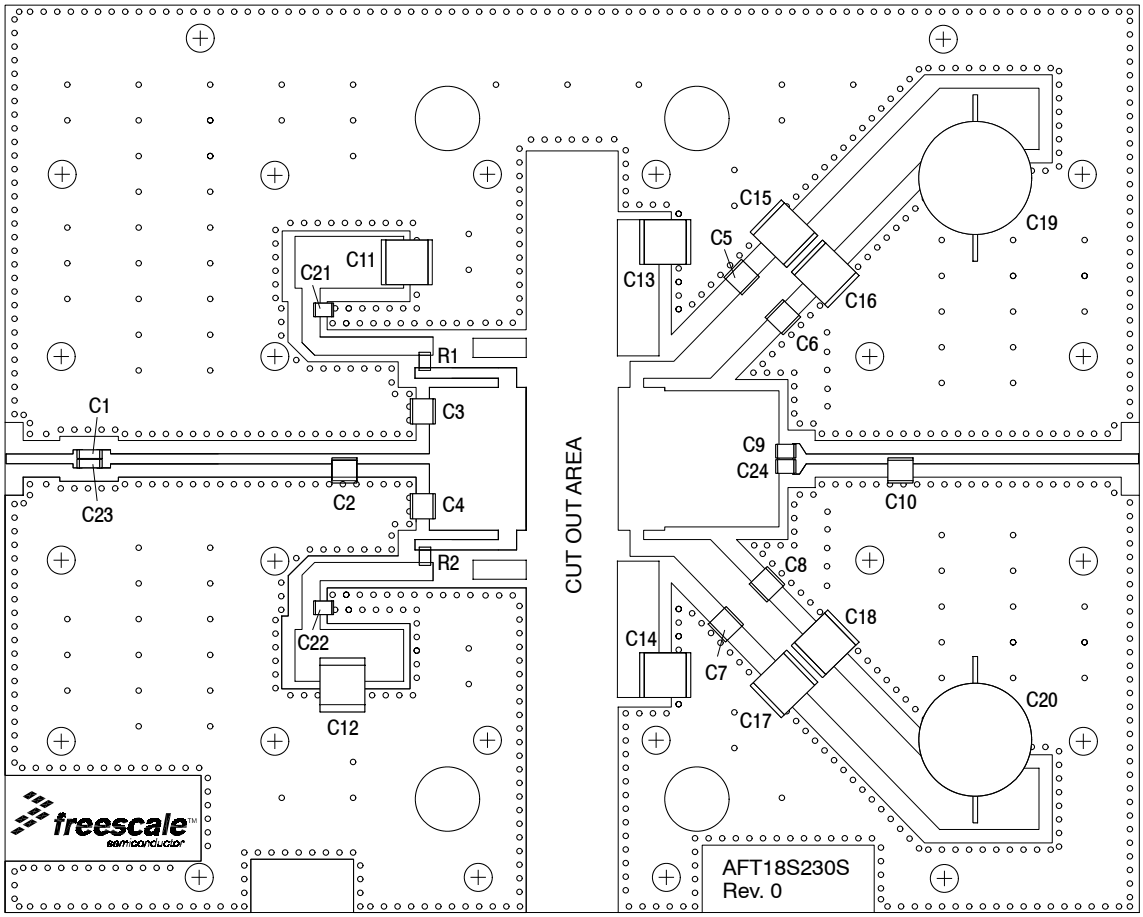


Figure 2. AFT18S230SR3 Test Circuit Component Layout

Table 5. AFT18S230SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C21, C22, C23	27 pF Chip Capacitors	ATC600F270JT250XT	ATC
C2	1.2 pF Chip Capacitor	ATC100B1R2BT500XT	ATC
C3, C4	1.0 pF Chip Capacitors	ATC100B1R0BT500XT	ATC
C5, C6, C7, C8	27 pF Chip Capacitors	ATC100B270JT500XT	ATC
C9, C24	39 pF Chip Capacitors	ATC600F390JT250XT	ATC
C10	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C11, C12, C13, C14, C15, C16, C17, C18	10 μF, 100 V Chip Capacitors	C5750X7S2A106M	TDK
C19, C20	330 μF, 63 V Electrolytic Capacitors	MCRH63V337M13X21-RH	Multicomp
R1, R2	4.75 Ω, 1/4 W Chip Resistors	CRCW12064R75FNEA	Vishay
PCB	0.020″, ε_r = 3.5	RO4350	Rogers

TYPICAL CHARACTERISTICS

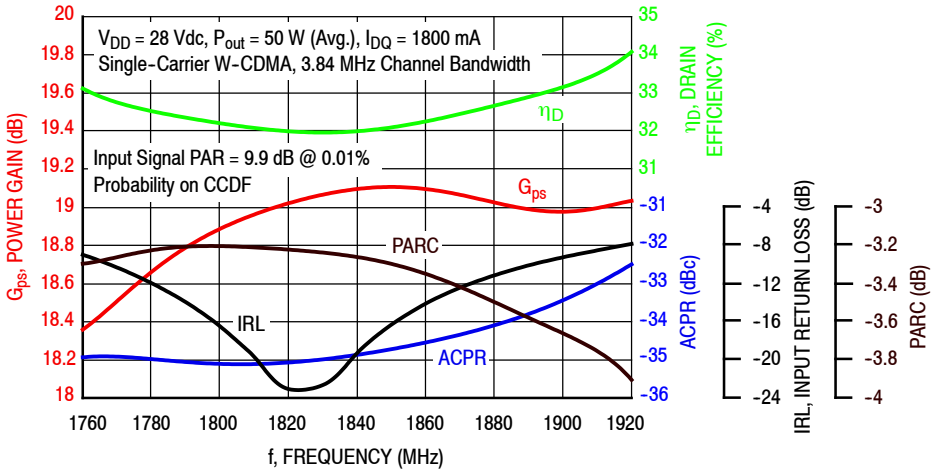


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

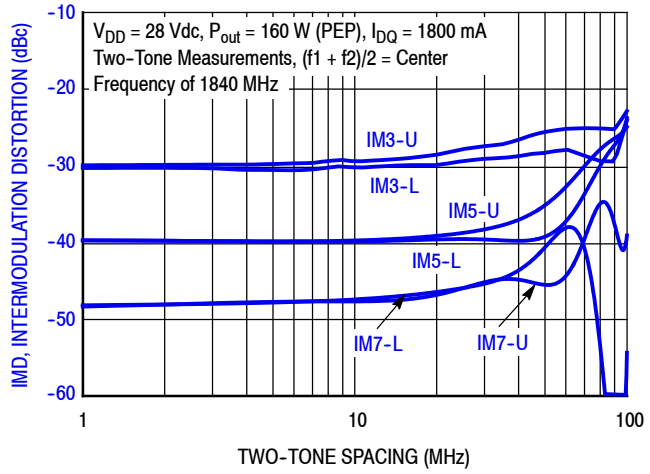


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

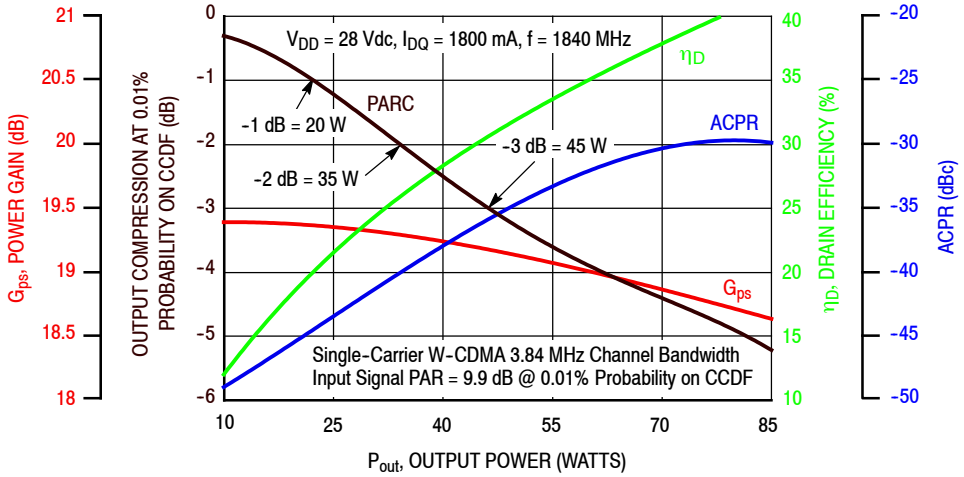


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

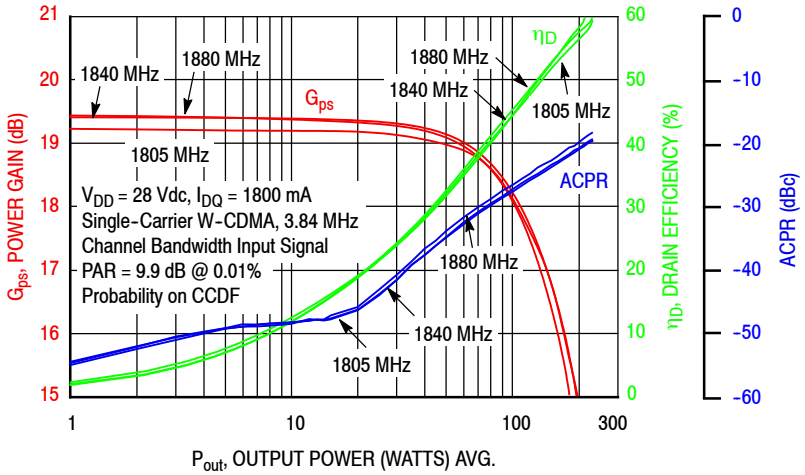


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

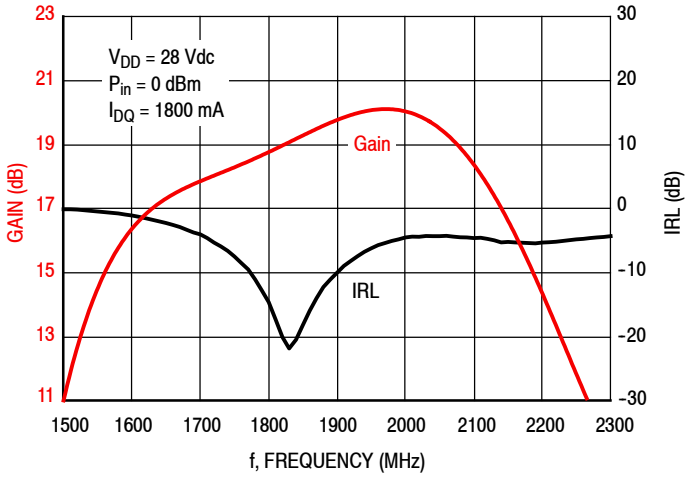


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 1800 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Output Power							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.80 - j3.40	1.00 + j3.41	1.09 - j2.10	18.5	54.2	263	57.8	-10	55.1	324	59.9	-16
1840	1.10 - j3.70	1.30 + j3.80	1.20 - j2.30	18.5	54.2	263	57.1	-9	55.2	331	61.1	-16
1880	1.40 - j4.10	1.70 + j4.13	1.11 - j2.30	18.7	54.2	263	57.9	-10	55.0	316	59.5	-16

(1) Load impedance for optimum P1dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

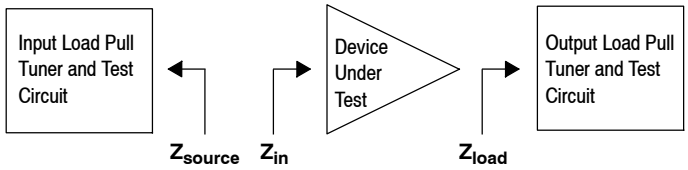


Figure 8. Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1800 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Drain Efficiency							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.80 - j3.40	1.00 + j3.50	1.90 - j0.50	21.7	51.5	141	70.0	-17	53.2	209	71.9	-22
1840	1.10 - j3.70	1.30 + j3.83	1.90 - j0.90	21.4	51.9	155	70.1	-15	52.9	195	72.8	-24
1880	1.40 - j4.10	1.80 + j4.30	1.50 - j1.10	21.3	52.2	166	69.9	-17	52.8	191	71.2	-25

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

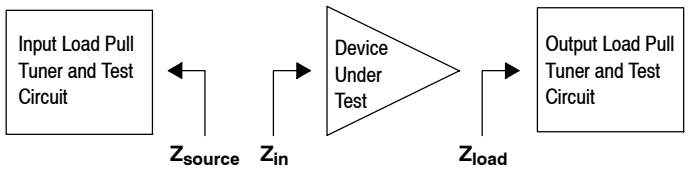


Figure 9. Load Pull Performance — Maximum Drain Efficiency Tuning

P1dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

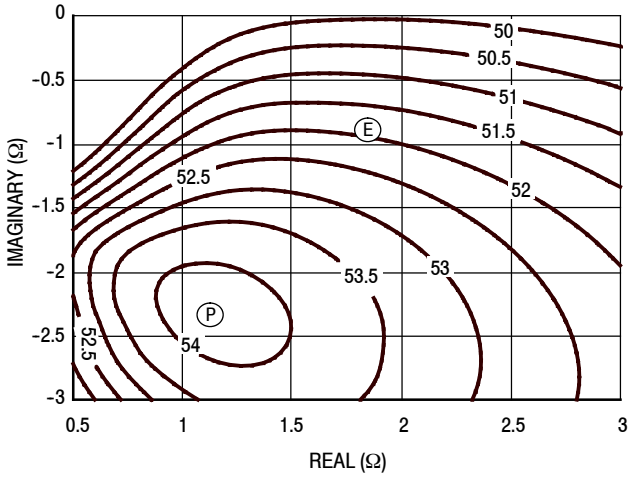


Figure 10. P1dB Load Pull Output Power Contours (dBm)

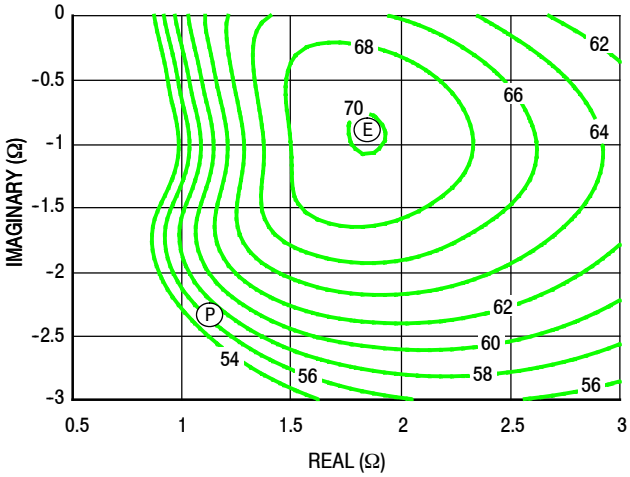


Figure 11. P1dB Load Pull Efficiency Contours (%)

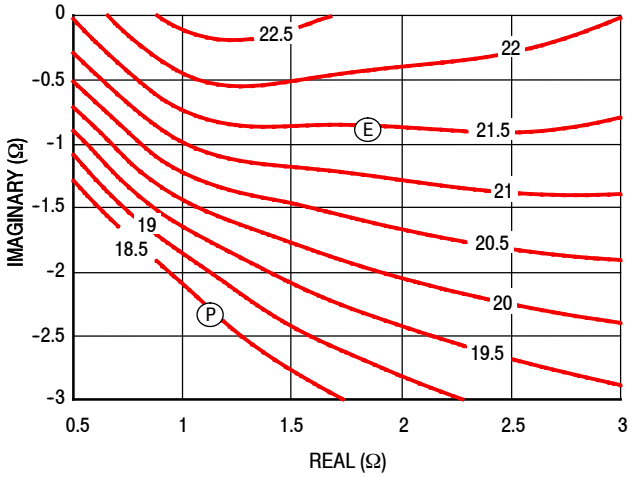


Figure 12. P1dB Load Pull Gain Contours (dB)

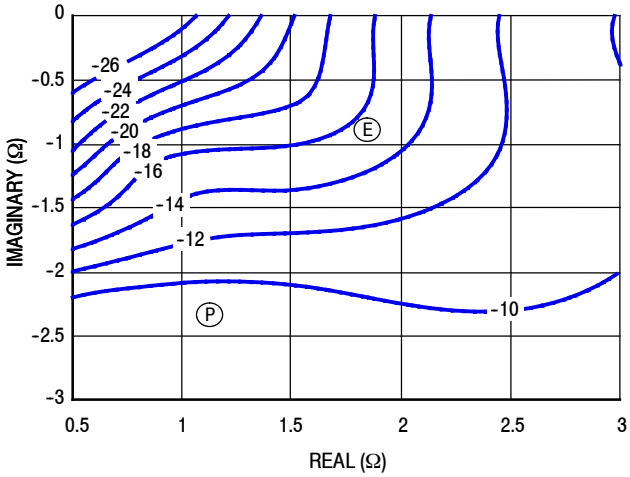


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

ACPR

PARC

P3dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

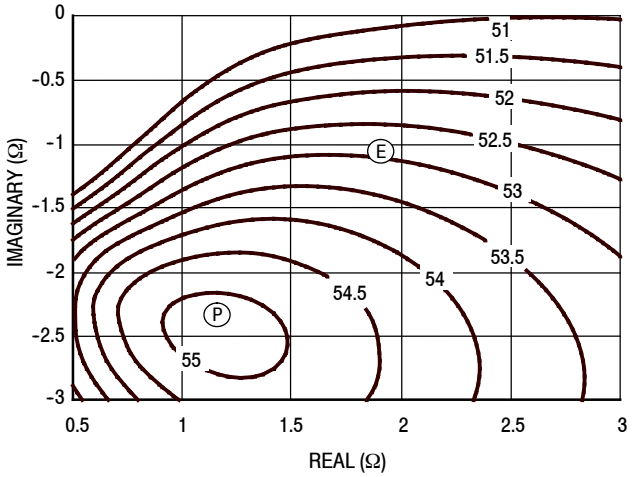


Figure 14. P3dB Load Pull Output Power Contours (dBm)

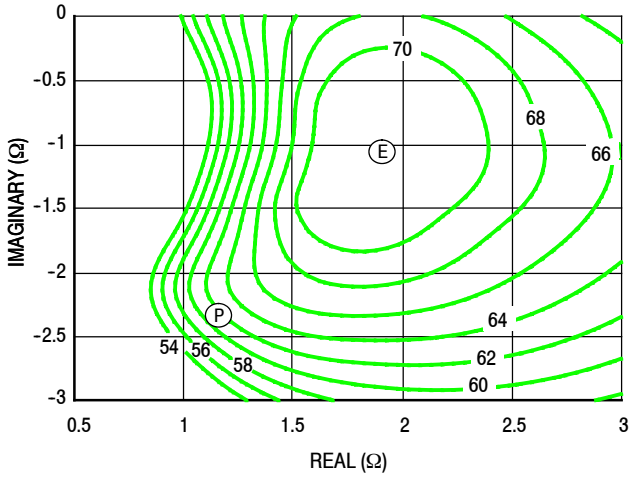


Figure 15. P3dB Load Pull Efficiency Contours (%)

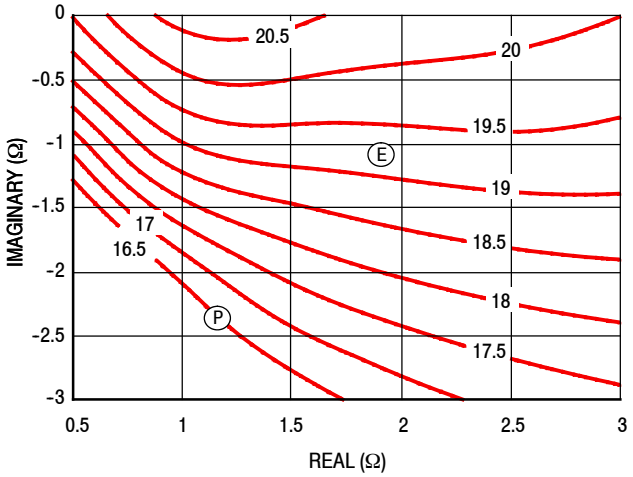


Figure 16. P3dB Load Pull Gain Contours (dB)

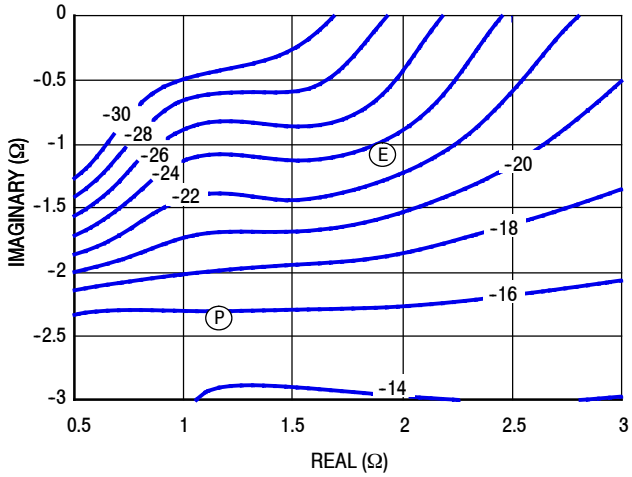


Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

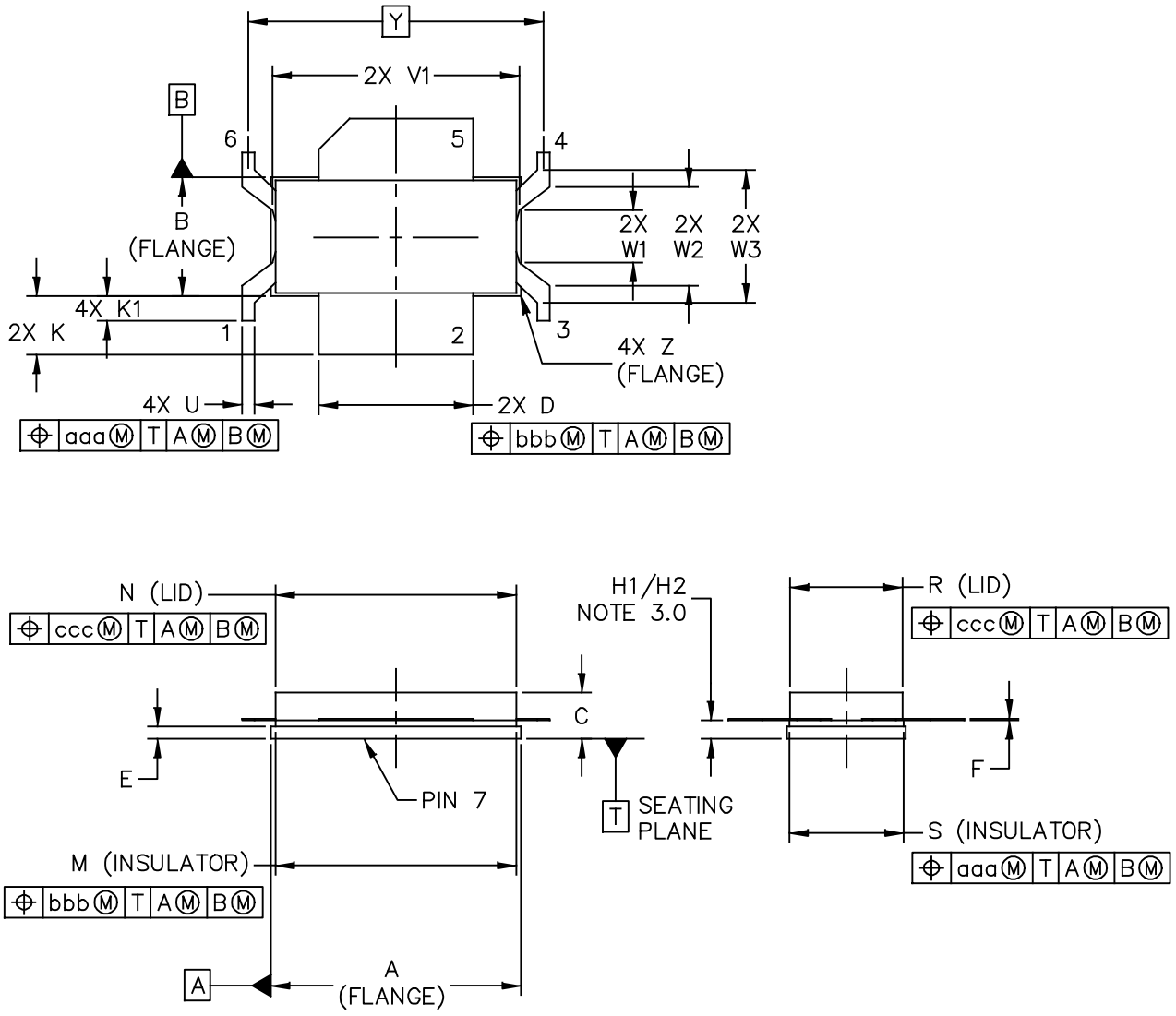
Power Gain

Drain Efficiency

ACPR

PARC

PACKAGE DIMENSIONS



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TITLE: NI-780S-6	DOCUMENT NO: 98ASA00443D	REV: A
	CASE NUMBER: 2268-02	24 MAY 2012
	STANDARD: NON-JEDEC	

NOTES:

1.0 CONTROLLING DIMENSION: INCH.

2.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3.0 DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2 & 5. H2 APPLIES TO PINS 1, 3, 4 & 6.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
C	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.165	.175	4.19	4.45
F	.004	.007	0.10	0.18	W2	.315	.325	8.00	8.26
H1	.057	.067	1.45	1.70	W3	.425	.435	10.80	11.05
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R.00	R1.02
K1	.070	.090	1.78	2.29	aaa	–	.005	–	0.127
M	.774	.786	19.66	19.96	bbb	–	.010	–	0.254
N	.772	.788	19.61	20.02	ccc	–	.015	–	0.381

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NI–780S–6	CASE NUMBER: 2268–02	24 MAY 2012
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 44 mm Tape Width, 13-inch Reel.

The R5 tape and reel option for AFT18S230S part will be available for 2 years after release of AFT18S230S. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased this device in the R5 tape and reel option will be offered AFT18S230S in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2012	• Initial Release of Data Sheet
1	Nov. 2012	• Corrected Tape and Reel tape width from 32 mm to 44 mm, p. 1, 12
2	Mar. 2013	• Table 1. Maximum Ratings: added CW Operation rating and derate factor if the part is biased through pin 4 and pin 6, p. 2

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Rev. 2, 3/2013

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