IS32LT3124A/B/C/D/E/F

QUAD CHANNEL, LINEAR LED DRIVER WITH FAULT REPORTING AND DYNAMIC HEADROOM CONTROL (DHC)

April 2024

GENERAL DESCRIPTION

The IS32LT3124 is a linear programmable current regulator consisting of 4 output channels capable of up to 150mA each. Individual external resistors set the maximum current level for each channel. The outputs can be combined to provide a higher current drive capability up to 600mA (Max.).

The IS32LT3124 features Dynamic Headroom Control (DHC) with an optional external PMOS FET to minimize IC thermal stress when the supply voltage exceeds the LED string forward voltage. It includes two modes for different output power: Shunt Regulator mode and Series Regulator mode. It can operate with power supply modulation (PSM) for applications requiring dimming without use of the EN pin.

For added system reliability, the IS32LT3124 integrates fault detection circuitry for open/short circuit and over temperature conditions. The fault pins (FLTB) can all be tied together to disable the device and other IS32LT3124 devices on the same parallel circuit.

To handle all these different fault detections and reporting features, the IS32LT3124 has six different versions: A, B, C, D, E and F. All of them can support the above features. See table 1 for the major difference. In IS32LT3124A/B/D/E, if any fault condition occurs, all output currents will be disabled. In IS32LT3124B/C/E/F, individual ISET pin for each LED channel is redefined as individual PWM dimming control, thus ISET open detection function is removed. The EN pin of IS32LT3124B/C/E/F is featured as the enable signal of the internal fault reporting block. See Table 4 for complete fault listing.

The IS32LT3124 is targeted at the automotive market such as interior accent lighting and exterior tail lighting. It is offered in a thermally enhanced eTSSOP-16 package.

APPLICATIONS

- Automotive LED driver
- RGBW automotive ambient lighting
- Tail light
- Turn light
- Daytime running light

FEATURES

- 5.0V to 28V input supply voltage range
  - Withstand 42V load dump
- Four output channels can source up to 150mA each
  - Four current set resistors
  - ±5% output current accuracy
  - Low dropout voltage of 1V (Max.) at 100mA
  - Combined for higher current capability with same current accuracy
- PWM dimming and shutdown control input
  - 100Hz~300Hz power supply modulation (PSM)
  - 100Hz~1kHz individual dimming via resistors of ISETx pins (IS32LT3124B/C/E/F only)
- Optional Dynamic Headroom Control (DHC) with an external PMOS FET to minimize IC thermal stress
  - Shunt regulator mode for heavy load
  - Series regulator mode for light load
- Additional external UVLO (Under Voltage Lockout Threshold) is programmable via EN pin (IS32LT3124A/D only)
- Fault protection and reporting
  - Externally enable/disable fault reporting (IS32LT3124B/C/E/F only)
  - Programmable fault reporting output delay time
  - Fault condition disables all output (IS32LT3124A/B/D/E only)
  - Parallel fault connection (one-fail-all-fail)
  - LED string open/short
  - Single LED short (Conditional, IS32LT3124B/C/D only)
  - ISET pin short
  - ISET pin open (IS32LT3124A/D only)
  - Over temperature
- RoHS & Halogen-Free Compliance
- TSCA Compliance
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- Operating temperature range (-40°C ~ +125°C)

Table 1 Major Difference Of Different Versions

Version	Dimming	Outx Pin Short To GND Threshold V_{SCD}	Support LED String Voltage	Fault Protection Action (See Table 4 For More Details)
IS32LT3124A	PSM dimming or Simultaneous dimming by EN pin	Typ. 1.22V	≥1 LED(s)	One channel fails all channels off
IS32LT3124B	PSM dimming or Individual dimming by ISET resistors	Typ. 4.8V		One channel fails all channels off
IS32LT3124C	PSM dimming or Individual dimming by ISET resistors	Typ. 4.8V	> (V_{SCD_MAX}+V_{SCD_HY})	One channel fails all channels on
IS32LT3124D	PSM dimming or Simultaneous dimming by EN pin	Typ. 4.8V		One channel fails all channels off
IS32LT3124E	PSM dimming or Individual dimming by ISET resistors	Typ. 1.22V	≥1 LED(s)	One channel fails all channels off
IS32LT3124F	PSM dimming or Individual dimming by ISET resistors	Typ. 1.22V	≥1 LED(s)	One channel fails all channels on

TYPICAL APPLICATION CIRCUIT

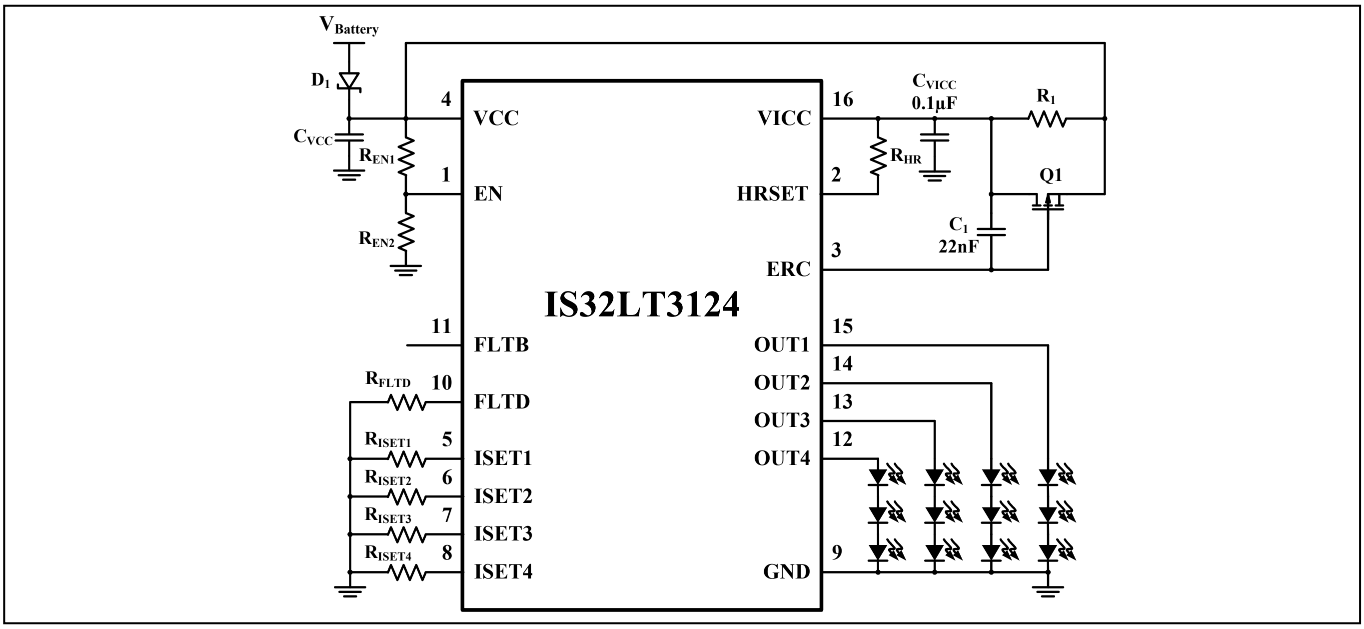


Figure 1 Typical Application Circuit

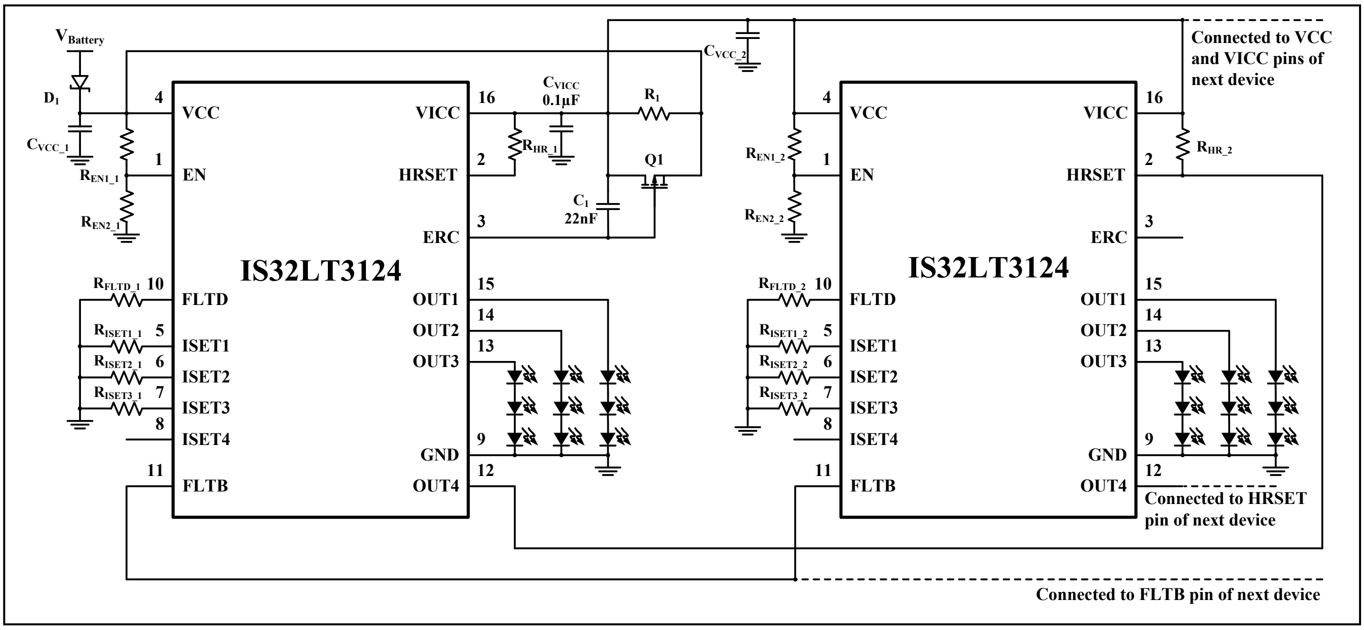


Figure 2 Typical Application Circuit (Several Devices in Parallel Share One External PMOS FET)

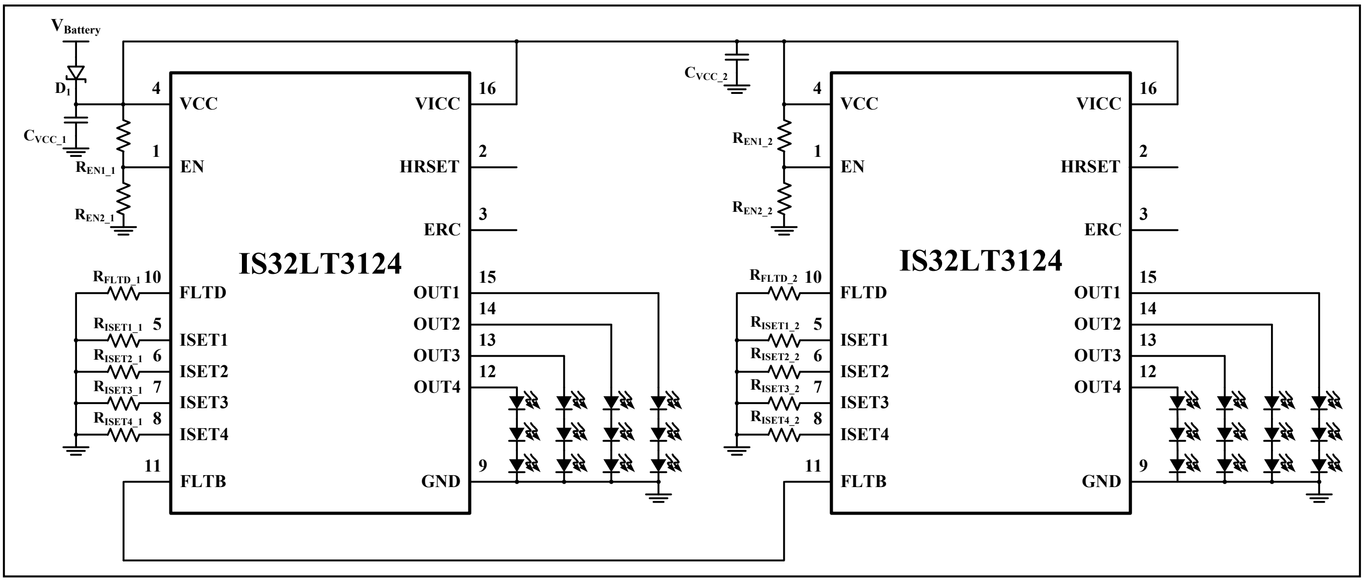


Figure 3 Typical Application Circuit (Several Devices in Parallel without External PMOS FET)

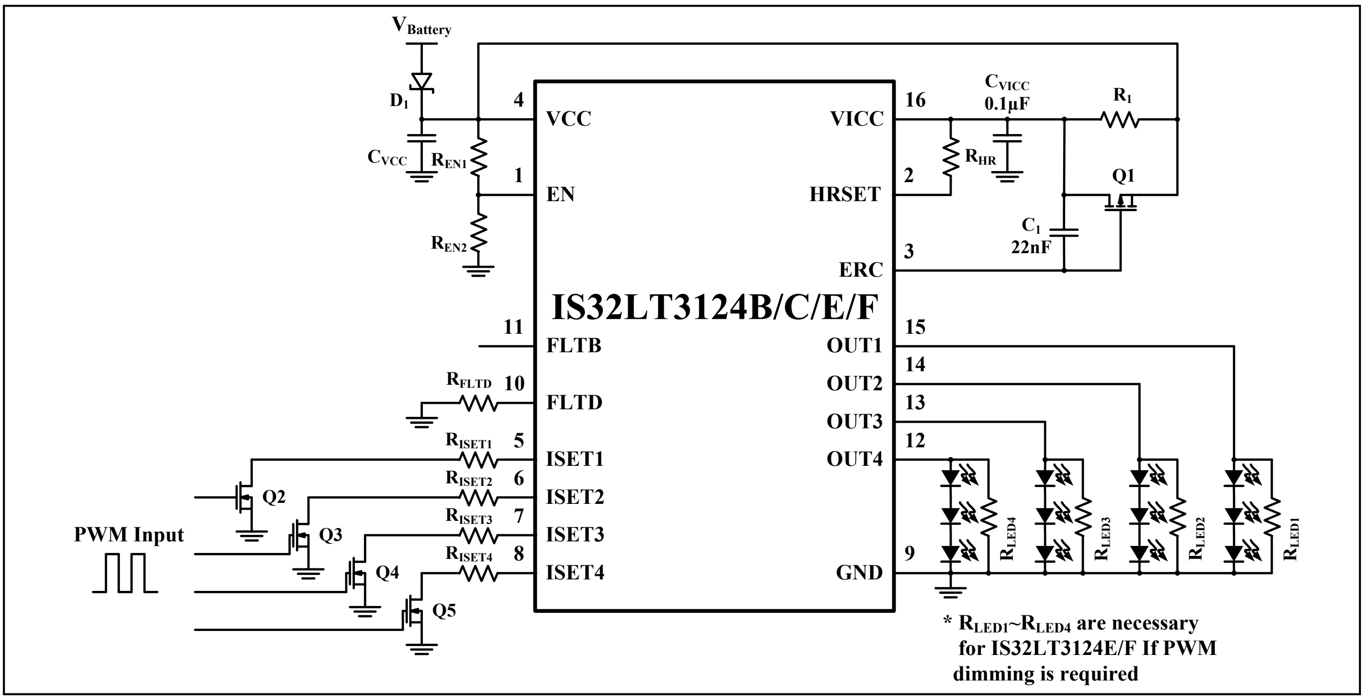


Figure 4 Typical Application Circuit with Additional Switches driving R_{ISET} Individual PWM Dimming (IS32LT3124B/C/E/F only) When PWM Generator is Far Away from Device

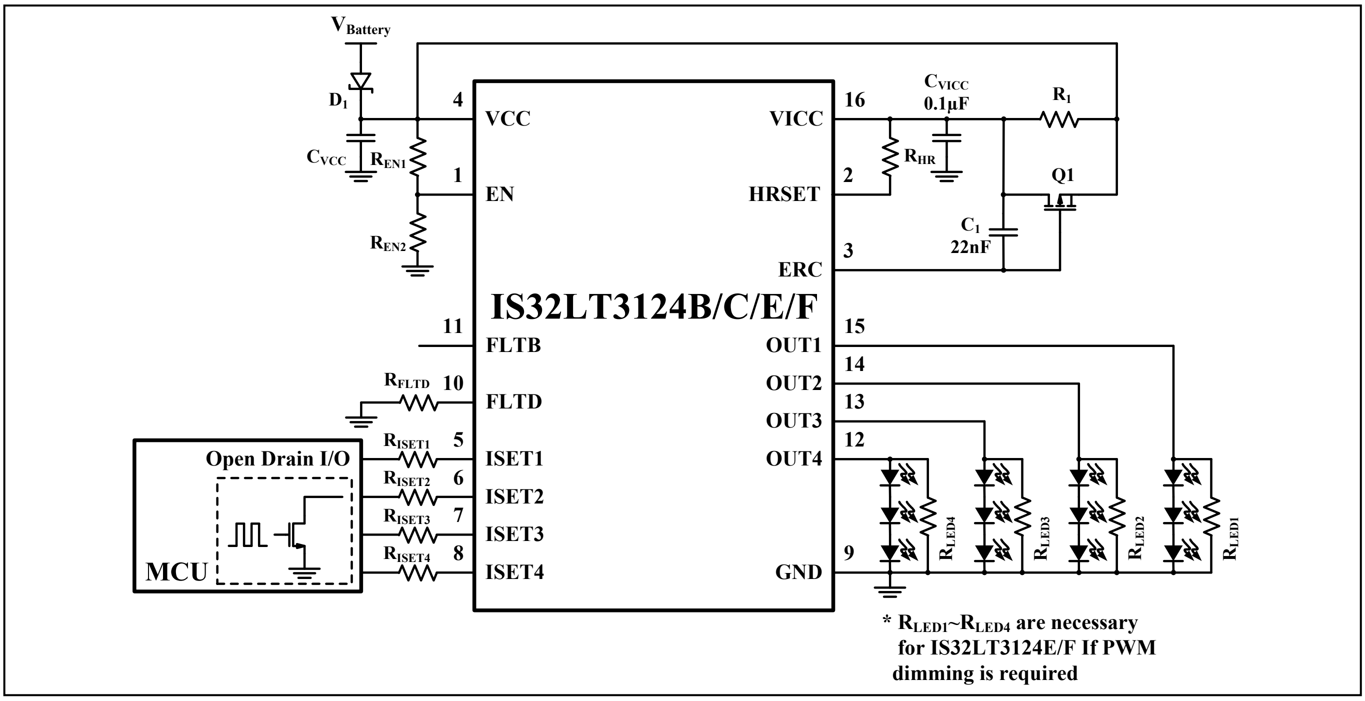
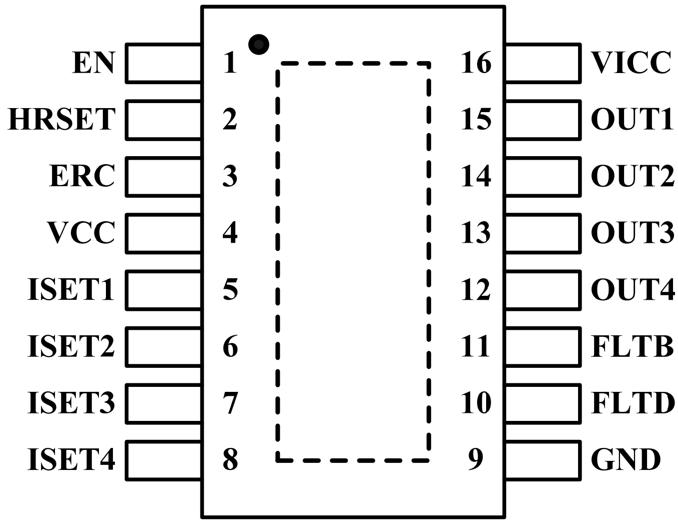


Figure 5 Typical Application Circuit With Open Drain I/O driving R_{ISET} Individual PWM Dimming (IS32LT3124B/C/E/F only) When PWM Generator is Close to Device

Note 1: The C_1 and C_{VICC} are fixed value.

Note 2: For PSM dimming application, high C_{VCC} capacitor value will affect the dimming accuracy. To get better dimming performance, recommend 0.1μF for it.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-16	

PIN DESCRIPTION

<table>
<tr><th>No.</th><th>Pin</th><th colspan="2">Description</th></tr>
<tr><td rowspan="2">1</td><td rowspan="2">EN</td><td>IS32LT3124A/D</td><td>Device enable pin. Pull low to disable all the outputs. Input a PWM signal will achieve all channels simultaneous dimming.</td></tr>
<tr><td>IS32LT3124B/C/E/F</td><td>Internal fault flag report enable pin. Pull it low to disable fault reporting, the output currents and the response to a fault remain functional except FLTB is not pulled low.</td></tr>
<tr><td>2</td><td>HRSET</td><td colspan="2">With the external PMOS FET, connect a resistor to VICC pin to set the maximum working headroom for the current sources.</td></tr>
<tr><td>3</td><td>ERC</td><td colspan="2">Gate driver of external PMOS FET to achieve dynamic headroom control.</td></tr>
<tr><td>4</td><td>VCC</td><td colspan="2">Raw supply voltage.</td></tr>
<tr><td rowspan="2">5~8</td><td rowspan="2">ISET1~ISET4</td><td>IS32LT3124A~F</td><td>Resistor on this pin to GND sets the maximum output current for channel OUT1~OUT4.</td></tr>
<tr><td>IS32LT3124B/C/E/F</td><td>The internal ISET open detection is removed. Therefore, PWM dimming and current adjust via the resistors of ISETx pins is feasible. Float the ground terminal of the resistor to turn off the corresponding output and ground to turn on.</td></tr>
<tr><td>9</td><td>GND</td><td colspan="2">Ground pin.</td></tr>
<tr><td>10</td><td>FLTD</td><td colspan="2">Resistor on this pin to GND sets the fault reporting output delay time.</td></tr>
<tr><td>11</td><td>FLTB</td><td colspan="2">Fault reporting output pin. Active low. Internally pulled up to 4.5V by a resistor. It is also an input pin (IS32LT3124A/B/D/E only). Pulling it low will disable all output currents.</td></tr>
<tr><td>12~15</td><td>OUT4~OUT1</td><td colspan="2">Output current source for Channel 4~Channel 1.</td></tr>
<tr><td>16</td><td>VICC</td><td colspan="2">Regulated LED string voltage from external PMOS FET.</td></tr>
<tr><td></td><td>Thermal Pad</td><td colspan="2">Must be connected to GND with sufficient copper plate for heat sink.</td></tr>
</table>

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3124A-ZLA3-TR IS32LT3124B-ZLA3-TR IS32LT3124C-ZLA3-TR IS32LT3124D-ZLA3-TR IS32LT3124E-ZLA3-TR IS32LT3124F-ZLA3-TR	eTSSOP-16, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

VCC, VICC, EN, ERC, HRSET	-0.3V ~ +42V (Note 3)
OUT1~ OUT4	-0.3V ~ V_{VICC}+0.3V
ISET1~ISET4, FLTD, FLTB	-0.3V ~ +7.0V
Operating junction temperature, T_A=T_J	-40°C ~ +125°C
Maximum continuous junction temperature, $T_{J(MAX)}$	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Power dissipation, $P_{D(MAX)}$	2.12W
Junction Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), $θ_{JA}$	47.1°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), $θ_{JP}$	1.62°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: The device can operate at 42V continuously subject only to thermal dissipation limit.
Note 4: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Valid are at V_{CC}= 12V, T_J= -40°C ~ +125°C, typical value at 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Up Parameter						
V_{CC}	Supply voltage range		5		28	V
I_{CC}	VCC supply current	R_{ISETx}= 20kΩ, V_{HR}= 1V	8	10	12	mA
V_{UVLO}	VCC supply threshold voltage (when device logic is enabled)	Voltage rising	4.3	4.5	4.7	V
V_{UVLO_HY}	VCC supply voltage hysteresis		0.2	0.25	0.3	V
I_{SD}	Shutdown current in normal mode (IS32LT3124A/D only)	V_{CC}= V_{ICC}= 12V, R_{FLTD}= 20kΩ, EN= Low, T_A= 25°C	0.8	1.1	1.3	mA
I_{SD_FLT}	Shutdown current as FAULTB pin externally pulled low (IS32LT3124A/B/D/E only)	V_{CC}= V_{ICC}= 12V, EN= High, FLTB= Low, R_{FLTD}= 20kΩ, T_A= 25°C	1.0	1.35	1.5	mA
t_{ON}	Startup turn on time (IS32LT3124A/D only)	I_{OUT}= -150mA, V_{CC}= V_{ICC}= 12V, V_{EN}> 1.23V (Note 5)			20	μs
t_{SD}	The low time of EN pin to shutdown the IC (IS32LT3124A/D only)		20	38	60	ms
t_{PC}	Power cycle ON (minimum)	(Note 5)			0.1	ms
Channel Parameter						
V_{ISETx}	The ISETx voltage			1		V
V_{ISET_SC}	ISETx pin short circuit detection threshold	Voltage falling	100	200	250	mV
V_{ISET_SCHY}	ISETx pin short circuit detection threshold hysteresis		50	100	150	mV
I_{OUT}	Output current per channel	R_{ISETx}= 20kΩ, V_{HR}= 1V	-105	-100	-95	mA
I_{OUT_R}	Output current per channel range		-150		-10	mA
I_{OUT_L}	Output limit current		-220	-190	-160	mA

ELECTRICAL CHARACTERISTICS (CONTINUE)

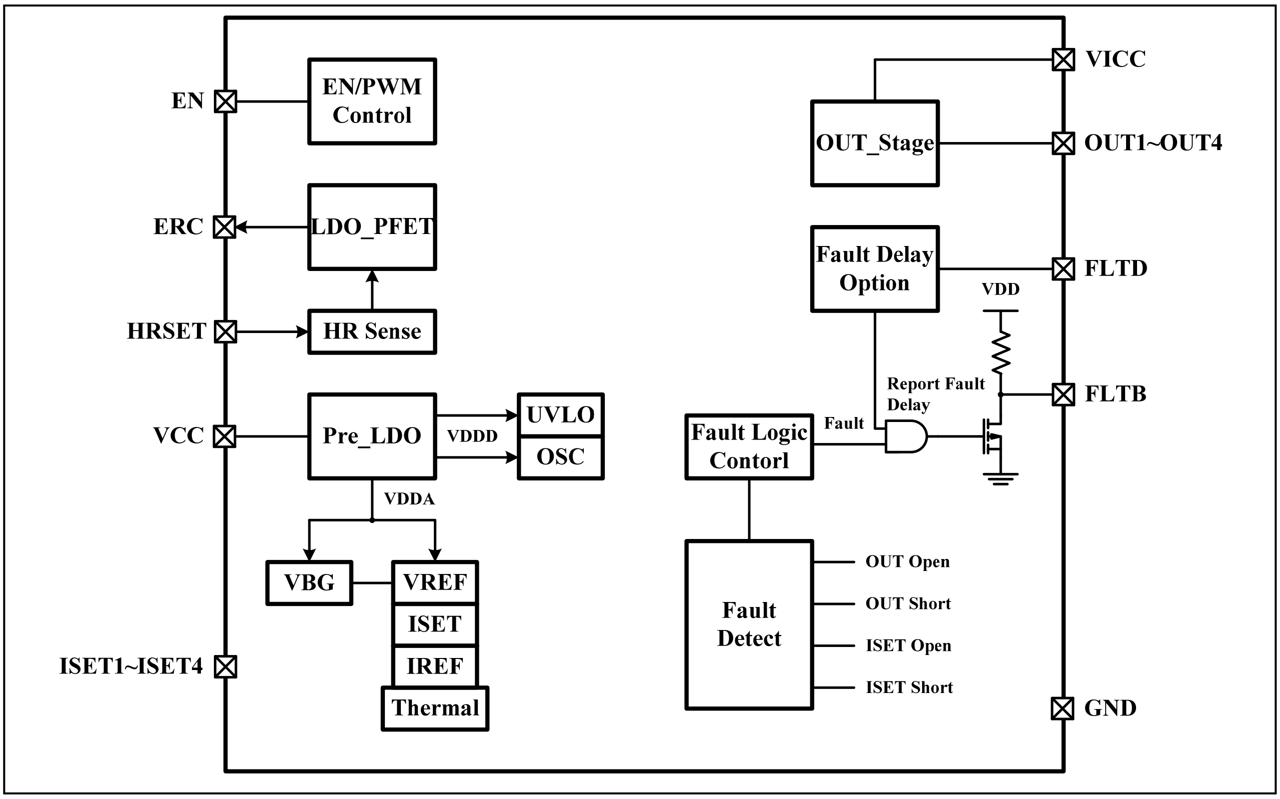
Valid are at V_{CC}= 12V, T_J= -40°C ~ +125°C, typical value at 25°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$\Delta I_S/I_S$	Channel current matching	R_{ISETx}= 20kΩ		-3		3	%
I_{LEAK}	Leakage current per channel (IS32LT3124A/D only)	EN= Low, V_{OUT}= 0V, V_{CC}= 28V				1	μA
V_{HRSET_MAX}	The maximum headroom set	(Note 5)				3.0	V
V_{HRSET}	Headroom voltage set accuracy	R_{HR}= 2kΩ (Note 6)		0.8	1.0	1.2	V
V_{HR}	Minimum headroom voltage	R_{ISETx}= 20kΩ (Note 6)				1.0	V
		R_{ISETx}= 13.3kΩ (Note 6)				1.3	
I_{ERC}	ERC pin current capability	(Note 5)			40		μA
Fault Protect Parameter							
V_{FLTD}	Fault delay pin voltage				1.23		V
t_{FLTD}	Fault delay time	R_{FLTD}= 20kΩ		9	9.6	10.5	ms
R_{FLT}	FLTB pull up resistor	(Note 5)			50		kΩ
V_{FAULTB}	FAULTB pin voltage	Sink current = 1mA			0.4	0.6	V
V_{FAULTB_H}	FAULTB pin high enable threshold (IS32LT3124A/B/D/E only)	Voltage rising		2.5			V
V_{FAULTB_L}	FAULTB pin low disable threshold (IS32LT3124A/B/D/E only)	Voltage falling				1	V
t_{FD}	Fault deglitch time	Fault must be present at least this long to trigger the fault detect		20	40	60	μs
V_{SCD}	OUTx pin short to GND threshold	Measured at OUTx voltage falling	IS32LT3124A/E/F	1.15	1.22	1.30	V
			IS32LT3124B/C/D	4.5	4.8	5.0	
V_{SCD_HY}	OUTx pin short to GND hysteresis	Measured at OUTx	IS32LT3124A/E/F	150	250	350	mV
			IS32LT3124B/C/D	150	200	250	
V_{OD}	OUTx pin open threshold	Measured at (V_{ICC}-V_{OUTx}) decreasing		150	220	300	mV
V_{OD_HY}	OUTx pin open hysteresis	Measured at (V_{ICC}-V_{OUTx})		50	120	200	mV
T_{SD}	Thermal shutdown threshold	(Note 5)			165		°C
T_{HY}	Over-temperature hysteresis	(Note 5)			25		°C
Logic Input EN							
V_{EN_TH}	Input enable voltage threshold	Voltage rising		1.18	1.23	1.28	V
V_{HY}	Input hysteresis			20	40	70	mV
f_{PWM}	PWM frequency					1	kHz
t_{ISET_DLY1}	ISET PWM dimming turn on delay time (IS32LT3124B/C/E/F only)	The time between R_{ISET} grounding and output current reaching 90% maximum (Note 5)		3	7	11	μs
t_{ISET_DLY2}	ISET PWM dimming turn off delay time (IS32LT3124B/C/E/F only)	The time between R_{ISET} floating and output current reaching 10% maximum (Note 5)		0.4	4	7	μs

Note 5: Guarantee by design.

Note 6: It is a recommended value to ensure a better line regulation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

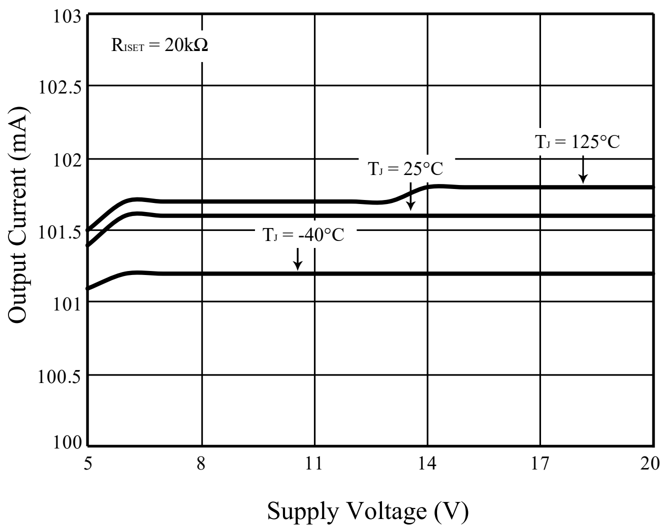


Figure 6 I_{OUT} vs. V_{CC}

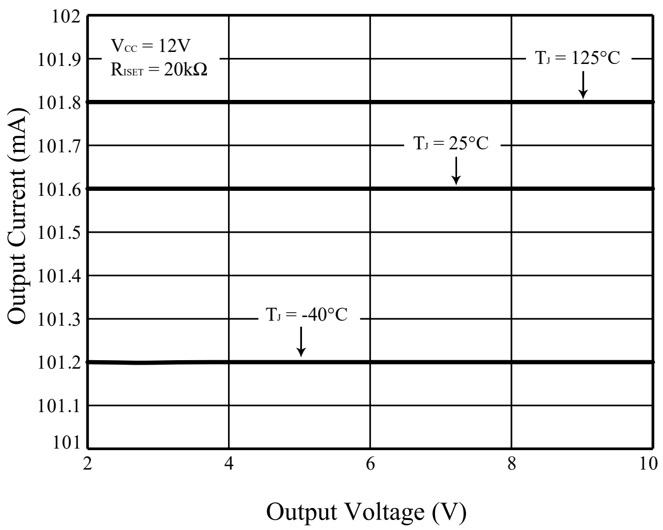


Figure 7 I_{OUT} vs. V_{OUT}

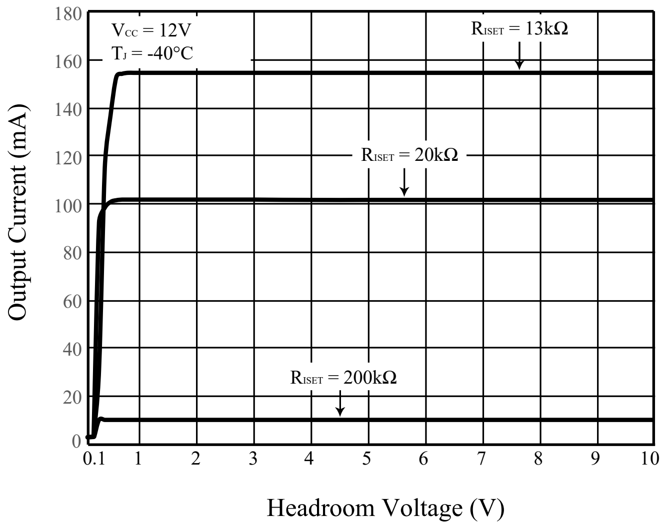


Figure 8 I_{OUT} vs. V_{HR}

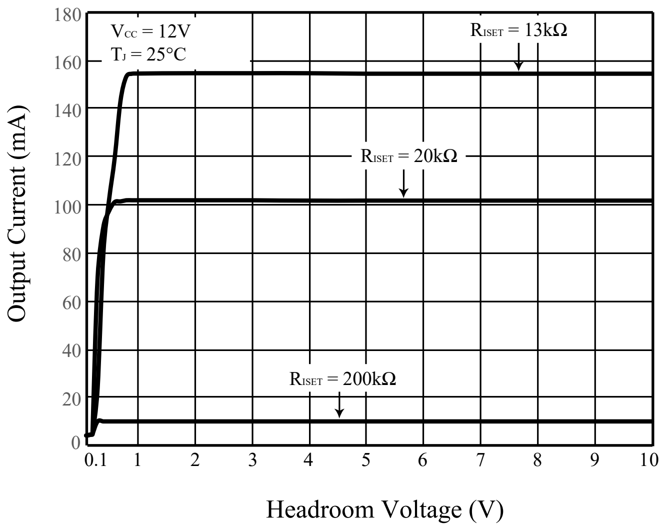


Figure 9 I_{OUT} vs. V_{HR}

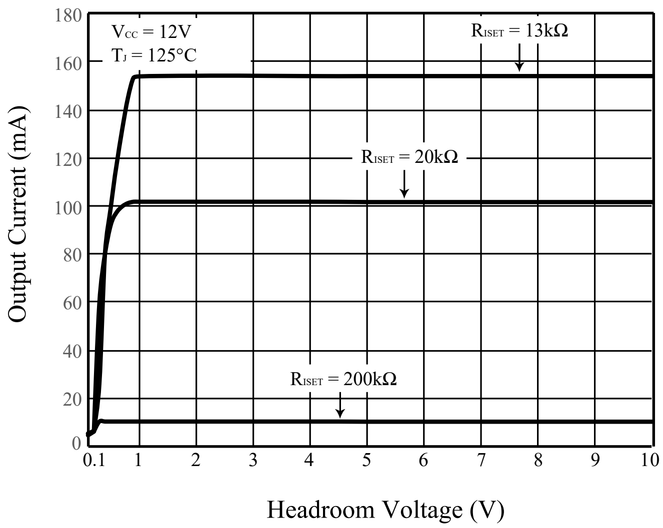


Figure 10 I_{OUT} vs. V_{HR}

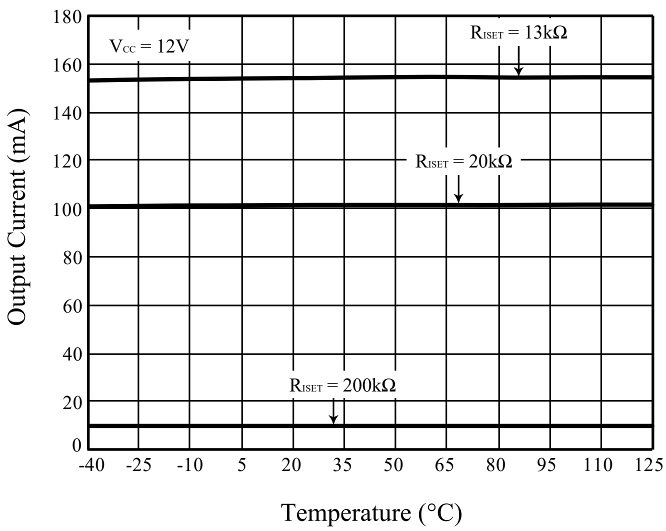


Figure 11 I_{OUT} vs. T_J

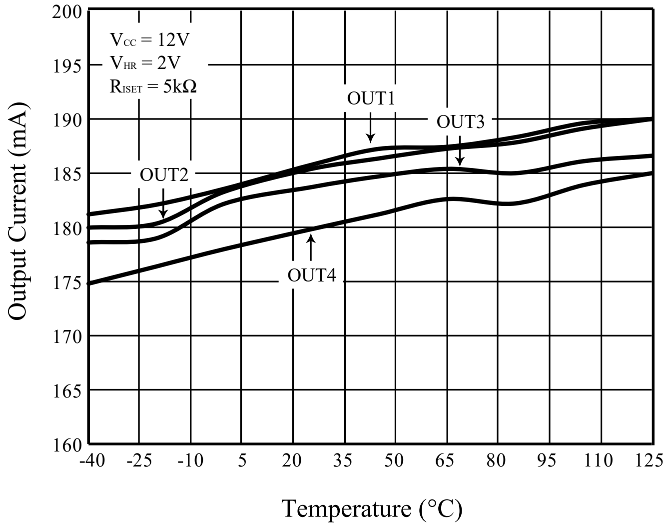


Figure 12 I_{OUT_L} vs. T_J

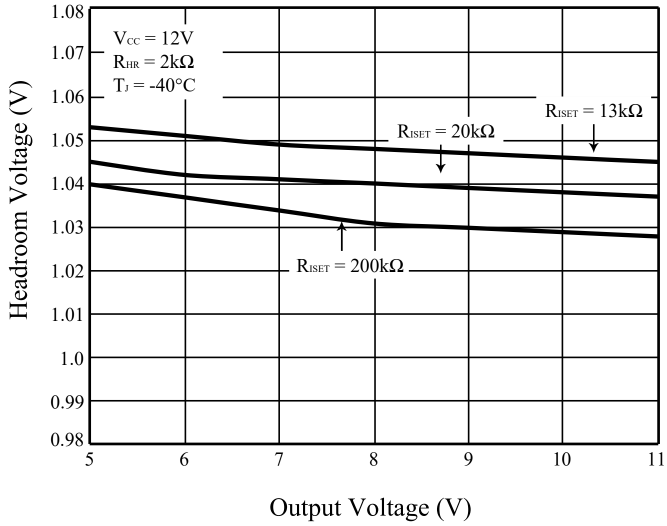


Figure 13 V_{HR} vs. V_{OUT}

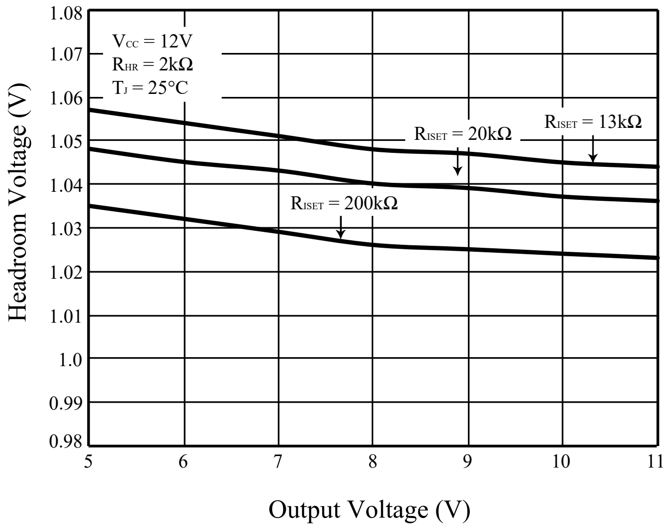


Figure 14 V_{HR} vs. V_{OUT}

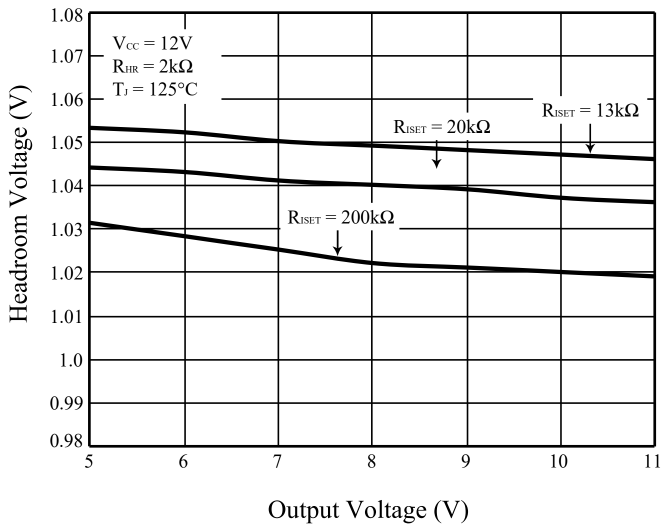


Figure 15 V_{HR} vs. V_{OUT}

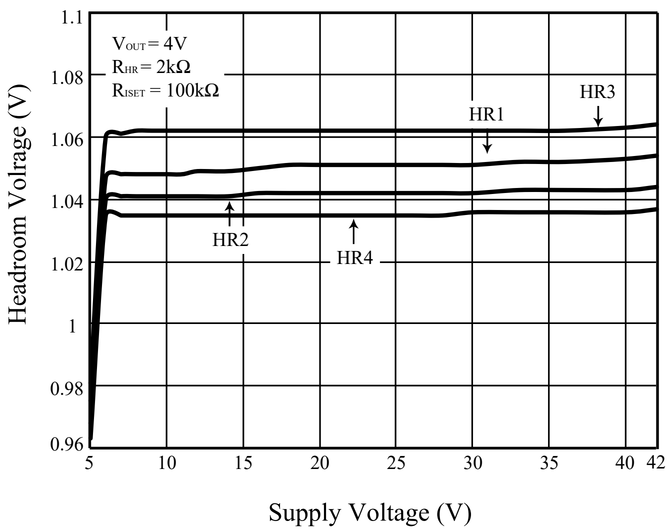


Figure 16 V_{HR} vs. V_{CC}

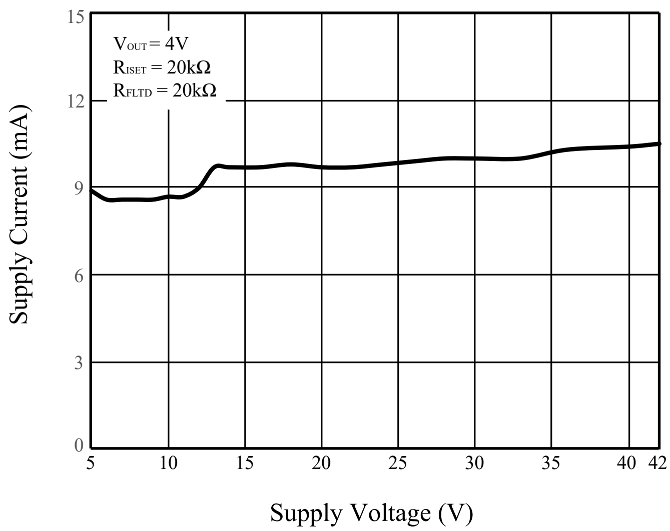


Figure 17 I_{CC} vs. V_{CC}

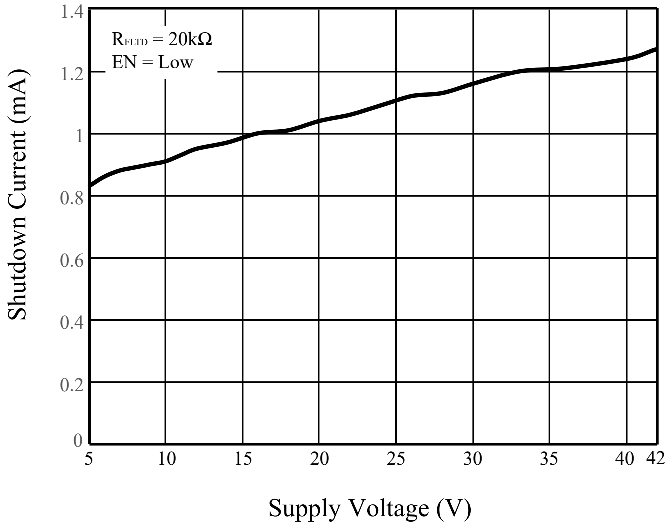


Figure 18 I_{SD} vs. V_{CC} for IS32LT3124A/D

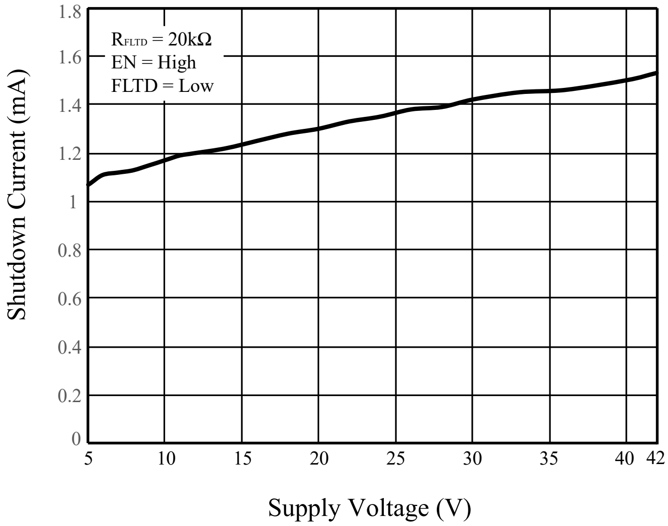


Figure 19 I_{SD_FLT} vs. V_{CC} for IS32LT3124A/B/D/E

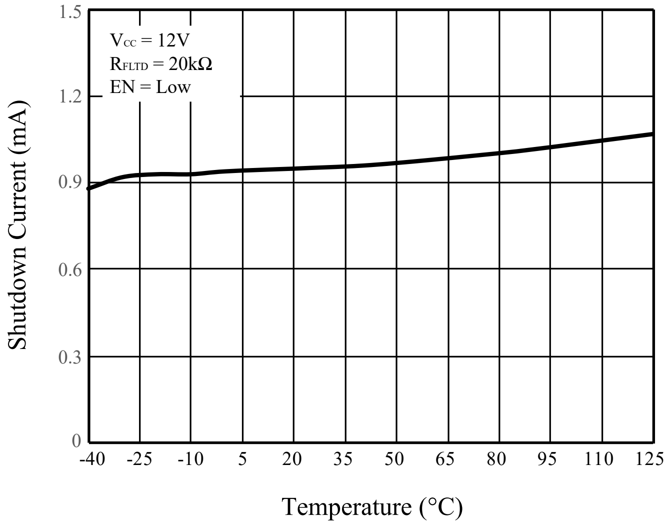


Figure 20 I_{SD} vs. T_J for IS32LT3124A/D

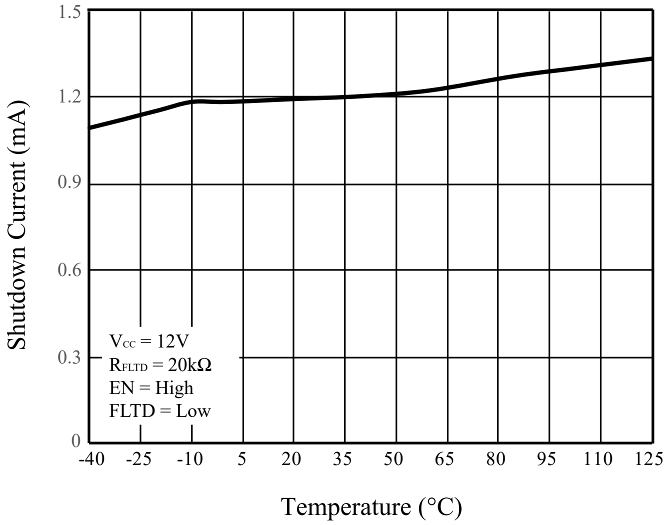


Figure 21 I_{SD_FLT} vs. T_J for IS32LT3124A/B/D/E

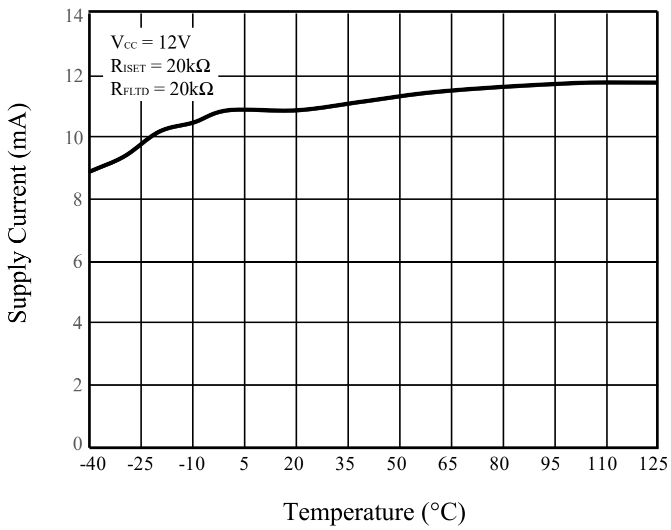


Figure 22 I_{CC} vs. T_J

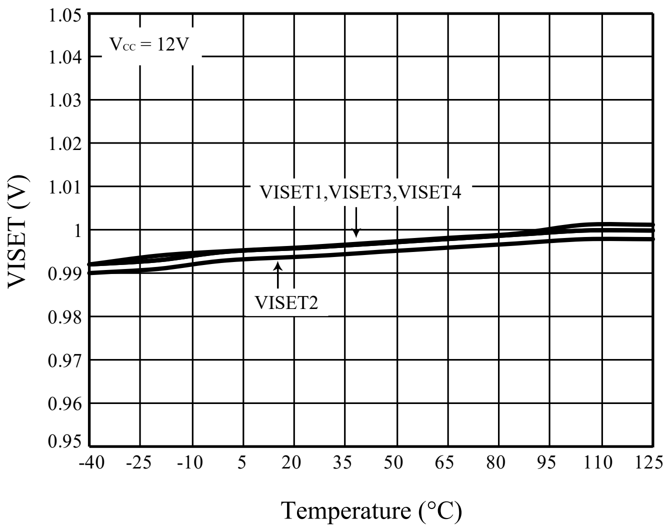


Figure 23 V_{ISET} vs. T_J

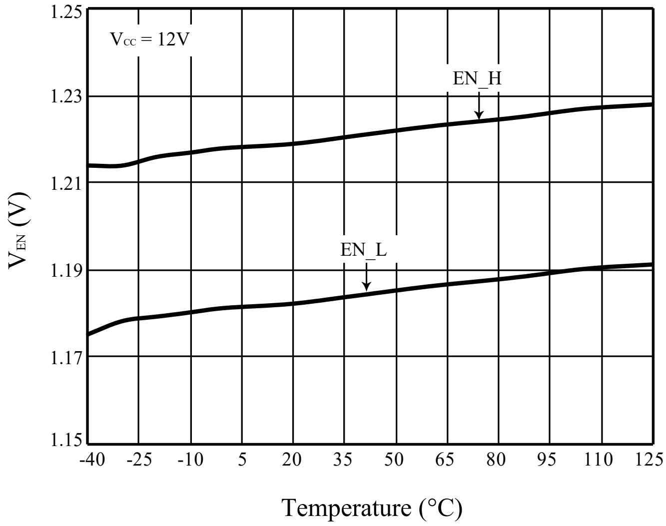


Figure 24 V_{EN_TH} vs. T_J

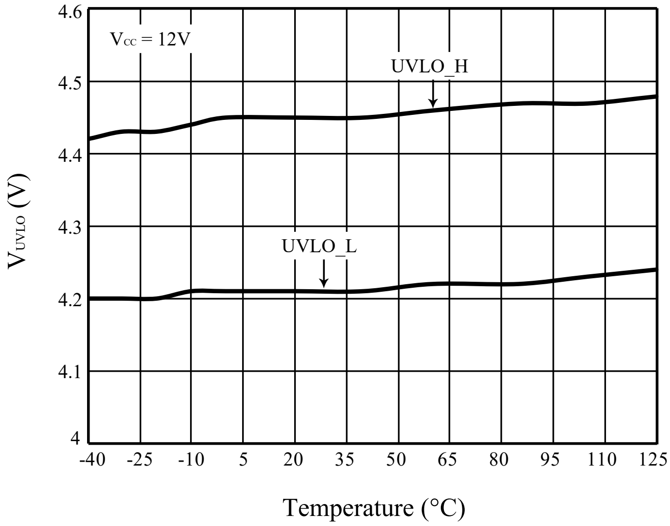


Figure 25 V_{UVLO} vs. T_J

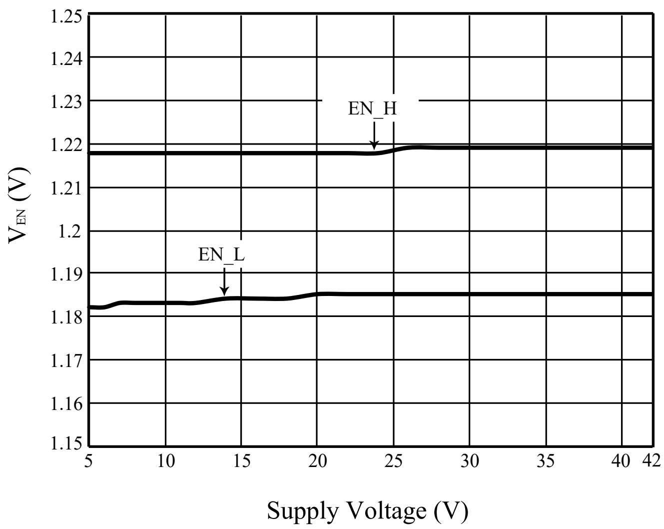


Figure 26 V_{EN_TH} vs. V_{CC}

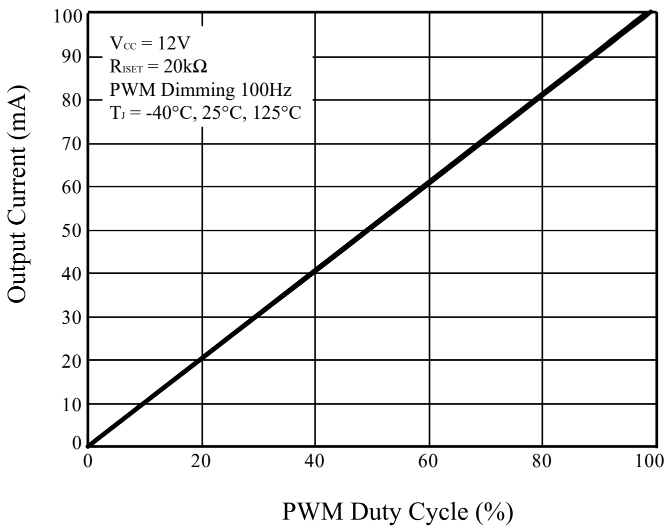


Figure 27 PWM Dimming at 100Hz

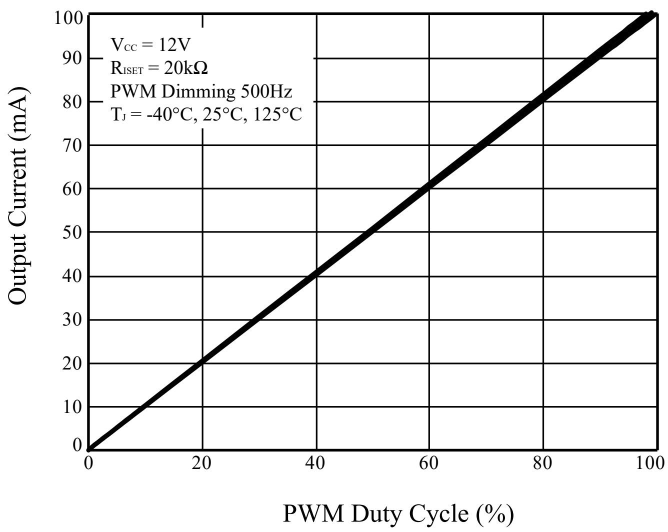


Figure 28 PWM Dimming at 500Hz

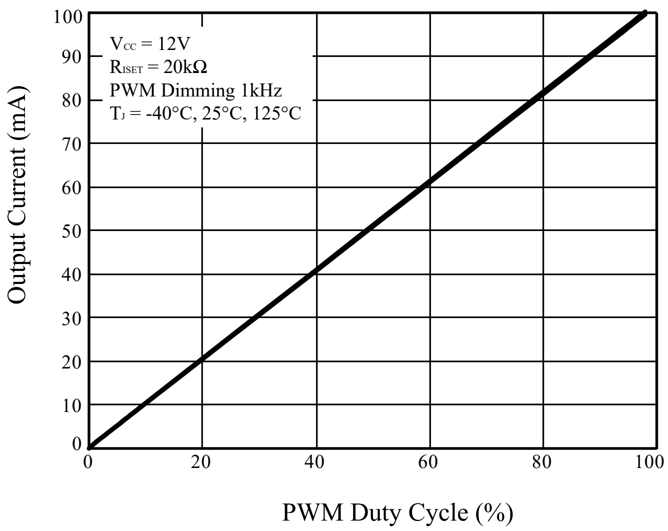


Figure 29 PWM Dimming at 1kHz

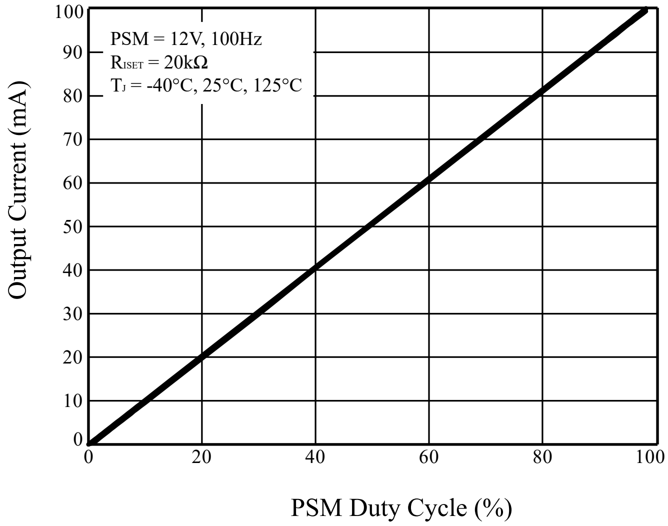


Figure 30 PSM Dimming at 100Hz

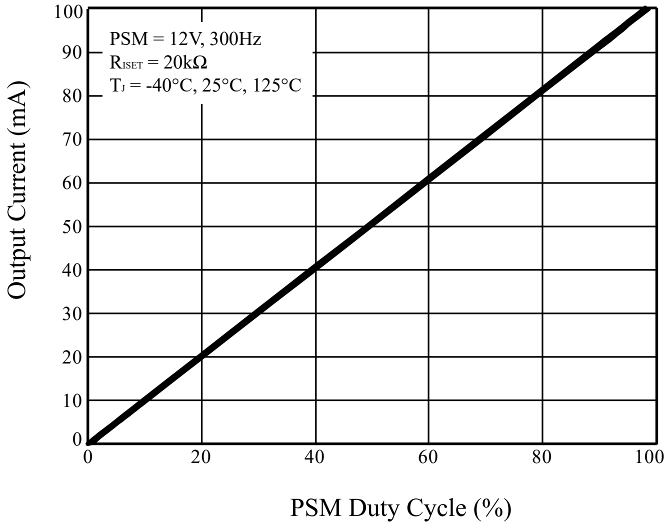


Figure 31 PSM Dimming at 300Hz

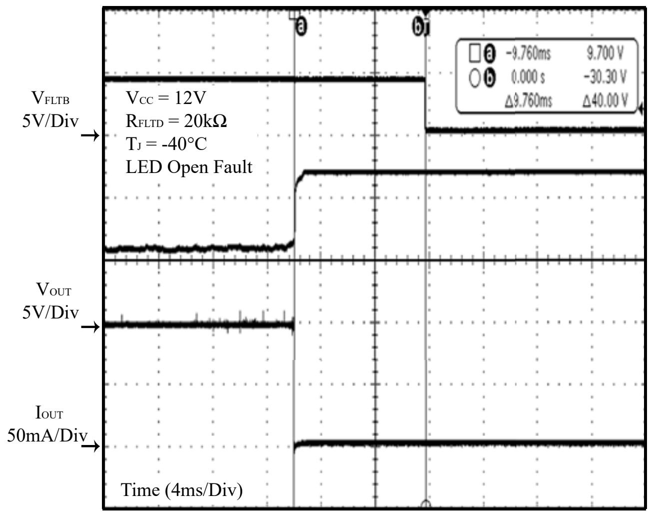


Figure 32 t_{FLTD}

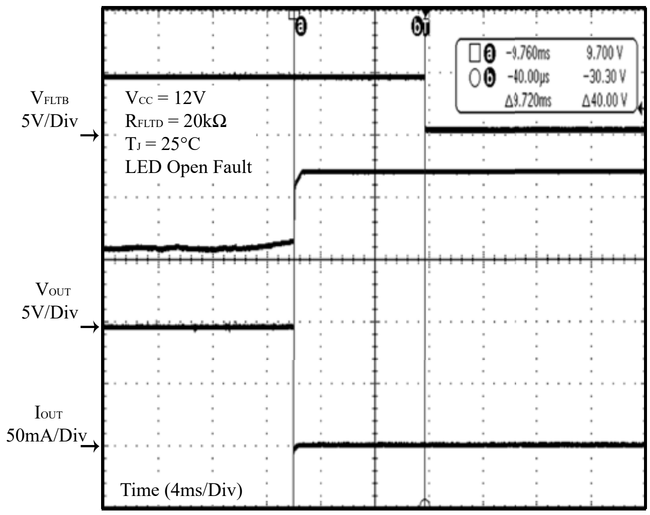


Figure 33 t_{FLTD}

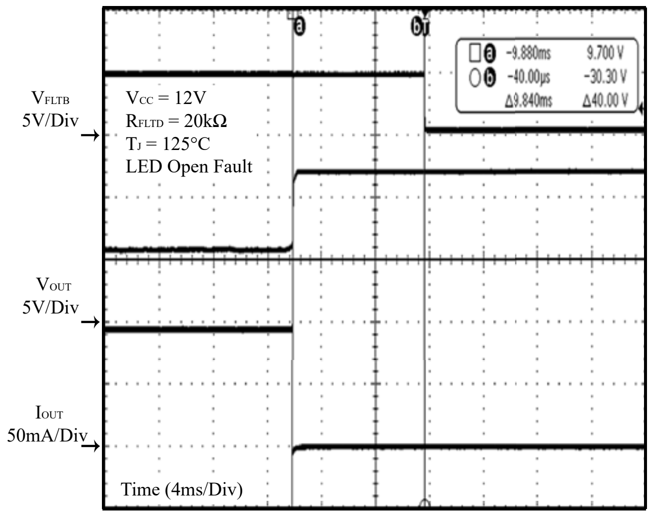


Figure 34 t_{FLTD}

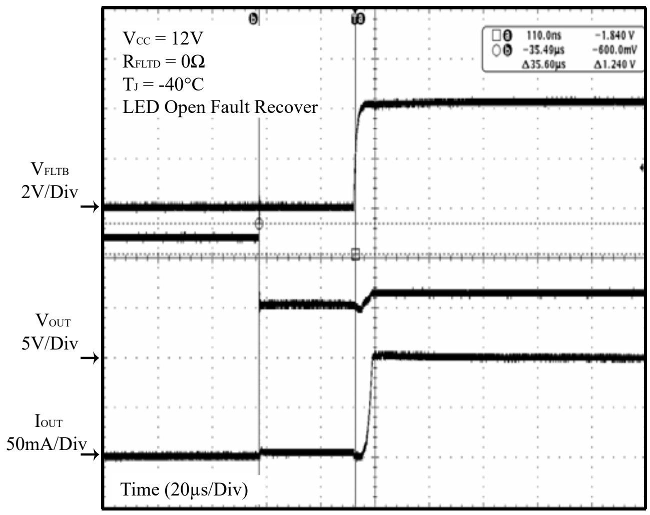


Figure 35 t_{FD}

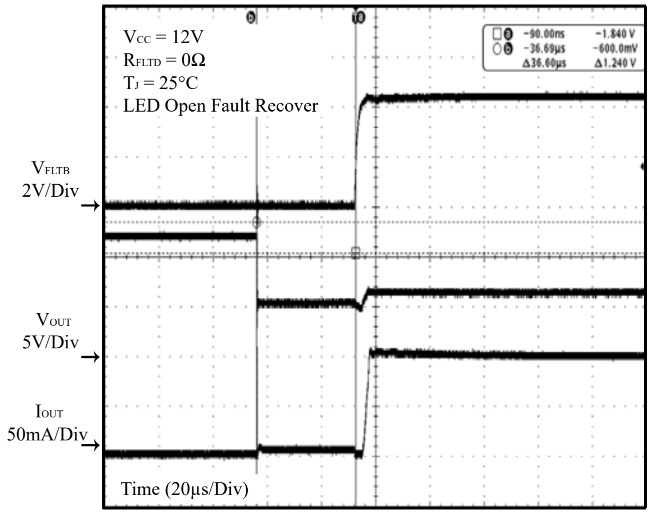


Figure 36 t_{FD}

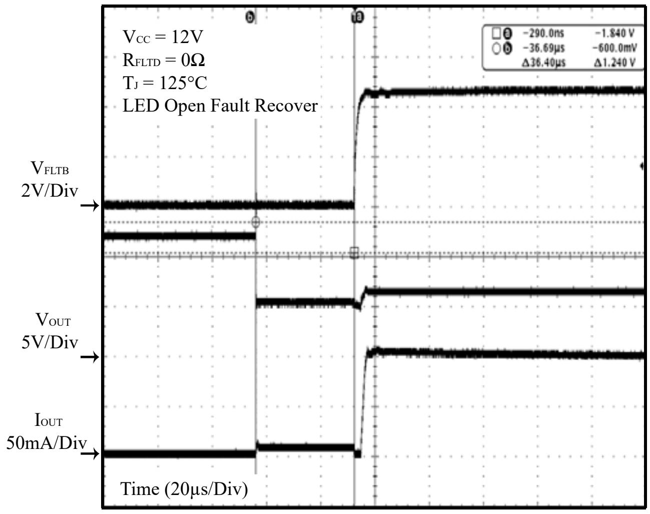


Figure 37 t_{FD}

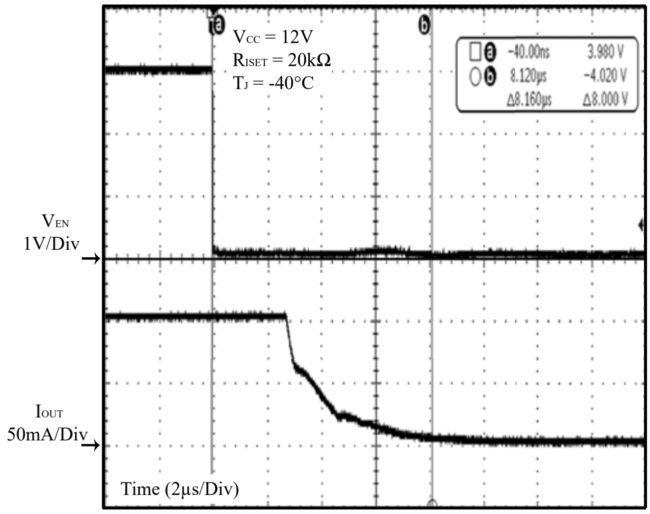


Figure 38 PWM Off Delay Time for IS32LT3124A/D

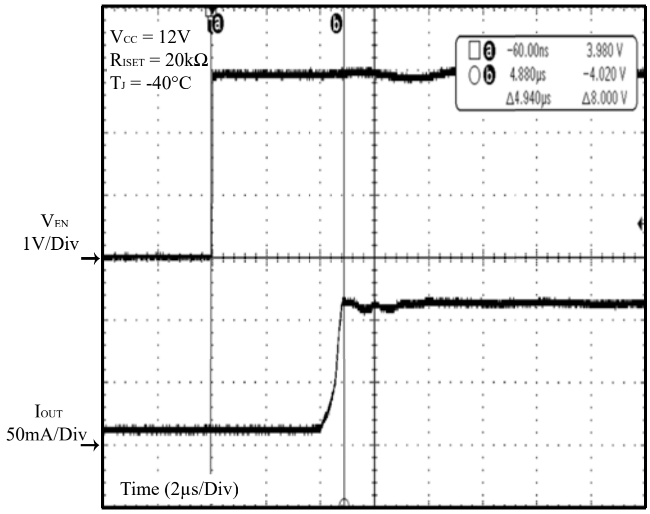


Figure 39 PWM On Delay Time for IS32LT3124A/D

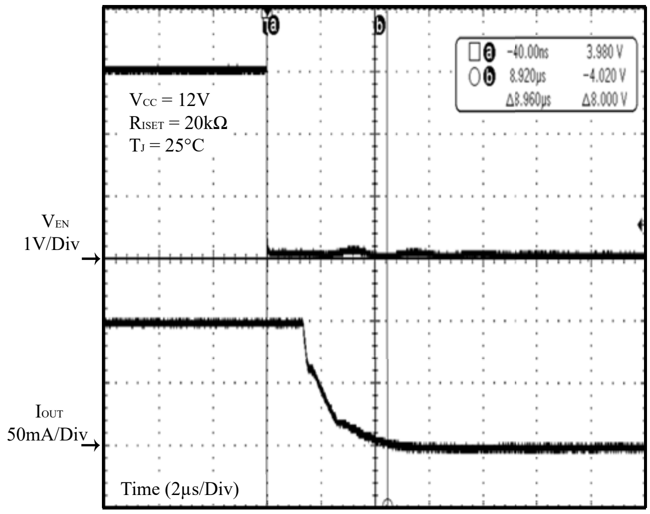


Figure 40 PWM Off Delay Time for IS32LT3124A/D

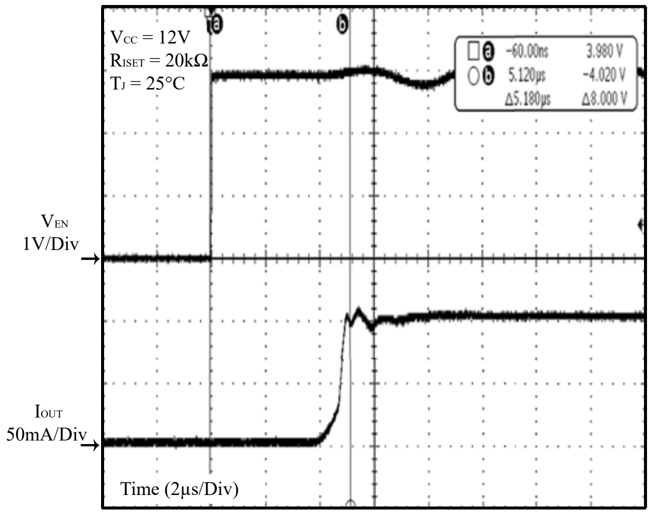


Figure 41 PWM On Delay Time for IS32LT3124A/D

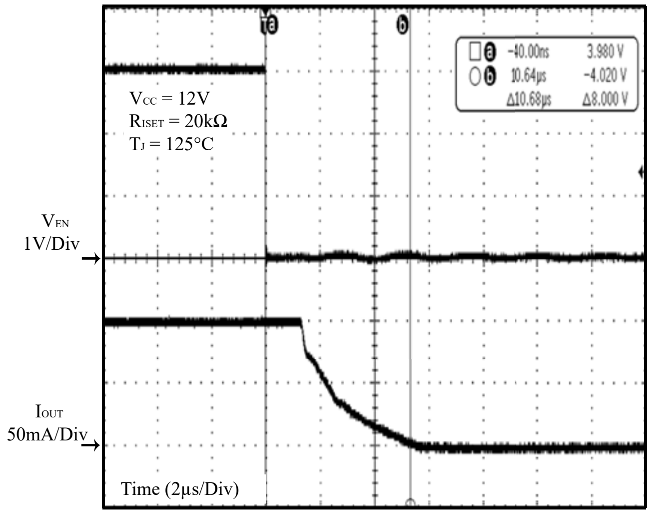


Figure 42 PWM Off Delay Time for IS32LT3124A/D

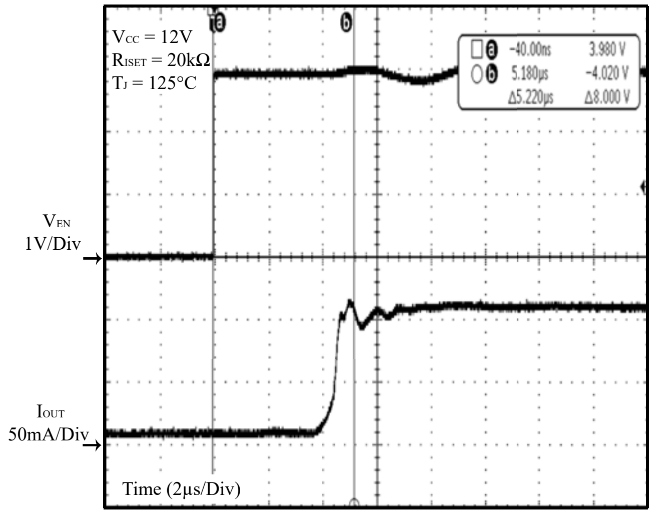


Figure 43 PWM On Delay Time for IS32LT3124A/D

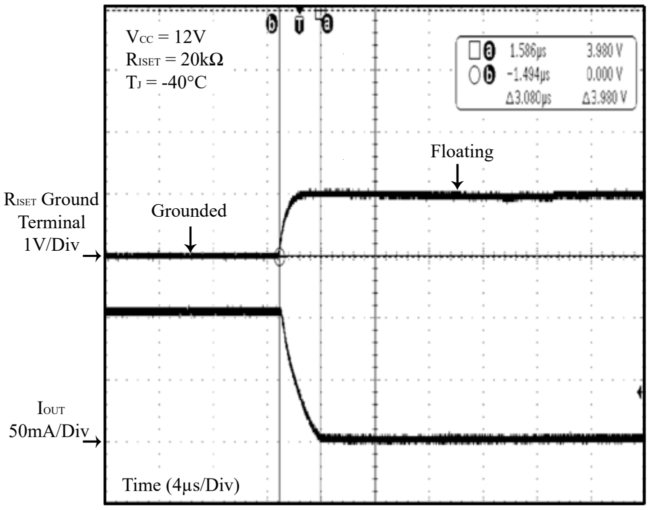


Figure 44 ISET PWM Off Delay Time for IS32LT3124B/C/E/F

Note: Reference Figure 4 and 5

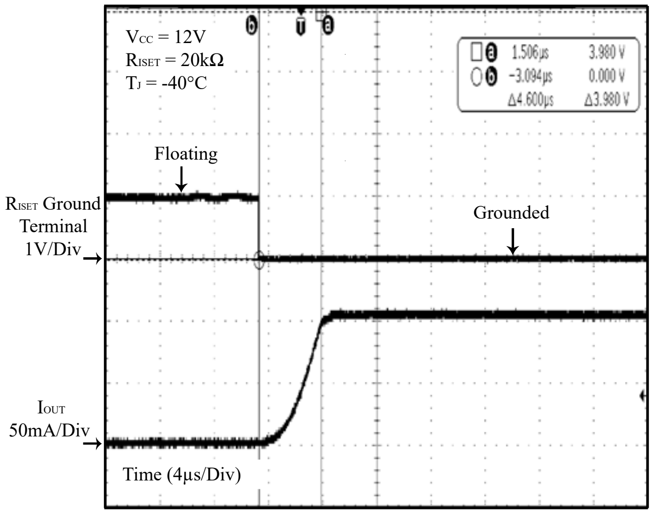


Figure 45 ISET PWM On Delay Time for IS32LT3124B/C/E/F

Note: Reference Figure 4 and 5

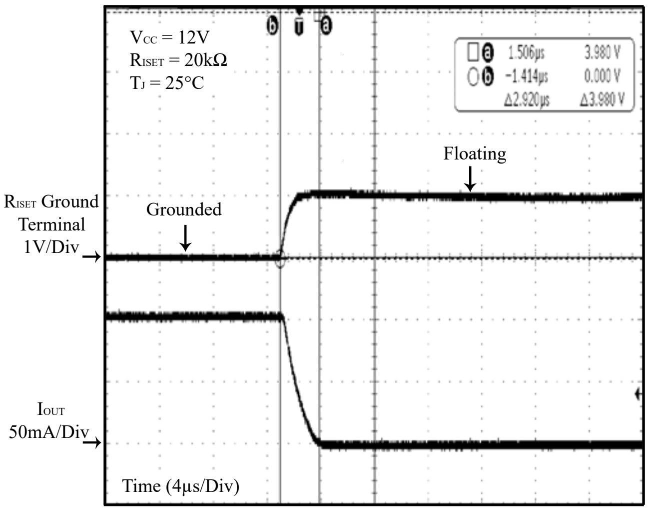


Figure 46 ISET PWM Off Delay Time for IS32LT3124B/C/E/F

Note: Reference Figure 4 and 5

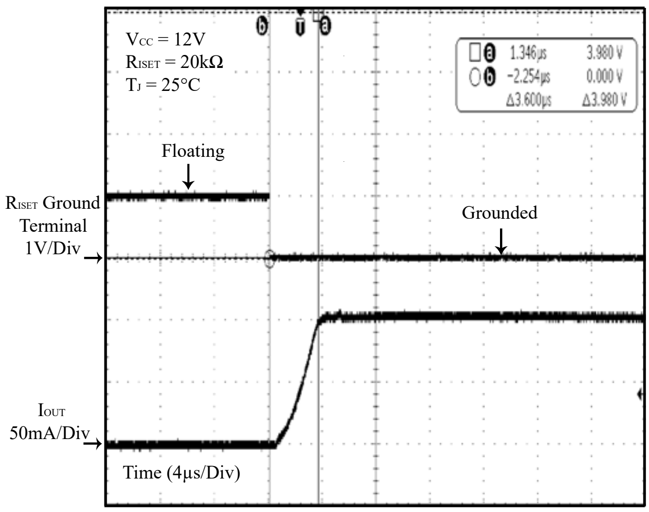


Figure 47 ISET PWM On Delay Time for IS32LT3124B/C/E/F

Note: Reference Figure 4 and 5

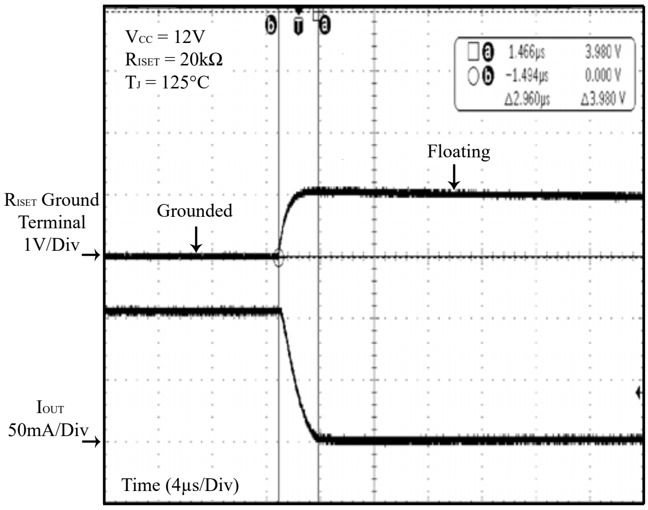


Figure 48 ISET PWM Off Delay Time for IS32LT3124B/C/E/F

Note: Reference Figure 4 and 5

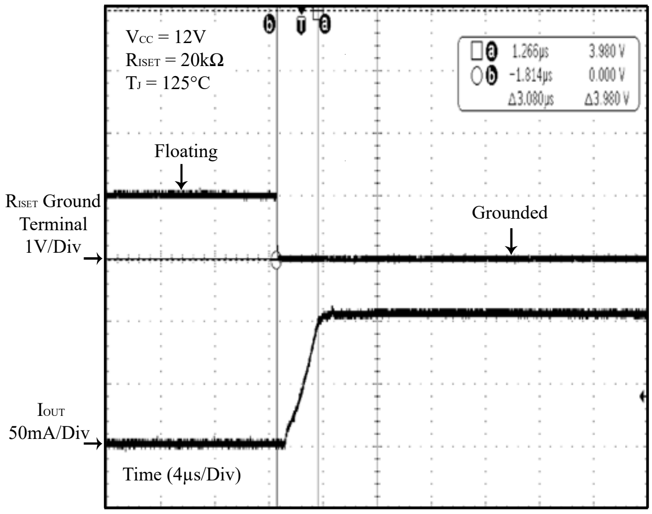


Figure 49 ISET PWM On Delay Time for IS32LT3124B/C/E/F

Note: Reference Figure 4 and 5

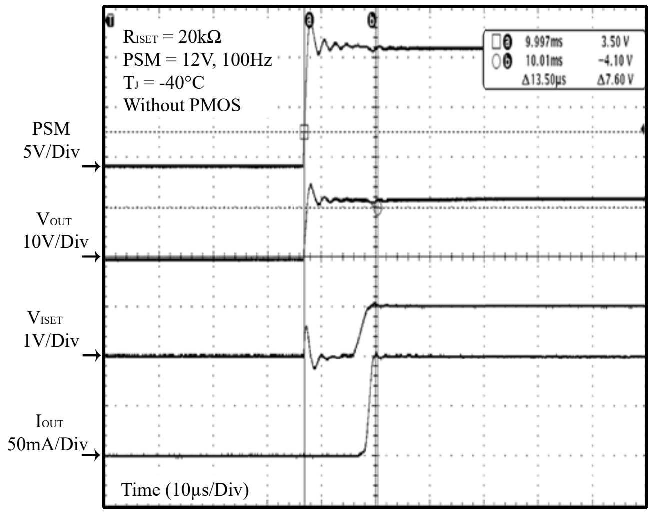


Figure 50 PSM On

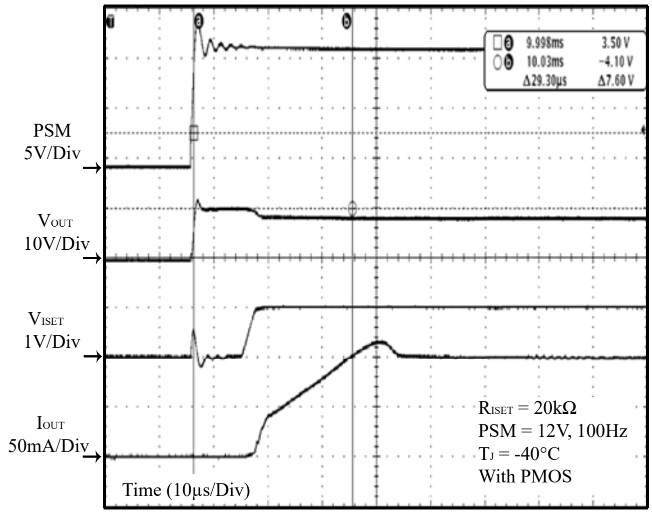


Figure 51 PSM On

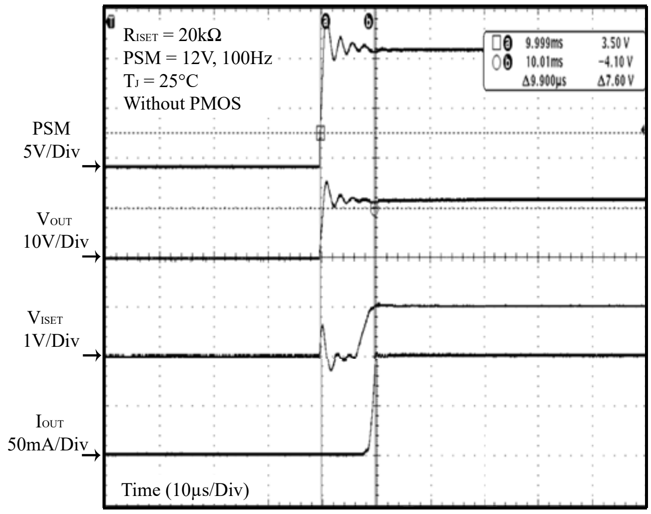


Figure 52 PSM On

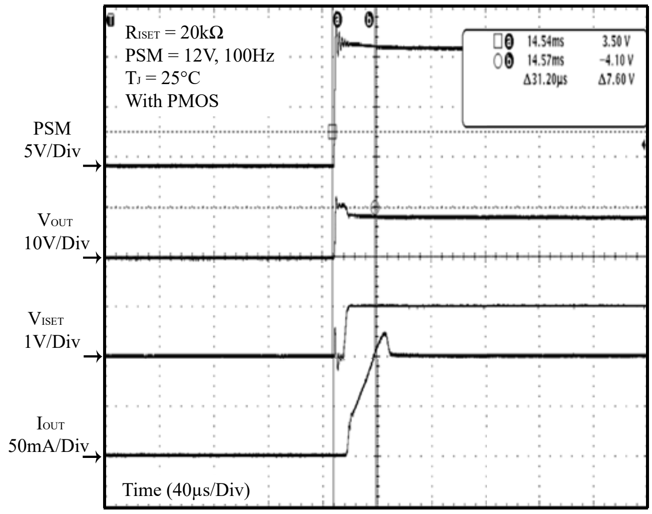


Figure 53 PSM On

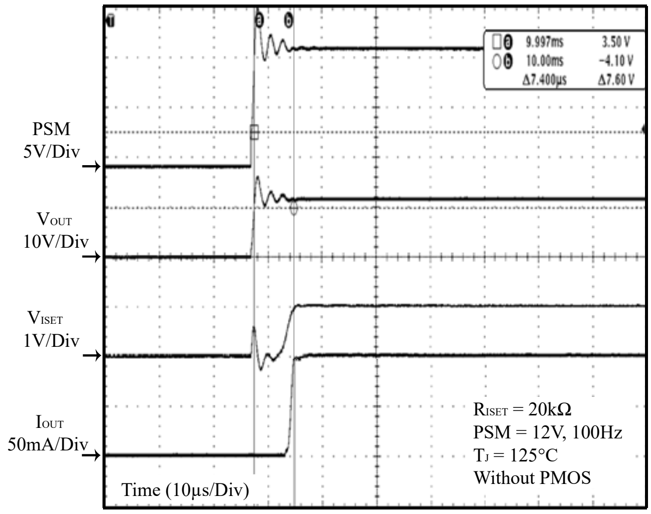


Figure 54 PSM On

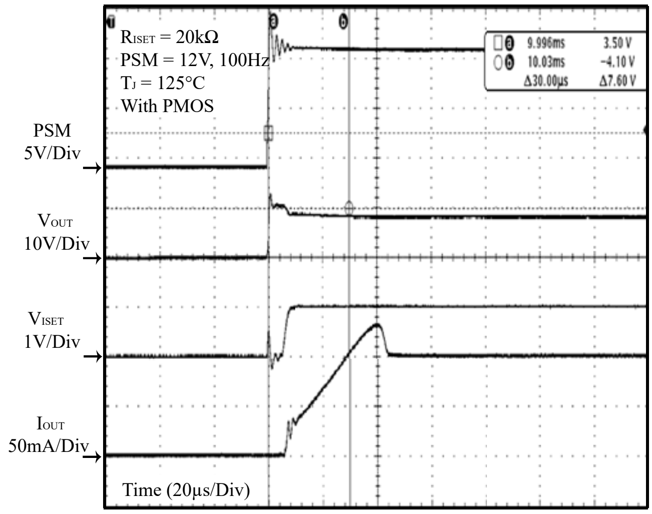


Figure 55 PSM On

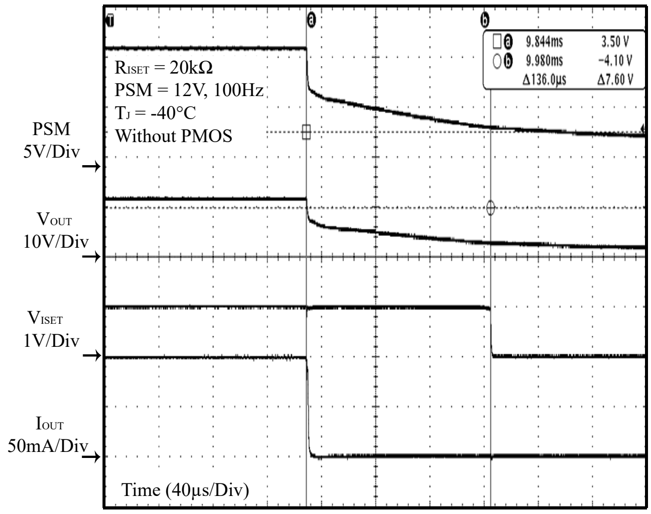


Figure 56 PSM Off

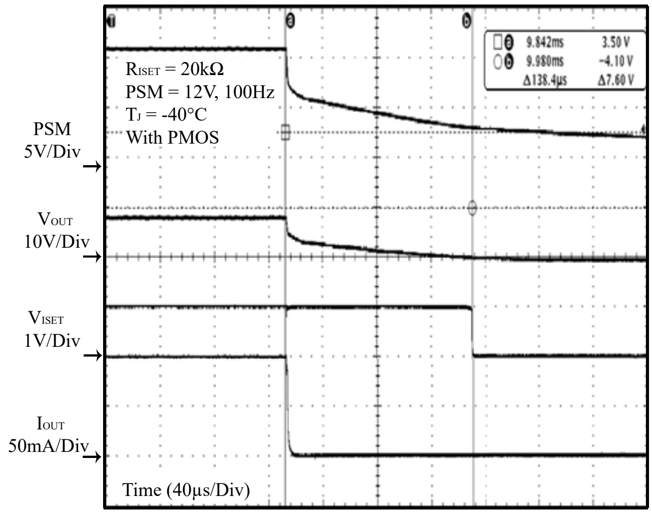


Figure 57 PSM Off

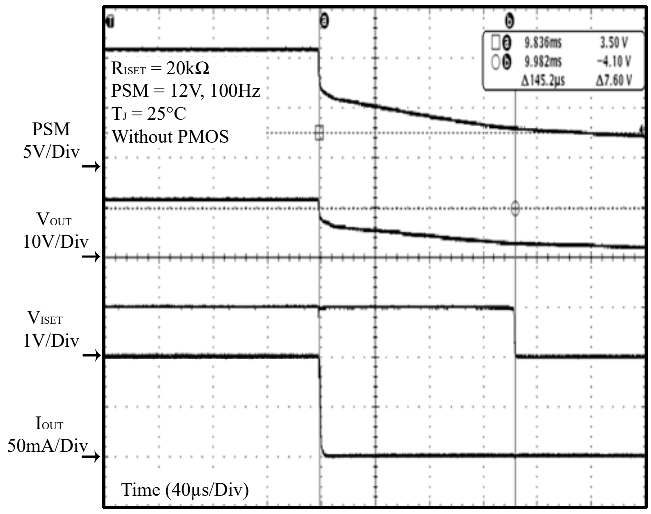


Figure 58 PSM Off

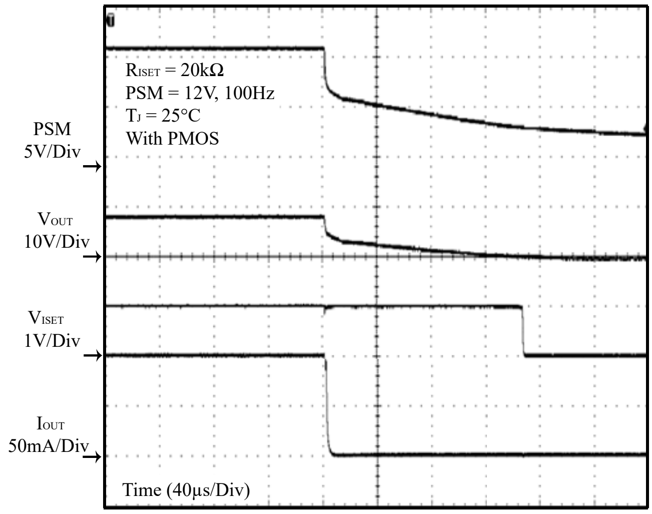


Figure 59 PSM Off

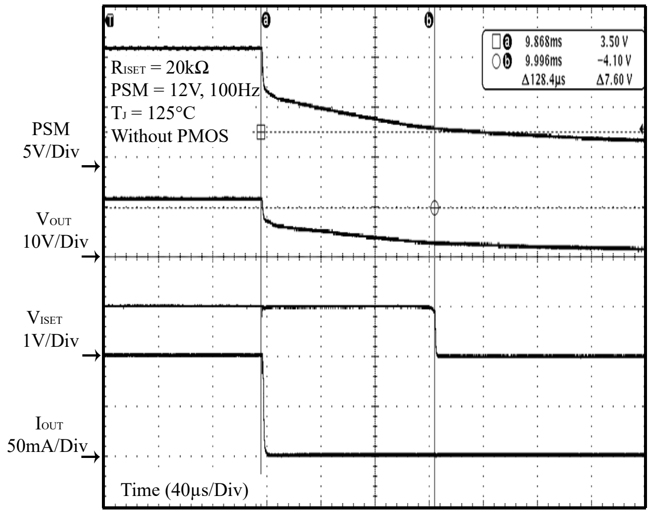


Figure 60 PSM Off

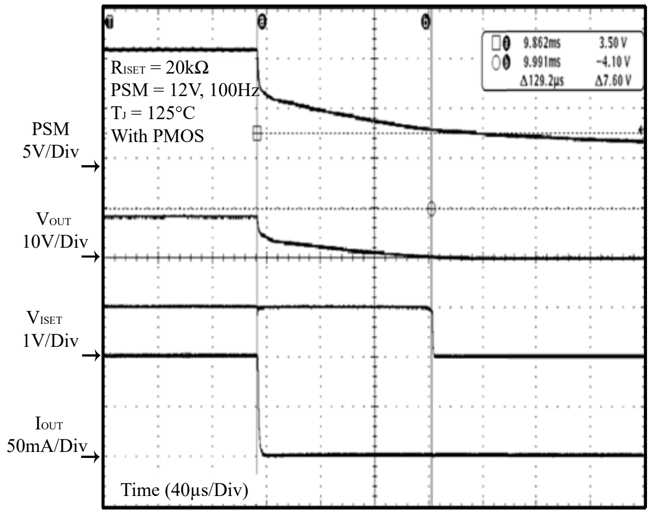


Figure 61 PSM Off

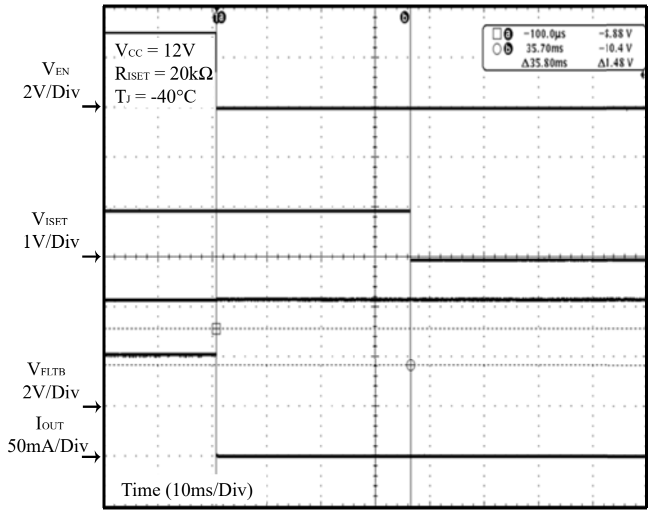


Figure 62 t_{SD} for IS32LT3124A/D

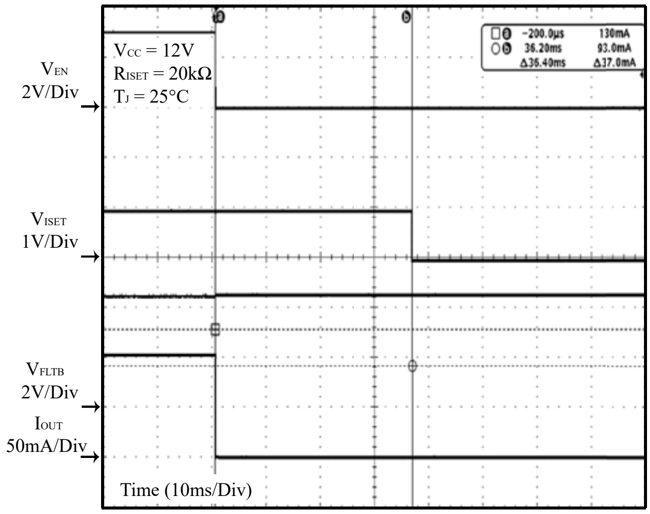


Figure 63 t_{SD} for IS32LT3124A/D

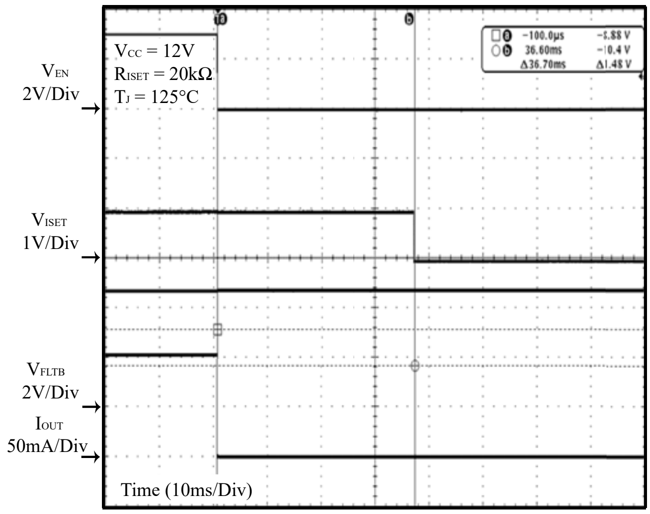


Figure 64 t_{SD} for IS32LT3124A/D

APPLICATION INFORMATION

The IS32LT3124 is a 4-channel linear constant current regulator capable of sourcing 150mA per channel. The device integrates one EN input control and four output currents with individual current set resistors; one for each of the four output current channels. The device can operate with a Power Supply Modulation (PSM) input at the VCC pin input. To minimize device thermal stress, an optional external shunt resistor and PMOS FET can be driven by the IS32LT3124 to share the power dissipation. FLTB pin can be used in a parallel combination to disable multiple IS32LT3124A/B/D/E devices once a fault condition is detected by any one of the devices (One-Fail-All-Fail).

UNDER VOLTAGE LOCKOUT (UVLO)

IS32LT3124 features an under voltage lockout (UVLO) function for the VCC pin. This is an internally fixed value and cannot be adjusted. The device is enabled when the VCC voltage rises to exceed V_{UVLO} (Typ. 4.5V), and disabled when the VCC voltage falls below (V_{UVLO}-V_{UVLO_HY}) (Typ. 4.25V). For the IS32LT3124A/D, the EN pin can be used to set additional UVLO via a resistor divider. Please refer to the EN PIN OPERATION section for more details.

OUTPUT CURRENT SETTING

The regulated LED current (up to 150mA) from each channel is individually set by its corresponding reference resistor (R_{ISETx}). The programming resistors may be computed using the following Equation (1):

$$R_{ISET} = \frac{V_{ISET}}{I_{OUT}} \times 2000 \qquad (1)$$

(13.3kΩ≤R_{ISET}≤200kΩ) and V_{ISET}=1V (Typ.)

It is recommended that R_{ISETx} be a 1% accuracy resistor with good temperature characteristic to ensure stable output current.

The current outputs can be connected in parallel for a combined 600mA or can be left unused as required. Several channels combined in parallel will have the same current accuracy as the independent channel.

In case of some channels are unused, please follow Table 2 to configure the corresponding ISETx and OUTx pins.

Table 2 Unused Channel Configuration

Device	Unused ISETx Pins	Unused OUTx Pins
IS32LT3124A/D	Floating	Connect to VICC
IS32LT3124 B/C/E/F	Floating	Connected to used OUT (refer to Figure 65)

Note: for IS32LT3124A/D, when the ISET pin is floating and the corresponding OUT pin is tied to VICC, the ISET open fault will be ignored and the channel will be recognized as unused.

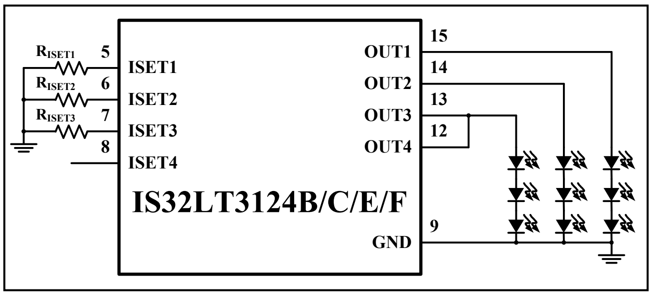


Figure 65 IS32LT3124B/C/E/F Unused Channel Configuration (OUT4 Unused)

EN PIN OPERATION

IS32LT3124A/D:

EN is the device enable pin. The EN voltage must be higher than V_{EN_TH} to enable all outputs and lower than (V_{EN_TH}-V_{HY}) to disable them.

The EN pin of the IS32LT3124A/D can accept a PWM signal to implement simultaneous dimming of all LED strings. The average LED current for each channel can be computed using the following Equation (2).

$$I_{LED} = D_{PWM} \times \frac{V_{ISET}}{R_{ISET}} \times 2000 \qquad (2)$$

D_{PWM} is PWM duty cycle and V_{ISET}=1V (Typ.).

So as to guarantee a reasonably good dimming effect, the recommended PWM frequency range is 100Hz ~ 1kHz. Driving the EN pin with a PWM signal can effectively adjust the LED intensity. The PWM signal voltage levels must meet the EN pin input voltage levels, (V_{EN_TH}-V_{HY}) and V_{EN_TH}. Note: because of the 40μs (typ.) fault deglitch time t_{FD}, the PWM on-time should be greater than 40us to avoid undetermined fault response.

The IC has an internal fixed VCC UVLO set at V_{UVLO}, 4.5V (Typ.). However, it may be desirable to externally set UVLO to track the number of LED's used in the string. For PSM dimming application, the higher UVLO will track the PSM off time to get more accurate PSM dimming. The EN pin can be used to set a VCC under voltage lockout threshold via a resistor divider.

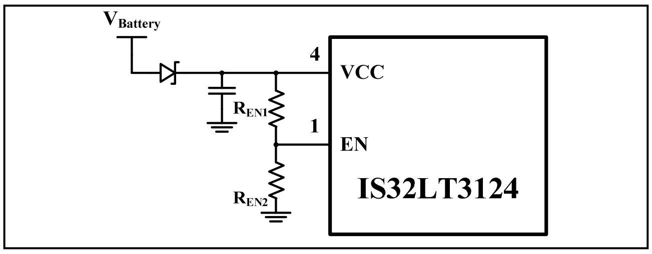


Figure 66 EN Pin Set External UVLO

The UVLO threshold voltage can be computed using the following Equation (3):

$$V_{CC\_UVLO} = V_{EN\_TH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} \quad (3)$$

IS32LT3124B/C/E/F:

The EN pin is fault reporting enable pin, when pulled low to disable fault reporting, the output currents and the internal IC fault action operate normally but no fault output is generated. The EN voltage is higher than V_{EN_TH} to enable fault reporting (FLTB low output) and lower than (V_{EN_TH}-V_{HY}) to disable all fault reporting (FLTB low output).

In some applications, the IS32LT3124A/B/C/D/E/F with a resistor divider from VCC as Figure 66, helps prevent false LED open detection due to the LED string losing its headroom voltage, such as when VCC rises up from zero during power up or PSM dimming. The recommended V_{CC_UVLO} setting level is:

$$V_{CC\_MIN} \geq V_{CC\_UVLO} \geq V_{OUT\_MAX} + V_{HRSET} \quad (4)$$

Where, V_{CC_MIN} is the minimum VCC voltage, V_{OUT_MAX} is the maximum forward voltage of 4 LED strings and V_{HRSET} is the setting minimum headroom voltage (refer to DYNAMIC HEADROOM CONTROL section).

DYNAMIC HEADROOM CONTROL (DHC) AND THERMAL CONSIDERATIONS

The power dissipation of a linear constant current LED driver depends on the ratio of the output and input voltages. When the input and output voltages are determined, an increase in output current will increase power dissipation on the driver IC and it can be calculated by the following Equation:

$$P_{IC} = (V_{CC} - V_{OUT}) \times I_{OUT} = V_{HR} \times I_{OUT} \quad (5)$$

Where, V_{HR} is the headroom voltage, which is the voltage drop on the OUTx pin. Due to the limited driver IC power rating, a typical linear constant current LED driver cannot be used for high current applications. To solve this power dissipation issue, IS32LT3124 features a Dynamic Headroom Control (DHC) function which splits the power dissipation among the driver IC and external components to significantly minimize the driver IC thermal. This enables the IS32LT3124 to support up to 600mA total output current with acceptable heat, independent of the output to input voltage ratio.

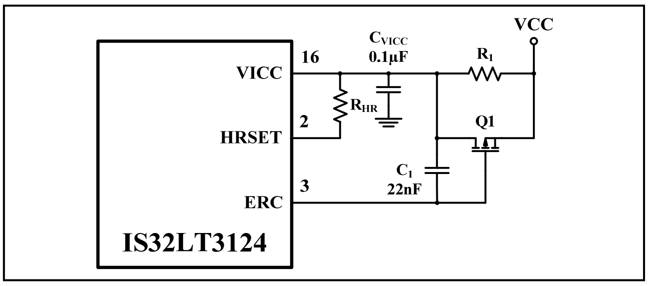


Figure 67 DHC Circuit

The DHC can be configured into two modes: Shunt Regulator mode and Series Regulator mode. The Series Regulator mode is recommended for the application of ≤300mA total output current and the Shunt Regulator mode is good for >300mA application. The basic circuits of both modes are the same however R_1 value decides the operating mode. To optimize the stability of the PMOS FET control loop, please use the fixed value for them: C_1=22nF and C_{VICC}=0.1µF.

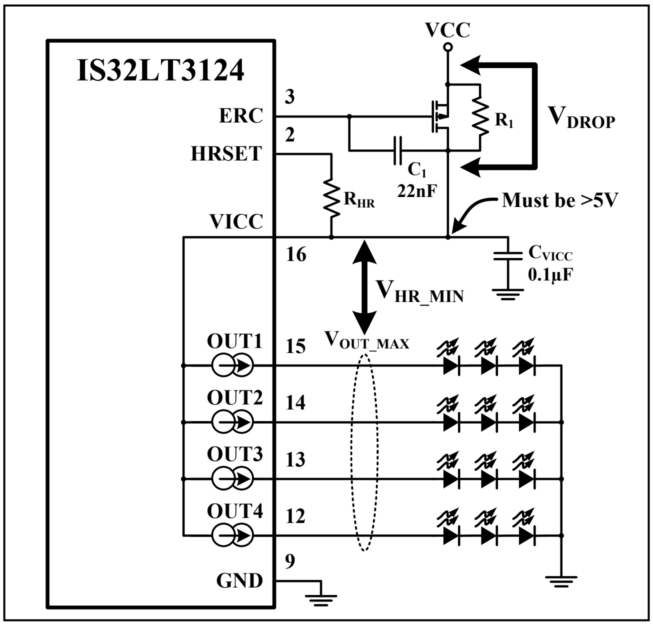


Figure 68 DHC Operating

Series Regulator Mode:

Choose 1kΩ value for R_1 and the DHC circuit will operate in Series Regulator mode. The integrated circuit compares the minimum headroom voltage of all four output channels against the headroom setting V_{HRSET}, which is set by the resistor R_{HR} from the HRSET and VICC pins, and dynamically drives the external power PMOS FET to maintain this minimum headroom voltage always equal to V_{HRSET}. As Figure 69 shows, the minimum headroom voltage will appear on the channel with the maximum LED string forward voltage. Therefore, the output voltage of the Series Regulator, V_{VICC}, can be calculated by the Equation (6) and (7):

$$V_{VICC} = V_{OUT\_MAX} + V_{HRSET} \quad (6)$$

$$V_{HRSET} = R_{HR} \times \left(\frac{1V}{2000}\right) \quad (7)$$

Where, V_{OUT_MAX} is the maximum voltage of four OUTx pins.

According to Equation (6), once the LED strings are determined and the input voltage is sufficient higher than V_{VICC}, the V_{VICC} is constant if R_{HR} is fixed. No matter how high the input voltage is, the headroom voltage of each channel is constant all the time, so the power dissipation on IS32LT3124 is constant as well (I_{CC} current is negligible and ignored in following calculation). However, it can be programmed by the V_{HRSET} setting; the higher V_{HRSET} the larger power dissipation on IS32LT3124. The remaining power dissipation is dropped on the external PMOS FET. Their power consumption can be calculated by:

$$P_{3124} = \sum_{x=1}^{4} (V_{VICC} - V_{OUTx}) \times I_{OUTx} \quad (8)$$

$$P_{PMOS} = (V_{CC} - V_{VICC}) \times I_{TOT} \quad (9)$$

Where, I_{TOT} is the total current of all output channels.

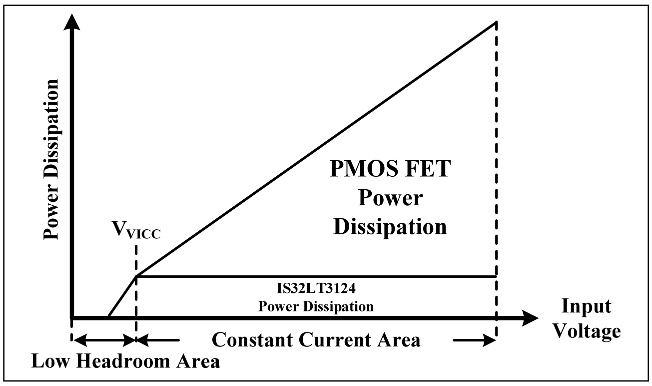


Figure 69 Power Dissipation Distribution in Series Regulator Mode

Shunt Regulator Mode:

In the Series Regulator mode, the headroom voltage is constant however the external PMOS FET must support any excess voltage. When the total output current exceeds 300mA, the V×I power dissipation on the PMOS FET may be excessive. To prevent thermal run away, the Shunt Regulator mode could be considered. Choose a proper value (lower than 1KΩ) for R_1, DHC circuit will operate in Shunt Regulator mode which manages the power dissipation among the IS32LT3124, external PMOS FET, and the shunt resistor R_1. R1 sharing the power dissipation will significantly minimize the power dissipation on the PMOS FET.

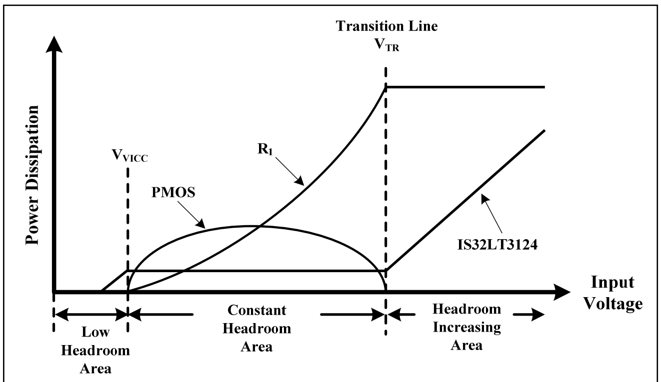


Figure 70 Power Dissipation Distribution in Shunt Regulator mode

As Figure 70 shows, the power dissipation has different distribution in different areas. When the input voltage is higher than V_{VICC}, the transition line (V_{TR}) splits it into two areas: constant headroom area and headroom increasing area.

In the Constant Headroom Area, the DHC circuit regulates the minimum headroom voltage equal to V_{HRSET}, same as the Series Regulator mode. So the IS32LT3124 power dissipation is constant:

$$P_{3124} = \sum_{x=1}^{4} (V_{VICC} - V_{OUTx}) \times I_{OUTx} \quad (10)$$

While the PMOS FET and R_1 share the remaining power dissipation which will vary following the input voltage. Their power dissipation in the Constant Headroom Area can be calculated by:

$$P_{R1} = \frac{(V_{CC} - V_{VICC})^2}{R_1} \quad (11)$$

$$P_{PMOS} = (I_{TOT} - \frac{V_{CC} - V_{VICC}}{R_1}) \times (V_{CC} - V_{VICC}) \quad (12)$$

The power dissipation of the PMOS FET peaks at the center point of (V_{TR}-V_{VICC}) and decreases to zero at V_{TR}. The transition point V_{TR} can be adjusted by the R_1 value:

$$V_{TR} = V_{VICC} + R_1 \times I_{TOT} \quad (13)$$

Beyond the transition line V_{TR} is the Headroom Increasing Area. DHC is no longer effective since the PMOS FET is off. PMOS FET has no power dissipation anymore and the power dissipation is solely shared by IS32LT3124 and R_1. The power dissipation of R1 becomes constant while the power dissipation of the IS32LT3124 starts to increase following the input voltage. Their power dissipation in the Headroom Increasing Area can be calculated by:

$$P_{3124} \approx \sum_{x=1}^{4} (V_{CC} - I_{TOT} \times R_1 - V_{OUTx}) \times I_{OUTx} \quad (14)$$

$$P_{R1} = I_{TOT}^{\ 2} \times R_1 \quad (15)$$

$$P_{PMOS} = 0 \quad (16)$$

In the Headroom Increasing Area, the system relies on the thermal shutdown protection feature of the IS32LT3124. Select a proper R1 value so the Constant Headroom Area covers the desired operating voltage range. For instance, the required operating voltage range is 9V~16V. The VICC should be set below 9V and set V_{TR} above 16V.

Lumissil has a downloadable Excel spread sheet to calculate the power dissipation of these key components: IS32LT3124, PMOS FET and shunt resistor. In the Shunt Regulator mode, the shunt resistor R_1 sustains plenty of power dissipation at high input voltage. Please make sure the R_1 has sufficient power rating to avoid thermal stress of the resistor.

Several large package resistors in parallel should be used for R_1.

EXTERNAL PMOS FET SELECT (OPTIONAL)

The PMOS FET must be chosen with its drain voltage rating V_{DS} greater than the Transient Voltage Suppressor (TVS) clamp voltage of the load dump protection. The IS32LT3124 integrates a 15V overvoltage protect circuit to clamp the voltage between VCC and ERC pins for PMOS FET gate protection purpose. So the gate to source maximum voltage rating V_{GS} of the PMOS FET should be greater than 15V to avoid accidental damage. And its current rating should be greater than the total current of all channels. Moreover, the static drain to source on resistance (R_{DS_ON}) of the PMOS FET should be considered. It affects the minimum voltage drop across VCC to VICC:

$$V_{DROP\_MIN} \le V_{CC\_MIN} - V_{VICC} \quad (17)$$

$$V_{DROP\_MIN} = R_{DS\_ON} \times (I_{OUT1} + I_{OUT2} + I_{OUT3} + I_{OUT4}) \quad (18)$$

Where, V_{CC_MIN} is the minimum input voltage.

In addition, because the PMOS FET doesn't have an over temperature protection mechanism, the power rating of the PMOS FET should be carefully considered to sustain the maximum power dissipation on it. A PMOS FET with a big thermal PAD and low thermal resistance is preferred, such as a D-PAK or SOT-223 package. When several devices are connected in parallel to share one PMOS FET (as Figure 2), all the output currents of those devices without PMOS FET should be calculated together as the total current thru the PMOS FET.

The DHC function is not necessary for the IS32LT3124 in low current applications. Such as when the total output current is much lower than 300mA. If not used, the external PMOS FET can be omitted and VICC should be tied to VCC pin, and leave HRSET and ERC pins floating (as Figure 3).

HEADROOM SETTING

As previously stated, the headroom voltage is set by the resistor R_{HR} from the HRSET and VICC pins:

$$V_{HRSET} = R_{HR} \times \left(\frac{1V}{2000}\right) \quad (19)$$

The IS32LT3124 internally limits the maximum V_{HRSET} to 3.0V (typical) to ensure reasonable thermal on the IS32LT3124. A headroom voltage setting of 1.5V~2.5V is recommended for most application.

To maintain the normal operation of the internal detection circuit and the dynamic head room control, the VICC voltage must be set above 5V, otherwise the DHC circuit will be abnormal and the V_{HR_MIN} cannot be maintained at set value.

$$R_{HR} \times \left(\frac{1V}{2000}\right) + V_{OUT\_MAX} > 5V \quad (20)$$

Therefore in low LED string voltage application, e.g. one RED LED with around 2V forward voltage, some appropriate value power resistors in series with LED strings should be used to increase the maximum voltage of four OUTx pins. The power resistor value R_P can be calculated by:

$$\frac{V_{VICC} - V_{OUT\_MAX}}{I_{OUT\_X}} > R_P > \frac{5V - V_{OUT\_MAX}}{I_{OUT\_X}} \quad (21)$$

Where, V_{OUT_MAX} is the maximum voltage of four OUTx pins without any power resistor and I_{OUT_X} is the current of this channel.

Note: the approach of adding the series power resistor is only available for IS32LT3124A/E/F versions. The IS32LT3124B/C/D using the series power resistor would falsely trigger short fault protection and latched all outputs off. So IS32LT3124B/C/D only can drive the LED string with the forward voltage > (V_{SCD_MAX}+V_{SCD_HY}).

DYNAMIC HEADROOM CONTROL (DHC) SHARING

To save the cost and PCB space in some application, several devices can be connected in parallel to share one PMOS FET (as Figure 2). This scheme is available for both the Series Regulator and the Shunt Regulator modes. The IC connected to system voltage (Supervisor) must connect one output channel (with its ISET pin left floating) to the HRSET pin of the next device (with ECR pin floating and same value R_{HR} as the supervisor). The supervisor IC's DHC circuit will manage the power dissipation of the devices without PMOS FET along with itself. In this way, the power dissipation on the PMOS FET and R_1 should be carefully considered to make sure its junction temperature won't exceed its maximum rating in extreme ambient temperature. This approach is suitable for applications with low per channel current.

POWER SUPPLY MODULATION (PSM) DIMMING

The IS32LT3124 can support Power Supply Modulation (PSM), which implements LED dimming by pulse width modulated on the power supply rail. The IS32LT3124 closed loop stability is not affected by PSM operation with or without an external PMOS FET. The HRSET and ERC controls can respond within the t_{PC} period when the supply VCC threshold voltage to properly drive and bias the PMOS FET in a linear fashion. To get better dimming linearity, the recommended PSM frequency should be in the range of 100Hz to 300Hz (200Hz Typ.) and the input capacitor, C_{VCC}, should be low value (0.1uF typical) to ensure rapid discharge during PSM low period.

FAULT REPORTING OPERATION

For robust system reliability, the IS32LT3124 integrates the detection circuitry to protect various fault conditions and report the fault by the FLTB pin which can be monitored by an external host. The FLTB pin is internally pulled up to 4.5V by a resistor R_{FLT} and so it can be left floating, or unconnected. The FLTB pin will go low when the device enables fault detection and detects a fault condition such as LED string open, short to GND, thermal shutdown, or ISET pin open/short (refer to Table 4). For IS32LT3124B/C/E/F, the fault detection and actions are always active, however the FLTB reporting is not active until EN pin voltage rise above V_{EN_TH}. For the IS32LT3124A/D, ISET open fault detection is disabled when the voltage of the OUTx pins are not floating or grounded, unused OUTx pins should be tied to VICC for unused purpose.

In PSM dimming application, with a fault condition, the fault reporting will be reset as VCC voltage goes low. So the external fault reporting monitor should checking cycle by cycle, and keep at least 100μs monitor blanking time after VCC rising up to prevent some spurious fault as shown in Figure 71.

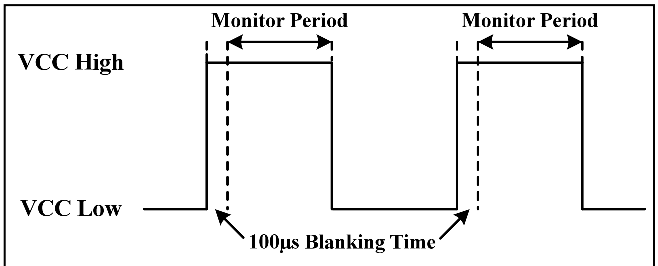


Figure 71 External Fault Reporting Monitor During PSM Dimming

FAULT REPORTING DELAY TIME SETTING

The IS32LT3124 supports programmable fault reporting delay time, as shown in Table 3. A fault reporting delay time is used to introduce a delay to the FLTB output signal when detecting a device fault condition. This delay is meant to avoid detecting and reporting a spurious fault.

Table 3 Fault Delays

FLTD Pin State	Report Fault Delay Time
GND	40μs
R_{FLTD}= 5kΩ	4.65ms
R_{FLTD}= 20kΩ	9.60ms
R_{FLTD}= 250kΩ	85.5ms
Floating	340ms

The delay time can be computed using the following Equation (22):

$$t_{FLTD}(ms) = 3.3 \times R_{FLTD} \times 10^{-4} + 3 \qquad (22)$$

Note: When FLTD pin is grounded, the fault delay time will be limited to a minimum value, 40μs. Except for being grounded, the R_{FLTD} value must be ≥ 5kΩ.

FLTB PARALLEL INTERCONNECTION

FLTB is a fault reporting output pin and it also is an input pin (IS31FL3124A/B/D/E only). Externally pulling FLTB pin low will disable all the output channels. For LED lighting systems which require the complete lighting system be shutdown when a fault is detected, the FLTB pin can be used in a parallel connection with multiple IS32LT3124A/B/D/E devices as shown in Figures 2 and 3. A detected fault output by any device will pull low the FLTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the “One-Fail-All-Fail” operating requirement.

LED STRING OPEN DETECTION

Detection of an open-load condition occurs when the measured voltage across any one of the four OUTx pins to VICC is lower than V_{OD}. When this condition is present for longer than the fault deglitch t_{FD}, then

IS32LT3124A/D:

It turns off all of the other channels. The FLTB pin goes low after fault delay time.

IS32LT3124B/E:

It turns off all of the other channels. If V_{EN}>V_{EN_TH}, the FLTB pin goes low after fault delay time.

IS32LT3124C/F:

It keeps all the other channels normal working. If V_{EN}>V_{EN_TH}, the FLTB pin goes low after fault delay time.

The device recovers after deglitch time t_{FD} as removal of the open condition and FLTB goes back high.

LED STRING SHORT-CIRCUIT DETECTION

The LED string short circuit is detected if the measured voltage across any of OUTx pin drops below OUTx pin short to GND threshold, V_{SCD}.

IS32LT3124B/C/D:

After V_{EN}>V_{EN_TH}, when any of OUTx pin voltage drops below V_{SCD} (typical 4.8V) and is present for longer than the fault deglitch time t_{FD}, IS32LT3124B/D will turn off all the other channels and reserve 4mA in faulty channel for recovery detection purpose, while all channels of IS32LT3124C will continue sourcing current. And the FLTB pin goes low after fault delay time. The channel recovers after deglitch time t_{FD} upon removal of the short condition and FLTB goes back high.

Since V_{SCD} of IS32LT3124B/C/D is higher than one LED forward voltage, it only can drive the LED string with the forward voltage > (V_{SCD_MAX}+V_{SCD_HY}) then it is possible to detect both LED string short (as Figure 72-1) and single LED in multi-LEDs string short detection with appropriate forward voltage LEDs (as Figure 72-2).

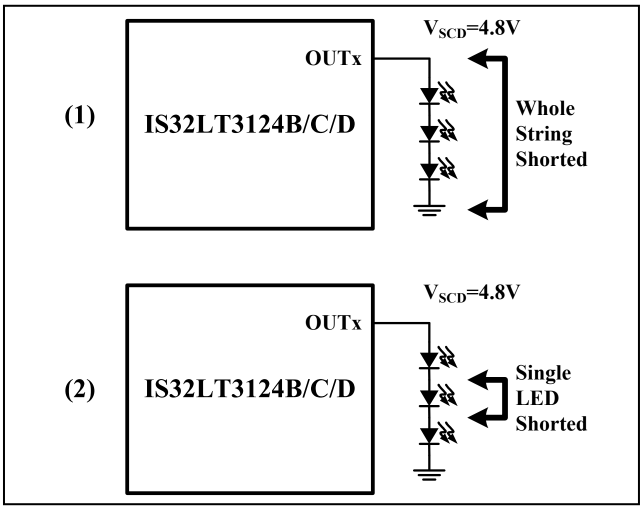


Figure 72 IS32LT3124B/C/D LED Short Detection

To achieve single LED short detection, please ensure that a single LED short can reduce the LED string voltage below V_{SCD_MIN}. So the LED string voltage must be set within the range of:

$$(V_{SCD\_MIN} + V_{f\_MIN}) > V_{STRING} > V_{SCD\_MAX} \qquad (23)$$

Where, V_{SCD_MAX} and V_{SCD_MIN} is the maximum and minimum value of the OUTx short detect threshold, V_{f_MIN} is the minimum forward voltage of the LED.

IS32LT3124A:

After the device being enabled (V_{EN}>V_{EN_TH}), when any of OUTx pin voltage drops below V_{SCD} (typical 1.22V) and is present for longer than the fault deglitch time t_{FD}, it will turn off all the other channels. The FLTB pin goes low after fault delay time. The channel recovers after deglitch time t_{FD} upon removal of the short condition and FLTB goes back high.

IS32LT3124E:

When any OUTx pin voltage drops below V_{SCD} (typical 1.22V) for longer than the fault deglitch time t_{FD}, it turns off all the other channels. If V_{EN}>V_{EN_TH}, the FLTB pin goes low after fault delay time. The device recovers after deglitch time t_{FD} upon removal of the short condition and FLTB goes back high.

IS32LT3124F:

When any OUTx pin voltage drops below V_{SCD} (typical 1.22V) for longer than the fault deglitch time t_{FD}, all channels will continue sourcing current. If V_{EN}>V_{EN_TH}, the FLTB pin goes low after fault delay time. The channel recovers after deglitch time t_{FD} upon removal of the short condition and FLTB goes back high. Note: An LED short will cause a larger headroom voltage on the faulty channel that may significantly increase the power dissipation on IS32LT3124F, especially in high output current applications.

Since V_{SCD} of IS32LT3124A/E/F is lower than one LED forward voltage, it can only detect OUTx short to GND condition, as Figure 73.

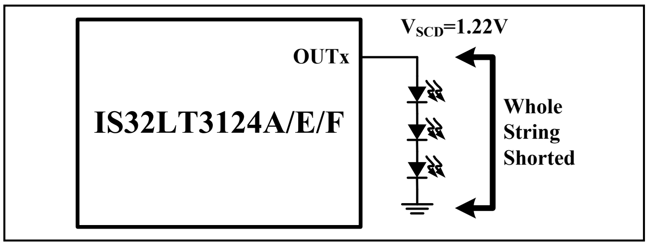


Figure 73 IS32LT3124A/E/F LED Short Detection

ISET OVER CURRENT OR SHORT DETECTION

The device is protected from an output overcurrent condition caused by ISETx pins. When a too low value resistor is connected to any ISET pin but pin voltage still is above V_{ISET_SC} (typical 0.2V), the corresponding channel current will be internally limited at 190mA (typical). If an excessive low value resistor is connected or accidental short circuit to pull ISETx pin voltage below 0.2V, the corresponding channel will be turned off with fault reporting after fault delay time t_{FLTD} and IS32LT3124A/B/D/E will turn off the other channels as well, while IS32LT3124C/F will keep the other channels operating normally. The device recovers after deglitch time t_{FD} upon removal of the fault condition and FLTB goes back high.

ISET OPEN DETECTION AND INDIVIDUAL PWM DIMMING

IS32LT3124A/D:

If ISETx pin is open and V_{EN} > V_{EN_TH}, all output channels will be turned off and FLTB will go low after fault delay time t_{FLTD} to report fault condition. The device recovers after deglitch time t_{FD} upon removal of the open condition and FLTB goes back high. Due to this protection, IS32LT3124A/D cannot support individual ISETx PWM dimming. However, if the ISET pin is floating and the corresponding OUT pin is tied to VICC, the ISET open fault will be ignored and the channel will be recognized as unused.

IS32LT3124B/C/E/F:

In these two devices, the ISETx pin open detection is removed, then ISETx pin is able to implement the individual PWM dimming to the corresponding output channel. When ISETx pin is floating, the corresponding OUTx is turned off. Ground it via a resistor (R_{ISETx}) to enable the output source. Refer to Figure 4 and 5. When the PWM generator is far away from the device, use Figure 4 approach to prevent noise coupling due to the long trace. When the PWM generator is close to the device, use open drain structure I/O of the MCU to directly control each ISETx pin. Since Push-pull I/Os will force current into ISETx pins, only open drain structure I/Os are acceptable.

With this individual PWM dimming, the LED current is inversely proportional to the source PWM duty cycle (due to the open drain inversion). That is, when the source PWM signal is 100% duty cycle, the output current is minimum, ideally zero, and when the PWM signal is 0% duty cycle, the output current is maximum. LED current is computed using the following Equation (24).

$$I_{LED} = (1 - D_{PWM}) \times \frac{V_{ISET}}{R_{ISET}} \times 2000 \qquad (24)$$

Note: because of the 40μs (typ.) fault deglitch time t_{FD}, the PWM on-time should be greater than 40us to avoid undetermined fault response.

THERMAL SHUTDOWN

In the event that the die temperature exceeds 165°C, all four output channels will go to the 'OFF' state and the FLTB pin will go low if $V_{EN} > V_{EN\_TH}$. At this point, the IC should begin to cool off. Any attempt to enable one or all four of the channels before the IC has cooled to < 140°C will be ignored by the IC.

THERMAL CONSIDERATIONS

When operating the IS32LT3124 at high ambient temperatures, or when driving high load current, care must be taken to avoid exceeding the package power dissipation limits. The major power components are IC, PMOS FET and shunt resistor. Therefore, their temperature should be carefully calculated and considered.

In the application with the DHC function, the power dissipation of these three components is described in the "DYNAMIC HEADROOM CONTROL (DHC) AND THERMAL CONSIDERATIONS" section.

In the application without the DHC function, the power dissipation on the IS32LT3124 can be computed by:

$$P_{3124} \approx V_{CC} \times I_{CC} + \sum_{x=1}^{4} (V_{CC} - V_{OUTx}) \times I_{OUTx} \qquad (25)$$

The maximum power dissipation of the IS32LT3124 and PMOS FET can be calculated using the following Equation (26):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (26)$$

Where, $T_{J(MAX)}$ is the maximum operating junction temperature which can be found from their datasheets, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. P_{3124} should not exceed $P_{D(MAX)}$.

For IS32LT3124, the recommended maximum operating junction temperature, $T_{J(MAX)}$, is 125°C and so maximum ambient temperature is determined by the junction to ambient thermal resistance, θ_{JA}.

Therefore, the maximum power rating at T_A= 25°C is:

$$P_{D(MAX)} = \frac{125°C - 25°C}{47.1°C/W} \approx 2.12W$$

Figure 74, shows the power derating of the IS32LT3124 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

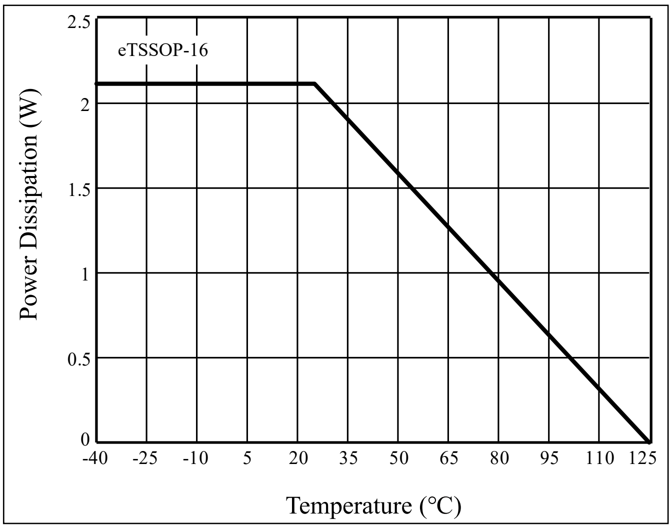


Figure 74 IS32LT3124 Dissipation Curve

The PMOS FET maximum power rating can be achieved by the same calculation method.

In the Shunt Regulator mode, R_1 will share quite a lot power dissipation. Its package power rating should be sufficient to prevent heat run away.

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3124 (eTSSOP-16 package), PMOS FET and the shunt resistor must be used. Multiple thermal vias, as shown in Figure 75, will help to conduct heat from the exposed pad of the IS32LT3124, PMOS FET and shunt resistor to the copper on each side of the board. The thermal resistance can be further reduced by using a metal substrate or by adding a heat sink. To avoid heat buildup, these power components should be spread out on the PCB board with some distance.

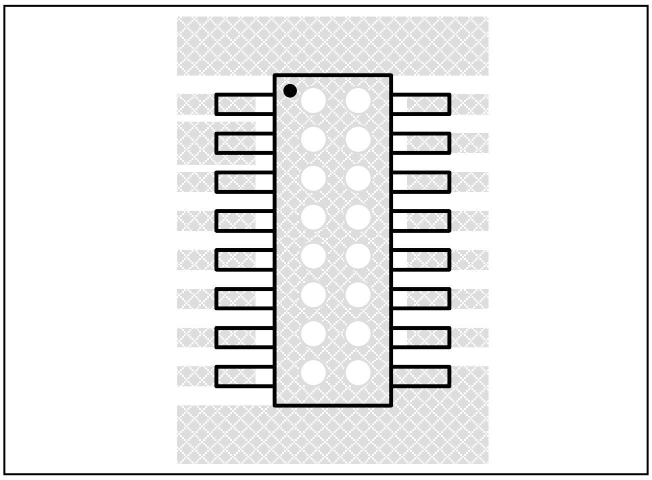


Figure 75 Board Via Layout For Thermal Dissipation

Table 4 DIFFERENT FAULT ACTION OF 3 TYPES

EN Voltage	Fault Type	Fault Condition	IS32LT3124A/D			IS32LT3124B/E			IS32LT3124C/F			Auto Recovery
			Faulty Channel	Other Channels	FLTB	Faulty Channel	Other Channels	FLTB	Faulty Channel	Other Channels	FLTB	
$<V_{EN\_TH}$	ISETx open	ISETx pin current close to zero	Device shutdown All channels are off		High	Off	Enabled	High	Off	Enabled	High	ISETx pin current goes back high
	ISETx short	ISETx pin voltage $<V_{ISET\_SC}$				Off	Off		Off	Enabled		ISETx pin voltage $>(V_{ISET\_SC}+V_{ISET\_SCHY})$
	LED string open	$(V_{ICC}-V_{OUTx})<V_{OD}$				Off	Off		Off	Enabled		$(V_{ICC}-V_{OUTx})>(V_{OD}+V_{OD\_HY})$
	OUTx short to GND	$V_{OUTx}<V_{SCD}$				Reserve 4mA for recovery detection	Off		Enabled (Note 7)	Enabled		$V_{OUTx}>(V_{SCD}+V_{SCD\_HY})$
	Thermal shutdown	$T_J>T_{SD}$				All channels are off			All channels are off			$T_J<(T_{SD}-T_{HY})$
$>V_{EN\_TH}$	ISETx open	ISETx pin current close to zero	Off	Off	Pull low after delay time t_{FLTD}.	Off	Enabled	High	Off	Enabled	High	ISETx pin current goes back high
	ISETx short	ISETx pin voltage $<V_{ISET\_SC}$	Off	Off		Off	Off	Pull low after delay time t_{FLTD}.	Off	Enabled	Pull low after delay time t_{FLTD}.	ISETx pin voltage $>(V_{ISET\_SC}+V_{ISET\_SCHY})$
	LED string open	$(V_{ICC}-V_{OUTx})<V_{OD}$	Off	Off		Off	Off		Off	Enabled		$(V_{ICC}-V_{OUTx})>(V_{OD}+V_{OD\_HY})$
	OUTx short to GND	$V_{OUTx}<V_{SCD}$	Reserve 4mA for recovery detection	Off		Reserve 4mA for recovery detection	Off		Enabled (Note 7)	Enabled		$V_{OUTx}>(V_{SCD}+V_{SCD\_HY})$
	Thermal shutdown	$T_J>T_{SD}$	All channels are off			All channels are off			All channels are off			$T_J<(T_{SD}-T_{HY})$

Note 7: The faulty channel keeps normal sourcing, but the LEDs are off due to the string is shorted.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

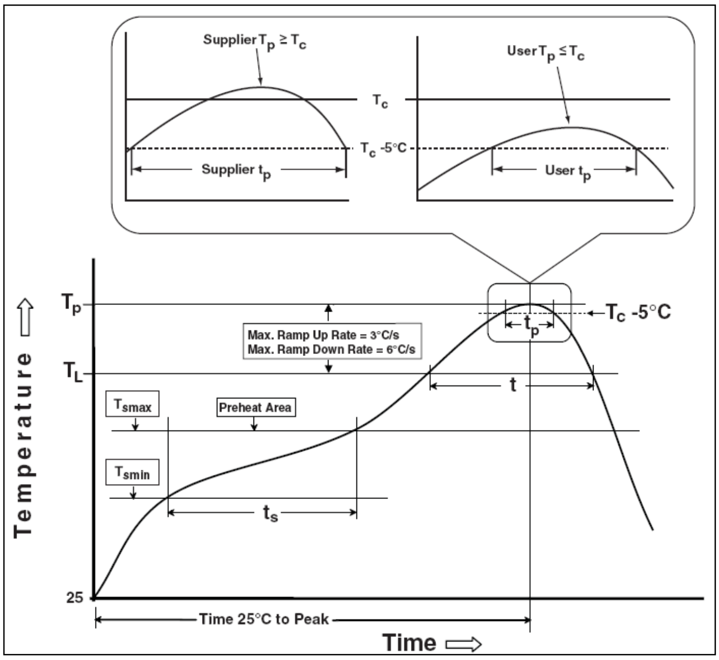
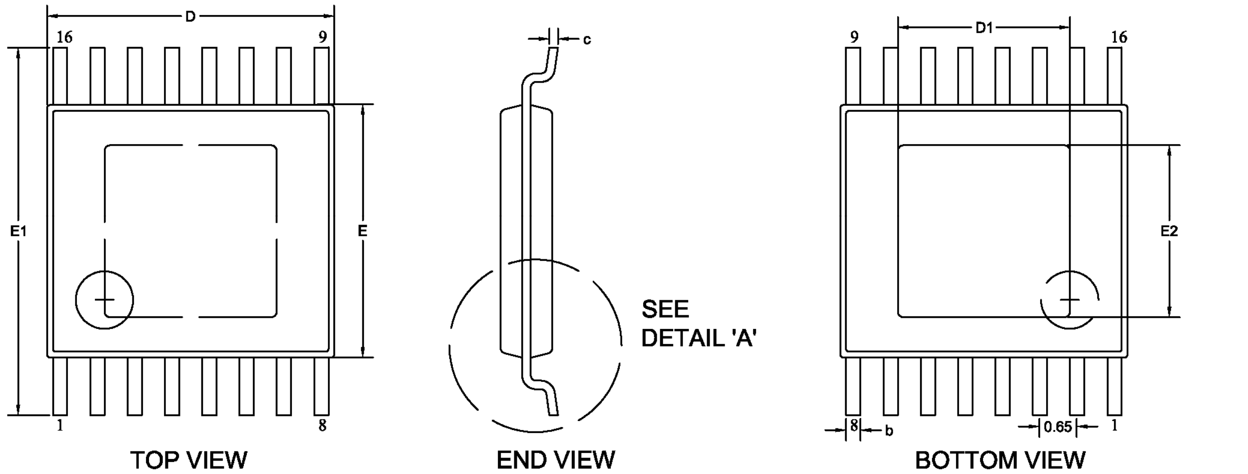
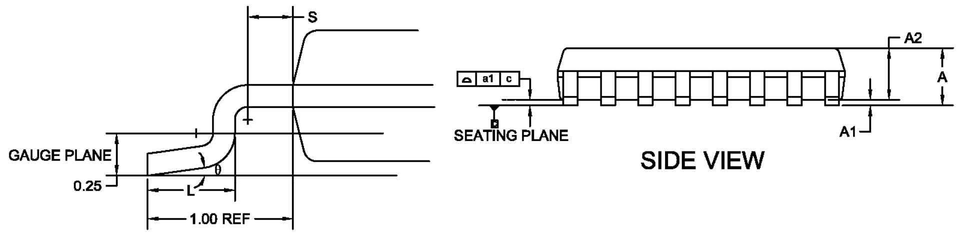


Figure 76 Classification Profile

PACKAGE INFORMATION

eTSSOP-16





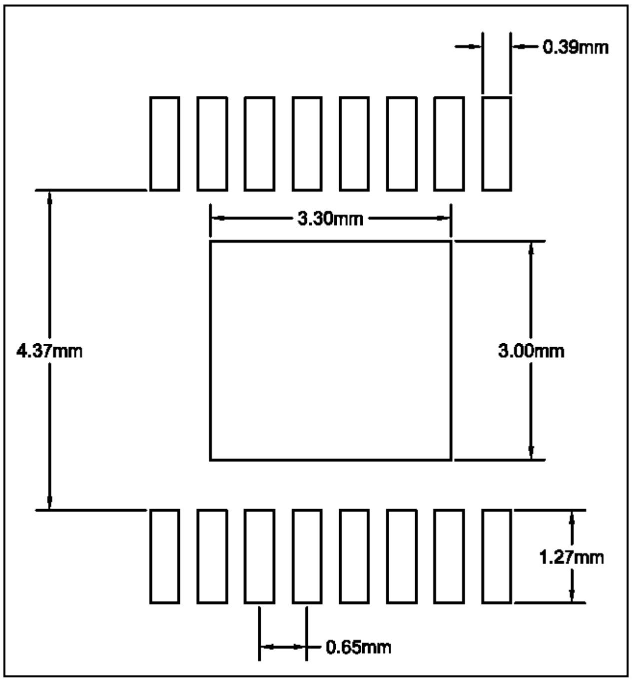
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

233-570-249 Rev. B

NOTES:
1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0C	Initial release	2018.03.01
0D	Update EC and Performance Characteristics	2018.09.20
A	Update to final version Remove tube packing	2018.12.12
B	1.Update to new Lumissil logo 2.Add RoHS, update AECQ information in Features 3.Update POD and LP	2024.04.23