24-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

GENERAL DESCRIPTION

IS31SE5120A is an ultra-low-power, 24-channel capacitive touch controller. The controller allows sleep mode (under 10uA) and uses auto-detection for wakeup. It also provides a shield output to increase moisture immunity. The built-in hardware monitor and calibration feature for the environment is to prevent false triggers.

A host MCU is required to communicate with IS31SE5120A. An on-chip I²C slave controller with 400kHz capability serves as the communication port for the host MCU. An interrupt, INT, can be configured and it is generated when a touch trigger event occurs. The trigger event can be configured by setting the interrupt register. IS31SE5120A can support proximity sensing.

IS31SE5120A is available in the QFN-32 package. It operates from 2.3V to 5.5V over the temperature range from -40°C to +105°C.

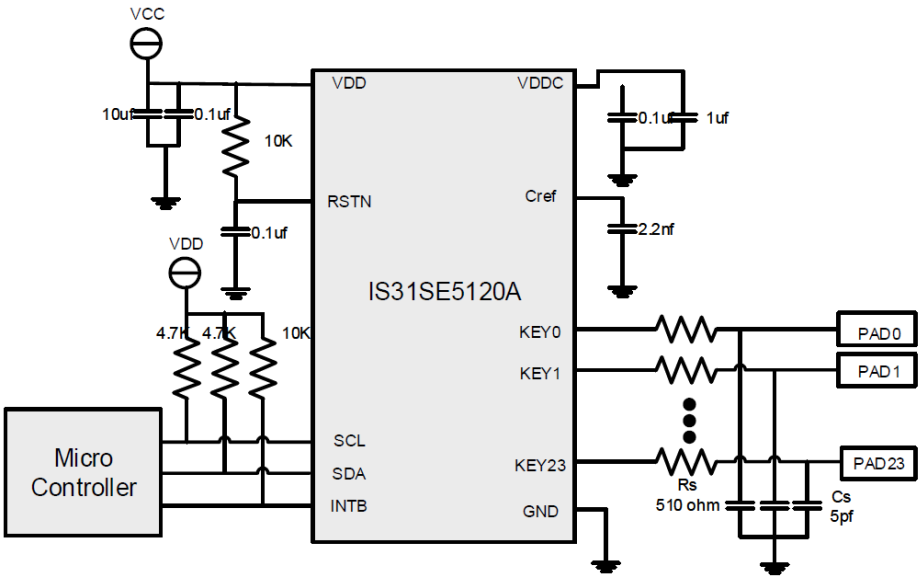
APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control

FEATURES

- 24-channel capacitive touch controller with readable key value
- Touch-related threshold settings for individual key
- Optional multiple-key function
- GPIO toggle/invert function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Shield output shared with touch key channels
- Buzzer/Melody Generator shared with touch key channels
- 400kHz fast-mode I²C interface
- Operating temperature between -40°C ~ +105°C
- QFN-32
- ROHS & Halogen-Free compliant package
- TSCA compliance

TYPICAL APPLICATION CIRCUIT (QFN-32)



Note 1: The IC should be placed far away from the noise source to prevent EMS.

Note 2: The RS and CS should be placed as close to the IC as possible to reduce EMI.

Note 3: The capacitors connected to VDD and VDDC should be as close to the IC as possible to reduce EMI.

Note 4: The capacitor 1uf connected to VDDC might need to be removed for quick VDD rising time application.

PINOUT

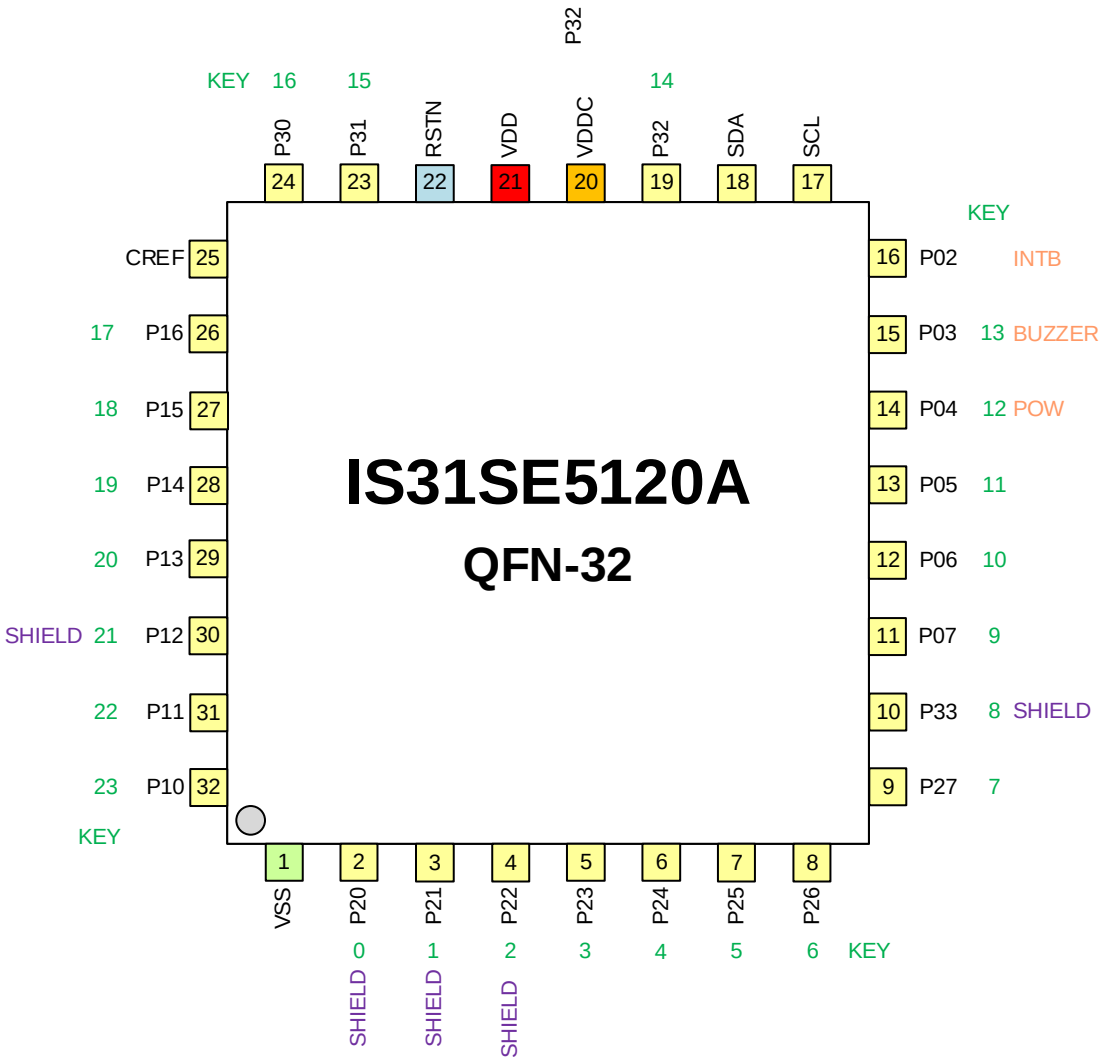

IS31SE5120A
QFN-32
KEY 16
15
P32
14
P30 24
P31 23
RSTN 22
VDD 21
VDDC 20
P32 19
SDA 18
SCL 17
CREF 25
17 P16 26
18 P15 27
19 P14 28
20 P13 29
SHIELD 21 P12 30
22 P11 31
23 P10 32
KEY
KEY
16 P02 INTB
15 P03 13 BUZZER
14 P04 12 POW
13 P05 11
12 P06 10
11 P07 9
10 P33 8 SHIELD
9 P27 7
1 VSS
2 P20 0 SHIELD
3 P21 1 SHIELD
4 P22 2 SHIELD
5 P23 3
6 P24 4
7 P25 5
8 P26 6 KEY

Table of Contents

List of Tables

List of Figures

List of Registers

1. Pin Description

No.	Pin	Description
1	VSS	Ground
2 - 4	KEY0– KEY2/SHIELD/P20 – P22	Multiple function pin. Can be configured to Input sense channels 0 – 2, or Shield output, or GPIO P20 – P22.
5 - 9	KEY3 – KEY7/P23 – P27	Multiple function pin. Can be configured to Input sense channels 3 – 7, or GPIO P23 – P27.
10	KEY8/SHIELD, P33	Multiple function pin. Can be configured to Input sense channel 8, or Shield output, or P33.
11 - 13	KEY9 – KEY11, P07 - P05	Multiple function pin. Can be configured to Input sense channels 9 – 11, or GPIO P07 – P05.
14	KEY12/POW, P04	Multiple function key. Can be configured to input sense channel 12, or Melody power control, or GPIO P04.
15	KEY13/Buzzer, P03	Multiple function key. Can be configured to input sense channel 13, or Buzzer output, or GPIO P03.
16	INTB, P02	Multiple function key. Can be configured to Interrupt output (active low), or GPIO P02.
17	SCL	I^2C serial clock
18	SDA	I^2C serial data
19	KEY14, P32	Multiple function key. Can be configured to Input sense channel 14, or GPIO P32.
20	VDDC	Internal 1.5V power supply. Typical decoupling capacitors of 0.1µF and 1µF should be added between VDDC and GND.
21	VDD	Power supply
22	RSTN	Reset signal and Low Active
23 - 24	KEY15 – KEY16, P31 - P30	Multiple function key. Can be configured to Input sense channels 15 – 16, or GPIO P31 – P30.
25	CREF	External reference Capacitor for touch sense
26 - 29	KEY17 – KEY20, P16 - P13	Multiple function key. Can be configured to Input sense channels 17 – 20, or GPIO P16 – P13.
30	KEY21/SHIELD, P12	Multiple function pin. Can be configured to Input sense channel 21, or Shield output, or GPIO P12.
31 - 32	KEY22 – KEY23, P11 - P10	Input sense channels 22 – 23, or GPIO P11 – P10.

Table 1-1 PIN Description

2. Ordering Information

Industrial Range: -40°C to +105°C

Order Part No.	Package	QTY
IS31SE5120A-QFLS3-TR	QFN-32, Lead-free	2500/Reel

3. Absolute Maximum Ratings

Supply voltage, V_{DD}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{DD}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range TA	-40°C ~ +105°C
Junction Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}(QFN-32)	37.6°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Table 3-1 Absolute maximum ratings

Note 5: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Electrical Characteristics

TA = 25°C, VDD= 2.3V ~ 5.5V, unless otherwise noted. Typical values are TA = 25°C, VDD= 3.6V.

Symbol	Parameter	Min	Typ	Max	Unit	Note
Power Supply Current						
IDD Normal	Total IDD through VDD at 16MHz Peripherals off	-	3.5	-	mA	
IDD Normal	Total IDD through VDD at 1MHz Peripherals off	-	1.0	-	mA	
IDD versus Frequency	IDD Core Current versus Frequency	-	150	-	uA/ MHz	
IDD, Stop	IDD, stop mode	-	500	-	µA	Main regulator on
IDD, Sleep	IDD, sleep mode, 25°C	-	1.5	5	µA	Main regulator off
	IDD, sleep mode, 85°C	-	4	10	µA	Main regulator off
GPIO DC Characteristics						
VOH,4.5V	Output High Voltage 1 mA	-	-0.2	-0.5	V	Reference to VDD
VOL,4.5V	Output Low Voltage 8 mA	-	0.3	0.5	V	Reference to VSS
VOH,3.0V	Output High Voltage 1 mA	-	-0.3	-0.6	V	Reference to VDD
VOL,3.0V	Output Low Voltage 8 mA	-	0.3	0.6	V	Reference to VSS
IIOT	Total IO Sink and Source Current	-80	-	80	mA	
VIH	Input High Voltage	¾VDD	-	-	V	
VIL	Input Low Voltage	-	-	¼VDD	V	
VIHYS	Input Hysteresis	-	1	-	-	
RPU	Equivalent Pull-Up resistance	-	25K	-	Ohm	
RPU,RSTN	RSTN Pull-Up resistance	-	5K	-	Ohm	
RPD	Equivalent Pull-Down Resistance	-	25K	-	Ohm	
REQAN1	Equivalent ANIO Switch Resistance @3.3V	-	110	-	Ohm	ANIO1 Switch
	Equivalent ANIO Switch Resistance @5V	-	100	-	Ohm	ANIO1 Switch
REQAN2	Equivalent ANIO Switch Resistance @3.3V	-	450	-	Ohm	ANIO2 Switch

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Equivalent ANIO Switch Resistance @5V	-	350	-	Ohm	ANIO2 Switch

3.2 Digital Input Switching Characteristics (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			µs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			µs
$t_{SU, STA}$	Repeated START condition setup time		0.6			µs
$t_{SU, STO}$	STOP condition setup time		0.6			µs
$t_{HD, DAT}$	Data hold time				0.9	µs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			µs
t_{HIGH}	SCL clock high period		0.7			µs
t_R	Rise time of both SDA and SCL signals.	(Note 7)		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals.	(Note 7)		$20+0.1C_b$	300	ns

Note 6: Guaranteed by design.

Note 7: Cb = total capacitance of one bus line in pF. ISINK ≤ 6mA. tR and tF measured between 0.3 × VDD and 0.7 × VDD.

4. Function Block Diagram

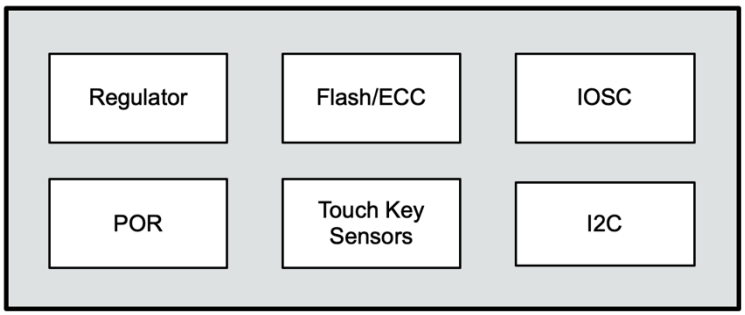


Figure 4-1 Function Block Diagram

4.1 Basic introduction for touch sense data process flow

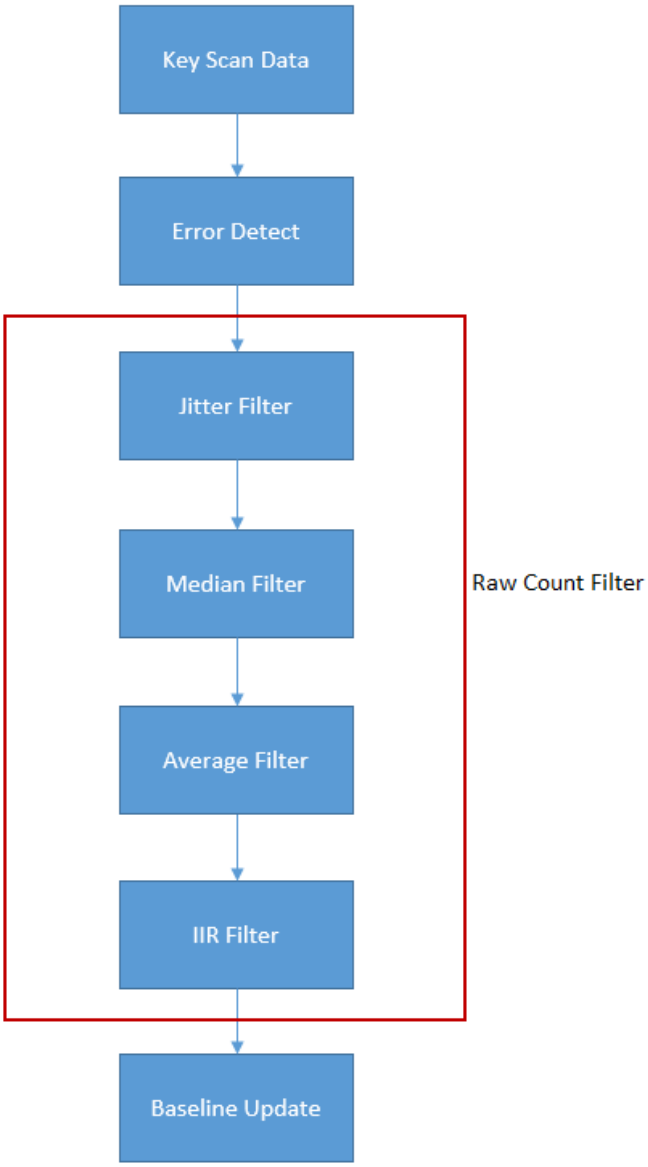


Figure 4-2 Touch Sense Data Process Flow

4.2 Baseline process based on difference of baseline and raw count

Baseline will be updated to the current raw count based on the below factors. For detailed information about baseline, please refer to Section 4.4.2 Key parameter in “IS31SE5120A Eval Board User's Manual” application note.

4.2.1 Positive noise threshold

Baseline is updated if the difference count of baseline count and raw count is below the positive noise threshold.

4.2.2 Negative noise threshold

It is used with the low baseline reset count to reset baseline count to the current raw count. Please refer to the description of Low baseline reset.

4.2.3 Low baseline reset

Low baseline reset count of each key. A reset count increases one if the absolute |raw count – baseline| > negative noise threshold. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute | raw count – baseline| <= negative noise threshold.

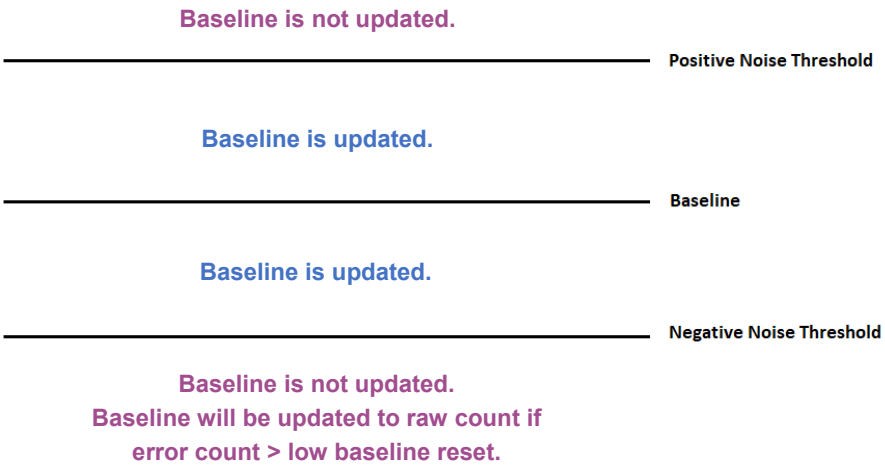


Figure 4-3 Baseline Process based on the difference between baseline and raw count

4.2.4 Touch sense data identification

Ignore touch key scan if the signal exceeds the lock threshold.

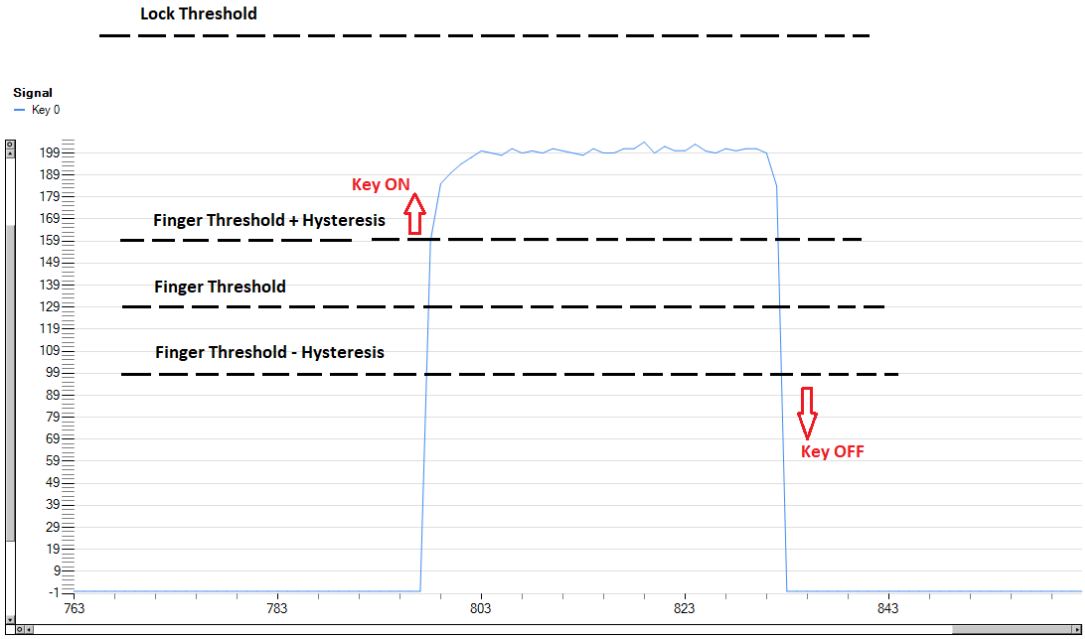


Figure 4-4 Touch Sense Data Identification

5. Detailed Description

5.1 I²C Interface

S31SE5120A uses a serial bus, which conforms to the I²C protocol, to control the chip's functions with two wires: SCL and SDA. IS31SE5120A has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 "0" for a write command and set A0 "1" for a read command.

The complete slave address is:

Bit	A7:A1	A0
Value	0111100	1/0

The SCL line is uni directional. The SDA line is bi-directional (open collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I²C standard is 400kHz. During communication, the microcontroller is the master and IS31SE5120A is the slave.

The timing diagram for the I²C is shown in Figure 5-1. The SDA is latched on to the stable high level of the SCL. When there is no bus activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, and the most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the device address is sent, the master checks for "acknowledge" from IS31SE5120A. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If IS31SE5120A has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5120A, the register address byte is sent, and the most significant bit first. IS31SE5120A must generate another acknowledgment indicating that the registered address has been received.

Then 8-bit of data bytes are sent next, the most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, IS31SE5120A must generate another acknowledgment to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

5.2 Read Port Registers

To read the device data, the bus master must first send the address of IS31SE5120A with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must send IS31SE5120A address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is sent from IS31SE5120A to the master (Figure 5-4).

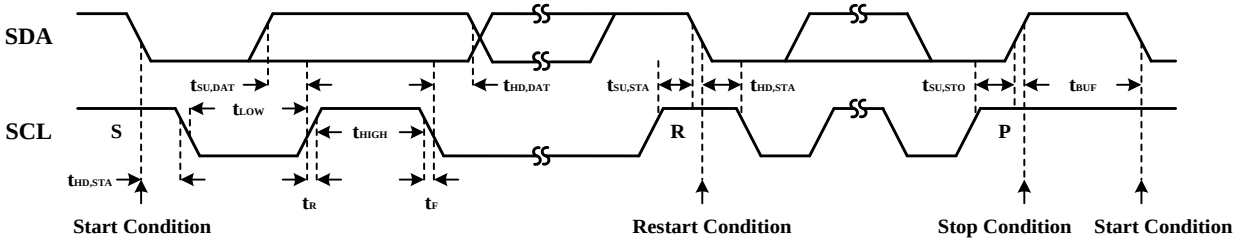


Figure 5-1 Interface Timing

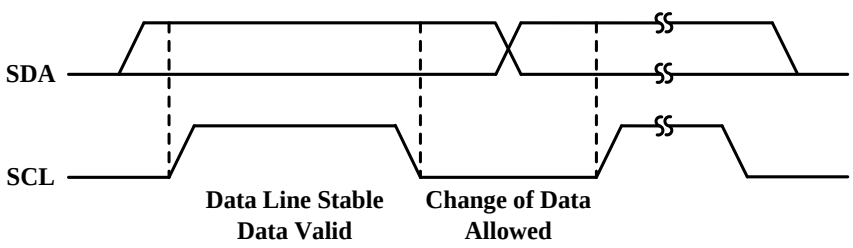


Figure 5-2 Bit Transfer

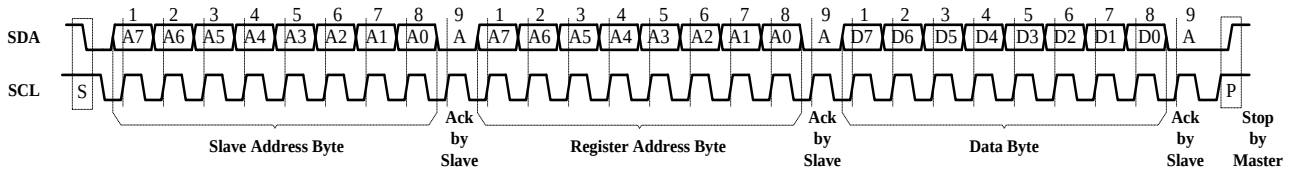


Figure 5-3 Writing to IS31SE5120A

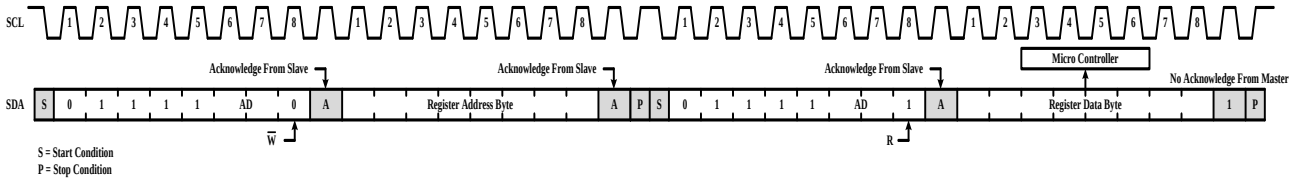


Figure 5-4 Reading from IS31SE5120A

Note: Successive read or write protocol is supported.

6. Register Definition

6.1 Page 0 Register list

Address	Name	Definition	R/W	Default
00h	Chip Part Number	Chip's part number	R	20h
01h-02h	Chip Version	Chip's version	R	-
03h	Firmware Version	Firmware version	R	40h
04h	Run Version	Run version	R/W	40h
05h	Main Control	Management of system reset, power-saving, and parameters	W	00h
06h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
07h-09h	Key Status	Key 0-Key 23 status bits	R	00h
0Ah	BM	Buzzer data or stop command	W	-
0Ah	BM	Available buzzer buffer size	R	0Ah
0Bh-22h	Key Signal	Key 0-Key 23 signal value	R	00h
23h-52h	Key Raw Count	Key 0-Key 23 raw count value	R	0000h
53h-82h	Key Baseline	Key 0-Key 23 baseline value	R	0000h
83h-9Ah	Key Finger Threshold	Key 0-Key 23 finger threshold setting	R/W	50h or 28h
9Bh-B2h	Key Noise Threshold	Key 0-Key 23 noise threshold setting	R/W	28h or 14h
B3h-CAh	Key Negative Noise Threshold	Key 0-Key 23 negative noise threshold setting	R/W	28h or 14h
CBh-D0h	Slider 1-2 status	3 slider status registers for each slider	R/W	Addr CDh value :80h, others value 00h
D1h	Self-Test Item	Safety function self-test item	R/W	00h
D2h-D3h	Self-Test Ram Start Addr	Safety function self-test ram start address	R/W	00h
D4h-D5h	Self-Test Ram Size	Safety function ram size	R/W	00h
D6h	Self-Test Result	Safety function self-test test result	R	00h
D7h-FFh	-	Reserved	-	-

Table 6-1 Page 0 Register list

6.2 Page 1 Register list (extension memory)

Address	Name	Definition	R/W	Default
100h	Chip Part Number	Chip's part number	R	20h
101h-102h	Chip Version	Chip's version	R	-
103h	Firmware Version	Firmware version	R	40h
104h	Run Version	Run version	R/W	40h
105h	Main Control	System reset, power-saving, and parameters management	W	00h
106h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
107h-109h	Key Status	Key 0-Key 23 status bits	R	00h
10Ah	BM	Buzzer data or stop command	W	-
10Ah	BM	Available buzzer buffer size	R	0Ah
10Bh-122h	Key Low Baseline Reset	Key 0-Key 23 low baseline reset setting	R/W	1Eh

Address	Name	Definition	R/W	Default
123h-13Ah	Key Hysteresis	Key 0-Key 23 hysteresis setting	R/W	08h or 04h
13Bh-152h	Key ON Debounce	Key 0-Key 23 debounce setting	R/W	03h
153h-155h	Key Interrupt Enable	Key 0-Key 23 enables Interrupts associated with capacitive touch sensor inputs	R/W	00h
156h	Raw Count Filter	Raw count filter setting	R/W	00h
157h	Baseline IIR Ratio	Baseline IIR ratio setting	R/W	01h
158h-159h	Lock Threshold	Lock threshold setting	R/W	03E8h
15Ah	Lock Scan Cycle	Lock scan cycle setting	R/W	08h
15Bh	Raw Count Difference Limit	Raw count difference limit setting	R/W	64h
15Ch	Multiple Touch Key Configure	Multiple touch key function setting	R/W	03h
15Dh	Max Duration Time	Maximum duration time setting	R/W	1Ah
15Eh	Interrupt Configuration	Interrupt configuration	R/W	0Ah
15Fh	Interrupt Repeat Time	Repeat cycle for pressing key interrupt setting	R/W	00h
160h-162h	Key Pin Select	Select pins as Key0-Key23	R/W	000000h
163h-165h	Shield Pin Select	Select pin as a shield pin	R/W	000001h
166h-168h	INT Pin Select	Select pin as INT	R/W	000000h
169h-16Bh	Buzzer Pin Select	Select pin as a buzzer pin	R/W	002000h
16Ch-16Eh	POW Pin Select	Select pin as buzzer power	R/W	000000h
16Fh-171h	GPIO Pin Select	Sets the GPIO enable KEY0~KEY23	R/W	01C000h
172h-174h	Slider 1 Pin Select	Max 8 keys	R/W	0000FCh
175h-177h	Slider 2 Pin Select	Max 8 keys	R/W	000000h
178h	TKIII Control register 1	Repeat sequence, initial setting delay, auto mode start delay, and low-frequency noise filter	R/W	13h
179h	TKIII Control register 2	Pseudo-random sequence setting	R/W	20h
17Ah	TKIII Control register 3	Multiple frequency scan/cycle count setting	R/W	03h
17Bh	TKIII CCHG	Internal charge capacitance setting	R/W	60h
17Ch	TKIII PUD	Pull-up current/ pull-up resistors setting	R/W	00h
17Dh	System Clock Select	System clock setting	R/W	00h
17Eh	Spread Spectrum	Spread spectrum setting	R/W	0Ch
17Fh	Auto Sleep Mode	Auto enter sleep mode time setting	R/W	0Fh
180h	Sleep Mode Control	Sleep mode control setting	R/W	00h
181h-183h	Wake Up Key Select	Select Key0~Key23 to exit sleep mode	R/W	000000h
184h	Wake Up Threshold	Wake up threshold setting	R/W	08h
185h	TKIII Sleep Mode CCHG	Sleep mode internal charge capacitance setting	R/W	60h

Address	Name	Definition	R/W	Default
186h	TKIII Sleep Mode PUD	Sleep mode pull-up current/ pull-up resistors setting	R/W	00h
187h-188h	SLP_RAW	Sleep mode raw count value	R	0000h
189h-18Ah	SLP_Baseline	Sleep mode baseline value	R	0000h
18Bh	I^2C Configuration	I^2C setting	R/W	00h
18Ch-190h	Reserved	Reserved	-	-
191h	Slider 1 Mapping	Slider 1 Key position	R/W	07h
192h	Slider 1 Mapping	Slider 1 Key position	R/W	06h
193h	Slider 1 Mapping	Slider 1 Key position	R/W	05h
194h	Slider 1 Mapping	Slider 1 Key position	R/W	04h
195h	Slider 1 Mapping	Slider 1 Key position	R/W	03h
196h	Slider 1 Mapping	Slider 1 Key position	R/W	02h
197h	Slider 1 Mapping	Slider 1 Key position	R/W	00h
198h	Slider 1 Mapping	Slider 1 Key position	R/W	00h
199h-1A0h	Slider 2 Mapping	Slider 2 Key position	R/W	00h
1A1h-1B0h	Reserved	Reserved	-	-
1B1h-1B3h	GPIO Value	Sensing the GPIO values for KEY0 – KEY23	R/W	01C000h
1B4h-1B6h	GPIO Enable	Enable KEY0 – KEY23 for GPIO	R/W	00001Ch
1B7h	GPIO Mapping 1	Key to GPIO mapping; see register for details	R/W	00h
1B8h	GPIO Mapping 2	Key to GPIO mapping; see register for details	R/W	00h
1B9h	GPIO Mapping 3	Key to GPIO mapping; see register for details	R/W	10h
1BAh	GPIO Mapping 4	Key to GPIO mapping; see register for details	R/W	0Fh
1BBh	GPIO Mapping 5	Key to GPIO mapping; see register for details	R/W	0Eh
1BCh-1CEh	GPIO Mapping 6-24	Key to GPIO mapping; see register for details	R/W	00h
1CFh-1D1h	GPIO Toggle EN	Enable GPIO Toggle mode for KEY0 – KEY23	R/W	100000h
1D2h	Key Scan Once	I^2C control key scan	R/W	00h
1D3h	Table Ready Mark	Mark for flash data ready	R	00h

Table 6-2 Page 1 Register list (extension memory)

6.3 Page 0 registers

00h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0010 0000

CPN Chip Part Number
Chip's part number 20h

01h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version information 1

02h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version information 2
CV1 & CV2 bytes contain chip revision. CV1 indicates the mask set version. CV2 indicates the minor version.

03h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	001	000	00

FV Firmware Version
Default version is 1.0.0
FV1[2:0] Major version
FV2[2:0] Minor version
FV3[1:0] Patch version

04h Run Version Register (RW)

Bit	D7:D0		
Name	RV1[2:0]	RV2[2:0]	RV3[1:0]
Default	-	-	-

RV Run Version
Set run firmware version
RV1[2:0] Major version
RV2[2:0] Minor version
RV3[1:0] Patch version

05h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset
1 System reset
RD Reset All Parameters to Manufacturer's Default Setting.
1 Reset all user-defined parameters to the manufacturer's default setting.
SP Sleep Mode
1 Sleep mode
SS Save User Defined Parameters
1 Save current parameters into flash.
DW Deep Sleep Wake Up Reset Baseline
Reset touch key baseline after waking up from deep sleep mode.
DS Deep Sleep Mode
1 Keep sleep until waking up by I^2C SDA falling edge.

Deep sleep mode will stop key scanning function and save more power consumption compared with the generic sleep mode.

06h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)
FLAG=1 Page 1 (Address: 0x100~0x1FF)

07h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key0~Key7 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.
0 Not detected.
1 Key is detected.

08h Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

KSx Key8~Key15 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.
0 Not detected.
1 Key is detected.

09h Key Status Register 3 (RO)

Bit	D7:D0
Name	KS[23:16]
Default	0000 0000

KSx Key16~Key23 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.
0 Not detected.
1 Key is detected.

0Ah Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

BM Buzzer Register Write
Buzzer data or stop command

0Ah Buzzer Register (R)

Bit	D7:D0
Name	BM[7:0]
Default	0000 1010

BM Buzzer Register Read
It shows the available tone buffer size. IS31SE5120A has 10 built-in note buffers.

0Bh~22h KEY0~KEY23 Signal Register (RO)

Bit	D7:D0
Name	KEYx_SIGNAL[7:0]
Default	0000 0000

KEYx_SIGNAL Key Signal Count

The difference between baseline and raw count.
The maximum value is 254. It will keep 254 if the value is over 254. Value 255 means noise existence.

23h, 25h…, 4Fh, 51h KEY0~KEY23 Raw Count High Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[15:8]
Default	0000 0000

24h, 26h…, 50h, 52h KEY0~KEY23 Raw Count Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[7:0]
Default	0000 0000

KEYx_RAWCOUNT Raw count of each key, provides an indication of the magnitude of the sensor's capacitance.

53h, 55h …, 7Fh, 81h KEY0~KEY23 Baseline High Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[15:8]
Default	0000 0000

54h, 56h …, 80h, 82h KEY0~KEY23 Baseline Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[7:0]
Default	0000 0000

KEYx_Baseline Baseline of each key

83h~9Ah KEY0~KEY23 Finger Threshold Register (RW)

Bit	D7:D0
Name	KEYx_TH[7:0]
Default Key0–Key16	0010 1000
Default Key17–Key23	0101 0000

KEYx_TH Finger threshold of each key. It is used with hysteresis to determine the key state.

9Bh~B2h KEY0~KEY23 Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NTH[7:0]
Default Key0–Key16	0001 0100
Default Key17–Key23	0010 1000

KEYx_NTH Noise threshold of each key
Baseline needs to be updated if the difference (baseline and raw count) is less than the noise threshold.

B3h~CAh KEY0~KEY23 Negative Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NNTH[7:0]
Default Key0–Key16	0001 0100
Default Key17–Key23	0010 1000

KEYx_NNTH Negative noise threshold of each key.

CBh Slider1 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

ACT Slider is active
0 Disable slider
1 Enable slider

INIP Initial position

CCh Slider1 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

DIR Direction of Slide1
0 Rotate to left
1 Rotate to right

ENDP End position of the slider

CDh Slider1 Status Register 3 (RW)

Bit	D7	D6:D0
Name	STA	DUR
Default	1	0000000

STA Status of Slider1
0 Wheel
1 Slider
STA is the only bit for write.

DUR Duration
The duration between the initial position to the end position. Every DUR bit increase presents 0.1s.

CEh Slider2 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

ACT Slider2 is active
0 Disable slider
1 Enable slider

INIP Initial position

CFh Slider2 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

DIR Direction of Slide2
0 Rotate to left
1 Rotate to right

ENDP End position of the slider

D0h Slider2 Status Register 3 (RW)

Bit	D7	D6:D0
Name	STA	DUR
Default	0	0000000

STA Status of Slider2

0 Wheel
1 Slider

DUR Duration
The duration between initial position to end position. Every DUR bit increase presents 0.1s.

D1h Self-Test Item Register (RW)

Bit	D7:D0
Name	STI [7:0]
Default	0000 0000

STI Self-Test Item
WRITE
1 CPU
2 PC
3 Stack
4 Flash
5 SRAM
6 Clock
7 INT
8 Touch Key
READ
00 Self-Test is completed
Not 00 Self-Test is busy

D2h Self-Test Ram Start Address Register 1 (RW)

Bit	D7:D0
Name	STADR[15:8]
Default	0000 0000

D3h Self-Test Ram Start Address Register 2 (RW)

Bit	D7:D0
Name	STADR [7:0]
Default	0000 0000

STADR Self-Test Ram Start Address

D4h Self-Test Ram Size Register 1 (RW)

Bit	D7:D0
Name	STRAMSIZE[15:8]
Default	0000 0000

D5h Self-Test Ram Size Register 2 (RW)

Bit	D7:D0
Name	STRAMSIZE[7:0]
Default	0000 0000

STRAMSIZE Self-Test Ram Size

D6h Self-Test Result Register (RO)

Bit	D7:D0
Name	STR[7:0]
Default	0000 0000

STR Self-Test Result
5Ah Test Result OK
Not 5Ah Error

D7h – FFh Reserved

Bit	D7:D0
Name	-
Default	-

Reserved

6.4 Page 1 Registers (For Expand Memory)

100h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0010 0000

CPN — Chip Part Number
Chip's part number 20h

101h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 — Chip Version information 1

102h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 — Chip Version information 2
CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

103h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	010	000	00

FV — Firmware Version
Default version is 2.0.0
FV1[2:0] — Major version
FV2[2:0] — Minor version
FV3[1:0] — Patch version

104h Run Version Register (RW)

Bit	D7:D0		
Name	RV1[2:0]	RV2[2:0]	RV3[1:0]
Default	-	-	-

RV — Run Version
Set run firmware version
RV1[2:0] — Major version
RV2[2:0] — Minor version
RV3[1:0] — Patch version

105h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset
1 System reset
RD Reset All Parameters to Manufacturer's Default Setting.
1 Reset all user-defined parameters to the manufacturer's default setting.
SP Sleep Mode
1 Sleep mode
SS Save User Defined Parameters
1 Save current parameters into flash.
DW Deep Sleep Wake Up Reset Baseline
1 Reset touch key baseline after waking up from deep sleep mode.
DS Deep Sleep Mode
Keep sleep until waking up by I^2C SDA falling edge.

Deep sleep mode will stop key scanning function and save more power consumption compared with the generic sleep mode.

106h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)
FLAG=1 Page 1 (Address: 0x100~0x1FF)

107h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key0~Key7 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".
0 Not detected.
1 Key is detected.

108h Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

KSx Key8~Key15 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".
0 Not detected.
1 Key is detected.

109h Key Status Register 3 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key16~Key23 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".
0 Not detected.
1 Key is detected.

10Ah Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

BM Buzzer Register Write

Buzzer data or stop command

10Ah Buzzer Register (R)

	D7:D0
Name	BM[7:0]
Default	0000 1010

BM — Buzzer Register Read
It shows the available tone buffer size. IS31SE5120A has 10 built-in note buffers.

10Bh~122h KEY0~KEY23 Low Baseline Reset Register (RW)

Bit	D7:D0
Name	RCx[7:0]
Default	0001 1110

RCx — Reset Count

Low baseline reset count of each key. A reset count increases one if the absolute |raw count – baseline| > absolute |negative noise threshold|. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute |raw count – baseline| <= absolute |negative noise threshold|.

123h~13Ah KEY0~KEY23 Hysteresis Register (RW)

Bit	D7:D0
Name	HYSTERESISx[7:0]
Default Key0–Key16	0000 0100
Default Key17–Key23	0000 1000

HYSTERESISx — Hysteresis of each key

13Bh~152h KEY0~KEY23 On Debounce Register (RW)

Bit	D7:D0
Name	DEBOUNCEx[7:0]
Default	0000 0011

DEBOUNCEx — Debounce number of each key. When the acquired number > debounce setting value, then the key is granted as ON state.

153h~155h Key Interrupt Enable Register (RW)

Bit	D7:D0
Name	INTEN[7:0]
Default	0000 0000

The Interrupt Enable Register determines whether a key causes the interrupt pin to be asserted when it is detected touched with the key's interrupt enable bit set.

INTEN — Key Interrupt Enable
0 Disable
1 Enable

The default value for Interrupt Enable Registers is interrupt disable. Setting INE bit of Interrupt Configuration Register (12Dh) to "1", INTB pin will generate an interrupt signal.

156h Raw Count Filter Register (RW)

Bit	D7	D6	D5:D4	D3	D2:D1	D0
Name	MF	AF	IIR[1:0]	JF	JD[1:0]	-
Default	0	0	00	0	00	0

MF — Median Filter
0 Disable
1 Enable

AF Average Filter
0 Disable
1 Enable

IIR IIR Filter
00 Disable
01 1/2
10 1/4
11 1/8

JF Jitter Filter
0 Disable
1 Enable

JD Jitter Delta
00 1
01 2
10 4
11 8

157h Baseline IIR Ratio Register (RW)

Bit	D7:D0
Name	RATIO[7:0]
Default	0000 0001

RATIO Range 1 ~ 255

158h Lock Threshold High Byte Register (RW)

Bit	D7:D0
Name	LT[15:8]
Default	0000 0011

159h Lock Threshold Low Byte Register (RW)

Bit	D7:D0
Name	LT[7:0]
Default	1110 1000

LT Lock Threshold

15Ah Lock Scan Cycle Register (RW)

Bit	D7:D0
Name	LSC[7:0]
Default	0000 1000

LSC Lock Scan Cycle
Ignore the key scan data for the setting Lock scan cycle if the |raw count – baseline| > Lock threshold.

15Bh Raw Count Difference Limit Register (RW)

Bit	D7:D0
Name	RCDL[7:0]
Default	0110 0100

RCDL Raw Count Difference Limit
Ignore the key scan data if the difference between the previous raw count and the current raw count exceeds the limit.

15Ch Multiple Touch Key Configure Register (RW)

Bit	D7:D2	D1:D0
Name	-	MTK[1:0]
Default	000000	11

MTK Multiple Touch Key
- 00 Allow all keys to be triggered at one time.
- 01 Allow one key to be triggered at one time.
- 10 Allow two keys to be triggered at one time.
- 11 Allow three keys to be triggered at one time.

15Dh Max Duration Time Register (RW)

Bit	D7	D6	D5	D4	D3:D0
Name	-	-	-	MDEN	MDT[3:0]-
Default	0	0	0	1	1010

MDEN Maximum Duration Time Enable
- 0 Disable
- 1 Enable

MDT Maximum Duration Time
- 0000 0.5s
- 0001 1s
- 0010 2s
- 0011 3s
- 0100 4s
- 0101 5s
- 0110 6s
- 0111 7s
- 1000 8s
- 1001 9s
- 1010 10s
- 1011 11s
- 1100 12s
- 1101 13s
- 1110 14s
- 1111 15s

MDT bits set the pressed time. When the key pressed duration exceeds the programmed time (MDT), the device will be forced to calibrate the pressed key. Set MDEN to “1” will enable this function.

15Eh Interrupt Configuration Register (RW)

Bit	D7	D6:D4	D3	D2:D0
Name	INE	-	ACEN	ACT[2:0]
Default	0	000	1	010

INE Interrupt Function Enable
- 0 Disable
- 1 Enable

ACEN Auto-Clear Interrupt Enable
- 0 Disable
- 1 Enable

ACT Auto-Clear Interrupt Time
- 000 10ms
- 001 20ms
- 010 30ms
- 011 40ms
- 100 50ms
- 101 100ms
- 110 150ms
- 111 200ms

When ACEN=0, the INT will keep low until the device’s 07h, 08h, and 09h registers are read, or the key is released. When ACEN=1, the INT will be released after the ACT setting time is expired even 07h, 08h, and 09h registers are not read, or the key is still pressed.

15Fh Interrupt Repeat Time Register (RW)

Bit	D7:D4	D3:D0
Name	-	INTRT[3:0]
Default	0000	0000

INTRT Interrupt Repeat Time

0000 disable
0001 50ms
0010 100ms
0011 150ms
0100 200ms
0101 250ms
0110 300ms
0111 350ms
1000 400ms
1001 450ms
1010 500ms
1011 600ms
1100 700ms
1101 800ms
1110 900ms
1111 1s

After INTRT is set, a second interrupt will be generated after the interrupt repeat time is expired If there is a key keeping pressed.

160h~162h Key Pin Select Register (RW)

Bit	D7:D0		
Name	KS[23:16]	KS[15:8]	KS[7:0]
Default	0000 0000	0000 0000	0000 0000

KS Key Pin Selection Setting

0 Disable
1 Enable

163h~165h Shield Pin Select Register (RW)

Bit	D7:D0		
Name	SHDE[23:16]	SHDE[15:8]	SHDE[7:0]
Default	- - 0 - - - - -	- - - - - - - 0	- - - - - - 001

SHDE Shield Enable (default for SHDE[0])

0 Disable shield driver
1 Enable shield driver

Only SHDE[0], SHDE[1], SHDE[2], SHDE[8], and SHDE[21], can be set as Shield Pins.

166h~168h INT Pin Select Register (RW)

Bit	D7:D0		
Name	IPS1[23:16]	IPS1[15:8]	IPS1[7:0]
Default	0000 0000	0000 0000	0000 0000

IS31SE5120A interrupt Pin has been fixed at Pin 16 INTB and it doesn't work to set INT Pin Select Register 135h, 136h, and 137h.

169h~16Bh Buzzer Pin Select Register 1 (RW)

Bit	D7:D0		
Name	BPS3[7:0]	BPS2[7:0]	BPS1[7:0]
Default	- - - - - - - -	- - 1 - - - - -	- - - - - - - -

BPS1/2 Buzzer output Select 1/2

Enable BPS2[5] will set Pin15 as the Buzzer output pin.
BPS1[7:9] & BPS3[7:0] unused register bits.

16Ch Enable Buzzer Power Register 1 (RW)

Bit	D7:D0
Name	EBP1 [7:0]
Default	- - - - - - - -

16Dh Enable Buzzer Power Register 2 (RW)

Bit	D7:D0
Name	EBP2 [0]
Default	- - - 1 - - - -

EBP1/2 Buzzer Power Select 1/2
EBP1[7:0] unused register bits.
EBP2[4] maps to KEY12. Writing 1 to EBP2[4] will enable KEY12 as the Buzzer Power. Setting other EBP2 bits doesn't work.

16Eh Enable Buzzer Power Register 3 (RW)

Bit	D7:D0
Name	EBP3 [7:0]
Default	- - - - - - - -

16Fh~171h GPIO Pin Select Register (RW)

Bit	D7:D0		
Name	GPIO[23:16]	GPIO[15:8]	GPIO[7:0]
Default	0000 0001	1100 0000	0000 0000

GPIO pin select will go with register 1B1h GPIO Value 1, register 1B2h GPIO Value 2, and register 1B3h GPIO Value 3 to have GPIO pin high or low.

172h~174h Slider1 Pin Select Register (RW)

Bit	D7:D0		
Name	GPIO[23:16]	GPIO[15:8]	GPIO[7:0]
Default	0000 0000	0000 0000	1111 1100

175h~177h Slider2 Pin Select Register (RW)

Bit	D7:D0		
Name	GPIO[23:16]	GPIO[15:8]	GPIO[7:0]
Default	0000 0000	0000 0000	0000 0000

178h TKIII Control Register 1 (RW)

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT	INI	ASTDLY	LFNF
Default	00	01	00	11

RPT Repeat Sequence Count
00 No repeat
01 Repeat 4 times
10 Repeat 8 times
11 Repeat 16 times

INI Initial Setting Delay
INI[1-0] defines the number of TKCLK periods for the initial settling of pin Cref. The delay is (INI[1-0] + 1) *4*TKCLK.

ASTDLY Auto Mode Start Delay

ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0] +1) * 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.

LFNF Low-Frequency Noise Filter Setting

Low-Frequency Noise Filter Setting

00 Disable LFNE

If the scan count with noise injection detection is larger than (LFNF [1-0] * 8), the scan result is ignored.

179h TKIII Control Register 2 (RW)

Bit	D7	D6	D5	D4	D3	D2:D1	D0
Name	-	-	PRS	-	-	-	-
Default	0	0	1	0	0	00	0

PRS Pseudo-Random Sequence

0 Disable PRS

1 Enable PRS

17Ah TKIII Control Register 3 (RW)

Bit	D7:D4	D3	D2:D0
Name	-	MFEN	CCNT[2:0]
Default	0000	0	011

MFEN Multiple Frequency Scan

0 Disable MF

1 Enable MF

CCNT Cycle Count of Each Conversion Sequence

000 1024

001 2048

010 4096

011 8192

100 12288

101 16384

110 32768

111 65536

17Bh TKIII CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select

000 10pF

001 20pF

010 30pF

011 40pF

100 50pF

101 60pF

110 70pF

111 80pF

17Ch TKIII PUD Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	PUDIEN	PUDREN	-	PUD [3:0]
Default	0	00	00	0000

TK3PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance which is caused by a high capacitance key. Connecting a constant current source or resistor can thus maintain touch key detection sensitivity. In general, we

will try to maintain the raw count around half of CCNT for the case without key touch.

For DC current, PUD [3:0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PUD [3-0] enables 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable
PUDREN Pull-up/Pull-down DC Resistor Enable

PUD Pull up DC Current
- 1000 Enable 8uA current source.
- 0100 Enable 4uA current source.
- 0010 Enable 2uA current source.
- 0001 Enable 1uA current source.

PUD Pull up Resistor
- 1000 Enable 5K resistor source.
- 0100 Enable 10K resistor source.
- 0010 Enable 20K resistor source.
- 0001 Enable 40K resistor source.

17Dh System Clock Select Register (RW)

Bit	D7:D4	D3:D0
Name	SCS[3:0]	TKCS[3:0]
Default	0000	0001

SCS System Clock Select
- 0000 16MHz / 1
- 0001 16MHz / 2
- 0010 16MHz / 4
- 0011 16MHz / 6
- 0100 16MHz / 8
- 0101 16MHz / 10
- 0110 16MHz / 12
- 0111 16MHz / 14
- 1000 16MHz / 16
- 1001 16MHz / 32
- 1010 16MHz / 64
- 1011 16MHz / 128
- 1100 16MHz / 256
- 1101 16MHz / 256
- 1110 16MHz / 256
- 1111 16MHz / 256

TKCS Touch Key Clock Select
- 0000 System Clock / 2
- 0001 System Clock / 4
- 0010 System Clock / 6
- 0011 System Clock / 8
- 0100 System Clock / 10
- 0101 System Clock / 16
- 0110 System Clock / 32
- 0111 System Clock / 64
- 1000 System Clock / 128
- 1001 System Clock / 256
- Other Reserved

17Eh Spread Spectrum Register (RW)

Bit	D7:D2		
Name	SSR[3:0]	SSA[1:0]	-
Default	0000	11	-

SS Spread Spectrum Setting

With spread spectrum technique, electromagnetic energy produced over a particular bandwidth is spread in the frequency domain, and that can reduce EMI. Two parameters are listed as follows:

SSR [3:0] Defines the spread spectrum sweep rate. If the SSR[3:0] =0, then spread spectrum is disabled.

SSA [1:0] Defines how to adjust the spread spectrum frequency bandwidth. The frequency is adjusted by adding SSA [1:0] range to the actual internal OSC control register.

SSA [1:0]=11 +/- 32
SSA [1:0]=10 +/- 16
SSA [1:0]=01 +/- 8
SSA [1:0]=00 +/- 4

17Fh Auto Sleep Mode Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	ASEN	-	BLMA[1:0]	AST[3:0]-
Default	0	0	00	1111

ASE N Auto-SLEEP Enable
0 Disable
1 Enable

BLMA Baseline moving average
The hardware baseline can be generated by the slow-moving average setting.
00 32 average
01 64 average
10 128 average
11 256 average

AST Auto Sleep Time
0000 0.5s
0001 1s
0010 1.5s
0011 2s
0100 2.5s
0101 3s
0110 3.5s
0111 4s
1000 4.5s
1001 5s
1010 6s
1011 7s
1100 8s
1101 9s
1110 10s
1111 11s

180h Sleep Mode Control Register (RW)

Bit	D7	D6	D5	D4	D3:D2	D1:D0
Name	-	PW	-	SC	T2[1:0]	T1[1:0]
Default	0	0	0	0	00	00

PW Proximity Wakeup
Disable: wake up>>scan key once>>go to sleep again
Enable: wake up>> generates INT signal (optional) >>go to sleep after Auto Sleep Time is expired if no key is detected.
0 Disable
1 Enable

SC Sleep Calibration
0 Disable
1 Enable

T2 Wake Up Period with Key Disable

The device will be woken up according to the T2 setting by polling the status of Key.
00 50ms
01 100ms
10 200ms
11 300ms

T1 Wake Up Period with Key Enable
The device will be woken up according to the T1 setting to maintain the baseline to prevent the change of environment from stopping Key waking up the device.
00 2s
01 4s
10 8s
11 16s

181h~183h Wake Up Key Select Register (RW)

Bit	D7:D0		
Name	WK[23:16]	WK[15:8]	WK[7:0]
Default	0000 0000	0000 0000	0000 0000

WK Wakeup Key Select Setting
0 Disable
1 Enable

184h Wake Up Threshold Register (RW)

Bit	D7:D0
Name	WTH[7:0]
Default	0000 1000

Wake up threshold range from 0 to 255

185h TKIII Sleep Mode CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select
000 10pF
001 20pF
010 30pF
011 40pF
100 50pF
101 60pF
110 70pF
111 80pF

186h TKIII Sleep Mode PUD Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	PUDIEN	PUDREN	-	PUD[3:0]
Default	0	0	00	0000

TK3 PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance caused by a high capacitance key. Connecting a switching current source or resistor can thus maintain touch key detection sensitivity.

For DC current, PUD[3:0] can enable 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] can enable 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable
PUDREN Pull-up/Pull-down DC Resistor Enable
PUD Pull up DC Current
1000 Enable 8uA current source.

0100 Enable 4uA current source.
0010 Enable 2uA current source.
0001 Enable 1uA current source.

PUD Pull up Resistor
1000 Enable 5K resistor source.
0100 Enable 10K resistor source.
0010 Enable 20K resistor source.
0001 Enable 40K resistor source.

187h Sleep Mode Raw Count Register 1 (RO)

Bit	D7:D0
Name	SLRC[15:8]
Default	0000 0000

188h Sleep Mode Raw Count Register 2 (RO)

Bit	D7:D0
Name	SLRC[7:0]
Default	0000 0000

SLRC Sleep Mode Raw Count
Read-only. Value for reference

189h Sleep Mode Baseline Register 1 (RO)

Bit	D7:D0
Name	SLB[15:8]
Default	0000 0000

18Ah Sleep Mode Baseline Register 2 (RO)

Bit	D7:D0
Name	SLB[7:0]
Default	0000 0000

SLB Sleep Mode Baseline
Read-only. Value for reference

18Bh I^2C Configuration (RW)

Bit	D7:D1	D0
Name	-	CLKS
Default	0000000	0

CLKS Clock Stretching (For I^2C)
0 Disable stretching
1 Enable stretching

18Ch-190h Reserved

Bit	D7:D0
Name	-
Default	---- ----

191h-198h Slider1 Map Register 1 (RW)

Bit	D7:D0
Name	S1Kx[7:0]
Default	xxxx xxxx

S1Kx Slider1 Keyx Map table
Slider1 KEYx is mapped to Touch Key S1Kx[7:0]

199h-1A0h Slider2 Map Register (RW)

Bit	D7:D0
Name	S2Kx[7:0]
Default	0000 0000

S2Kx Slider2 Keyx Map table
Slider2 KEYx is mapped to Touch Key S2Kx[7:0]

1A1h – 1A8h Reserved

Bit	D7:D0
Name	-
Default	---- ----

1A9h – 1B0h Reserved

Bit	D7:D0
Name	-
Default	---- ----

1B1h GPIO Value Register 1 (R/W)

Bit	D7:D0
Name	GPV [7:0]
Default	0000 0000

1B2h GPIO Value Register 2 (R/W)

Bit	D7:D0
Name	GPV [15:8]
Default	1100 0000

1B3h GPIO Value Register 3 (R/W)

Bit	D7:D0
Name	GPV [23:16]
Default	0000 0001

GPV GPIO Value
Define GPIO values
0 GPIO pin LOW
1 GPIO pin HIGH
Above GPIO pin HIGH or LOW will be set only when the corresponding bits of the register GPIO Pin Select registers (16Fh~171h) are enabled.

1B4h GPIO Enable Register 1 (R/W)

Bit	D7:D0
Name	GPE [7:0]
Default	0001 1100

1B5h GPIO Enable Register 2 (R/W)

Bit	D7:D0
Name	GPE [15:8]
Default	0000 0000

1B6h GPIO Enable Register 3 (R/W)

Bit	D7:D0
Name	GPE [23:16]
Default	0000 0000

GPE GPIO Enable
0 Disable GPIO function
1 Enable GPIO function

1B7h-1CEh GPIO Map Register (R/W)

Bit	D7:D0
Name	GMx [7:0]
Default	xxxx xxxx

GMx [7:0] Map touch key x to which IS31SE5120A pin according to the following table and the value of GMx [7:0].

IS31SE5120A Pin #	GMx [7:0]
P2	0
P3	1
P4	2
P5	3
P6	4
P7	5
P8	6
P9	7
P10	8
P11	9
P12	10
P13	11
P14	12
P15	13
P19	14
P23	15
P24	16
P26	17
P27	18
P28	19
P29	20
P30	21
P31	22
P32	23

1CFh GPIO Toggle Enable Register 1 (R/W)

Bit	D7:D0
Name	TOEN [7:0]
Default	0001 0000

1D0h GPIO Toggle Enable Register 2 (R/W)

Bit	D7:D0
Name	TOEN [15:8]
Default	0000 0000

1D1h GPIO Toggle Enable Register 3 (R/W)

Bit	D7:D0
Name	TOEN [23:16]
Default	0000 0000

TOENx Enable GPIO Toggle Mode
0 Disable Touch Key channel to enter GPIO Toggle Mode.
1 Enable Touch Key channel to enter GPIO Toggle Mode.

1D2h Key Scan Once Register (RW)

Bit	D7:D2	D1	D0
Name	-	TR	EN
Default	0000	00	00

TR Write 1 Trigger one scan
Read 1 Busy
Read 0 Data ready

EN Enable Key Scan Once
0 Continuous scan of all enabled keys
1 Scan all enabled keys once

1D3h Table Ready Mark Register (RO)

Bit	D7	D6:D0
Name	INIRDY	MARK[6:0]
Default	0	0000000

INIRDY Touch Key Init Ready
1 Touch key is initializing
0 Touch key initialization is completed

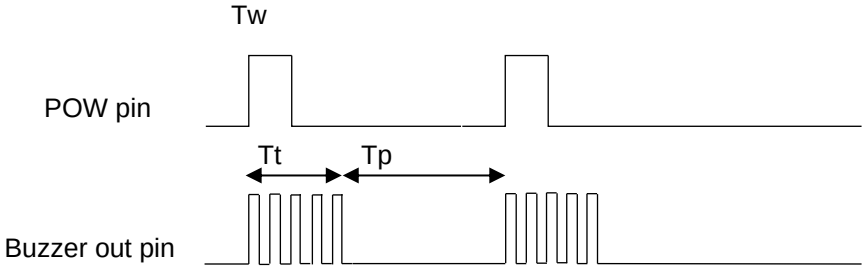
MARK This register is used by the firmware to indicate parameters are correctly programmed.
Ready/Fail status
00 ready
Others not ready

7. Buzzer / Melody Application

0Ah Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

1st byte	2nd byte	3rd byte	4th byte
Scale ID	Tt	Tw	Tp



Tt, Tw and Tp range from 0 to 255 @ 4ms step

A Tone played duration is defined as Tt + Tp.

The support scale is from 3A to 8G#.

Frequencies for equal-tempered scale, A4 = 440 Hz
"Middle C" is C4

	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%
	6	freq	divisor	freq error	7	freq	divisor	freq error	8	freq	divisor	freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%
C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%
D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%

Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B

0Ah Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

Clear Melody buffer and stop play.

0Ah Buzzer/Melody Register (R)

Bit	D7:D0
Name	BM
Default	0000 1010

BM Buzzer/Melody Register Read. It shows the available tone buffer size. IS31SE5120A has 10 built-in note buffers.

I^2C command format - Each node is composed of 4-byte data, and the incomplete note will be ignored. The incoming note data will be ignored if the FIFO is full.

0x78, 0x09, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp), ….

0x78, 0x09, 0xFF stop the melody play and clear the FIFO

0x78, 0x09 Set the register number to 0xF0

0x79 Read FIFO remaining length

Reference schematic and tone waveform are introduced as follows:

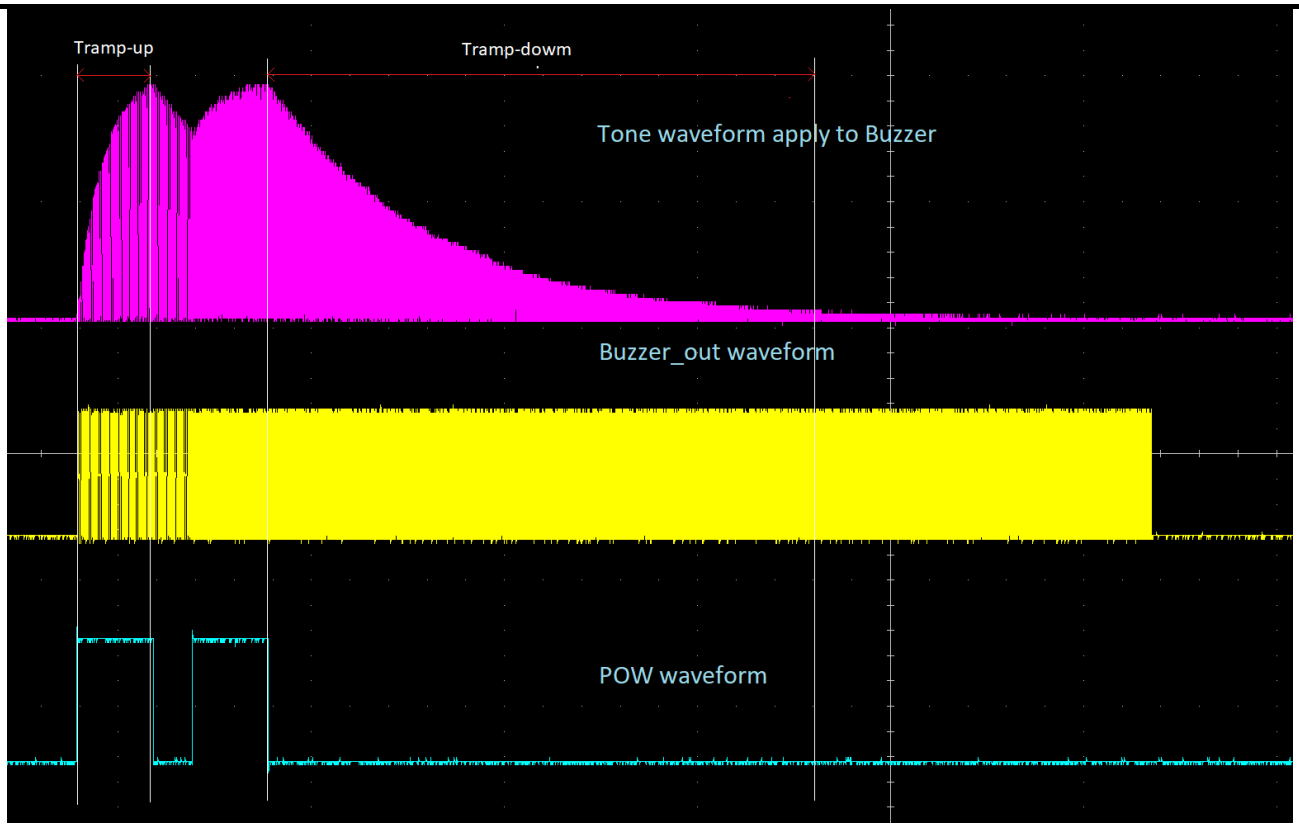


Figure 7-1 Buzzer/ Melody waveform example

Note:

Tramp-up: 100R as below Figure 7-2 decides the signal ramp-up rate.

Tramp-down: The signal ramps down because POW is low and 47uF capacitor as below Figure 7-2 decides the ramp-down rate.

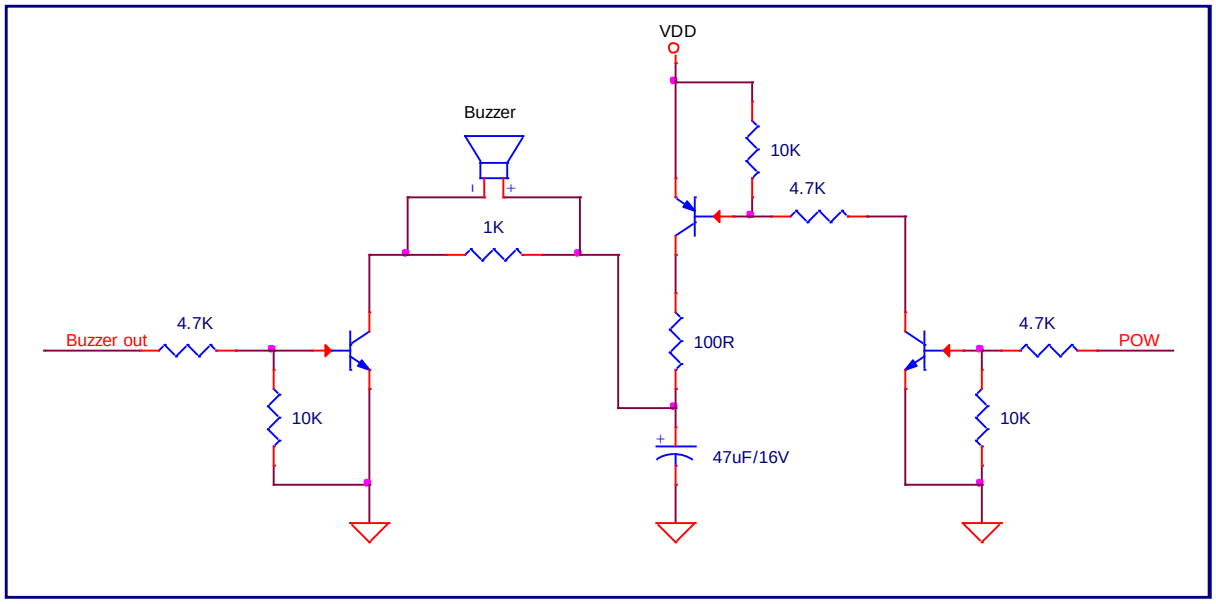


Figure 7-2 Typical application circuit for Melody

8. Typical Application Information

The IS31SE5120A is an ultra-low-power, fully integrated 24-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric material such as glass or plastic.

8.1 Sensitivity Adjusting

Sensitivity can be adjusted by the external capacitor or internal register.

A higher capacitor value will yield lower detection sensitivity. A lower capacitor value will yield higher detection sensitivity.

8.2 Interrupt

Touch key detection event will trigger the INTB pin. The INTB pin will be driven low when the selected channel is pressed or released.

8.3 Sleep Mode

IS31SE5120A can be put in sleep mode to save power consumption and the device can be woken up by touching the selected keys. For the detailed application, please refer to Section 3.8 Generate Sample Code of Lumissil application note “IS31SE5120A Eval Board User's Manual”.

9. Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

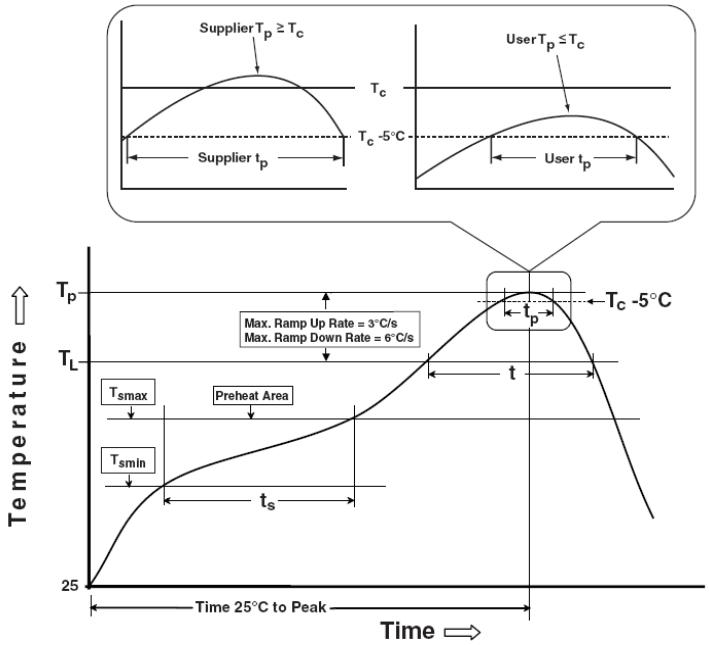
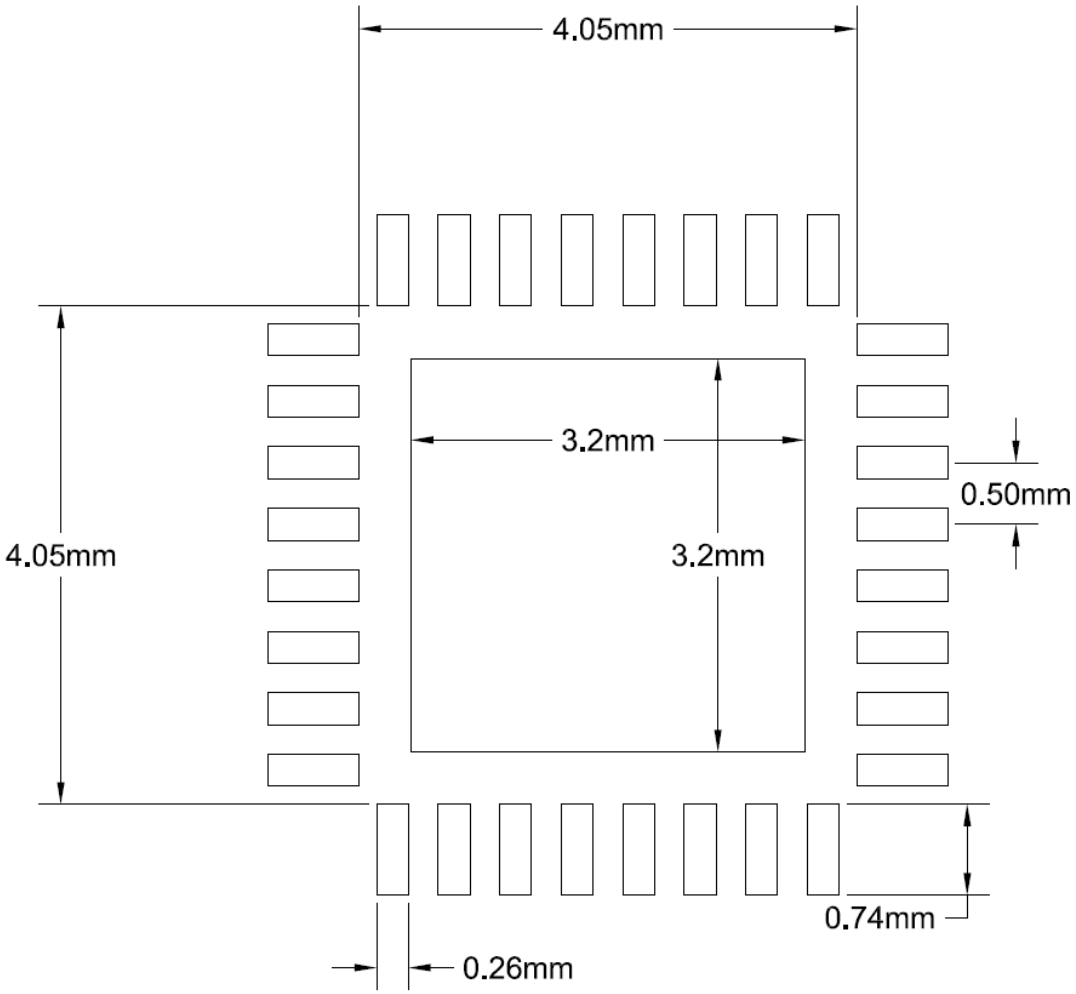


Figure 9-1 Classification Profile

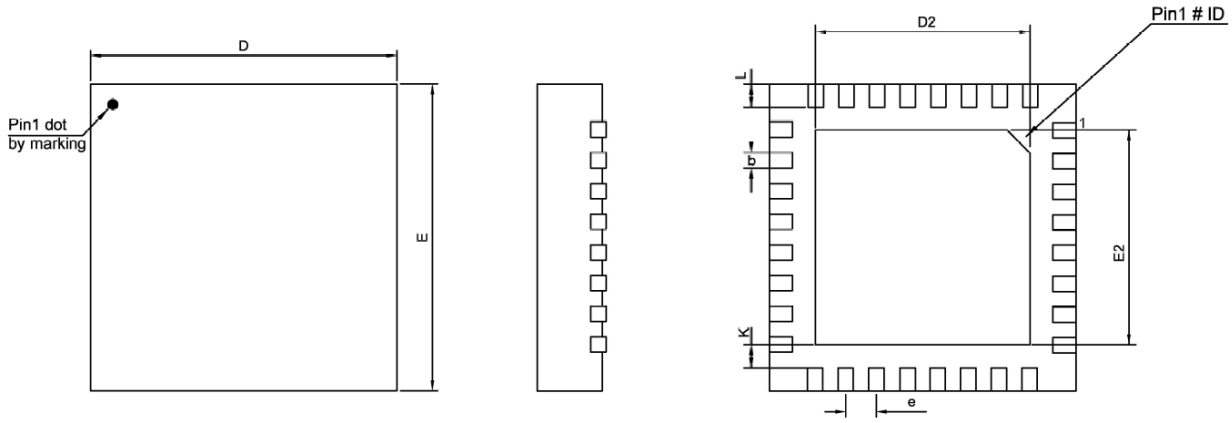
10. Package Information

10.1 32-pin QFN

10.1.1 Recommended Land Pattern

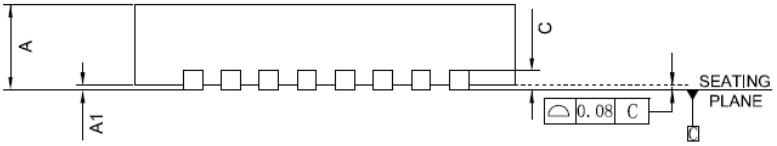


10.1.2POD



TOP VIEW

BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
c	0.203 REF.		
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.10	3.20	3.30
E2	3.10	3.20	3.30
L	0.35	0.40	0.45
e	0.50BSC		
K	0.20	-	-

Notes:

1. Controlling dimension: mm
2. Reference document: JEDEC MO-220
3. The pin's sharp and thermal pad shows different shapes among different factories.

11. Errata

12. Revision History

Revision	Detailed Information	Date
A	First formal release	2023.07.26
B	1. Only SHDE[0], SHDE[1], SHDE[2], SHDE[8], and SHDE[21] can be set as Shield Pins for registers 163h~165h Shield Pin Select Register. 2. Update Sleep mode of Typical Application Information as: For the detailed application, please refer to Section 3.8 Generate Sample Code of Lumissil application note “IS31SE5120A Eval Board User's Manual”	2024.04.09
C	Modify PINOUT and PIN Description.	2024.10.12

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Lumissil:

IS31SE5120A-QFLS3-TR