

GTI-ATM3330e Module

Extreme Low Power Bluetooth 5.3 SoC with RF Energy Harvesting Module

Datasheet

Rev 1.4- Aug 03, 2023



Revision history

Date	Revision	Board Rev	Section/ page	Description
Feb 08, 2023	Rev 1.0			Preliminary
May 15, 2023	Rev 1.1			Update CH2, CH10,CH12, CH13, CH14
May 20, 2023	Rev 1.2			Update CH14
May 28, 2023	Rev 1.3			Add CH30 Packaging , update CH3 block diagram
Aug 03, 2023	Rev 1.4			Change module name from GTI-M3330e to GTI-ATM3330e Add FCC ID on CH31, FCC warning on CH33
				Add FGG ID OII G131, FGG waiting oil G133



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1. Overview

The GTI-ATM3330e Bluetooth module uses Wireless SoC Series and is part of a family of extremely low-power Bluetooth® 5.3 system-on-chip (SoC) solutions. This Bluetooth Low Energy SoC integrates a Bluetooth 5.3 compliant radio with ARM® Cortex® M33F application processor,128 KB Random Access Memory (RAM), 64 KB Read Only Memory (ROM), 512 KB nonvolatile memory (NVM), with ARM® TrustZone® enabled security features, and state-of-the-art power management to enable maximum lifetime in battery-operated devices.

The GTI_M3330E Bluetooth module, with a 0.85 mA radio receiver and a 2.1 mA radio transmitter power consumption, is designed to extend battery life for the Internet-of-Things (IoT) markets. Support for low-duty cycle operation allows systems to run for significantly longer periods without battery replacement. In addition, this series of SoCs supports direct operation from harvested energy sources, including RF, photovoltaic, thermal, and mechanical. Innovative wakeup mechanisms are supported to provide options for further power consumption reduction.

2. Key Features

Bluetooth LE

- Bluetooth Low-Energy 5.3 compliant
- 2 Mbps, 1 Mbps 500 kbps, and 125 kbps PHY rates
- Supports Bluetooth Angle-of-arrival (AoA) and Angle-of-Departure (AoD) direction finding

MCU and **Memory**

- 64 MHz ARM® Cortex® M33F MCU
- 64 KB ROM, 128 KB RAM, 512 KB NVM
- Retention RAM configuration: 16 KB to 128 KB in 16KB step sizes
- 16 MHz Crystal Oscillator

Security

- ARM® TrustZone®, HW Root of Trust, Secure Boot, Secure Execution & Debug
- AES-128/256, SHA-2/HMAC 256 Encryption/Cryptographic Hardware Accelerators
- True Random Number Generator (TRNG)

Energy Harvesting

- On-module 915MHz RF Energy Harvester
- Separate input for photovoltaic, thermal, mechanical, and other energy harvesting sources
- External energy storage interface supports a variety of storage options



RF and Power Management

■ Fully integrated RF front-end

Rx Sensitivity: -95 dBm Max. Tx Power: <10 dBm

■ Sensor Hub

■ RF Wakeup Receiver

PRELIMINARY

■ 1.1 V to 4.2 V battery input voltage with integrated Power Management Unit (PMU)

■ Radio power consumption with a 3.3 V battery

Rx@ -95 dBM: 0.85 mA Tx@ 0 dBm: 2.5 mA

■ Soc typical power consumption with 3.3 V battery including PMU

Active Rx @ -95 dBm: 1.4 mA Active Tx@ 0 dBm: 2.9 mA Retention@ 32 KB RAM: 1.8 µA

Hibernate: 1.3 µA

Hibernation with Wakeup Receiver: $1.6 \mu A$ Soc Off with Harvesting Enabled: 700 nA

Interfaces

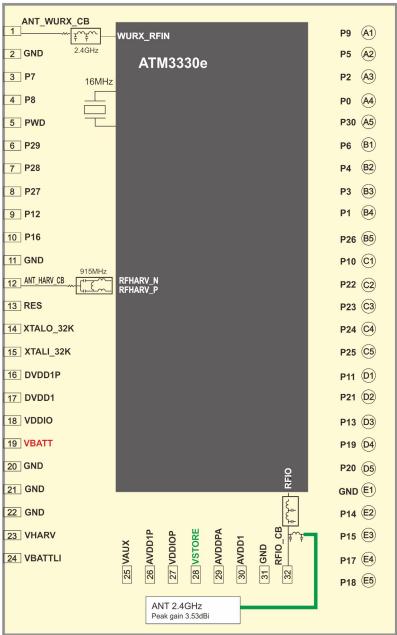
- I2C, SPI, UART, GPIOs
- Quad SPI
- SWD for interactive debugging

Module Package (see CH. 7)



3. Block diagram

GTI-M3330e module





4. Applications

Industrial and Enterprise

- Beacons
- Industrial IoT Sensors
- Remote Sensors
- Environmental Monitors

Healthcare

- Asset Trackers
- Location
- Wearables
- Health monitors
- Sports and Fitness

Home

- Human Interface Devices (HID)
- Entertainment
- Advanced Home Automation
- Advanced Remote Controls

Smart Cities

- Asset Trackers
- Beacons

Personal

- Gaming
- Advanced Wearables

Auto

- Key fobs and Accessories
- Infotainment



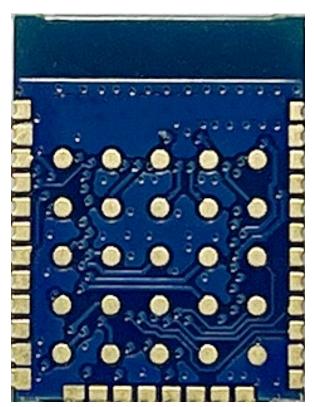
5. Specifications

Model	GTI-ATM3330e
Product Name	Bluetooth module
Major Chipset	ATM3330e
Wireless Standard	Bluetooth® V5.3 specification
RF Output Power	-6~10 dBm (typical)
RX Sensitivity	-95 dBm (typical)
Modulation Method	GFSK
Frequency Band	2.402~2.480 GHz
Supply Voltage (BAT)	BAT +2.7V ~ +4.2V
Operating Temperature	-20~ +70°C
Storage Temperature	-40 ~ 85°C
Humidity	5 to 90 % maximum (non-condensing)
ESD Protection	2KV
Dimension	14.5 x 11 x 2 mm (LxWxH) ±0.2mm



6. Module pictures

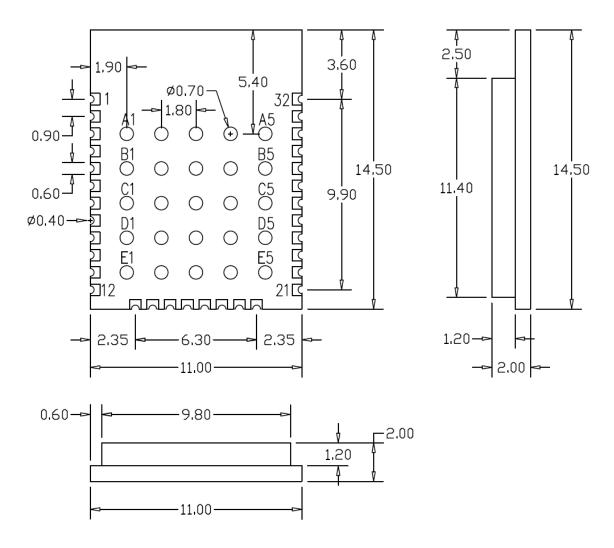




Top view Bottom view

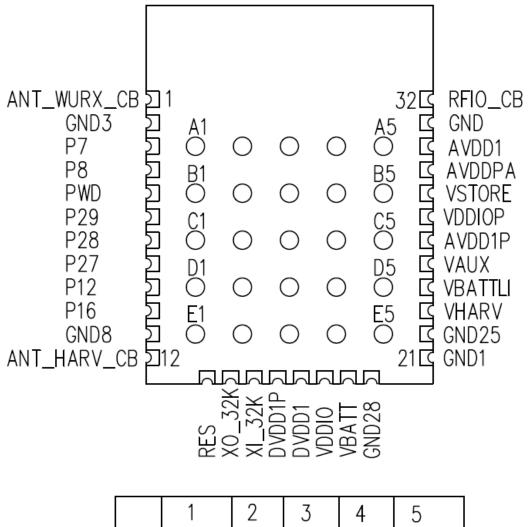


7. Module Dimensions





8. Pin name and layout



	1	2	3	4	5
Α	P9	P5	P2	P0	P30
В	P6	P4	Р3	P1	P26
С	P10	P22	P23	P24	P25
D	P11	P21	P13	P19	P20
E	GND10	P14	P15	P17	P18



9. Pin description

Pin#	Name	Description	Default I/O
1	ANT_WURX_CB	Wakeup receiver RF input	
2	GND	Ground	
3	P7	Programmable Digital I/O	I2C1_SDA
4	P8	Programmable Digital I/O	S3
5	PWD	Power Down Input (Active High)	1M resistor to GND
6	P29	Programmable Digital I/O	O/P, LED2
7	P28	Programmable Digital I/O	I/P, Harvest meter
8	P27	Programmable Digital I/O	
9	P12	Programmable Digital I/O	UR0_CTS
10	P16	Programmable Digital I/O	LTE_RI
11	GND	Ground	
12	ANT_HARV_CB	Differential RF Harvester Input	
13	RES	Reserved, must tie to ground	
14	XO_32K	32.768 kHz crystal oscillator output for sleep operation. Can be programmed by using internal oscillator	
15	XI_32K	32.768 kHz crystal oscillator input for sleep operation. Can be programmed by using internal oscillator	
16	DVDD1P	PMU generated digital core power supply output	
17	DVDD1	Digital circuit power input	
18	VDDIO	Digital I/O Power Supply	
19	VBATT	Battery supply from 1.1V to 3.3V. Must connect to a 10uF capacitor if VBATTLI is used	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	VHARV	Output of RF Harvester; can be used as input from other harvesting modalities to supply energy to the ATM chip	
24	VBATTLI	2.7 V to 4.2 V lithium ion battery supply in place of VBAT. If lithium ion battery is not used, this pin must be connected to ground	
25	VAUX	Reserved for switching regulator internal use	
26	AVDD1P	PMU generated analog core supply output.	
27	VDDIOP	1.8 V I/O power supply generated by switcher, connect to VAUX if unused	



Pin description (continued)

Pin#	Name	Description	
28	VSTORE	Storage node for Switching regulator	
29	AVDDPA	PA power supply	
30	AVDD1	Analog core power input	
31	GND	Ground	
32	RFIO_CB	2.4 GHz Single-ended RF I/O for Bluetooth radio	
A1	P9	Programmable Digital I/O	UR_S0
A2	P5	Programmable Digital I/O	
А3	P2	Programmable Digital I/O	
A4	P0	Programmable Digital I/O	SWD_CLK
A5	P30	Programmable Digital I/O	
B1	P6	Programmable Digital I/O	I2C1_SCK
B2	P4	Programmable Digital I/O	
В3	P3	Programmable Digital I/O	
B4	P1	Programmable Digital I/O	SWD_IO
B5	P26	Programmable Digital I/O	
C1	P10	Programmable Digital I/O	UR_S1
C2	P22	Programmable Digital I/O	
C3	P23	Programmable Digital I/O	
C4	P24	Programmable Digital I/O	
C5	P25	Programmable Digital I/O	
D1	P11	Programmable Digital I/O	
D2	P21	Programmable Digital I/O	
D3	P13	Programmable Digital I/O	UR0_RTS
D4	P19	Programmable Digital I/O	
D5	P20	Programmable Digital I/O	
E1	GND	Ground	
E2	P14	Programmable Digital I/O	
E3	P15	Programmable Digital I/O	UR0_TX
E4	P17	Programmable Digital I/O	
E5	P18	Programmable Digital I/O	



10. Pin Multiplexing

	P 0	P 1	P 2	P 3	P 4	P 5	P 6	P 7	P 8	P 9	P 1	P 1	P 1	P 1	P 1	P 1	P 1	P 1	P 1	P 1	P 2	P 2	P 2	P 2 3	P 2	P 2 5	P 2 6	P 2 7	P 2 8	P 2	P 3
swdclk	х										0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	b	1	Ö	9	0
Swdcik	^	Х																													
qspi_clk	Х	^					Х						Х						Х												Х
qspi_cik qspi_csn	^	Х					^	Х					^	Х					^	Х						Х					^
qspi_dsi		^	Х					^						^	Х					^	Х					^	Х				
qspi_d0 qspi_d1			^	Х					Х						^	Х					^	Х					^	Х			
qspi_d1 qspi_d2				^	Х											^	Х					^	Х					^	Х		
qspi_d2 qspi_d3					^												^	· ·					^						^	Х	
qspi_us						Х												Х						Х						Α.	
0:0																															
Spi0_csn	Х								Х								Χ				Χ										Х
Spi0_sclk		X																Х								Х		Χ	-		
Spi0_mosi			Х																Х								Χ		Х		
Spi0_miso				Х																Χ									\vdash	Χ	
spi1_csn					Х	<u> </u>							Х	<u> </u>							Х								Н		
spi1_sclk						Χ								Χ								Χ							Щ		<u> </u>
spi1_mosi							Χ								Х								Х						Н		
spi1_miso								Х								Χ								Х							
10.0																															
i2c0_sck	Х				Х				Х				Х				Х				Х						Χ				Х
i2c0_sda		Х				Х								Х				Χ				Х				Х		Х		Χ	
i2c1_sck			Х				Х								Х				Х				Х				Χ		Х		
i2c1_sda				Х				Х								Χ				Χ				Х					Щ	Χ	
Pdm0_clk	Χ				Χ				Х				Х				Х				Х										Χ
Pdm0_in		Х				Х								Х				Χ				Х				Х		Х			
pdm1_clk			Х				Χ								Х				Х				Х				Χ		Χ		
pdm1_in				Х				Х								Χ				Χ				Х						Χ	
i2s0_sck_out	Х			Х			Χ						Х			Χ			Х			Х						Х			Χ
i2s0_ws_out		Х			Χ			Х						Х			Х			Χ			Х			Х			Χ		
i2s0_sd_out			Х			Х			Х						Х			Χ			Х			Х			Χ			Χ	
i2s0_sck_in	Х			Х			Χ						Х			Χ			Х			Х						Х			Χ
i2s0_ws_in		Χ			Χ			Χ						Х			Χ			Χ			Х			Х			Χ		
i2s0_sd_in			Χ			Χ			Х						Х			Χ			Χ			Х			Χ			Χ	
Uart0_rx	Х		Х		Х		Х		Х				Х		Х		Χ		Х		Х		Х				Χ		Χ		Х
Uart0_tx		Х		Х		Х		Х						Х		Χ		Χ		Χ		Х		Х		Х			Ш	Χ	
Uart0_cts	Х				Χ				Х				Х				Х				Χ									Χ	Χ
Uart0_rts		Χ				Х								Х				Χ				Χ				Х					
uart1_rx		Х				Х								Х				Х				Х				Х		Х			
uart1_tx			Х				Х								Х				Х				Х				Χ	Х	Χ		
uart1_cts				Х				Х								Χ				Χ				Х						Χ	
uart1_rts	Х				Х				Х				Х				Χ				Х										Χ
Pwm0	Х					Х			Х				Х				Χ														Х
pwm1		Х																Х								Х		Х			
pwm2			Х																Х								Χ		Х		
pwm3				Х																Х										Х	
pwm4					Х								Х								Х										



	P 0	P 1	P 2	P 3	P 4	P 5	P 6	P 7	P 8	P 9	P 1 0	P 1	P 1 2	P 1 3	P 1 4	P 1 5	P 1 6	P 1 7	P 1 8	P 1 9	P 2 0	P 2 1	P 2 2	P 2 3	P 2 4	P 2 5	P 2 6	P 2 7	P 2 8	P 2 9	P 3 0
pwm5						Х								Χ								Χ									
pwm6							Χ								Χ								Χ								
pwm7								Χ								Х								Χ							
ksi19																											Χ				
ksi18																												Χ			
ksi17																				Χ											
ksi16																			Χ												
ksi15																		Χ													
ksi14																	Χ														
ksi13																Χ															
ksi12													Χ													Χ					
ksi11												Χ																		Χ	Χ
ksi10											Х													Х					Х		
ksi9										Х													Х					Х			
ksi8									Х													Х	Ť								
ksi7								Х													Х										
ksi6							Х													Х											
ksi5						Х	Ė												Χ												
ksi4					Х	_												Х													
ksi3				Х	^												Х														
ksi2			Х	^												Х	^														
ksi1		Х	^												Х	^															
Ksi0		^												~	^												~				
1/210	Χ													Χ													Χ				
kso19																											Х				
kso18																											٨	· ·			
kso17																												Χ			~
kso16																														.,	Χ
																														Χ	
kso15																													Χ		
kso14																									Χ						
kso13																								Χ							
kso12													Х													Χ					
kso11												Х																		Х	Χ
kso10											Х													Х					Χ		
kso9										Χ													Χ					Χ			
kso8									Χ													Χ									
kso7								Χ													Χ										
kso6							Χ													Χ											
kso5						Χ													Χ												
kso4					Х													Х													
kso3				Χ													Χ														
kso2			Χ													Χ															
kso1		Χ													Χ																
Kso0	Χ													Χ													Χ				
shub_spi0_csn	Χ								Χ								Χ				Χ										
shub_spi0_sclk		Χ		L		L												Χ			[Х		Х			
shub_spi0_mosi			Х																Х								Х		Х		
shub_spi0_miso				Χ																Х										Х	
shub_spi1_csn					х								Х								Х										



	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р	Р
	0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3
											0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0
shub_spi1_mosi							Х								Χ								Χ								
shub_spi1_miso								Χ								Х								Х							
shub_i2c0_sck	Х				Х				Х				Х				Х				Х										Х
shub_i2c0_sda		Х				Х								Х				Х				Х				Х		Х		Х	
shub_i2c1_sck			Х																Х												
shub_i2c1_sda				Х																Х											
Qdec0_a	Χ						Х						χ						Х												Х
Qdec0_b		Χ						Χ					$\stackrel{\sim}{-}$	Х						Х						Χ					
qdec1_a		^	Х					^	Х					^	Х					^	Х					^	Х				
qdec1_b			^	Х					^						^	Х					^	Х					^	Х			
qdec1_b				^	· ·											^	· ·					^	٧.					^	v		
					Χ												Χ						Χ						Χ		
qdec2_b						X												Χ						Χ		.,			-	Χ	
xlna_xpa0	Χ	-				Х							_			Χ					Χ					Χ			Χ		
xlna_xpa1		Χ					Х						_				Χ					Χ					Χ			Χ	
xlna_xpa2			Χ		ļ		<u> </u>	Χ					Χ					Χ					Χ								
xlna_xpa3				Χ					Х					Χ					Χ					Χ							
xlna_xpa4					Х		<u> </u>								Χ					Х								Χ			Х
mdm_in4																												Χ			
mdm_in3									Χ																						
Mdm_in2								Х																							
mdm_in1							Х																								
mdm_in0						Х																									
mdm_out7																											Χ				
mdm_out6																										Χ					
mdm_out5																															Х
mdm_out4																								Х							
mdm_out3																							Х								
mdm_out2																						Χ									
mdm_out1																					Х										
mdm_out0																				Х	^										
Lc_rx_en	Х		Х		Х		Х		Х				Х		Х		Х		Х	^	Х		Х				Х		Х		Х
	^	· ·	^		^	· ·	^	· ·	^				^	· ·	^		^	· ·	^		^	· ·	^			· ·	^	_	^	· ·	^
Lc_tx_en		Χ		Х		Χ		Χ						Χ		Χ		Χ		Χ		Χ		Х		Χ		Χ		Χ	
ant out7					_		_	.,								,,								-					_		
ant_out7								Х								Х								Х							
ant_out6					-	-	Х								Χ							**	Χ								
ant_out5					<u> </u>	Х	-							Χ								Χ									
ant_out4					Х								Χ								Χ										
ant_out3				Χ			-													Χ										Χ	
ant_out2			Х		<u> </u>		<u> </u>												Χ								Χ		Χ		
ant_out1		Χ					<u> </u>											Χ								Χ		Χ			
ant_out0	Χ								Χ								Χ														Х
ble_sync	Χ																				Х								Χ		
ble_in_process		Χ																				Χ								Χ	
ble_tx			Х										Χ										Χ								
ble rx				Х										Х										Х							
ble_pti0		_													Х																Х
bie_pilo					Х										,,,																
ble_pti1					Х	Х										Χ										Χ					
					Х	Χ	х									Х	Х									Х	Х				



	P 0	P 1	P 2	P 3	P 4	P 5	P 6	P 7	P 8	P 9	P 1	P 2	P 3																		
											0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0
wlan_tx																			Х												
wlan_rx																				Χ								Х			
Tracedata_iq3					Х								Х								Χ										
tracedata_iq4						Х								Х								Х									
tracedata_iq5							Х								Х								Χ								
tracedata_iq6								Х								Χ								Х							
tracedata_iq7	Х								Х								Χ														Χ
tracedata_iq8		Х																Х								Х		Х			
tracedata_iq9			Χ																Х								Х		Χ		
tracedata_iq10				Х																Χ										Х	
tracedata_iq11					Χ								Χ								Χ										
tracedata_iq12						Χ								Χ								Χ									
tracedata_iq13							Х								Х								Χ								
tracedata_iq14								Х								Χ								Х							
tracedata_iq15	Х								Х								Χ														Χ
dbg	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Χ	Χ	Х	Х	Χ	Χ	Х	Χ	Х	Х	Х	Х	Х	Χ	Χ	Х
dtopbyp	Х	Х	Χ	Х	Х	Х	Х	Х	Х	Х	Х	Χ	Х	Х	Х	Χ	Χ	Х	Х	Х	Χ	Х	Χ	Х	Х	Х	Х	Х	Х	Х	Х
gpio	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Χ	Χ	Х	Х	Χ	Χ	Х	Χ	Х	Х	Х	Х	Х	Χ	Х	Χ



11. More about PMU external pins

Pin	Description
VBATT	Battery input from 1.1V to 3.3V. Must connect to a 10uF capacitor if VBATTLI is used Note: see CH 12 PMU configurations
VBATTLI	2.7 V to 4.2 V Lithium ion battery supply in place of VBAT. If Lithium ion battery is not used, this pin must be connected to ground
VDDPA	PA power supply
VSTORE	Connection to a large storage capacitor (typical value 220uF) Must be grounded when the harvester is not used.
VHARV	Connection to a storage capacitor of typical value 10uF. Must be grounded when the harvester is not used.
DVDD1P, AVDD1P	PMU generated digital and analog core supply outputs
DVDD1, AVDD1	Power supply input for digital and analog core circuits Note: DVDD1 is connected to DVDD1P via R2 0-ohm resistor AVDD1 is connected to AVDD1P via R3 0-ohm resistor in this module
VDDIOP	PMU generated 1.8V IO supply output Note: see CH 12 PMU configurations
VAUX	Auxiliary supply output of typical value oof 3.2V, used internally by the PMU
VDDIO	Power supply input for the digital and analog IO circuits Note: see CH12 PMU configurations



12. PMU configurations

The PMU must be configured correctly to ensure correct operation. The following modes of operation are supported by the PMU:

PMU Configuration	VBAT connection	VBATLI Connection	VDDIO Connection
Battery or external power supply (1.1 V-3.3 V) with internally generated I/O supply	Battery or power supply	VBAT	VDDIOP
Battery or external power supply (1.8 V-3.3 V) with externally generated I/O supply	Battery or power supply	VBAT	VBAT or other externally generated 1/0 supply that is between 1.8V-3.3V. VDDIOP should be connected to VAUX if it is not used with VDDPA.
High Voltage battery or power source (2.7 V-4.2 V) with internally generated I/O supply	Unconnected (keep the bypass capacitor connected)	High voltage battery or power source	VDDIOP

Note: the term VBAT is the same as VBATT and the VBATLI as VBATTLI



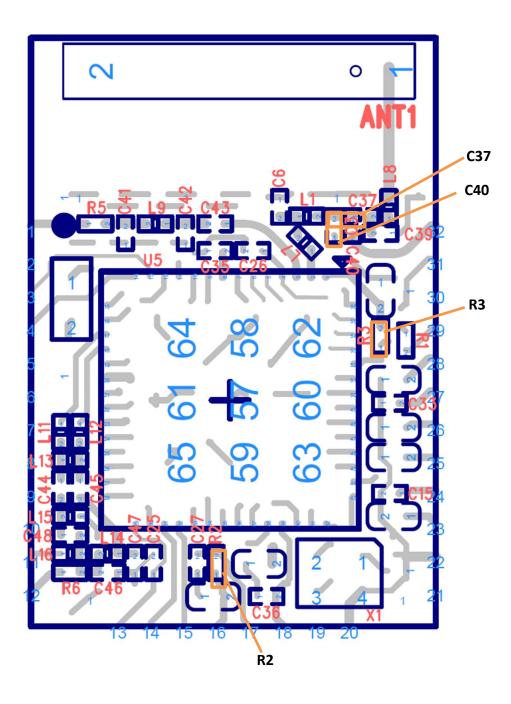
13. Power modes

The Module's SoC supports six primary power states which are Active, WFI, Retention, Hibernation, SoC Off, and Powerdown. Each primary state may have several secondary states depending on the number of active power domains and clock gating.

- 1. **Active:** All regions of the SoC are powered on. Active power can be optimized by utilizing clock gating registers and/or by putting the Cortex-M33F into Wait for Interrupt (WFI).
 - Bluetooth LE Deep Sleep: Bluetooth subsystem is powered down while the remainder of the Soc is powered up. This state is useful when data needs to be processed but does not need to be transmitted over RF.
- 2. **WFI:** When the MCU is Idle, it can be placed into WFI state to conserve power.
- 3. Retention: All or some of the 128KB SRAM, in increments of 16 KB, can be retained. All register/flip-flop states are retained. Digital I/Os will hold the state they were at when the transition into either Hibernate or Retain started. Wake can be from a timer expiring, activity detected on GPIOs, activity detected on the keyboard, activity detected on the mouse, the sensor hub reading measurements crossing a threshold, and the detection of a connection over the SWD interface. All selections about how to wake need to be programmed before the transition into the low-power state is triggered. The SRAM supply voltage can be lowered to further reduce leakage power consumption.
- 4. **Hibernation:** Powers down system memory. Retains only a minimal amount of flip-flop state. Retains I/O state.
 - Wake upsetting must be programmed before transitioning into this state.
- 5. **SoC Off:** All digital domains including the top-level digital domain are powered down, but the PMU remains on in an ultra low-power state with limited functionality. The system must do a complete, cold start reboot when returning from this state to an active state. Wake mechanisms are limited to
 - special 40-bit timer
 - external pin edge on PS
 - ultra-low power analog comparator with input on either P3 or P4.
- 6. **Powerdown** (PWD pin asserted): All power domains including the PMU are completely shut off. No supplies are internally generated or maintained.



14. Options by setting resistors

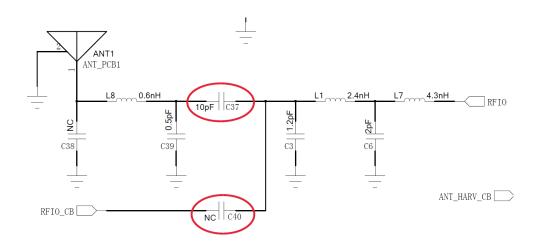




- Digital and analog core power supply
 - DVDD1 digital core power input has been connected to internal power DVDD1P through R2
- AVDD1 analog core power input has been connected to internal power AVDD1P through R3 If an external core power supply will be used, please remove R2 and R3 then connect DVDD1 and AVDD1 to external power.

■ RF antenna

- RFIO output has been connected to the onboard PCB trace antenna ant1.
- If using an external antenna, please remove C37 and then put on C40. The external antenna should be connected to RFIO_CB.





15. Maximum Electrical Ratings

Symbol	Parameter	Min.	Тур	Max.	Unit
VBATT	Battery supply	-0.2		3.6	V
VBATTLI	Lithium-ion battery supply	2.4		4.6	V
VDDPA	PA supply	1.0		1.8	V
VDDIO	I/O supply	-0.2		3.6	V
VIO	I/O pin	-0.2		3.4	V
ESD (HBM)	ESD HBM class 2			2000	V
ESD (CDM)	ESD CDM			500	V
T-store	Storage Temperature	-40		125	°C

Note: ESD(HBM) for TMC and PWD pins are 1250V

16. Recommended Operating condition

Operating Condition		Min.	Тур	Max.	Unit
VDDIO	I/O supply	1.7	1.8	3.3	V
VBATT	Battery supply	1.1		3.3	V
VBATTLI	Lithium-ion battery supply	2.4		4.6	V
VDDPA	PA supply	1.0		1.8	V
VPP25	OTP Programming Voltage	2.3	2.5	2.7	V
VIO	I/O pin voltage level	-0.2		VIO+0.2	V
Crystal OSC	16.000 MHz	-20		20	ppm
32K-OSC (*)	Crystal OSC-32.768KHz	-500		500	ppm
TA	Operating (Ambient) Temperature	-40	25	85	°C

Note:

1. VPP25 is physically connected to VDDIO. Set VDDIO to within the VPP25 range when programming the OTP.



17. Radio Tranceiver Characteristics (VCC=3.0V Temperature =27°C)

Parameter	Conditions	Min.	Typical	Max.	Units
Frequency range		2.402		24.80	GHz
Rx sensitivity	37-byte packets, clean Tx				
-	125 kbps		-101		dBm
	500 kbps		-98		dBm
	1 Mbps		-95		dBm
	2 Mbps		-92		dBm
	255-byte packets, dirty Tx				
	125 kbps		-100		dBm
	500 kbps		-96		dBm
	1 Mbps		-93		dBm
	2 Mbps		-90		dBm
Tx output power	10, 8, 6, 4, 2, 0, -2, -4, -6,-8,	-20		10	dBm
	-10, -20				
Tx power accuracy			+/- 1.5		dB
Tx spectral mask	2 MHz offset	-20			dBm
@ 1M sym/s	> 3 MHz offset	-30			dBm
Rx	Co-channel interference	21		-100	dB
Carrier-to-Interferer	Adjacent 1 MHz interference	15			dB
(LE 1M PHY)	Adjacent 2 MHz interference	-17			dB
	Adjacent 3 MHz interference	-27			dB
RSSI resolution			1		dB
RSSI accuracy	-90 to -20 dBm		TBD		dB

18. Wakeup Receiver Characteristics

Parameter	Conditions	Min.	Тур	Max.	Units
Sensitivity	2440 MHz, 14-byte packets at 1 ms		TBD		dBm
(>= 90% wakeup success rate)	intervals for 40 ms				

19. PMU Characteristics

Parameter	Conditions	Min.	Тур	Max.	Units
AVDD1P Output Voltage		0.975	1.0	1.025	V
DVDD1P Output Voltage		1.075	1.1	1.125	V
VDDIOP Output Voltage		1.71	1.8	1.89	V
VAUX Output Voltage		3.09	3.2	3.41	V



20. GPIO Characteristics

Parameter	Conditions	Min.	Тур	Max.	Units
Input VIH	VDDIO=3.3V	1.4		1.65	V
·	VDDIO=1.8V	8.0		0.95	V
Input VIL	VDDIO=3.3V	1.4		1.65	V
·	VDDIO=1.8V	0.8		0.95	V
Output VOH	2 mA Load				
	VDDIO=3.3V		3.24		V
	VDDIO=1.8V		1.71		V
Output VOL	2 mA Load				
	VDDIO=3.3V		0.02		V
	VDDIO=1.8V		0.03		V
Drive Strength	VDDIO=3.3V, high		95		mA
	VDDIO=3.3V, low		48		mA
	VDDIO=1.8V, high		26		mA
	VDDIO=1.8V, low		16		mA
Pull-up/down Resistance			125		kΩ

21. Radio Power Consumptions

VBAT current at 3V with internally generated IO supply					
Parameter	Conditions	Min.	Тур	Max.	Units
Radio Receiver Rx	Sensitivity at -95 dBm		0.85		mA
Radio Transmitter Tx	Output power at 0dBm		2.1		mA

22. SoC Power consumption

VBAT current at 3 V with internally generated IO supply

Parameter	Conditions	Min.	Тур	Max.	Units
Active RX	Sensitivity at -95 dBm 1 mA		1.4		mA
Active TX @ 0 dBm	Output power at 0 dBm		2.5		mA
Active TX @ 4 dBm	Output power at 4 dBm		3.5		mA
Active TX @ 8 dBm	Output power at 8 dBm		TBD		mA
Active TX @ 10 dBm	Output power at 10 dBm		TBD		mA
Active TX @ -10 dBm	Output power at -10 dBm		1.6		mA
CPU Active (16MHz)			1.0		mA
CPU Idle + BLE Deep Sleep			0.5		mA
Retention (32 KB RAM)			1.6		μA
Hibernation			1.1		μA
Hibernation with Harvesting Enabled			1.4		μΑ
Hibernation with Wakeup Receiver			1.4		μΑ
SoC Off with Harvesting Enabled			700		nA
SoC Off			400		nA
Powerdown	PWD pin asserted		100		nA



23. Energy Harvesting

Parameter	Conditions	Min.	Тур	Max.	Units
VHARV	Cold Start Voltage	TBD	0.5	TBD	V
	Steady State Regulated Voltage	0.4		3.3	V
	Input Current @ 3V	1	3.5	10,000	uA
VSTORE	Voltage		3.3		V
HARV_IN	RF Input Level (operation) @915MHz	-18		10	dBm
	RF Input Level (Cold Start) @915MHz	TBD		TBD	dBm
	RF Input Level (operation) @2450MHz	-15		10	dBm
	Frequency Range	400		2500	MHz

24. DRAM Characteristics

Parameter	Conditions	Min.	Тур	Max.	Units
VDDIO		1.62	1.8	3.6	V
Endurance			10K		Cycles
Data Retention			10		Year
Read Cycle (4-bytes)	Current @1.8V		220		uA
	Duration		0.372		us
Write Cycle (4-bytes)	Current @1.8V		3100		uA
	Duration		167.3		us

25. Wakeup Timer

The wakeup timer is a 40-bit timer based on the low-power 32 kHz clock. When this timer is enabled during SoC Off mode, it will determine the SoC off duration

Note: please refer to the software manual

26. Peripherals and I/O

The following peripherals are supported by the SoC.

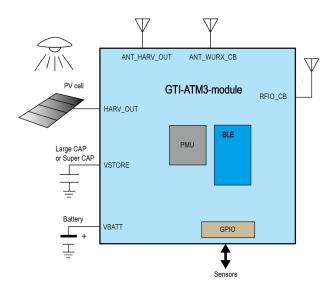
Note: please refer to the software manual for the details

- GPIO
- I2C
- Serial Peripheral Interface (SPI)
- UART
- PDM



27. Energy Harvesting

The GTI-ATM3330e module integrates Bluetooth LE module with advanced energy harvesting and power management to support battery-free and forever battery life.



27.1 Energy Harvesting sources supported

Here is a list of some power sources for GTI-ATM3330e to capture from:

■ RF energy harvesting

The GTI-ATM3330e supports RF sources between 400MHz and 2.5GHz. The preferred frequency bands are the ISM bands at 433MHz, 915MHz, and 2.4GHz. Low frequencies will have less attenuation over the same distance as higher frequencies.

The GTI-ATM3330e module has already been integrated with the 915MHz frequency band matching network which is capable of harvesting RF inputs between -10dBm and +10 dBm, all you need is an external antenna



■ Photovoltaic PV cell energy harvesting

In the case of battery-free design, the PV cell must have an open circuit voltage of 1.65V or higher with at least 30uW of energy to meet the cold start requirement.

Once operating, the PMU regulates the PV input levels between 1.1V and 1.9V.

Actual measured data for a 10cm2 PV cell operating at 320 lux (300-500 lux indoors typical) produces over 100uW at 1.5V is more than enough to support a typical beaconing application.

■ Thermal energy harvesting

Thermal harvesting can be considered anytime if there is an available heat source or air flow generating a temperature gradient.

■ Mechanical energy harvesting

As measured, harvesting the energy from the press and release of a switch button will generate 0.3mJ of energy
The press actuation creates a positive electrical pulse while the release actuation creates a negative pulse. Both pulses are
captured directly from the generator into a storage capacitor attached to VSTORE through a full wave rectifier and Zener diode.
For this type of energy harvesting, it is not necessary to use the HARV_OUT input since the pulse energy is directly captured by
the storage capacitor.

27.2 Energy Harvesting PMU Pins

The PMU manages two harvesting inputs:

- 1. ANT_HARV_CB antenna
- 2. HARV OUT

There are also two separate storage connections:

- 1. VBATT for a battery
- 2. VSTORE for capacitive storage elements

These are the potential energy sources for the PMU to draw from.

While the VBATT is only available as a source to the PMU, the VSTORE is also used by the PMU to store excess energy from the harvesting input.



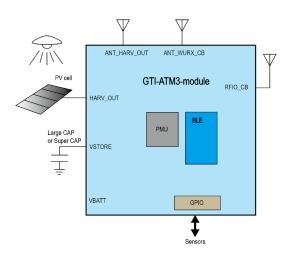
27.3 Energy Storage Options

There are three possible energy storage configurations, battery-free, rechargeable battery, and standard battery.

■ Battery-free

The PMU will rely only on energy harvesting to run the GTI-ATM3330E module and charge a storage capacitor connected to VSTORE when excess energy is available.

If the VSTORE level drops below a threshold sufficient for BLE transmissions, the PMU will shut the CPU down until sufficient energy has been harvested to continue operation.

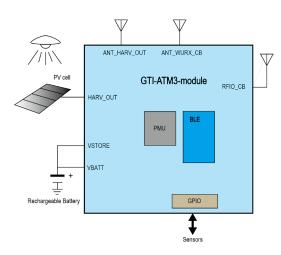




■ Rechargeable Battery

The rechargeable battery is connected to VSTORE through a series resistor for charging when excess harvesting energy is available, and to VBATT directly as the power source when harvesting energy is not immediately available.

The PMU is only able to support single and double-cell rechargeable batteries up to 3.3V. Battery like 4.2V Lithium Ion cannot be supported directly by the GTI-ATM3330E module, additional charging hardware may require.

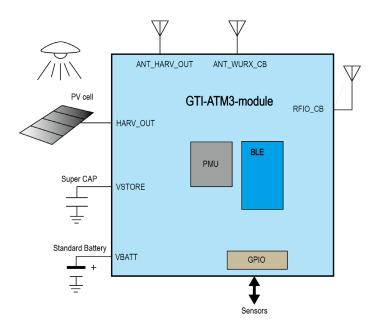


■ Standard Battery

The GTI-ATM3330E module also supports operation from single or dual-cell battery voltage between 1.1V and 3.3V in conjunction with energy harvesting.

When energy harvesting is also applied, the battery is only used when there is insufficient energy available from VSTORE and energy harvesting





27.4 PMU Operation

■ Cold start

In a battery-free configuration, the PMU can cold start if the voltage at HARV_OUT is above 0.5V and the available input power is at least 30uW. The PMU will begin to harvest and direct energy to VSTORE until it reaches its operational threshold.

For configurations that include a battery, the PMU will start without any latency or input power requirement provided a source above 1.1V is available on VBATT, otherwise, the PMU will need some harvested energy to begin operating.

■ Regular Operation

Once started, the PMU will endeavor to meet the power needs of the application while continuing to monitor the levels of VBATT, VSTORE, and HARV_OUT



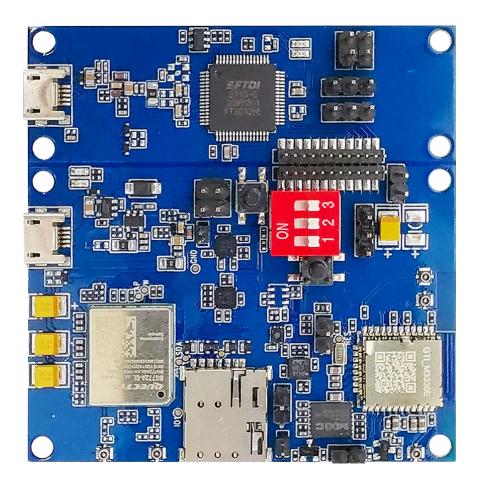
■ Shutdown

The PMU will shutdown the execution of the application when insufficient energy is available across VBATT and VSTORE and HARV_OUT. During this period the PMU will continue to operate and harvest energy until sufficient energy has been restored. If there is not enough harvested energy available at this time, the system may lose power and a cold start would be required again.



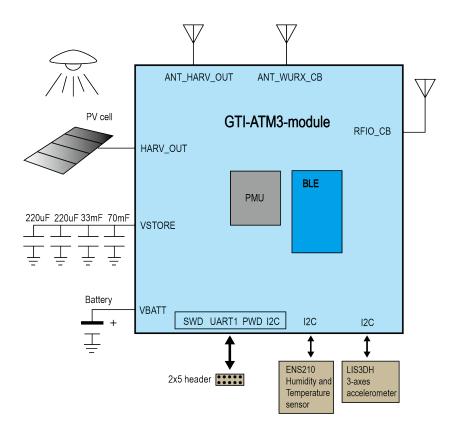
28. Development Board

There is the development board (DVB) for the GTI-ATM3330E module, please contact Globalscale Technologies for more information.





Example of GTI-ATM3330e DVB connection

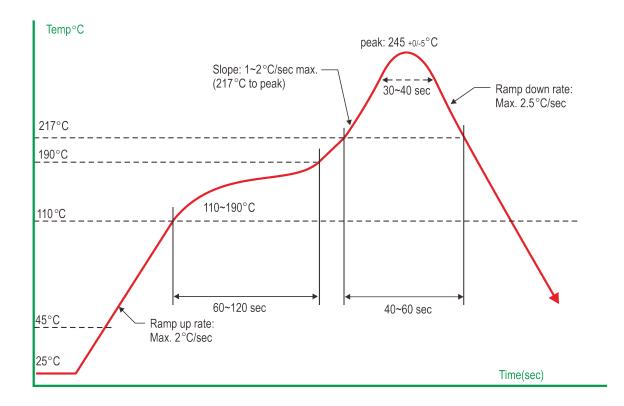




29. Reflow Profile

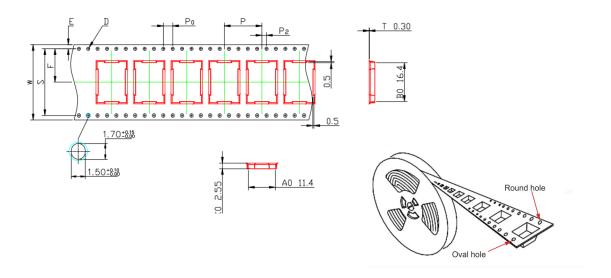
Referred IPC/JEDEC standard. Peak Temperature: < 250 $^{\circ}\,$ C.

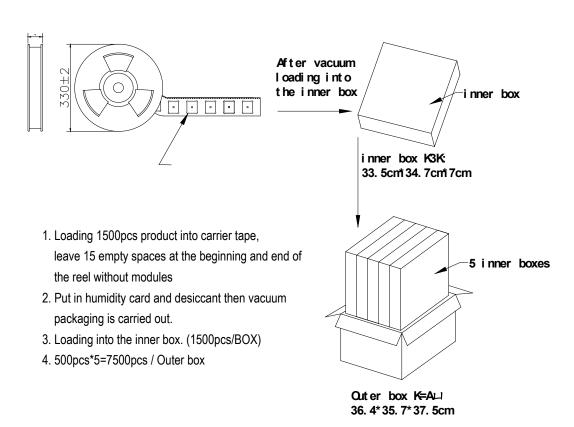
Number of Times: 2





30. Packaging







31. Onboard antenna specification

Parameter	Value	Unit
Central Frequency	2450	MHz
Bandwidth	100 (Min.)	MHz
Return Loss	-10 (Max.)	dB
Peak Gain	3.53	dBi
Impedance	50	Ohm
Maximum Power	4	W
Polarization	Linear	
Azimuth Beamwidth	Omni-directional	



32. FCC and CE compliant

FCC ID:

YCJGTI-3330E

CE RED Certificate:

EN 55032:2015+A11:2020+A1:2020 EN 55035:2017+A11:2020 ENI EC 61000-3-2:2019+A1:2021 EN 61000-3-3:2013+A1:2019+A2:2021



33. FCC Warning

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: —Reorient or relocate the receiving antenna. — Increase the separation between the equipment and receiver. —Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. —Consult the dealer or an experienced radio / TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.



2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C&E has been investigated. It is applicable to the modular.

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

To maintain compliance with FCC's RF Exposure guidelines, This equipment should be installed and operated with minimum distance of 20cm from your body. Additional RF exposure statement: the modular transmitter must comply with any applicable RF exposure requirements (as defined §2.1091 and §2.1093,) in its final configuration, per KDB996369 D03.

2.7 Antennas

This radio transmitter FCC ID:YCJGTI-3330E has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Antenna type	Input impedance (Ohm)	Maximum antenna gain
Chip	50	3.53dBi/2402MHZ-2480Hz

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID:YCJGTI-3330E

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

The OEM integrator or the host manufacturer is responsible for the overall compliance of the host products, the module grantees to ensure that proper test data for multiple transmitter operations are included in the application filings for the modules.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part $15~\mathrm{B}$



34. Contact information

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