

The S-82D1A Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes temperature protection circuits, high-accuracy voltage detection circuits, and delay circuits. Temperature protection is possible by connecting an NTC thermistor to the dedicated connection pin. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.

## ■ Features

- High-accuracy temperature protection circuit by an external NTC thermistor
 

High temperature charge-discharge inhibition temperature	+40°C to +85°C (1°C step)	Accuracy ±3°C <sup>*1</sup>
High temperature charge inhibition temperature	+40°C to +85°C (1°C step)	Accuracy ±3°C <sup>*1</sup>
Low temperature charge inhibition temperature	−40°C to +10°C (1°C step)	Accuracy ±3°C <sup>*1</sup>
Low temperature charge-discharge inhibition temperature	−40°C to +10°C (1°C step)	Accuracy ±3°C <sup>*1</sup>
- High-accuracy voltage detection circuit
 

Overcharge detection voltage	3.500 V to 4.600 V (5 mV step)	Accuracy ±15 mV
Overcharge release voltage	3.100 V to 4.600 V <sup>*2</sup>	Accuracy ±50 mV
Overdischarge detection voltage	2.000 V to 3.000 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.000 V to 3.400 V <sup>*3</sup>	Accuracy ±75 mV
Discharge overcurrent detection voltage 1	0.003 V to 0.100 V (0.5 mV step)	Accuracy ±1.5 mV
Discharge overcurrent detection voltage 2	0.010 V to 0.100 V (1 mV step)	Accuracy ±3 mV
Load short-circuiting detection voltage	0.020 V to 0.100 V (1 mV step)	Accuracy ±5 mV
Charge overcurrent detection voltage	−0.100 V to −0.003 V (0.5 mV step)	Accuracy ±1.5 mV
- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Charge-discharge control function
 

CTL pin control logic:	Active "H", active "L"
CTL pin internal resistance:	Pull-up, pull-down
CTL pin internal resistance value:	1 MΩ to 5 MΩ (1 MΩ step)
- Discharge overcurrent control function
 

Release condition of discharge overcurrent status:	Load disconnection
Release voltage of discharge overcurrent status:	Discharge overcurrent release voltage ( $V_{RIOV}$ ) = $V_{DD} \times 0.8$ (typ.)
- Discharge overcurrent status reset function by CTL pin: Available, unavailable
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- High-withstand voltage: VM pin and CO pin: Absolute maximum rating 28.0 V
- Wide operation temperature range:  $T_a = -40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Low current consumption
 

During operation:	2.5 μA typ., 5.0 μA max. ( $T_a = +25^\circ\text{C}$ )
During power-down:	100 nA max. ( $T_a = +25^\circ\text{C}$ )
During overdischarge:	0.5 μA max. ( $T_a = +25^\circ\text{C}$ )
- Lead-free (Sn 100%), halogen-free

\*1. Temperature detection accuracy varies with NTC thermistor specifications.

When an NTC thermistor listed in **Table 6** is connected, the detection temperature and accuracy can be achieved.

\*2. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)

\*3. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

## ■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

## ■ Package

- HSNT-8(1616)

■ **Block Diagram**

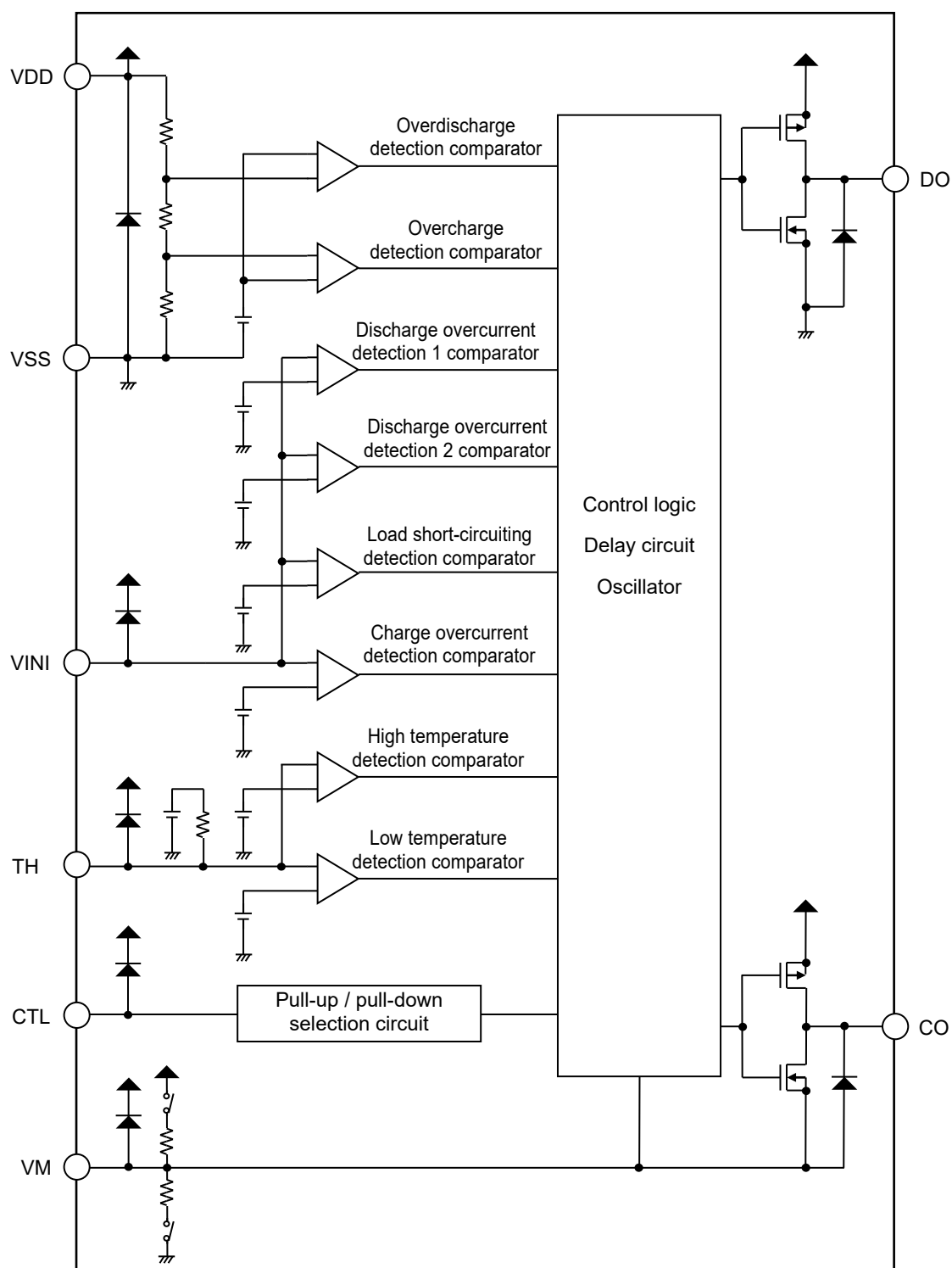
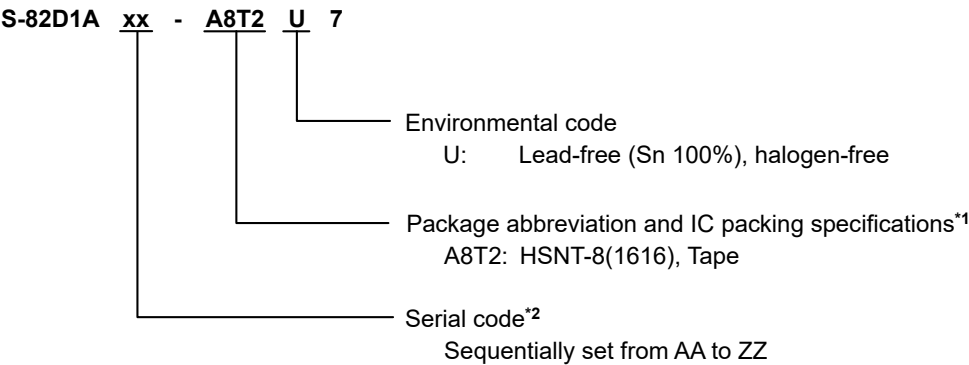


Figure 1

■ **Product Name Structure**

**1. Product name**



\*1. Refer to the tape drawing.  
\*2. Refer to "3. Product name list".

**2. Package**

**Table 1 Package Drawing Codes**

Package Name	Dimension	Tape	Reel	Land
HSNT-8(1616)	PY008-A-P-SD	PY008-A-C-SD	PY008-A-R-SD	PY008-A-L-SD

### 3. Product name list

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage [V <sub>CU</sub> ]	Overcharge Release Voltage [V <sub>CL</sub> ]	Overdischarge Detection Voltage [V <sub>DL</sub> ]	Overdischarge Release Voltage [V <sub>DU</sub> ]	Discharge Overcurrent Detection Voltage 1 [V <sub>DIOV1</sub> ]	Discharge Overcurrent Detection Voltage 2 [V <sub>DIOV2</sub> ]	Load Short- circuiting Detection Voltage [V <sub>SHORT</sub> ]	Charge Overcurrent Detection Voltage [V <sub>CIOV</sub> ]
S-82D1AAA-A8T2U7	4.475 V	4.275 V	2.500 V	2.900 V	0.0150 V	–	0.040 V	–0.0150 V
S-82D1AAB-A8T2U7	4.425 V	4.225 V	2.300 V	2.500 V	0.0105 V	0.015 V	0.030 V	–0.0105 V
S-82D1AAD-A8T2U7	4.280 V	4.080 V	3.000 V	3.400 V	0.0300 V	–	0.050 V	–0.0300 V
S-82D1AAE-A8T2U7	4.500 V	4.300 V	2.500 V	2.900 V	0.0270 V	–	0.054 V	–0.0210 V
S-82D1AAI-A8T2U7	4.250 V	4.250 V	2.800 V	3.000 V	0.0150 V	–	0.040 V	–0.0150 V
S-82D1AAJ-A8T2U7	4.400 V	4.400 V	2.800 V	3.000 V	0.0150 V	–	0.040 V	–0.0150 V
S-82D1AAK-A8T2U7	4.450 V	4.450 V	2.800 V	3.000 V	0.0150 V	–	0.040 V	–0.0150 V
S-82D1AAL-A8T2U7	4.500 V	4.500 V	2.800 V	3.000 V	0.0150 V	–	0.040 V	–0.0150 V
S-82D1AAM-A8T2U7	4.260 V	4.260 V	3.120 V	3.320 V	0.0480 V	0.060 V	0.090 V	–0.0380 V
S-82D1AAN-A8T2U7	4.550 V	4.350 V	2.000 V	2.100 V	0.0500 V	–	0.100 V	–0.0500 V
S-82D1AAO-A8T2U7	4.250 V	4.150 V	2.800 V	3.000 V	0.0200 V	–	0.040 V	–0.1000 V
S-82D1AAP-A8T2U7	4.100 V	3.700 V	2.800 V	3.000 V	0.0400 V	–	0.100 V	–0.0120 V
S-82D1AAQ-A8T2U7	4.180 V	3.980 V	2.480 V	2.880 V	0.0250 V	–	0.060 V	–0.0050 V

Table 2 (2 / 2)

Product Name	Delay Time Combination*1	CTL Pin Combination*2	0 V Battery Charge*3	Power-down Function*4
S-82D1AAA-A8T2U7	(1)	(1)	Inhibited	Unavailable
S-82D1AAB-A8T2U7	(2)	(1)	Enabled	Unavailable
S-82D1AAD-A8T2U7	(1)	(1)	Enabled	Available
S-82D1AAE-A8T2U7	(1)	(1)	Inhibited	Unavailable
S-82D1AAI-A8T2U7	(6)	(1)	Enabled	Available
S-82D1AAJ-A8T2U7	(6)	(1)	Enabled	Available
S-82D1AAK-A8T2U7	(6)	(1)	Enabled	Available
S-82D1AAL-A8T2U7	(6)	(1)	Enabled	Available
S-82D1AAM-A8T2U7	(5)	(2)	Inhibited	Available
S-82D1AAN-A8T2U7	(3)	(1)	Enabled	Unavailable
S-82D1AAO-A8T2U7	(7)	(1)	Inhibited	Available
S-82D1AAP-A8T2U7	(8)	(1)	Inhibited	Available
S-82D1AAQ-A8T2U7	(9)	(3)	Enabled	Available

\*1. Refer to **Table 3** about the details of the delay time combinations.

\*2. Refer to **Table 5** about the details of the CTL pin combinations.

\*3. 0 V battery charge: Enabled, inhibited

\*4. Power-down function: Available, unavailable

**Remark** Please contact our sales representatives for products other than the above.

# BATTERY PROTECTION IC WITH TEMPERATURE PROTECTION FUNCTION FOR 1-CELL PACK

Rev.1.2\_00

S-82D1A Series

Table 3

Delay Time Combination	Overcharge Detection Delay Time [t <sub>CU</sub> ]	Overdischarge Detection Delay Time [t <sub>DL</sub> ]	Discharge Overcurrent Detection Delay Time 1 [t <sub>DIOV1</sub> ]	Discharge Overcurrent Detection Delay Time 2 [t <sub>DIOV2</sub> ]	Load Short-circuiting Detection Delay Time [t <sub>SHORT</sub> ]	Charge Overcurrent Detection Delay Time [t <sub>CIOV</sub> ]	Charge-discharge Inhibition Delay Time [t <sub>CTL</sub> ]
(1)	1.0 s	64 ms	32 ms	–	280 μs	16 ms	48 ms
(2)	1.0 s	64 ms	3750 ms	16 ms	280 μs	16 ms	48 ms
(3)	1.0 s	128 ms	1.0 s	–	530 μs	128 ms	64 ms
(4)	256 ms	64 ms	32 ms	–	280 μs	16 ms	48 ms
(5)	1.0 s	128 ms	512 ms	128 ms	530 μs	128 ms	32 ms
(6)	1.0 s	128 ms	16 ms	–	280 μs	16 ms	48 ms
(7)	1.0 s	128 ms	8 ms	–	280 μs	8 ms	32 ms
(8)	1.0 s	64 ms	64 ms	–	280 μs	8 ms	48 ms
(9)	1.0 s	128 ms	128 ms	–	280 μs	16 ms	48 ms

**Remark** The delay times can be changed within the range listed in Table 4. For details, please contact our sales representatives.

Table 4

Delay Time	Symbol	Selection Range						Remark
Overcharge detection delay time	t <sub>CU</sub>	256 ms	512 ms	1.0 s	–	–	–	Select a value from the left.
Overdischarge detection delay time	t <sub>DL</sub>	32 ms	64 ms	128 ms	–	–	–	Select a value from the left.
Discharge overcurrent detection delay time 1	t <sub>DIOV1</sub>	8 ms	16 ms	32 ms	64 ms	128 ms	256 ms	Select a value from the left.
		512 ms	1.0 s	2.0 s	3.0 s	3.75 s	4.0 s	
Discharge overcurrent detection delay time 2	t <sub>DIOV2</sub>	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Load short-circuiting detection delay time	t <sub>SHORT</sub>	280 μs	530 μs	–	–	–	–	Select a value from the left.
Charge overcurrent detection delay time	t <sub>CIOV</sub>	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Charge-discharge inhibition delay time	t <sub>CTL</sub>	2 ms	4 ms	48 ms	64 ms	128 ms	256 ms	Select a value from the left.

Table 5

CTL Pin Combination	Control Logic*1	Internal Resistance*2	Internal Resistance Value*3 [R <sub>CTL</sub> ]	CTL Pin Voltage "H"*4 [V <sub>CTLH</sub> ]	CTL Pin Voltage "L"*5 [V <sub>CTL</sub> ]
(1)	Active "H"	Pull-down	5.0 MΩ	V <sub>DD</sub> – 0.9 V	V <sub>SS</sub> + 0.6 V
(2)	Active "L"	Pull-up	10.0 MΩ	V <sub>DD</sub> – 0.9 V	V <sub>SS</sub> + 0.6 V
(3)	Active "L"	Pull-up	5.0 MΩ	V <sub>DD</sub> – 0.9 V	V <sub>SS</sub> + 0.6 V

\*1. CTL pin control logic: Active "H", active "L"

\*2. CTL pin internal resistance: Pull-up, pull-down

\*3. CTL pin internal resistance value: 1 MΩ to 5 MΩ (1 MΩ step)

\*4. CTL pin voltage "H": V<sub>SS</sub> + 0.65 V, V<sub>DD</sub> – 0.9 V

\*5. CTL pin voltage "L": V<sub>SS</sub> + 0.60 V, V<sub>DD</sub> – 0.9 V

**Remark** Please contact our sales representatives for products with CTL pin combinations other than the above.

# BATTERY PROTECTION IC WITH TEMPERATURE PROTECTION FUNCTION FOR 1-CELL PACK

## S-82D1A Series

Rev.1.2\_00

**Table 6**

Product Name	High Temperature Charge-discharge Inhibition Temperature [THCD]	High Temperature Charge Inhibition Temperature [THC]	Low Temperature Charge Inhibition Temperature [TLC]	Low Temperature Charge-discharge Inhibition Temperature [TLCD]	Hysteresis Temperature* 1 [THYS]	Sampling Wait Time* 2 [TSLEEP]	Continuous Detection / Release Count* 3 [N]	Resistance* 4 [RNTC]	B-value* 4 [B]
S-82D1AAA-A8T2U7	–	63°C	–3°C	–	5°C	512 ms	2	100 kΩ ± 1%	4250 K ± 1%
S-82D1AAB-A8T2U7	82°C	63°C	–3°C	–37°C	10°C	512 ms	2	100 kΩ ± 1%	4250 K ± 1%
S-82D1AAD-A8T2U7	42°C	–	–	–7°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%
S-82D1AAE-A8T2U7	60°C	45°C	0°C	–20°C	5°C	512 ms	2	100 kΩ ± 1%	4250 K ± 1%
S-82D1AAI-A8T2U7	60°C	45°C	0°C	–20°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%
S-82D1AAJ-A8T2U7	60°C	45°C	0°C	–20°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%
S-82D1AAK-A8T2U7	60°C	45°C	0°C	–20°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%
S-82D1AAL-A8T2U7	60°C	45°C	0°C	–20°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%
S-82D1AAM-A8T2U7	43°C	–	–	2°C	5°C	512 ms	2	100 kΩ ± 1%	4250 K ± 1%
S-82D1AAN-A8T2U7	82°C	49°C	–3°C	–37°C	5°C	1.0 s	5	100 kΩ ± 1%	4250 K ± 1%
S-82D1AAO-A8T2U7	65°C	50°C	–5°C	–25°C	5°C	512 ms	2	100 kΩ ± 1%	4250 K ± 1%
S-82D1AAP-A8T2U7	60°C	50°C	0°C	–20°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%
S-82D1AAQ-A8T2U7	75°C	–	–	–35°C	5°C	512 ms	2	10 kΩ ± 1%	3380 K ± 1%

\*1. Hysteresis Temperature: 5°C, 10°C

\*2. Sampling wait time: 256 ms, 512 ms, 1.0 s

\*3. Continuous detection / release count: 1, 2, 3, 4, 5, 6

\*4. Temperature detection accuracy varies with NTC thermistor specifications.

When an NTC thermistor listed in **Table 6** is connected, the detection temperature and accuracy can be achieved.

## ■ Pin Configuration

### 1. HSNT-8(1616)

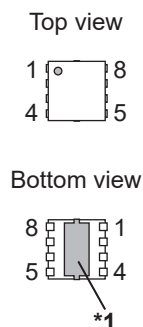


Figure 2

Table 7

Pin No.	Symbol	Description
1	CTL	Input pin for charge-discharge control signal
2	VM	Input pin for external negative voltage
3	CO	Connection pin of charge control FET gate (CMOS output)
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	VSS	Input pin for negative power supply
6	VDD	Input pin for positive power supply
7	VINI	Overcurrent detection pin
8	TH	Thermistor connection pin

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential open or  $V_{DD}$ . However, do not use it as the function of electrode.

## ■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V <sub>DS</sub>	VDD	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 6.0	V
VINI pin input voltage	V <sub>VINI</sub>	VINI	V <sub>DD</sub> – 6.0 to V <sub>DD</sub> + 0.3	V
CTL pin input voltage	V <sub>CTL</sub>	CTL	V <sub>DD</sub> – 6.0 to V <sub>DD</sub> + 0.3	V
VM pin input voltage	V <sub>VM</sub>	VM	V <sub>DD</sub> – 28.0 to V <sub>DD</sub> + 0.3	V
TH pin input voltage	V <sub>TH</sub>	TH	V <sub>DD</sub> – 6.0 to V <sub>DD</sub> + 0.3	V
DO pin output voltage	V <sub>DO</sub>	DO	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
CO pin output voltage	V <sub>CO</sub>	CO	V <sub>VM</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
Operation ambient temperature	T <sub>opr</sub>	–	–40 to +85	°C
Storage temperature	T <sub>stg</sub>	–	–55 to +125	°C

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Thermal Resistance Value

Table 9

Table 5							
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	$\theta_{JA}$	HSNT-8(1616)	Board A	—	214	—	°C/W
			Board B	—	172	—	°C/W
			Board C	—	—	—	°C/W
			Board D	—	—	—	°C/W
			Board E	—	—	—	°C/W

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

# BATTERY PROTECTION IC WITH TEMPERATURE PROTECTION FUNCTION FOR 1-CELL PACK

Rev.1.2\_00

S-82D1A Series

## ■ Electrical Characteristics

1. Ta = +25°C

Table 10

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
<b>Detection Voltage</b>							
Overcharge detection voltage	V <sub>CU</sub>	–	V <sub>CU</sub> – 0.015	V <sub>CU</sub>	V <sub>CU</sub> + 0.015	V	1
Overcharge release voltage	V <sub>CL</sub>	V <sub>CL</sub> ≠ V <sub>CU</sub>	V <sub>CL</sub> – 0.050	V <sub>CL</sub>	V <sub>CL</sub> + 0.050	V	1
		V <sub>CL</sub> = V <sub>CU</sub>	V <sub>CL</sub> – 0.020	V <sub>CL</sub>	V <sub>CL</sub> + 0.015	V	1
Overdischarge detection voltage	V <sub>DL</sub>	–	V <sub>DL</sub> – 0.050	V <sub>DL</sub>	V <sub>DL</sub> + 0.050	V	1
Overdischarge release voltage	V <sub>DU</sub>	V <sub>DL</sub> ≠ V <sub>DU</sub>	V <sub>DU</sub> – 0.075	V <sub>DU</sub>	V <sub>DU</sub> + 0.075	V	2
		V <sub>DL</sub> = V <sub>DU</sub>	V <sub>DU</sub> – 0.050	V <sub>DU</sub>	V <sub>DU</sub> + 0.050	V	2
Discharge overcurrent detection voltage 1	V <sub>DIOV1</sub>	–	V <sub>DIOV1</sub> – 0.0015	V <sub>DIOV1</sub>	V <sub>DIOV1</sub> + 0.0015	V	2
Discharge overcurrent detection voltage 2	V <sub>DIOV2</sub>	–	V <sub>DIOV2</sub> – 0.003	V <sub>DIOV2</sub>	V <sub>DIOV2</sub> + 0.003	V	2
Load short-circuiting detection voltage	V <sub>SHORT</sub>	–	V <sub>SHORT</sub> – 0.005	V <sub>SHORT</sub>	V <sub>SHORT</sub> + 0.005	V	5
Load short-circuiting detection voltage 2	V <sub>SHORT2</sub>	–	V <sub>DD</sub> – 1.2	V <sub>DD</sub> – 0.8	V <sub>DD</sub> – 0.5	V	2
Charge overcurrent detection voltage	V <sub>CIOV</sub>	–	V <sub>CIOV</sub> – 0.0015	V <sub>CIOV</sub>	V <sub>CIOV</sub> + 0.0015	V	2
Discharge overcurrent release voltage	V <sub>RIOV</sub>	V <sub>DD</sub> = 3.4 V	V <sub>DD</sub> × 0.77	V <sub>DD</sub> × 0.80	V <sub>DD</sub> × 0.83	V	2
<b>0 V Battery Charge</b>							
0 V battery charge starting charger voltage	V <sub>0CHA</sub>	0 V battery charge enabled	0.7	1.1	1.5	V	4
0 V battery charge inhibition battery voltage	V <sub>0INH</sub>	0 V battery charge inhibited	0.9	1.2	1.5	V	2
<b>Internal Resistance</b>							
Resistance between VDD pin and VM pin	R <sub>VMD</sub>	V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V	500	1250	2500	kΩ	3
Resistance between VM pin and VSS pin	R <sub>VMS</sub>	V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 1.0 V	5	10	15	kΩ	3
CTL pin internal resistance	R <sub>CTL</sub>	–	R <sub>CTL</sub> × 0.5	R <sub>CTL</sub>	R <sub>CTL</sub> × 2.0	MΩ	3
<b>Input Voltage</b>							
Operation voltage between VDD pin and VSS pin	V <sub>DSOP1</sub>	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V <sub>DSOP2</sub>	–	1.5	–	28.0	V	–
CTL pin voltage "H"	V <sub>CTLH</sub>	–	V <sub>CTLH</sub> – 0.2	V <sub>CTLH</sub>	V <sub>CTLH</sub> + 0.2	V	–
CTL pin voltage "L"	V <sub>CTLL</sub>	–	V <sub>CTLL</sub> – 0.2	V <sub>CTLL</sub>	V <sub>CTLL</sub> + 0.2	V	–
<b>Input Current</b>							
Current consumption during operation	I <sub>OPE</sub>	V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 0 V	–	2.5	5.0	μA	3
Current consumption during power-down	I <sub>PDN</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	–	–	0.1	μA	3
Current consumption during overdischarge	I <sub>OPED</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	–	–	0.5	μA	3
<b>Output Resistance</b>							
CO pin resistance "H"	R <sub>COH</sub>	–	5	10	20	kΩ	4
CO pin resistance "L"	R <sub>COL</sub>	–	5	10	20	kΩ	4
DO pin resistance "H"	R <sub>DOH</sub>	–	5	10	20	kΩ	4
DO pin resistance "L"	R <sub>DOL</sub>	–	1	2	4	kΩ	4
<b>Delay Time</b>							
Overcharge detection delay time	t <sub>CU</sub>	–	t <sub>CU</sub> × 0.7	t <sub>CU</sub>	t <sub>CU</sub> × 1.3	–	5
Overdischarge detection delay time	t <sub>DL</sub>	–	t <sub>DL</sub> × 0.7	t <sub>DL</sub>	t <sub>DL</sub> × 1.3	–	5
Discharge overcurrent detection delay time 1	t <sub>DIOV1</sub>	–	t <sub>DIOV1</sub> × 0.75	t <sub>DIOV1</sub>	t <sub>DIOV1</sub> × 1.25	–	5
Discharge overcurrent detection delay time 2	t <sub>DIOV2</sub>	–	t <sub>DIOV2</sub> × 0.7	t <sub>DIOV2</sub>	t <sub>DIOV2</sub> × 1.3	–	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	–	t <sub>SHORT</sub> × 0.7	t <sub>SHORT</sub>	t <sub>SHORT</sub> × 1.3	–	5
Charge overcurrent detection delay time	t <sub>CIOV</sub>	–	t <sub>CIOV</sub> × 0.7	t <sub>CIOV</sub>	t <sub>CIOV</sub> × 1.3	–	5
Charge-discharge inhibition delay time	t <sub>CTL</sub>	–	t <sub>CTL</sub> × 0.7	t <sub>CTL</sub>	t <sub>CTL</sub> × 1.3	–	5
Sampling wait time	t <sub>SLEEP</sub>	–	t <sub>SLEEP</sub> × 0.7	t <sub>SLEEP</sub>	t <sub>SLEEP</sub> × 1.3	–	6

# BATTERY PROTECTION IC WITH TEMPERATURE PROTECTION FUNCTION FOR 1-CELL PACK

## S-82D1A Series

Rev.1.2\_00

2. Ta = -20°C to +60°C\*1

Table 11

(Ta = -20°C to +60°C\*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
<b>Detection Voltage</b>							
Overcharge detection voltage	V <sub>CU</sub>	—	V <sub>CU</sub> - 0.020	V <sub>CU</sub>	V <sub>CU</sub> + 0.020	V	1
Overcharge release voltage	V <sub>CL</sub>	V <sub>CL</sub> ≠ V <sub>CU</sub>	V <sub>CL</sub> - 0.065	V <sub>CL</sub>	V <sub>CL</sub> + 0.057	V	1
		V <sub>CL</sub> = V <sub>CU</sub>	V <sub>CL</sub> - 0.025	V <sub>CL</sub>	V <sub>CL</sub> + 0.020	V	1
Overdischarge detection voltage	V <sub>DL</sub>	—	V <sub>DL</sub> - 0.060	V <sub>DL</sub>	V <sub>DL</sub> + 0.055	V	1
Overdischarge release voltage	V <sub>DU</sub>	V <sub>DL</sub> ≠ V <sub>DU</sub>	V <sub>DU</sub> - 0.085	V <sub>DU</sub>	V <sub>DU</sub> + 0.080	V	2
		V <sub>DL</sub> = V <sub>DU</sub>	V <sub>DU</sub> - 0.060	V <sub>DU</sub>	V <sub>DU</sub> + 0.055	V	2
Discharge overcurrent detection voltage 1	V <sub>DIOV1</sub>	—	V <sub>DIOV1</sub> - 0.002	V <sub>DIOV1</sub>	V <sub>DIOV1</sub> + 0.002	V	2
Discharge overcurrent detection voltage 2	V <sub>DIOV2</sub>	—	V <sub>DIOV2</sub> - 0.003	V <sub>DIOV2</sub>	V <sub>DIOV2</sub> + 0.003	V	2
Load short-circuiting detection voltage	V <sub>SHORT</sub>	—	V <sub>SHORT</sub> - 0.005	V <sub>SHORT</sub>	V <sub>SHORT</sub> + 0.005	V	5
Load short-circuiting detection voltage 2	V <sub>SHORT2</sub>	—	V <sub>DD</sub> - 1.4	V <sub>DD</sub> - 0.8	V <sub>DD</sub> - 0.3	V	2
Charge overcurrent detection voltage	V <sub>CIOV</sub>	—	V <sub>CIOV</sub> - 0.002	V <sub>CIOV</sub>	V <sub>CIOV</sub> + 0.002	V	2
Discharge overcurrent release voltage	V <sub>RIOV</sub>	V <sub>DD</sub> = 3.4 V	V <sub>DD</sub> × 0.77	V <sub>DD</sub> × 0.80	V <sub>DD</sub> × 0.83	V	2
<b>0 V Battery Charge</b>							
0 V battery charge starting charger voltage	V <sub>0CHA</sub>	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage	V <sub>0INH</sub>	0 V battery charge inhibited	0.7	1.2	1.7	V	2
<b>Internal Resistance</b>							
Resistance between VDD pin and VM pin	R <sub>VMD</sub>	V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V	250	1250	3500	kΩ	3
Resistance between VM pin and VSS pin	R <sub>VMS</sub>	V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 1.0 V	3.5	10	20	kΩ	3
CTL pin internal resistance	R <sub>CTL</sub>	—	R <sub>CTL</sub> × 0.25	R <sub>CTL</sub>	R <sub>CTL</sub> × 3.0	MΩ	3
<b>Input Voltage</b>							
Operation voltage between VDD pin and VSS pin	V <sub>DSOP1</sub>	—	1.5	—	6.0	V	—
Operation voltage between VDD pin and VM pin	V <sub>DSOP2</sub>	—	1.5	—	28.0	V	—
CTL pin voltage "H"	V <sub>CTLH</sub>	—	V <sub>CTLH</sub> - 0.3	V <sub>CTLH</sub>	V <sub>CTLH</sub> + 0.3	V	—
CTL pin voltage "L"	V <sub>CTLL</sub>	—	V <sub>CTLL</sub> - 0.3	V <sub>CTLL</sub>	V <sub>CTLL</sub> + 0.3	V	—
<b>Input Current</b>							
Current consumption during operation	I <sub>OPE</sub>	V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 0 V	—	2.5	6.0	μA	3
Current consumption during power-down	I <sub>PDN</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	—	—	0.15	μA	3
Current consumption during overdischarge	I <sub>OPED</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	—	—	1.0	μA	3
<b>Output Resistance</b>							
CO pin resistance "H"	R <sub>COH</sub>	—	2.5	10	30	kΩ	4
CO pin resistance "L"	R <sub>COL</sub>	—	2.5	10	30	kΩ	4
DO pin resistance "H"	R <sub>DOH</sub>	—	2.5	10	30	kΩ	4
DO pin resistance "L"	R <sub>DOL</sub>	—	0.5	2	6	kΩ	4
<b>Delay Time</b>							
Overcharge detection delay time	t <sub>CU</sub>	—	t <sub>CU</sub> × 0.6	t <sub>CU</sub>	t <sub>CU</sub> × 1.4	—	5
Overdischarge detection delay time	t <sub>DL</sub>	—	t <sub>DL</sub> × 0.6	t <sub>DL</sub>	t <sub>DL</sub> × 1.4	—	5
Discharge overcurrent detection delay time 1	t <sub>DIOV1</sub>	—	t <sub>DIOV1</sub> × 0.65	t <sub>DIOV1</sub>	t <sub>DIOV1</sub> × 1.35	—	5
Discharge overcurrent detection delay time 2	t <sub>DIOV2</sub>	—	t <sub>DIOV2</sub> × 0.6	t <sub>DIOV2</sub>	t <sub>DIOV2</sub> × 1.4	—	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	—	t <sub>SHORT</sub> × 0.6	t <sub>SHORT</sub>	t <sub>SHORT</sub> × 1.4	—	5
Charge overcurrent detection delay time	t <sub>CIOV</sub>	—	t <sub>CIOV</sub> × 0.6	t <sub>CIOV</sub>	t <sub>CIOV</sub> × 1.4	—	5
Charge-discharge inhibition delay time	t <sub>CTL</sub>	—	t <sub>CTL</sub> × 0.6	t <sub>CTL</sub>	t <sub>CTL</sub> × 1.4	—	5
Sampling wait time	t <sub>SLEEP</sub>	—	t <sub>SLEEP</sub> × 0.6	t <sub>SLEEP</sub>	t <sub>SLEEP</sub> × 1.4	—	6

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

**BATTERY PROTECTION IC WITH TEMPERATURE PROTECTION FUNCTION FOR 1-CELL PACK**  
**Rev.1.2\_00** **S-82D1A Series**

**3. Ta = -40°C to +85°C\***

**Table 12**

(Ta = -40°C to +85°C\* unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
<b>Detection Voltage</b>							
Overcharge detection voltage	V <sub>CU</sub>	—	V <sub>CU</sub> - 0.045	V <sub>CU</sub>	V <sub>CU</sub> + 0.030	V	1
Overcharge release voltage	V <sub>CL</sub>	V <sub>CL</sub> ≠ V <sub>CU</sub>	V <sub>CL</sub> - 0.080	V <sub>CL</sub>	V <sub>CL</sub> + 0.060	V	1
		V <sub>CL</sub> = V <sub>CU</sub>	V <sub>CL</sub> - 0.050	V <sub>CL</sub>	V <sub>CL</sub> + 0.030	V	1
Overdischarge detection voltage	V <sub>DL</sub>	—	V <sub>DL</sub> - 0.080	V <sub>DL</sub>	V <sub>DL</sub> + 0.060	V	1
Overdischarge release voltage	V <sub>DU</sub>	V <sub>DL</sub> ≠ V <sub>DU</sub>	V <sub>DU</sub> - 0.105	V <sub>DU</sub>	V <sub>DU</sub> + 0.085	V	2
		V <sub>DL</sub> = V <sub>DU</sub>	V <sub>DU</sub> - 0.080	V <sub>DU</sub>	V <sub>DU</sub> + 0.060	V	2
Discharge overcurrent detection voltage 1	V <sub>DIOV1</sub>	—	V <sub>DIOV1</sub> - 0.002	V <sub>DIOV1</sub>	V <sub>DIOV1</sub> + 0.002	V	2
Discharge overcurrent detection voltage 2	V <sub>DIOV2</sub>	—	V <sub>DIOV2</sub> - 0.003	V <sub>DIOV2</sub>	V <sub>DIOV2</sub> + 0.003	V	2
Load short-circuiting detection voltage	V <sub>SHORT</sub>	—	V <sub>SHORT</sub> - 0.005	V <sub>SHORT</sub>	V <sub>SHORT</sub> + 0.005	V	5
Load short-circuiting detection voltage 2	V <sub>SHORT2</sub>	—	V <sub>DD</sub> - 1.4	V <sub>DD</sub> - 0.8	V <sub>DD</sub> - 0.3	V	2
Charge overcurrent detection voltage	V <sub>CIOV</sub>	—	V <sub>CIOV</sub> - 0.002	V <sub>CIOV</sub>	V <sub>CIOV</sub> + 0.002	V	2
Discharge overcurrent release voltage	V <sub>RIOV</sub>	V <sub>DD</sub> = 3.4 V	V <sub>DD</sub> × 0.77	V <sub>DD</sub> × 0.80	V <sub>DD</sub> × 0.83	V	2
<b>0 V Battery Charge</b>							
0 V battery charge starting charger voltage	V <sub>0CHA</sub>	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage	V <sub>0INH</sub>	0 V battery charge inhibited	0.7	1.2	1.7	V	2
<b>Internal Resistance</b>							
Resistance between VDD pin and VM pin	R <sub>VMD</sub>	V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V	250	1250	3500	kΩ	3
Resistance between VM pin and VSS pin	R <sub>VMS</sub>	V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 1.0 V	3.5	10	20	kΩ	3
CTL pin internal resistance	R <sub>CTL</sub>	—	R <sub>CTL</sub> × 0.25	R <sub>CTL</sub>	R <sub>CTL</sub> × 3.0	MΩ	3
<b>Input Voltage</b>							
Operation voltage between VDD pin and VSS pin	V <sub>DSOP1</sub>	—	1.5	—	6.0	V	—
Operation voltage between VDD pin and VM pin	V <sub>DSOP2</sub>	—	1.5	—	28.0	V	—
CTL pin voltage "H"	V <sub>CTLH</sub>	—	V <sub>CTLH</sub> - 0.3	V <sub>CTLH</sub>	V <sub>CTLH</sub> + 0.3	V	—
CTL pin voltage "L"	V <sub>CTLL</sub>	—	V <sub>CTLL</sub> - 0.3	V <sub>CTLL</sub>	V <sub>CTLL</sub> + 0.3	V	—
<b>Input Current</b>							
Current consumption during operation	I <sub>OPE</sub>	V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 0 V	—	2.5	6.0	μA	3
Current consumption during power-down	I <sub>PDN</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	—	—	0.15	μA	3
Current consumption during overdischarge	I <sub>OPED</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	—	—	1.0	μA	3
<b>Output Resistance</b>							
CO pin resistance "H"	R <sub>COH</sub>	—	2.5	10	30	kΩ	4
CO pin resistance "L"	R <sub>COL</sub>	—	2.5	10	30	kΩ	4
DO pin resistance "H"	R <sub>DOH</sub>	—	2.5	10	30	kΩ	4
DO pin resistance "L"	R <sub>DOL</sub>	—	0.5	2	6	kΩ	4
<b>Delay Time</b>							
Overcharge detection delay time	t <sub>CU</sub>	—	t <sub>CU</sub> × 0.4	t <sub>CU</sub>	t <sub>CU</sub> × 1.6	—	5
Overdischarge detection delay time	t <sub>DL</sub>	—	t <sub>DL</sub> × 0.4	t <sub>DL</sub>	t <sub>DL</sub> × 1.6	—	5
Discharge overcurrent detection delay time 1	t <sub>DIOV1</sub>	—	t <sub>DIOV1</sub> × 0.4	t <sub>DIOV1</sub>	t <sub>DIOV1</sub> × 1.6	—	5
Discharge overcurrent detection delay time 2	t <sub>DIOV2</sub>	—	t <sub>DIOV2</sub> × 0.4	t <sub>DIOV2</sub>	t <sub>DIOV2</sub> × 1.6	—	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	—	t <sub>SHORT</sub> × 0.4	t <sub>SHORT</sub>	t <sub>SHORT</sub> × 1.6	—	5
Charge overcurrent detection delay time	t <sub>CIOV</sub>	—	t <sub>CIOV</sub> × 0.4	t <sub>CIOV</sub>	t <sub>CIOV</sub> × 1.6	—	5
Charge-discharge inhibition delay time	t <sub>CTL</sub>	—	t <sub>CTL</sub> × 0.4	t <sub>CTL</sub>	t <sub>CTL</sub> × 1.6	—	5
Sampling wait time	t <sub>SLEEP</sub>	—	t <sub>SLEEP</sub> × 0.4	t <sub>SLEEP</sub>	t <sub>SLEEP</sub> × 1.6	—	6

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

**4. High-accuracy temperature protection circuit by an external NTC thermistor**

**Table 13**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
High temperature charge-discharge inhibition temperature	$T_{HCD}$	—	$T_{HCD} - 3$	$T_{HCD}$	$T_{HCD} + 3$	°C	6
High temperature charge inhibition temperature	$T_{HC}$	—	$T_{HC} - 3$	$T_{HC}$	$T_{HC} + 3$	°C	6
Low temperature charge inhibition temperature	$T_{LC}$	—	$T_{LC} - 3$	$T_{LC}$	$T_{LC} + 3$	°C	6
Low temperature charge-discharge inhibition temperature	$T_{LCD}$	—	$T_{LCD} - 3$	$T_{LCD}$	$T_{LCD} + 3$	°C	6
Hysteresis temperature	$T_{HYS}$	—	$T_{HYS} - 2$	$T_{HYS}$	$T_{HYS} + 2$	°C	6
Continuous detection / release count	N	—	—	N	—	—	6

## ■ Test Circuits

When CTL pin control logic is active "H", SW1 and SW3 are turned off, SW2 and SW4 are turned on. When CTL pin control logic is active "L", SW1 and SW3 are turned on, SW2 and SW4 are turned off.

For R5 in "Figure 8 Test Circuit 6", make sure to use a resistor with the same resistance as  $R_{NTC}$  in Table 6.

**Caution** Unless otherwise specified, the output voltage levels "H" and "L" at CO pin ( $V_{CO}$ ) and DO pin ( $V_{DO}$ ) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to  $V_{VM}$  and the DO pin level with respect to  $V_{SS}$ .

### 1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage ( $V_{CU}$ ) is defined as the voltage  $V_1$  at which  $V_{CO}$  goes from "H" to "L" when the voltage  $V_1$  is gradually increased after setting  $V_1 = 3.4$  V,  $V_7 = 0.25$  V. Overcharge release voltage ( $V_{CL}$ ) is defined as the voltage  $V_1$  at which  $V_{CO}$  goes from "L" to "H" when the voltage  $V_1$  is then gradually decreased. Overcharge hysteresis voltage ( $V_{HC}$ ) is defined as the difference between  $V_{CU}$  and  $V_{CL}$ .

### 2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage ( $V_{DL}$ ) is defined as the voltage  $V_1$  at which  $V_{DO}$  goes from "H" to "L" when the voltage  $V_1$  is gradually decreased after setting  $V_1 = 3.4$  V,  $V_2 = V_5 = V_6 = 0$  V,  $V_7 = 0.25$  V. Overdischarge release voltage ( $V_{DU}$ ) is defined as the voltage  $V_1$  at which  $V_{DO}$  goes from "L" to "H" when setting  $V_2 = 0.01$  V,  $V_5 = V_6 = 0$  V and when the voltage  $V_1$  is then gradually increased. Overdischarge hysteresis voltage ( $V_{HD}$ ) is defined as the difference between  $V_{DU}$  and  $V_{DL}$ .

### 3. Discharge overcurrent detection voltage 1, discharge overcurrent release voltage (Test circuit 5)

Discharge overcurrent detection voltage 1 ( $V_{DIOV1}$ ) is defined as the voltage  $V_5$  whose delay time for changing  $V_{DO}$  from "H" to "L" is discharge overcurrent detection delay time 1 ( $t_{DIOV1}$ ) when the voltage  $V_5$  is increased after setting  $V_1 = 3.4$  V,  $V_2 = 1.4$  V,  $V_5 = V_6 = 0$  V,  $V_7 = 0.25$  V. Discharge overcurrent release voltage ( $V_{RIOV}$ ) is defined as the voltage  $V_2$  at which  $V_{DO}$  goes from "L" to "H" when setting  $V_2 = 3.4$  V,  $V_5 = 0$  V and when the voltage  $V_2$  is then gradually decreased.

When the voltage  $V_2$  falls below  $V_{RIOV}$ ,  $V_{DO}$  will go to "H" after 1.0 ms typ. and maintain "H" during load short-circuiting detection delay time ( $t_{SHORT}$ ).

### 4. Discharge overcurrent detection voltage 2 (Test circuit 2)

Discharge overcurrent detection voltage 2 ( $V_{DIOV2}$ ) is defined as the voltage  $V_5$  whose delay time for changing  $V_{DO}$  from "H" to "L" is discharge overcurrent detection delay time 2 ( $t_{DIOV2}$ ) when the voltage  $V_5$  is increased after setting  $V_1 = 3.4$  V,  $V_2 = 1.4$  V,  $V_5 = V_6 = 0$  V,  $V_7 = 0.25$  V.

### 5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage ( $V_{SHORT}$ ) is defined as the voltage  $V_5$  whose delay time for changing  $V_{DO}$  from "H" to "L" is  $t_{SHORT}$  when the voltage  $V_5$  is increased after setting  $V_1 = 3.4$  V,  $V_2 = 1.4$  V,  $V_5 = V_6 = 0$  V,  $V_7 = 0.25$  V.

### 6. Load short-circuiting detection voltage 2 (Test circuit 2)

Load short-circuiting detection voltage 2 ( $V_{SHORT2}$ ) is defined as the voltage  $V_2$  whose delay time for changing  $V_{DO}$  from "H" to "L" is  $t_{SHORT}$  when the voltage  $V_2$  is increased after setting  $V_1 = 3.4$  V,  $V_2 = V_5 = V_6 = 0$  V,  $V_7 = 0.25$  V.

**7. Charge overcurrent detection voltage**  
**(Test circuit 2)**

Charge overcurrent detection voltage ( $V_{CIOV}$ ) is defined as the voltage  $V_5$  whose delay time for changing  $V_{CO}$  from "H" to "L" is charge overcurrent detection delay time ( $t_{CIOV}$ ) when the voltage  $V_5$  is decreased after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**8. CTL pin voltage "H", CTL pin voltage "L"**  
**(Test circuit 2)**

**8. 1 CTL pin control logic active "H"**

The CTL pin voltage "H" ( $V_{CTLH}$ ) is defined as the voltage  $V_6$  at which  $V_{CO}$  and  $V_{DO}$  go from "H" to "L" when the voltage  $V_6$  is gradually increased after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

After that, the CTL pin voltage "L" ( $V_{CTLL}$ ) is defined as the voltage  $V_6$  at which  $V_{CO}$  and  $V_{DO}$  go from "L" to "H" after  $V_6$  is gradually decreased.

**8. 2 CTL pin control logic active "L"**

$V_{CTLL}$  is defined as the voltage difference between the voltage  $V_6$  and the voltage  $V_1$ ,  $V_1 - V_6$ , at which  $V_{CO}$  and  $V_{DO}$  go from "H" to "L" when the voltage  $V_6$  is gradually increased after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ . After that,  $V_{CTLH}$  is defined as  $V_1 - V_6$  at which  $V_{CO}$  and  $V_{DO}$  go from "L" to "H" after  $V_6$  is gradually decreased.

**9. High-accuracy temperature protection circuit by an external NTC thermistor  
(Test circuit 6)**

**9.1 High temperature charge-discharge inhibition temperature, high temperature charge-discharge inhibition release temperature**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ ,  $R5 = R_{NTC} [\text{k}\Omega]$ , and setting SW7 to off, R5 is gradually decreased. R5 is assigned to equation (1) when  $V_{CO}$  and  $V_{DO}$  go from "H" to "L". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as high temperature charge-discharge inhibition temperature ( $T_{HCD}$ ). Subsequently, R5 is gradually increased. R5 is assigned to equation (1) when  $V_{CO}$  and  $V_{DO}$  go from "L" to "H". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as high temperature charge-discharge inhibition release temperature ( $T_{RHCD}$ ). The difference between  $T_{HCD}$  and  $T_{RHCD}$  is defined as hysteresis temperature ( $T_{HYS}$ ). When S-82D1A Series has the setting of high temperature charge inhibition temperature ( $T_{HC}$ ) as well, only  $V_{DO}$  is switched as long as the detection temperature of an NTC thermistor is maintained at high temperature charge inhibition release temperature ( $T_{RHC}$ ) or higher.

**9.2 High temperature charge inhibition temperature, high temperature charge inhibition release temperature**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ ,  $R5 = R_{NTC} [\text{k}\Omega]$ , and setting SW7 to off, R5 is gradually decreased. R5 is assigned to equation (1) when  $V_{CO}$  goes from "H" to "L". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as  $T_{HC}$ . Subsequently, R5 is gradually increased. R5 is assigned to equation (1) when  $V_{CO}$  goes from "L" to "H". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as  $T_{RHC}$ . The difference between  $T_{HC}$  and  $T_{RHC}$  is defined as  $T_{HYS}$ .

**9.3 Low temperature charge inhibition temperature, low temperature charge inhibition release temperature**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ ,  $R5 = R_{NTC} [\text{k}\Omega]$ , and setting SW7 to off, R5 is gradually increased. R5 is assigned to equation (1) when  $V_{CO}$  goes from "H" to "L". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as low temperature charge inhibition temperature ( $T_{LC}$ ). Subsequently, R5 is gradually decreased. R5 is assigned to equation (1) when  $V_{CO}$  goes from "L" to "H". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as low temperature charge inhibition release temperature ( $T_{RLC}$ ). The difference between  $T_{RLC}$  and  $T_{LC}$  is defined as  $T_{HYS}$ .

**9.4 Low temperature charge-discharge inhibition temperature, low temperature charge-discharge inhibition release temperature**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ ,  $R5 = R_{NTC} [\text{k}\Omega]$ , and setting SW7 to off, R5 is gradually increased. R5 is assigned to equation (1) when  $V_{CO}$  and  $V_{DO}$  go from "H" to "L". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as low temperature charge-discharge inhibition temperature ( $T_{LCD}$ ). Subsequently, R5 is gradually decreased. R5 is assigned to equation (1) when  $V_{CO}$  and  $V_{DO}$  go from "L" to "H". Temperature  $T [^{\circ}\text{C}]$  obtained from the calculation result is defined as low temperature charge-discharge inhibition release temperature ( $T_{RLCD}$ ). The difference between  $T_{RLCD}$  and  $T_{LCD}$  is defined as  $T_{HYS}$ . When S-82D1A Series has the temperature setting of  $T_{LC}$  as well, only  $V_{DO}$  is switched as long as the detection temperature of an NTC thermistor is maintained at  $T_{RLC}$  or lower.

$$T [^{\circ}\text{C}] = \frac{1}{\frac{1}{B [\text{K}] \times \log_e \frac{R_s [\text{k}\Omega]}{R_{NTC} [\text{k}\Omega]} + \frac{1}{25 [^{\circ}\text{C}] + 273.15}}} - 273.15 \dots\dots\dots (1)$$

$$R_{TDET} [\text{k}\Omega] = R_{NTC} [\text{k}\Omega] \exp \left\{ B [\text{K}] \left( \frac{1}{T_{DET} [^{\circ}\text{C}] + 273.15} - \frac{1}{25 [^{\circ}\text{C}] + 273.15} \right) \right\} \dots\dots\dots (2)$$

**Remark** Refer to **Table 6** for  $R_{NTC} [\text{k}\Omega]$  and  $B [\text{K}]$ .  
Resistance  $R_{TDET} [\text{k}\Omega]$  of an NTC thermistor at  $T_{DET} [^{\circ}\text{C}]$  can be calculated by the equation (2).

**10. Sampling wait time  
(Test circuit 6)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$  and setting SW7 to off, time interval when "L" is output between continuous voltage pulses output from the TH pin ( $V_{TH}$ ) is defined as sampling wait time ( $t_{SLEEP}$ ).

**11. Continuous detection / release count**  
**(Test circuit 6)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ , SW7 is switched from off to on. The number of pulses from the SW7 switching until  $V_{CO}$  goes to "L" is continuous detection / release count (N).

**12. Current consumption during operation**  
**(Test circuit 3)**

The current consumption during operation ( $I_{OPE}$ ) is the current that flows through the VDD pin ( $I_{DD}$ ) under the set conditions of  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ ,  $V7 = 0.25\text{ V}$ . However, the current flowing through the CTL pin internal resistance is excluded.

**13. Current consumption during power-down, current consumption during overdischarge**  
**(Test circuit 3)****13.1 With power-down function**

The current consumption during power-down ( $I_{PDN}$ ) is  $I_{DD}$  under the set conditions of  $V1 = V2 = 1.5\text{ V}$ ,  $V5 = V6 = 0\text{ V}$ ,  $V7 = 0.25\text{ V}$ .

**13.2 Without power-down function**

The current consumption during overdischarge ( $I_{OPED}$ ) is  $I_{DD}$  under the set conditions of  $V1 = V2 = 1.5\text{ V}$ ,  $V5 = V6 = 0\text{ V}$ ,  $V7 = 0.25\text{ V}$ .

**14. Resistance between VDD pin and VM pin**  
**(Test circuit 3)**

$R_{VMD}$  is the resistance between VDD pin and VM pin under the set conditions of  $V1 = 1.8\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ ,  $V7 = 0.25\text{ V}$ .

**15. Resistance between VM pin and VSS pin**  
**(Test circuit 3)**

$R_{VMS}$  is the resistance between VM pin and VSS pin when the voltage  $V5$  is decreased to  $0\text{ V}$  after setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = 1.0\text{ V}$ ,  $V6 = 0\text{ V}$ ,  $V7 = 0.25\text{ V}$ .

**16. CTL pin internal resistance  
(Test circuit 3)****16. 1 CTL pin control logic active "H", CTL pin internal resistance "pull-up"**

The CTL pin internal resistance ( $R_{CTL}$ ) is the resistance between CTL pin and VDD pin under the set conditions of  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**16. 2 CTL pin control logic active "H", CTL pin internal resistance "pull-down"**

$R_{CTL}$  is the resistance between CTL pin and VSS pin under the set conditions of  $V_1 = V_6 = 3.4\text{ V}$ ,  $V_2 = V_5 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**16. 3 CTL pin control logic active "L", CTL pin internal resistance "pull-up"**

$R_{CTL}$  is the resistance between CTL pin and VDD pin under the set conditions of  $V_1 = V_6 = 3.4\text{ V}$ ,  $V_2 = V_5 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**16. 4 CTL pin control logic active "L", CTL pin internal resistance "pull-down"**

$R_{CTL}$  is the resistance between CTL pin and VSS pin under the set conditions of  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**17. CO pin resistance "H"  
(Test circuit 4)**

The CO pin resistance "H" ( $R_{COH}$ ) is the resistance between VDD pin and CO pin under the set conditions of  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = 0\text{ V}$ ,  $V_3 = 3.0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**18. CO pin resistance "L"  
(Test circuit 4)**

The CO pin resistance "L" ( $R_{COL}$ ) is the resistance between VM pin and CO pin under the set conditions of  $V_1 = 4.7\text{ V}$ ,  $V_2 = V_5 = 0\text{ V}$ ,  $V_3 = 0.4\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**19. DO pin resistance "H"  
(Test circuit 4)**

The DO pin resistance "H" ( $R_{DOH}$ ) is the resistance between VDD pin and DO pin under the set conditions of  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = 0\text{ V}$ ,  $V_4 = 3.0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**20. DO pin resistance "L"  
(Test circuit 4)**

The DO pin resistance "L" ( $R_{DOL}$ ) is the resistance between VSS pin and DO pin under the set conditions of  $V_1 = 1.8\text{ V}$ ,  $V_2 = V_5 = 0\text{ V}$ ,  $V_4 = 0.4\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**21. Overcharge detection delay time  
(Test circuit 5)**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_1$  is increased. The time interval from when the voltage  $V_1$  exceeds  $V_{CU}$  until  $V_{CO}$  goes to "L" is the overcharge detection delay time ( $t_{CU}$ ).

**22. Overdischarge detection delay time  
(Test circuit 5)**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_1$  is decreased. The time interval from when the voltage  $V_1$  falls below  $V_{DL}$  until  $V_{DO}$  goes to "L" is the overdischarge detection delay time ( $t_{DL}$ ).

**23. Discharge overcurrent detection delay time 1**  
**(Test circuit 5)**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = 1.4\text{ V}$ ,  $V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_5$  is increased. The time interval from when the voltage  $V_5$  exceeds  $V_{DIOV1}$  until  $V_{DO}$  goes to "L" is the discharge overcurrent detection delay time 1 ( $t_{DIOV1}$ ).

**24. Discharge overcurrent detection delay time 2**  
**(Test circuit 5)**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = 1.4\text{ V}$ ,  $V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_5$  is increased. The time interval from when the voltage  $V_5$  exceeds  $V_{DIOV2}$  until  $V_{DO}$  goes to "L" is the discharge overcurrent detection delay time 2 ( $t_{DIOV2}$ ).

**25. Load short-circuiting detection delay time**  
**(Test circuit 5)**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = 1.4\text{ V}$ ,  $V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_5$  is increased. The time interval from when the voltage  $V_5$  exceeds  $V_{SHORT}$  until  $V_{DO}$  goes to "L" is the load short-circuiting detection delay time ( $t_{SHORT}$ ).

**26. Charge overcurrent detection delay time**  
**(Test circuit 5)**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_5$  is decreased. The time interval from when the voltage  $V_5$  falls below  $V_{CIOV}$  until  $V_{CO}$  goes to "L" is the charge overcurrent detection delay time ( $t_{CIOV}$ ).

**27. Charge-discharge inhibition delay time**  
**(Test circuit 5)****27. 1 CTL pin control logic active "H"**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_6$  is increased. The time interval from when the voltage  $V_6$  exceeds  $V_{CTLH}$  until  $V_{CO}$  and  $V_{DO}$  go to "L" is the charge-discharge inhibition delay time ( $t_{CTL}$ ).

**27. 2 CTL pin control logic active "L"**

After setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ , the voltage  $V_6$  is increased. The time interval from when the voltage  $V_1 - V_6$  falls below  $V_{CTLL}$  until  $V_{CO}$  and  $V_{DO}$  go to "L" is  $t_{CTL}$ .

**28. 0 V battery charge starting charger voltage (0 V battery charge enabled)**  
**(Test circuit 4)**

The 0 V battery charge starting charger voltage ( $V_{0CHA}$ ) is defined as the absolute value of voltage  $V_2$  at which the current flowing through the CO pin ( $I_{CO}$ ) exceeds  $1.0\text{ }\mu\text{A}$  when the voltage  $V_2$  is gradually decreased after setting  $V_1 = V_5 = 0\text{ V}$ ,  $V_2 = V_3 = -0.5\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

**29. 0 V battery charge inhibition battery voltage (0 V battery charge inhibited)**  
**(Test circuit 2)**

The 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) is defined as the voltage  $V_1$  at which  $V_{CO}$  goes to "L" ( $V_{CO} = V_{VM}$ ) when the voltage  $V_1$  is gradually decreased after setting  $V_1 = 1.8\text{ V}$ ,  $V_2 = -2.0\text{ V}$ ,  $V_5 = V_6 = 0\text{ V}$ ,  $V_7 = 0.25\text{ V}$ .

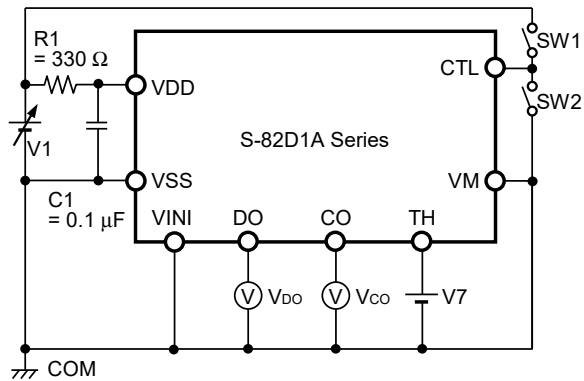


Figure 3 Test Circuit 1

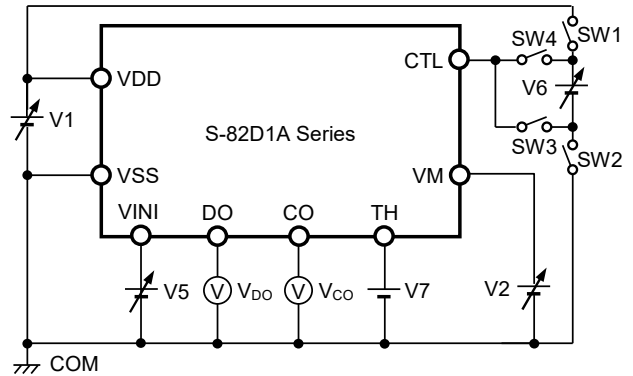


Figure 4 Test Circuit 2

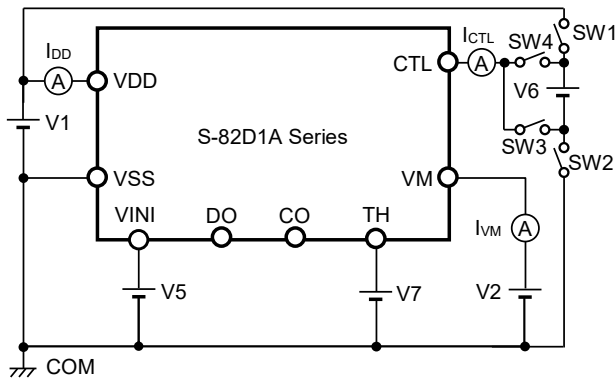


Figure 5 Test Circuit 3

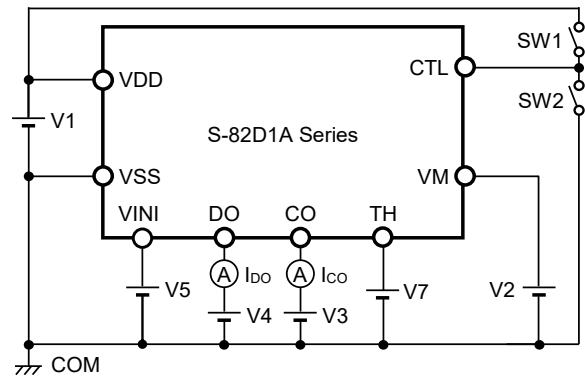


Figure 6 Test Circuit 4

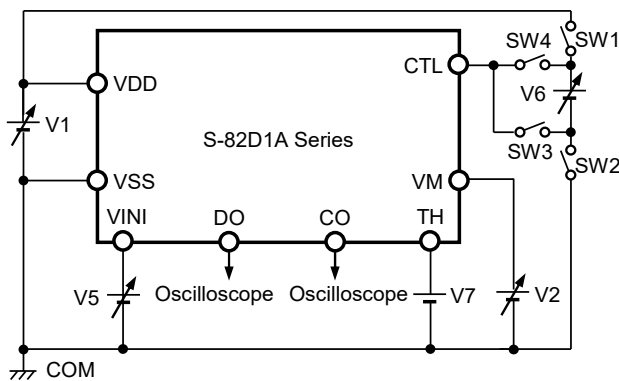


Figure 7 Test Circuit 5

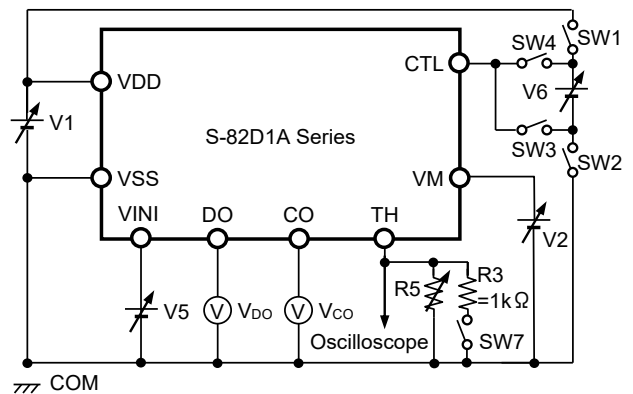


Figure 8 Test Circuit 6

## ■ Operation

**Remark** Refer to "■ Battery Protection IC Connection Example".

### 1. Normal status

The S-82D1A Series monitors the voltage of the battery connected between VDD pin and VSS pin, the voltage between VINI pin and VSS pin, the voltage between CTL pin and VSS pin, and the resistance of an NTC thermistor to control charging and discharging.

#### 1.1 CTL pin control logic active "H"

The S-82D1A Series turns both the charge control FET and discharge control FET on when the battery voltage is in the range from overdischarge detection voltage ( $V_{DL}$ ) to overcharge detection voltage ( $V_{CU}$ ), the VINI pin voltage is in the range from charge overcurrent detection voltage ( $V_{CIOV}$ ) to discharge overcurrent detection voltage 1 ( $V_{DIOV1}$ ), the CTL pin voltage is equal to or lower than the CTL pin voltage "L" ( $V_{CTL L}$ ), and the temperature of an NTC thermistor is in the range from low temperature charge inhibition temperature ( $T_{LC}$ ) to high temperature charge inhibition temperature ( $T_{HC}$ ). This status is called the normal status, and in this condition charging and discharging can be carried out freely.

The resistance between VDD pin and VM pin ( $R_{VMD}$ ), and the resistance between VM pin and VSS pin ( $R_{VMS}$ ) are not connected in the normal status.

#### 1.2 CTL pin control logic active "L"

The S-82D1A Series turns both the charge control FET and discharge control FET on when the battery voltage is in the range from  $V_{DL}$  to  $V_{CU}$ , the VINI pin voltage is in the range from  $V_{CIOV}$  to  $V_{DIOV1}$ , the CTL pin voltage is equal to or higher than the CTL pin voltage "H" ( $V_{CTL H}$ ), and the temperature of an NTC thermistor is in the range from  $T_{LC}$  to  $T_{HC}$ . This status is called the normal status, and in this condition charging and discharging can be carried out freely.

$R_{VMD}$  and  $R_{VMS}$  are not connected in the normal status.

**Caution** After the battery is connected, discharging may not be carried out. In this case, the S-82D1A Series returns to the normal status by connecting a charger.

### 2. Overcharge status

#### 2.1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than  $V_{CU}$  during charging in the normal status and the condition continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the S-82D1A Series turns the charge control FET off to stop charging. This status is called the overcharge status.

The overcharge status is released in the following two cases.

- (1) In the case that the VM pin voltage is lower than 0.35 V typ., the S-82D1A Series releases the overcharge status when the battery voltage falls below overcharge release voltage ( $V_{CL}$ ).
- (2) In the case that the VM pin voltage is equal to or higher than 0.35 V typ., the S-82D1A Series releases the overcharge status when the battery voltage falls below  $V_{CU}$ .

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the  $V_f$  voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82D1A Series releases the overcharge status when the battery voltage is equal to or lower than  $V_{CU}$ .

**Caution** If the battery is charged to a voltage higher than  $V_{CU}$  and the battery voltage does not fall below  $V_{CU}$  even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below  $V_{CU}$ . Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

## 2. 2 $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than  $V_{CU}$  during charging in the normal status and the condition continues for  $t_{CU}$  or longer, the S-82D1A Series turns the charge control FET off to stop charging. This status is called the overcharge status.

In the case that the VM pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below  $V_{CU}$ , the S-82D1A Series releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the  $V_f$  voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82D1A Series releases the overcharge status when the battery voltage is equal to or lower than  $V_{CU}$ .

**Caution 1.** If the battery is charged to a voltage higher than  $V_{CU}$  and the battery voltage does not fall below  $V_{CU}$  even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below  $V_{CU}$ . Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

**2.** When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below  $V_{CL}$ . The overcharge status is released when the discharge current flows and the VM pin voltage goes over 0.35 V typ. by removing the charger.

## 3. Overdischarge status

When the battery voltage falls below  $V_{DL}$  during discharging in the normal status and the condition continues for the overdischarge detection delay time ( $t_{DL}$ ) or longer, the S-82D1A Series turns the discharge control FET off to stop discharging. This status is called the overdischarge status.

Under the overdischarge status, VDD pin and VM pin are shorted by  $R_{VMD}$  in the S-82D1A Series. The VM pin voltage is pulled up by  $R_{VMD}$ .

When connecting a charger in the overdischarge status, the battery voltage reaches  $V_{DL}$  or higher and the S-82D1A Series releases the overdischarge status if the VM pin voltage is below 0 V typ.

The battery voltage reaches the overdischarge release voltage ( $V_{DU}$ ) or higher and the S-82D1A Series releases the overdischarge status if the VM pin voltage is not below 0 V typ.

$R_{VMS}$  is not connected in the overdischarge status.

### 3. 1 With power-down function

Under the overdischarge status, when voltage difference between VDD pin and VM pin is 0.8 V typ. or lower, the power-down function works and the current consumption is reduced to the current consumption during power-down ( $I_{PDN}$ ). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage  $\geq 0.7$  V typ., the S-82D1A Series maintains the overdischarge status even when the battery voltage reaches  $V_{DU}$  or higher.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches  $V_{DU}$  or higher and the S-82D1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ.  $\geq$  the VM pin voltage, the battery voltage reaches  $V_{DL}$  or higher and the S-82D1A Series releases the overdischarge status.

### 3. 2 Without power-down function

Under the overdischarge status, the power-down function does not work even when voltage difference between VDD pin and VM pin is 0.8 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage  $\geq 0.7$  V typ., the battery voltage reaches  $V_{DU}$  or higher and the S-82D1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches  $V_{DU}$  or higher and the S-82D1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ.  $\geq$  the VM pin voltage, the battery voltage reaches  $V_{DL}$  or higher and the S-82D1A Series releases the overdischarge status.

#### **4. Discharge overcurrent status (discharge overcurrent 1, discharge overcurrent 2, load short-circuiting, load short-circuiting 2)**

##### **4. 1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting**

When a battery in the normal status is in the status where the VINI pin voltage is equal to or higher than  $V_{DIOV1}$  because the discharge current is equal to or higher than the specified value and the status continues for the discharge overcurrent detection delay time 1 ( $t_{DIOV1}$ ) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

Under the discharge overcurrent status, VM pin and VSS pin are shorted by  $R_{VMS}$  in the S-82D1A Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin returns to the VSS pin voltage.

When the VM pin voltage returns to  $V_{RIOV}$  or lower, the S-82D1A Series releases the discharge overcurrent status.

$R_{VMD}$  is not connected in the discharge overcurrent status.

##### **4. 2 Load short-circuiting 2**

When a battery in the normal status is in the status where a load causing discharge overcurrent is connected, and the VM pin voltage is equal to or higher than  $V_{SHORT2}$  and the status continues for the load short-circuiting detection delay time ( $t_{SHORT}$ ) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

The S-82D1A Series releases the discharge overcurrent status in the same way as in "4. 1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting".

##### **4. 3 Discharge overcurrent status reset function by CTL pin**

###### **4. 3. 1 With discharge overcurrent status reset function by CTL pin**

Under the discharge overcurrent status, when the CTL pin is active and the condition continues for the charge-discharge inhibition delay time ( $t_{CTL}$ ) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. The S-82D1A Series then becomes the charge-discharge inhibition status.

The S-82D1A Series returns to the normal status if the CTL pin is made inactive and the charge-discharge inhibition status is released.

###### **4. 3. 2 Without discharge overcurrent status reset function by CTL pin**

Under the discharge overcurrent status, even when the CTL pin is active and the condition continues for  $t_{CTL}$  or longer, the S-82D1A Series does not become the charge-discharge inhibition status and maintains the discharge overcurrent status.

The S-82D1A Series does not return to the normal status and maintains the discharge overcurrent status even if the CTL pin is made inactive.

#### **5. Charge overcurrent status**

When a battery in the normal status is in the status where the VINI pin voltage is equal to or lower than  $V_{CIOV}$  because the charge current is equal to or higher than the specified value and the status continues for the charge overcurrent detection delay time ( $t_{CIOV}$ ) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.

The S-82D1A Series releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.

The charge overcurrent detection does not function in the overdischarge status.

## 6. Charge-discharge inhibition status

### 6. 1 CTL pin control logic active "H"

When the CTL pin voltage is equal to or higher than CTL pin voltage "H" ( $V_{CTLH}$ ) and the status continues for the charge-discharge inhibition delay time ( $t_{CTL}$ ) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status.

The S-82D1A Series releases charge-discharge inhibition status when the CTL pin voltage is equal to or lower than CTL pin voltage "L" ( $V_{CTL L}$ ).

### 6. 2 CTL pin control logic active "L"

When the CTL pin voltage is equal to or lower than  $V_{CTL L}$  and the status continues for  $t_{CTL}$  or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status.

The S-82D1A Series releases charge-discharge inhibition status when the CTL pin voltage is equal to or higher than  $V_{CTLH}$ .

## 6. 3 CTL pin internal resistance connection

### 6. 3. 1 CTL pin internal resistance "pull-up"

The CTL pin is shorted to the VDD pin by the CTL pin internal resistance ( $R_{CTL}$ ).

### 6. 3. 2 CTL pin internal resistance "pull-down"

The CTL pin is shorted to the VSS pin by  $R_{CTL}$ .

When the S-82D1A Series becomes overdischarge status,  $R_{CTL}$  is disconnected, and the input current and the output current to the CTL pin are cut off.

The charge-discharge control by the CTL pin does not function in the overdischarge status.

## **7. Temperature protection status (high temperature charge-discharge inhibition status, high temperature charge inhibition status, low temperature charge inhibition status, low temperature charge-discharge inhibition status)**

The S-82D1A Series carries out intermittent operation in the normal status.

The S-82D1A Series monitors the temperature of an NTC thermistor for the sampling time ( $t_{\text{AWAKE}}$ ) of 4 ms typ. after sampling wait time ( $t_{\text{SLEEP}}$ ).

### **7.1 High temperature charge-discharge inhibition status**

When the temperature of an NTC thermistor is equal to or higher than high temperature charge-discharge inhibition temperature ( $T_{\text{HCD}}$ ) and the condition continues until the number of the temperature sampling reaches continuous detection / release count (N), the S-82D1A Series becomes the high temperature charge-discharge inhibition status.

Under the high temperature charge-discharge inhibition status, both the charge control FET and discharge control FET are turned off, and charging and discharging are stopped.

The S-82D1A Series releases the high temperature charge-discharge inhibition status when the temperature of the NTC thermistor falls below  $T_{\text{HCD}}$  by hysteresis temperature ( $T_{\text{HYS}}$ ) and the condition continues until the number of the temperature sampling reaches N.

### **7.2 High temperature charge inhibition status**

When the temperature of an NTC thermistor is equal to or higher than high temperature charge inhibition temperature ( $T_{\text{HC}}$ ) and the condition continues until the number of the temperature sampling reaches N, the S-82D1A Series becomes the high temperature charge inhibition status.

- When a battery is not connected to a charger and the VM pin voltage  $> 3 \text{ mV typ.}$ , the charge control FET is not turned off.
- When a battery is connected to a charger and  $3 \text{ mV typ.} \geq$  the VM pin voltage, the charge control FET is turned off and charging is stopped.

The S-82D1A Series releases the high temperature charge inhibition status when the temperature of the NTC thermistor falls below  $T_{\text{HC}}$  by  $T_{\text{HYS}}$  and the condition continues until the number of the temperature sampling reaches N.

### **7.3 Low temperature charge inhibition status**

When the temperature of an NTC thermistor is equal to or lower than low temperature charge inhibition temperature ( $T_{\text{LC}}$ ) and the condition continues until the number of the temperature sampling reaches N, the S-82D1A Series becomes the low temperature charge inhibition status.

- When a battery is not connected to a charger and the VM pin voltage  $> 3 \text{ mV typ.}$ , the charge control FET is not turned off.
- When a battery is connected to a charger and  $3 \text{ mV typ.} \geq$  the VM pin voltage, the charge control FET is turned off and charging is stopped.

The S-82D1A Series releases the low temperature charge inhibition status when the temperature of the NTC thermistor exceeds  $T_{\text{LC}}$  by  $T_{\text{HYS}}$  and the condition continues until the number of the temperature sampling reaches N.

### **7.4 Low temperature charge-discharge inhibition status**

When the temperature of an NTC thermistor is equal to or lower than low temperature charge-discharge inhibition temperature ( $T_{\text{LCD}}$ ) and the condition continues until the number of the temperature sampling reaches N, the S-82D1A Series becomes the low temperature charge-discharge inhibition status.

Under the low temperature charge-discharge inhibition status, both the charge control FET and discharge control FET are turned off, and charging and discharging are stopped.

The S-82D1A Series releases the low temperature charge-discharge inhibition status when the temperature of the NTC thermistor exceeds  $T_{\text{LCD}}$  by  $T_{\text{HYS}}$  and the condition continues until the number of the temperature sampling reaches N.

## 8. 0 V battery charge enabled

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage ( $V_{0CHA}$ ) or a higher voltage is applied between the EB+ and EB- pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.

When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than  $V_{DL}$ , the S-82D1A Series returns to the normal status.

**Caution 1.** Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

**2.** The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than  $V_{DL}$ .

## 9. 0 V battery charge inhibited

This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) or lower, the charge control FET gate is fixed to the EB- pin voltage to inhibit charging. When the battery voltage is  $V_{0INH}$  or higher, charging can be performed.

**Caution** Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

## 10. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

**Remark**  $t_{DIOV1}$ ,  $t_{DIOV2}$  and  $t_{SHORT}$  start when  $V_{DIOV1}$  is detected. When  $V_{DIOV2}$  or  $V_{SHORT}$  is detected over  $t_{DIOV2}$  or  $t_{SHORT}$  after the detection of  $V_{DIOV1}$ , the S-82D1A Series turns the discharge control FET off within  $t_{DIOV2}$  or  $t_{SHORT}$  of each detection.

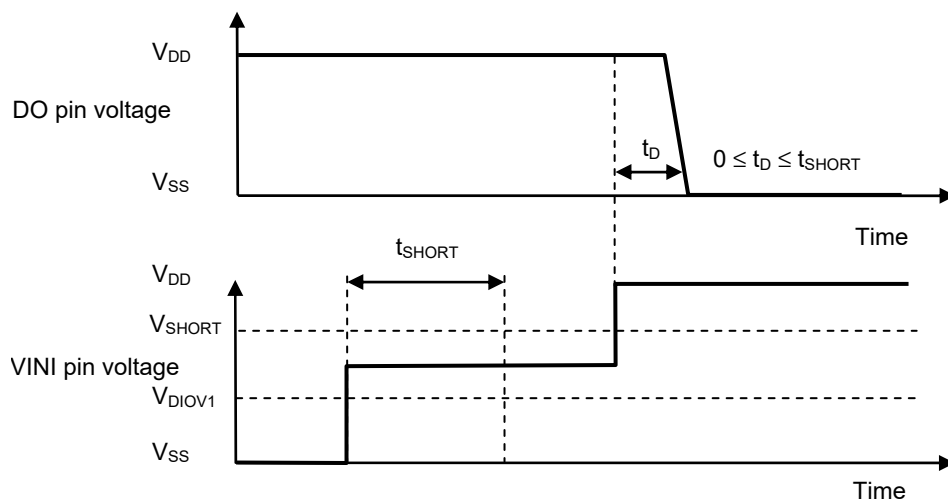


Figure 9

## ■ Timing Charts

### 1. Overcharge detection, overdischarge detection

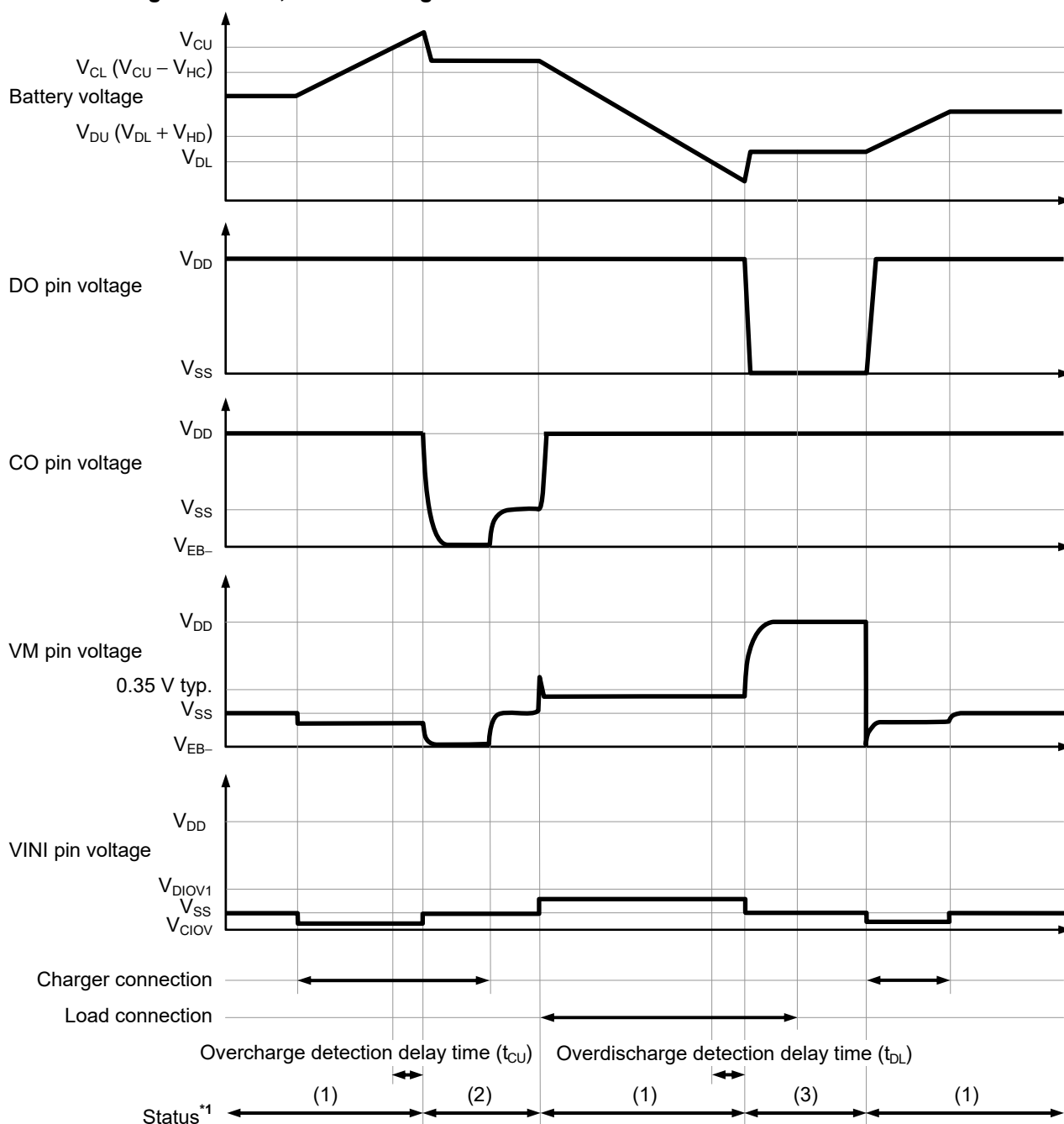


Figure 10

- \*1. (1): Normal status  
(2): Overcharge status  
(3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

## 2. Discharge overcurrent detection

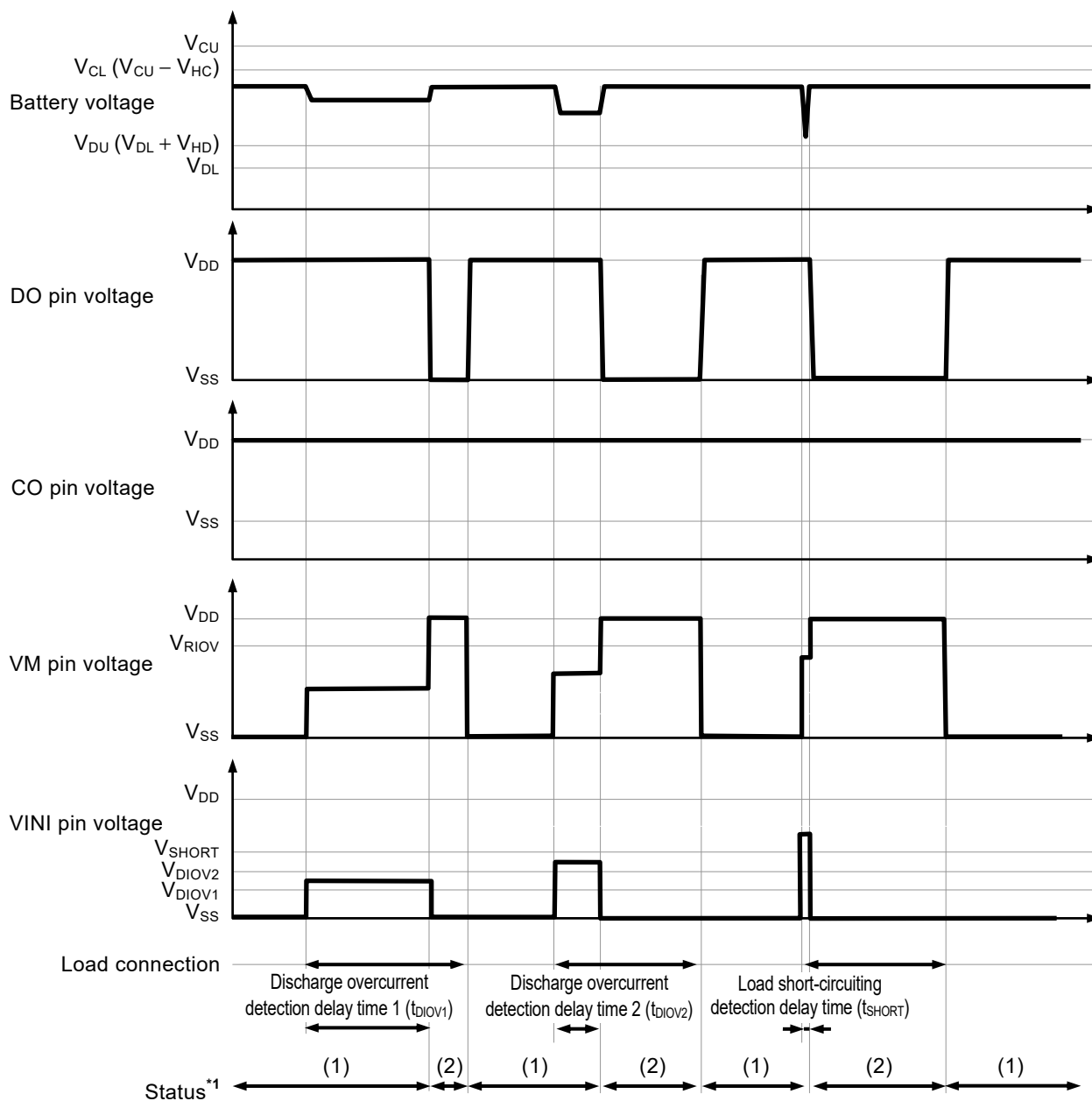
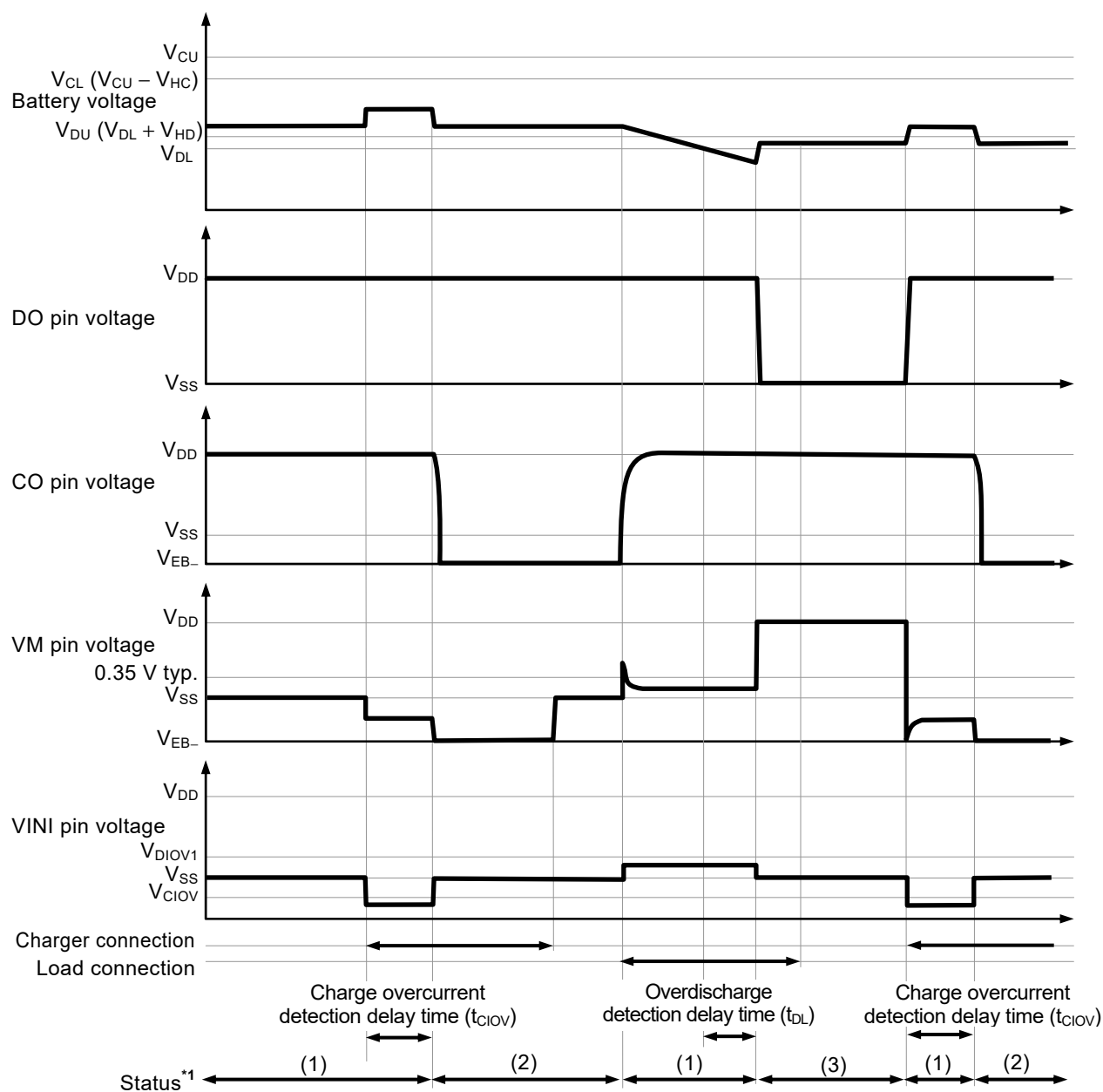


Figure 11

- \*1. (1): Normal status  
 (2): Discharge overcurrent status

### 3. Charge overcurrent detection



**Figure 12**

- \*1.** (1): Normal status  
 (2): Charge overcurrent status  
 (3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

#### 4. Charge-discharge inhibition operation

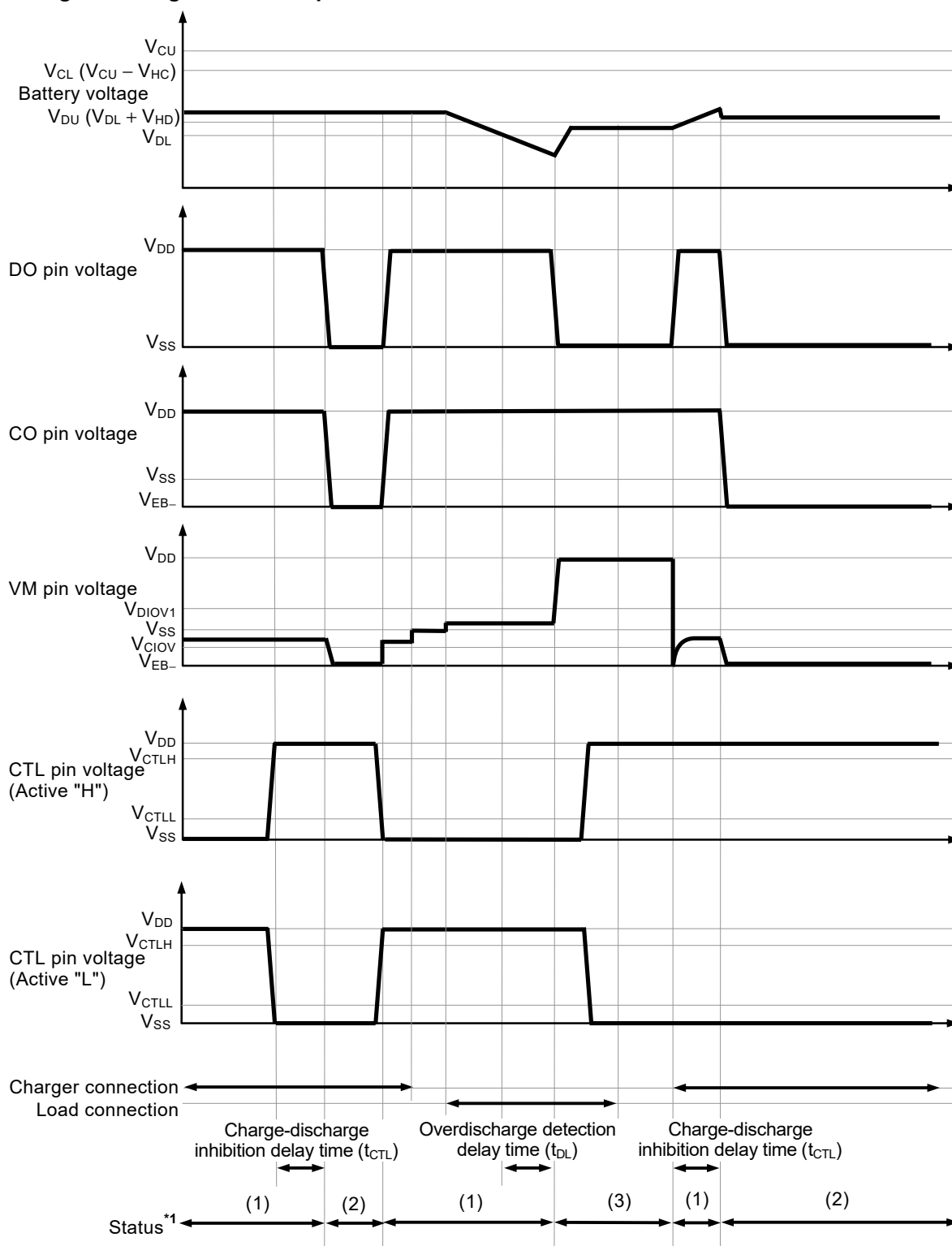


Figure 13

- \*1. (1): Normal status  
 (2): Charge-discharge inhibition status  
 (3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

## 5. Temperature protection operation

### 5.1 High temperature charge inhibition temperature detection

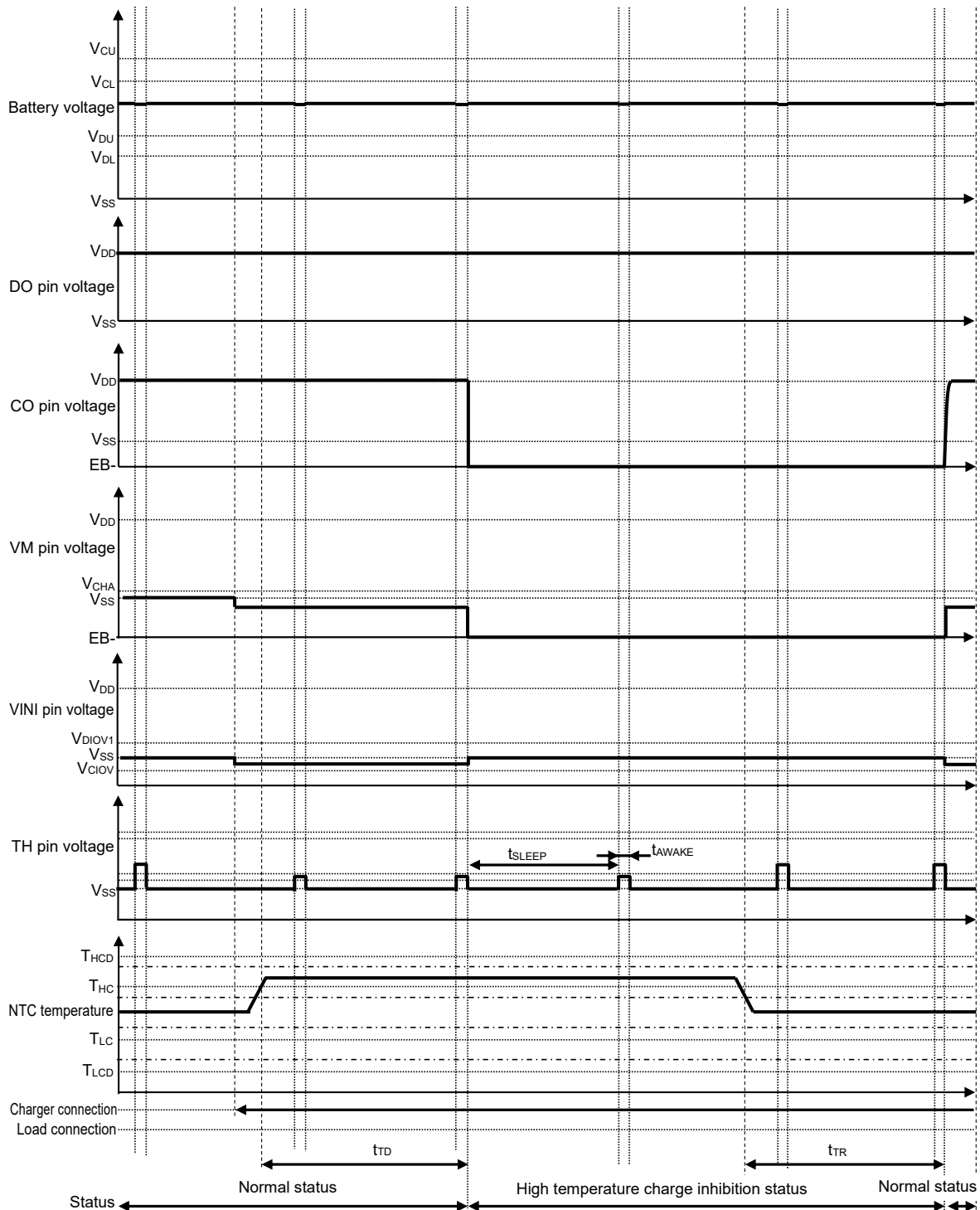


Figure 14

**Remark 1.** Figure 14 shows an example when  $N = 2$ .  $t_{TD}$  and  $t_{TR}$  have the following ranges.

$$(t_{SLEEP} + t_{AWAKE}) \times N - t_{SLEEP} \leq t_{TD} \leq (t_{SLEEP} + t_{AWAKE}) \times N$$

$$(t_{SLEEP} + t_{AWAKE}) \times N - t_{SLEEP} \leq t_{TR} \leq (t_{SLEEP} + t_{AWAKE}) \times N$$

2.  $t_{TD}$ : Delay time to detect high temperature charge inhibition temperature

$t_{TR}$ : Delay time to detect high temperature charge inhibition release temperature

## 5.2 High temperature charge-discharge inhibition temperature detection

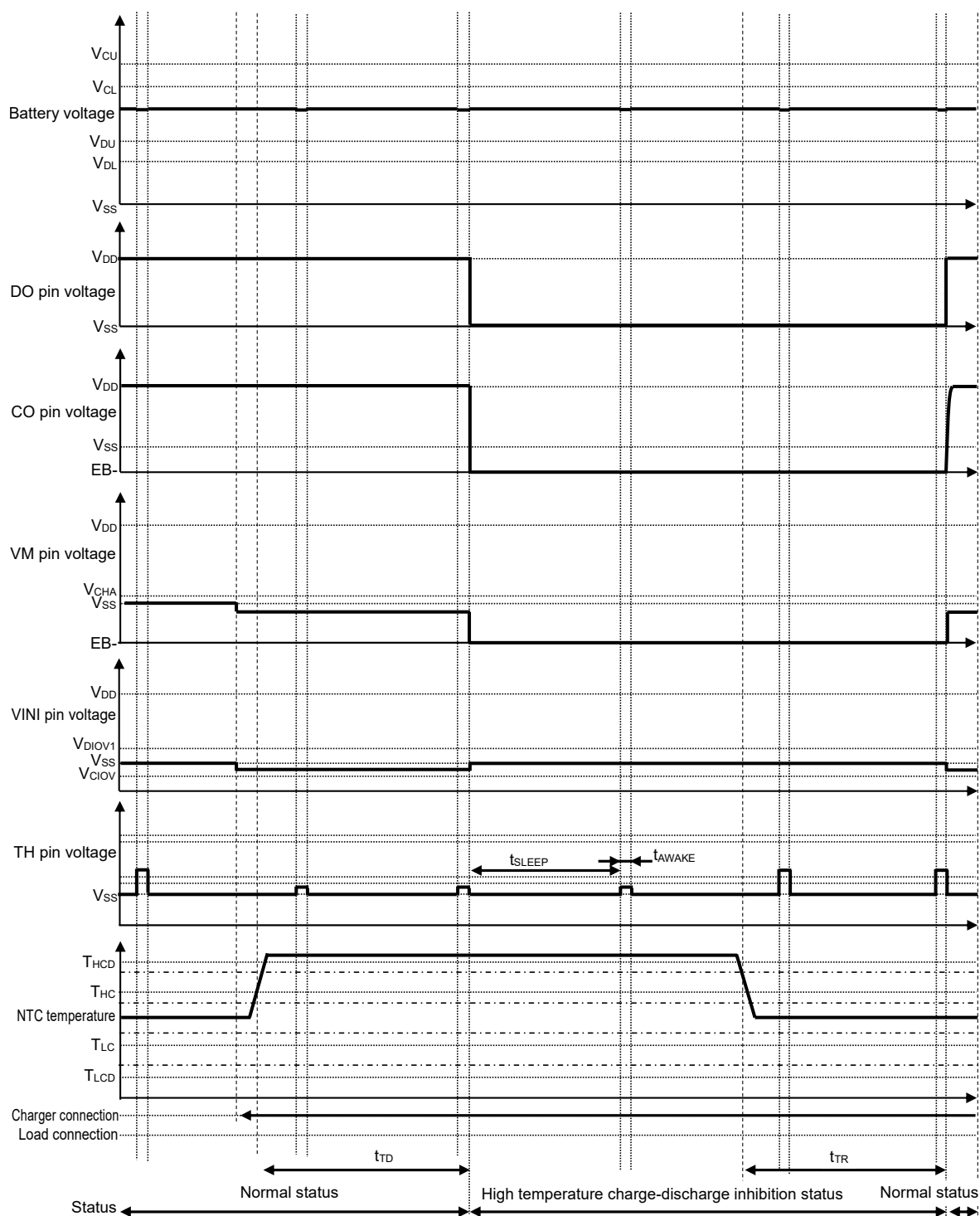


Figure 15

**Remark 1.** Figure 15 shows a time chart when  $N = 2$  and the temperature of an NTC thermistor changes from below  $T_{HC}$  to above  $T_{HCD}$ .

Since the temperature of the NTC thermistor is above  $T_{HCD}$  twice in a row at sampling, S-82D1A Series switches from the normal status to the high temperature charge-discharge inhibition status.

2.  $t_{TD}$ : Delay time to detect high temperature charge-discharge inhibition temperature

$t_{TR}$ : Delay time to detect high temperature charge-discharge inhibition release temperature

## ■ Battery Protection IC Connection Example

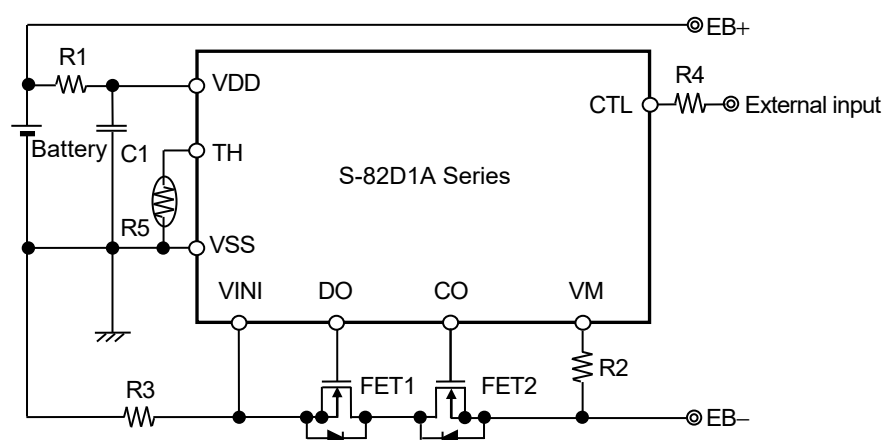


Figure 16

Table 14 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage*1
FET2	N-channel MOS FET	Charge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage*1
R1	Resistor	ESD protection, For power fluctuation	270 Ω	330 Ω	1.2 kΩ*2	—
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	2.2 μF	—
R2	Resistor	ESD protection, Protection for reverse connection of a charger	300 Ω	470 Ω	1.5 kΩ	—
R3	Resistor	Overcurrent detection	—	1.5 mΩ	—	—
R4	Resistor	CTL pin input protection	—	1 kΩ	—	—
R5	NTC Thermistor	Temperature sensing	10 kΩ*3	100 kΩ*3	100 kΩ*3	—

\*1. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

\*2. Accuracy of overcharge detection voltage is guaranteed by R1 = 330 Ω. Connecting resistors with other values will worsen the accuracy.

\*3. Temperature detection accuracy varies with NTC thermistor specifications.

When an NTC thermistor listed in **Table 6** is connected, the detection temperature and accuracy can be achieved.

**Caution 1. The constants may be changed without notice.**

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

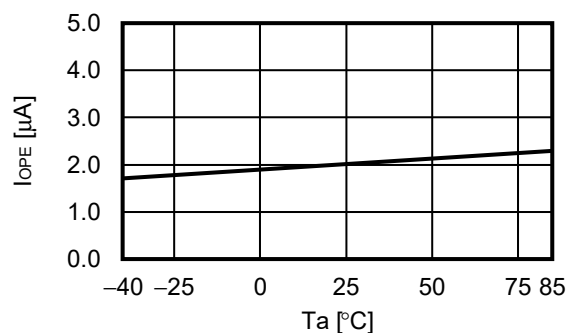
**■ Precautions**

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

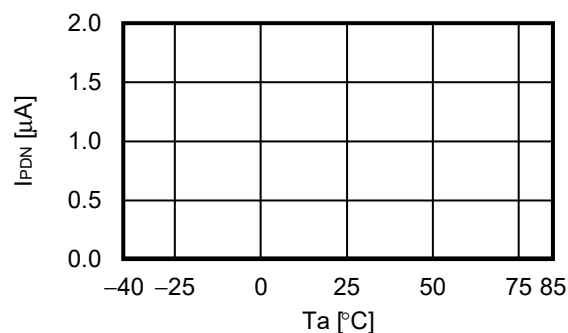
## ■ Characteristics (Typical Data)

### 1. Current consumption

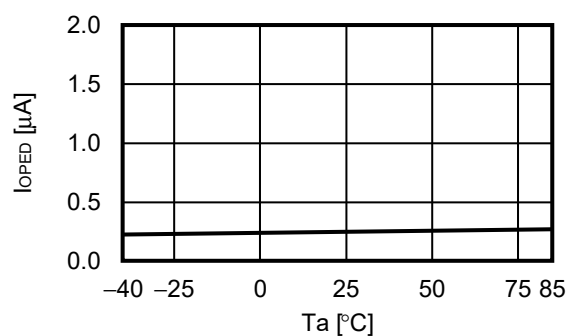
1. 1  $I_{OPE}$  vs.  $T_a$



1. 2  $I_{PDN}$  vs.  $T_a$

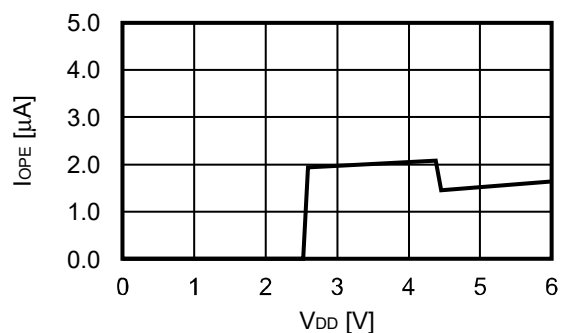


1. 3  $I_{OPED}$  vs.  $T_a$

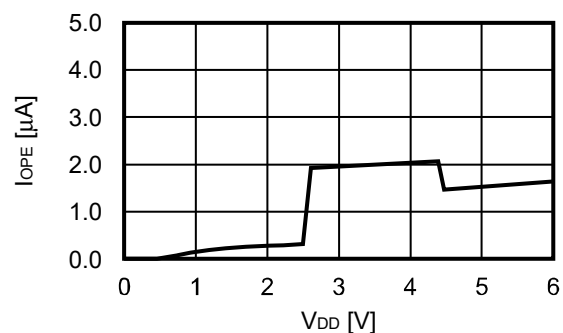


1. 4  $I_{OPE}$  vs.  $V_{DD}$

1. 4. 1 With power-down function

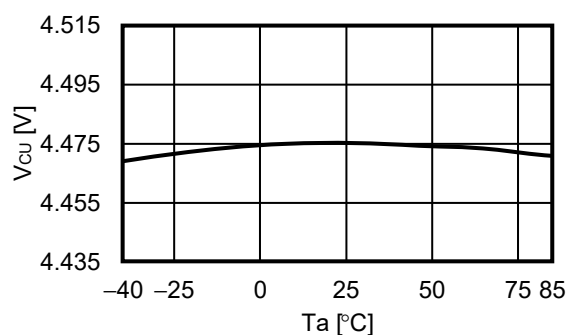


1. 4. 2 Without power-down function

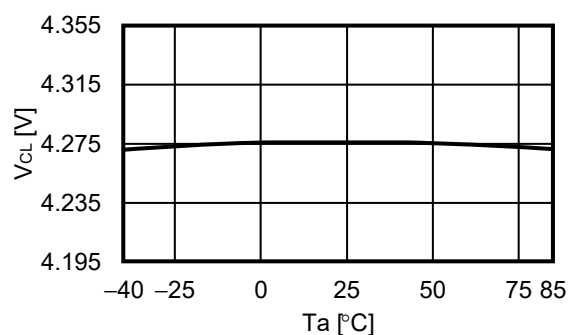


## 2. Detection voltage, release voltage

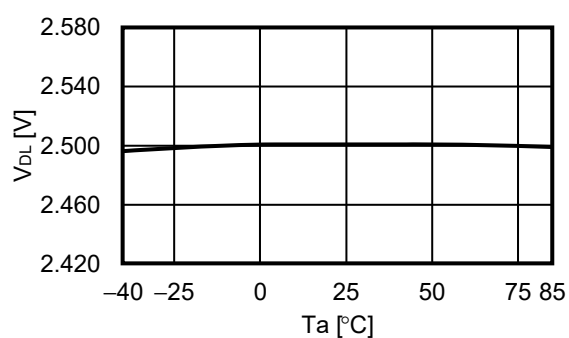
2. 1  $V_{CU}$  vs.  $T_a$



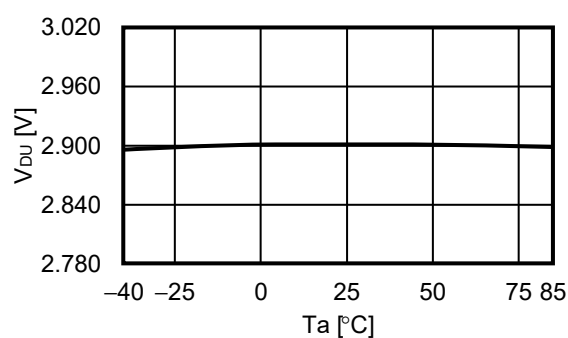
2. 2  $V_{CL}$  vs.  $T_a$



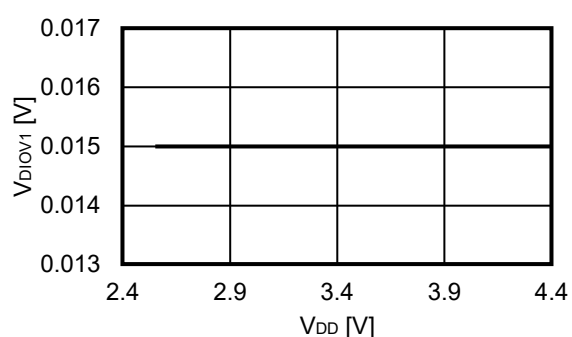
2. 3  $V_{DL}$  vs.  $T_a$



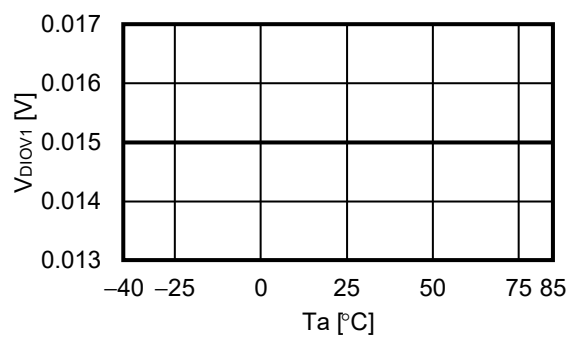
2. 4  $V_{DU}$  vs.  $T_a$



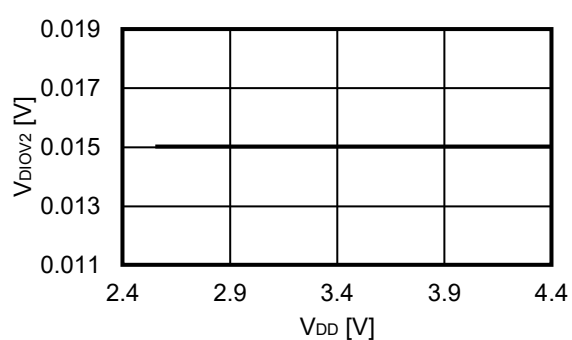
2. 5  $V_{DIOV1}$  vs.  $V_{DD}$



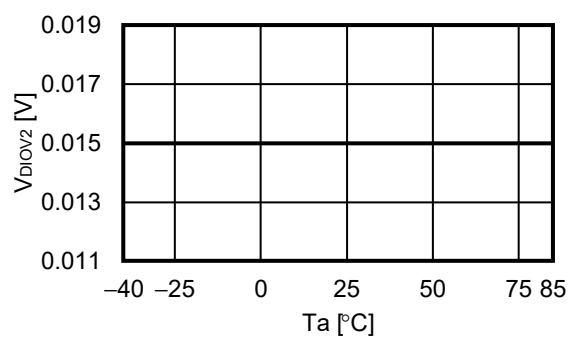
2. 6  $V_{DIOV1}$  vs.  $T_a$



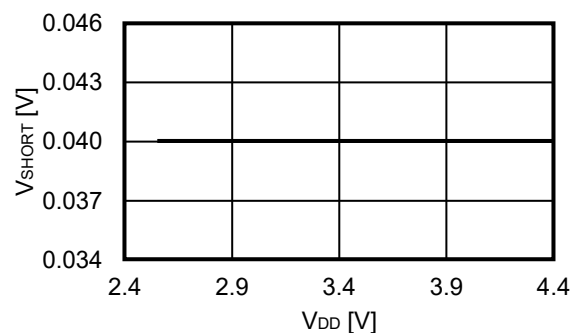
2. 7  $V_{DIOV2}$  vs.  $V_{DD}$



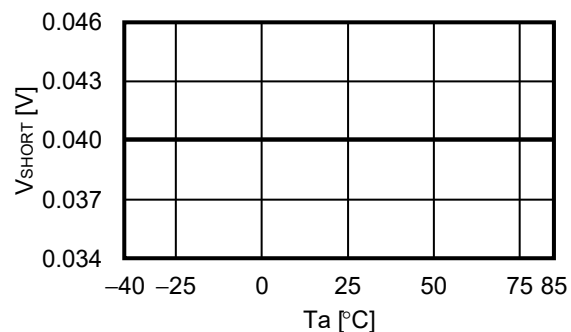
2. 8  $V_{DIOV2}$  vs.  $T_a$



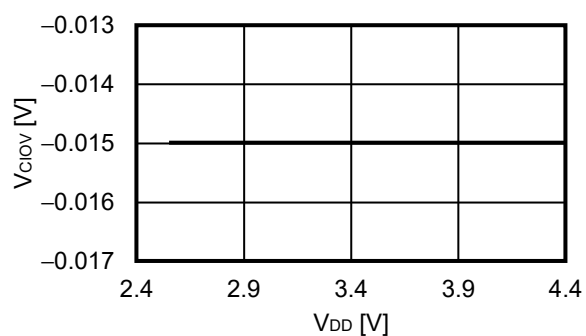
**2. 9  $V_{\text{SHORT}}$  vs.  $V_{\text{DD}}$**



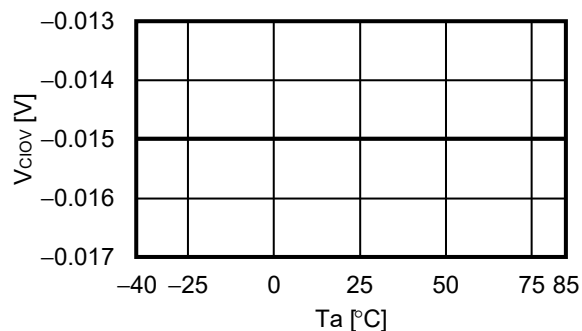
**2. 10  $V_{\text{SHORT}}$  vs.  $T_a$**



**2. 11  $V_{\text{CLOV}}$  vs.  $V_{\text{DD}}$**

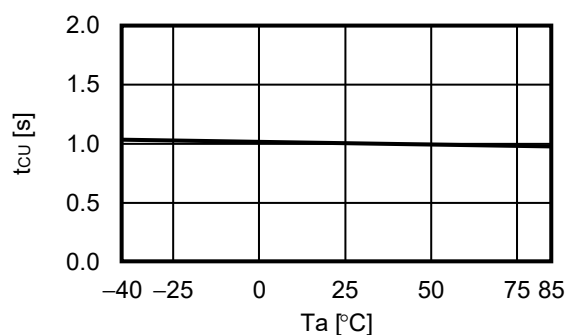


**2. 12  $V_{\text{CLOV}}$  vs.  $T_a$**

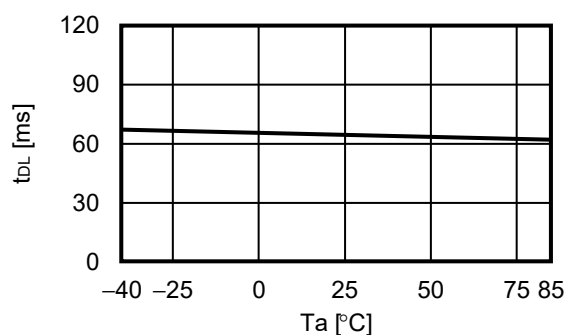


### 3. Delay time

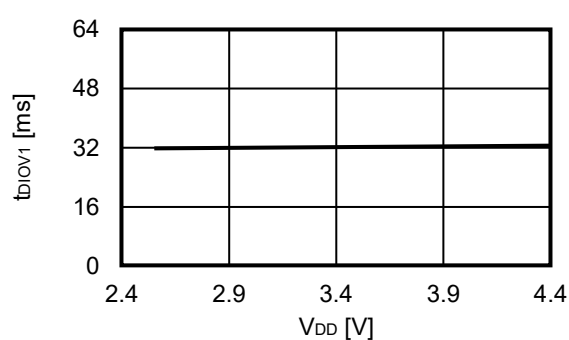
3. 1  $t_{CU}$  vs.  $T_a$



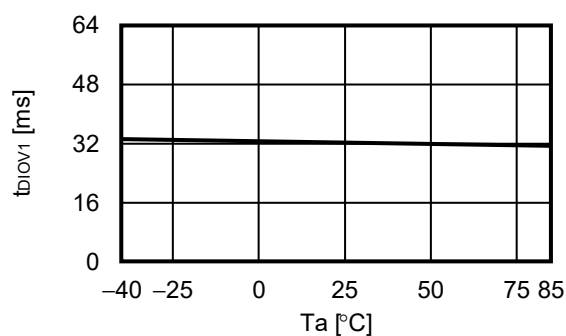
3. 2  $t_{DL}$  vs.  $T_a$



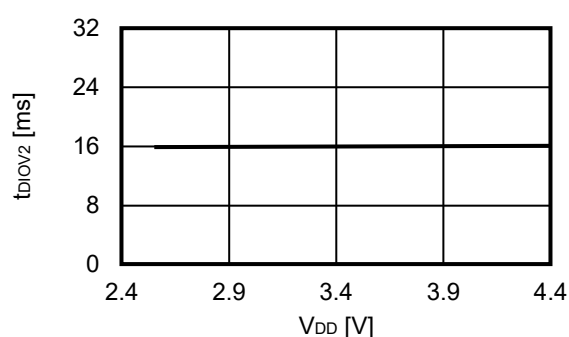
3. 3  $t_{DIOV1}$  vs.  $V_{DD}$



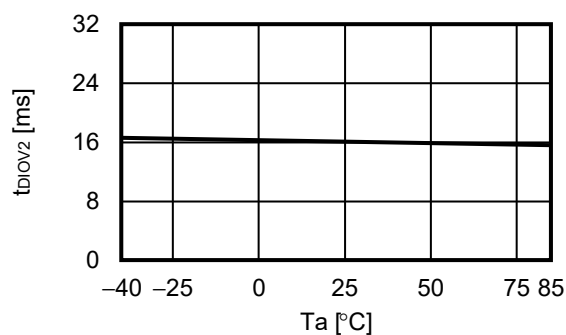
3. 4  $t_{DIOV1}$  vs.  $T_a$



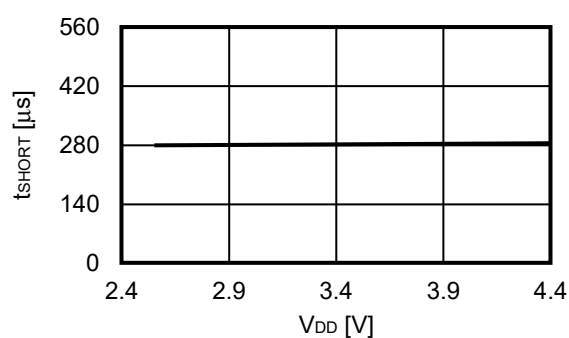
3. 5  $t_{DIOV2}$  vs.  $V_{DD}$



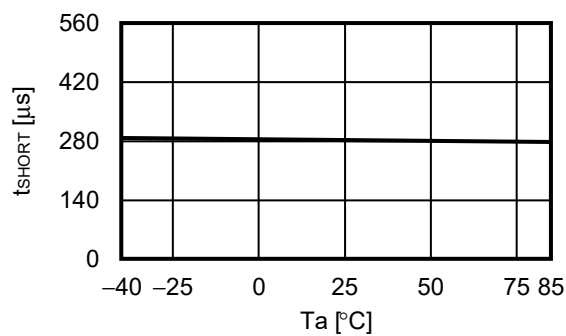
3. 6  $t_{DIOV2}$  vs.  $T_a$



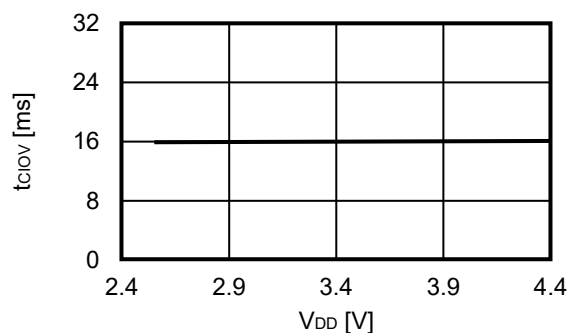
3. 7  $t_{SHORT}$  vs.  $V_{DD}$



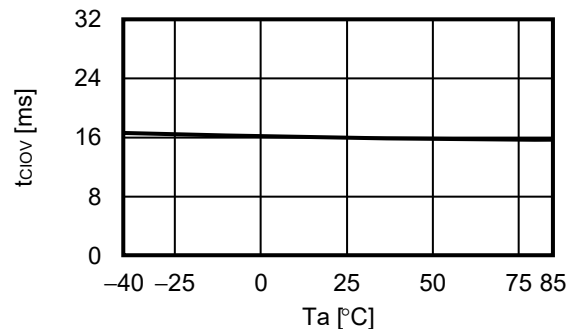
3. 8  $t_{SHORT}$  vs.  $T_a$



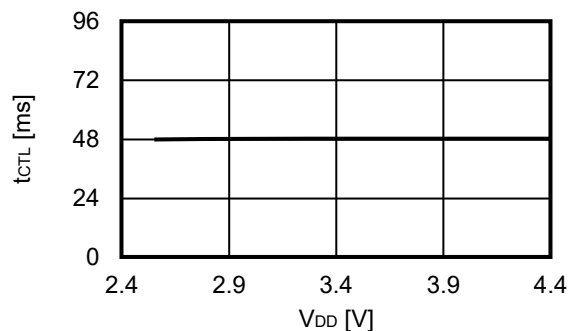
**3. 9  $t_{CIOV}$  vs.  $V_{DD}$**



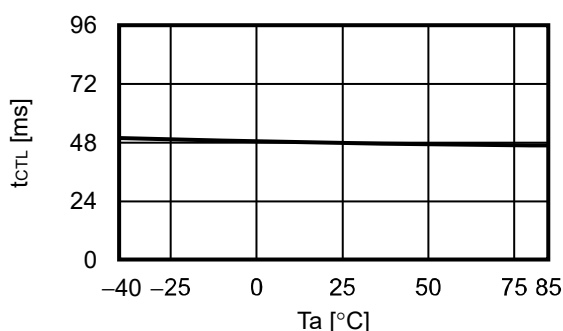
**3. 10  $t_{CIOV}$  vs.  $T_a$**



**3. 11  $t_{CTL}$  vs.  $V_{DD}$**

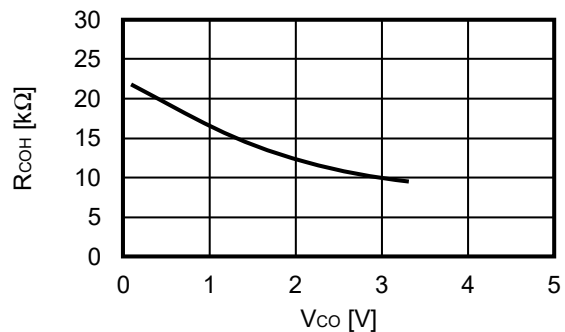


**3. 12  $t_{CTL}$  vs.  $T_a$**

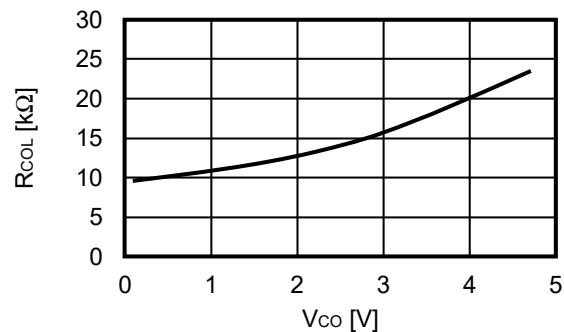


## 4. Output resistance

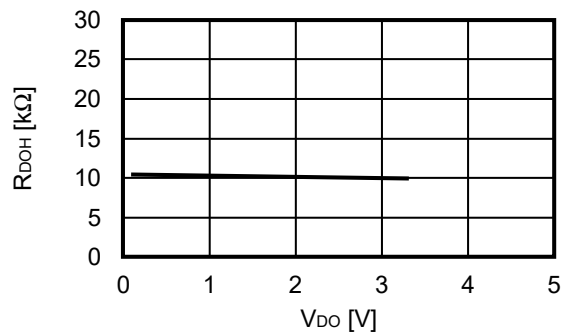
**4. 1  $R_{COH}$  vs.  $V_{CO}$**



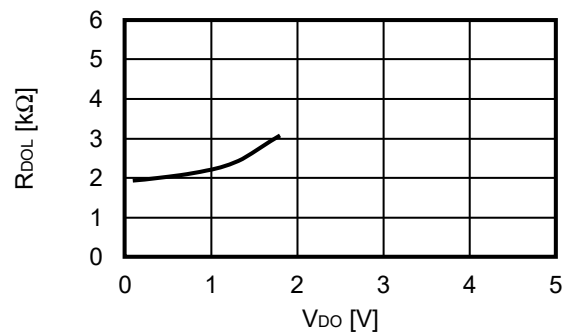
**4. 2  $R_{COL}$  vs.  $V_{CO}$**



**4. 3  $R_{DOH}$  vs.  $V_{DO}$**

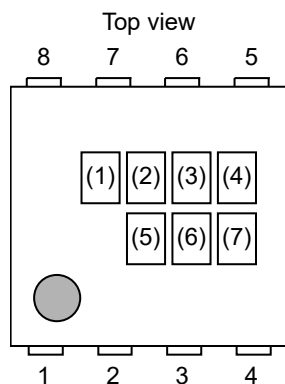


**4. 4  $R_{DOL}$  vs.  $V_{DO}$**



## ■ Marking Specifications

### 1. HSNT-8(1616)



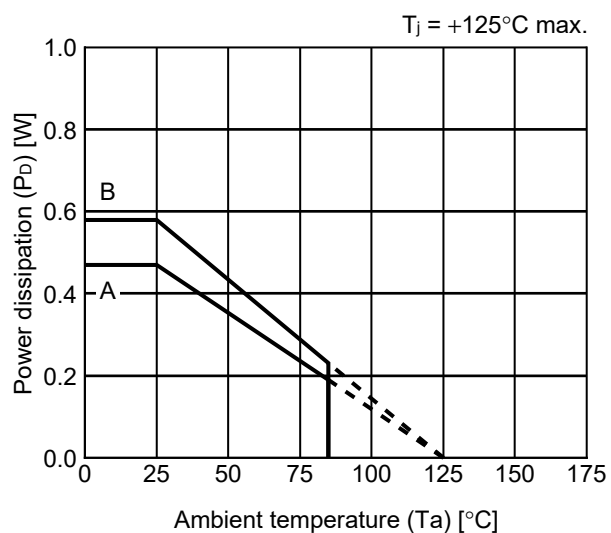
- (1): Product code (Blank)  
 (2) to (4): Product code (refer to **Product name vs. Product code**)  
 (5) to (7): Lot number

#### Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-82D1AAA-A8T2U7	7	4	A
S-82D1AAB-A8T2U7	7	4	B
S-82D1AAD-A8T2U7	7	4	E
S-82D1AAE-A8T2U7	7	4	F
S-82D1AAI-A8T2U7	7	4	K
S-82D1AAJ-A8T2U7	7	4	L
S-82D1AAK-A8T2U7	7	4	M
S-82D1AAL-A8T2U7	7	4	N
S-82D1AAM-A8T2U7	7	4	O
S-82D1AAN-A8T2U7	7	4	P
S-82D1AAO-A8T2U7	7	4	Q
S-82D1AAP-A8T2U7	7	4	R
S-82D1AAQ-A8T2U7	7	4	S

## ■ Power Dissipation

### HSNT-8(1616)

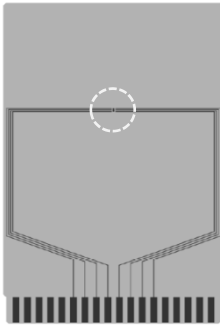


Board	Power Dissipation ( $P_D$ )
A	0.47 W
B	0.58 W
C	—
D	—
E	—

# HSNT-8(1616) Test Board

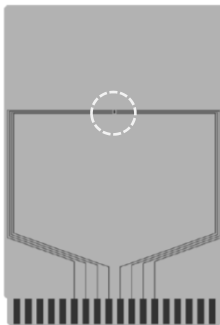


## (1) Board A



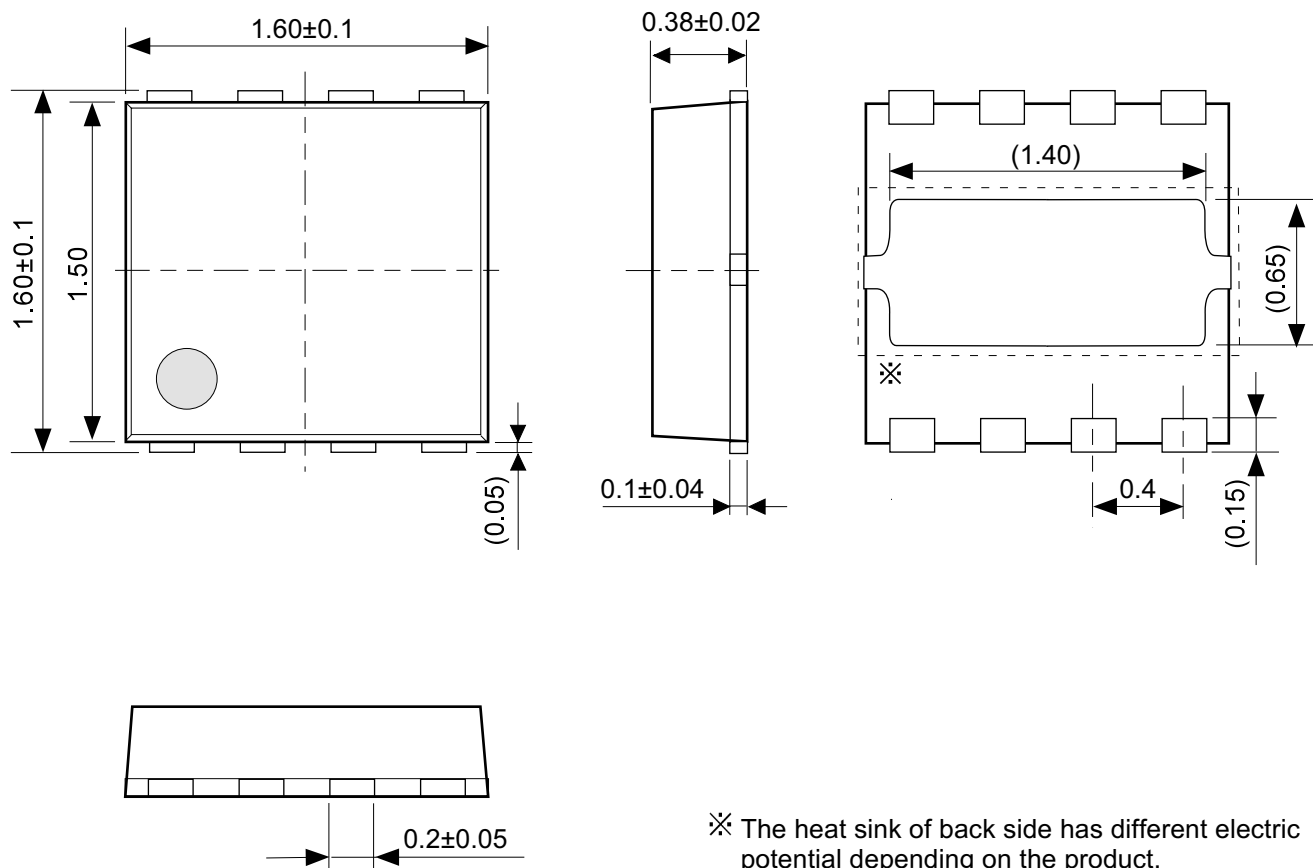
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

## (2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

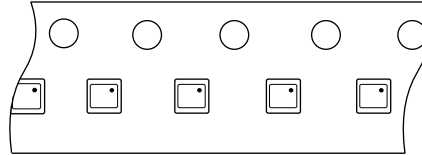
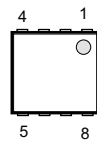
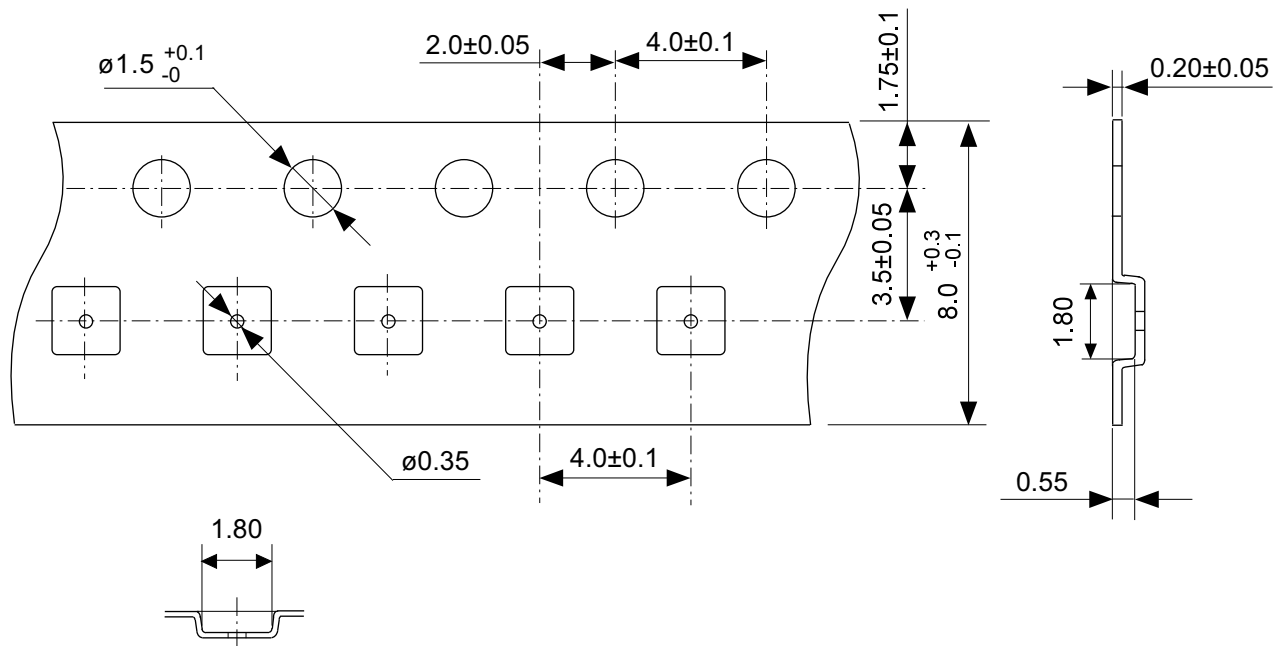
No. HSNT8-B-Board-SD-1.0



※ The heat sink of back side has different electric potential depending on the product.  
Confirm specifications of each product.  
Do not use it as the function of electrode.

No. PY008-A-P-SD-1.0

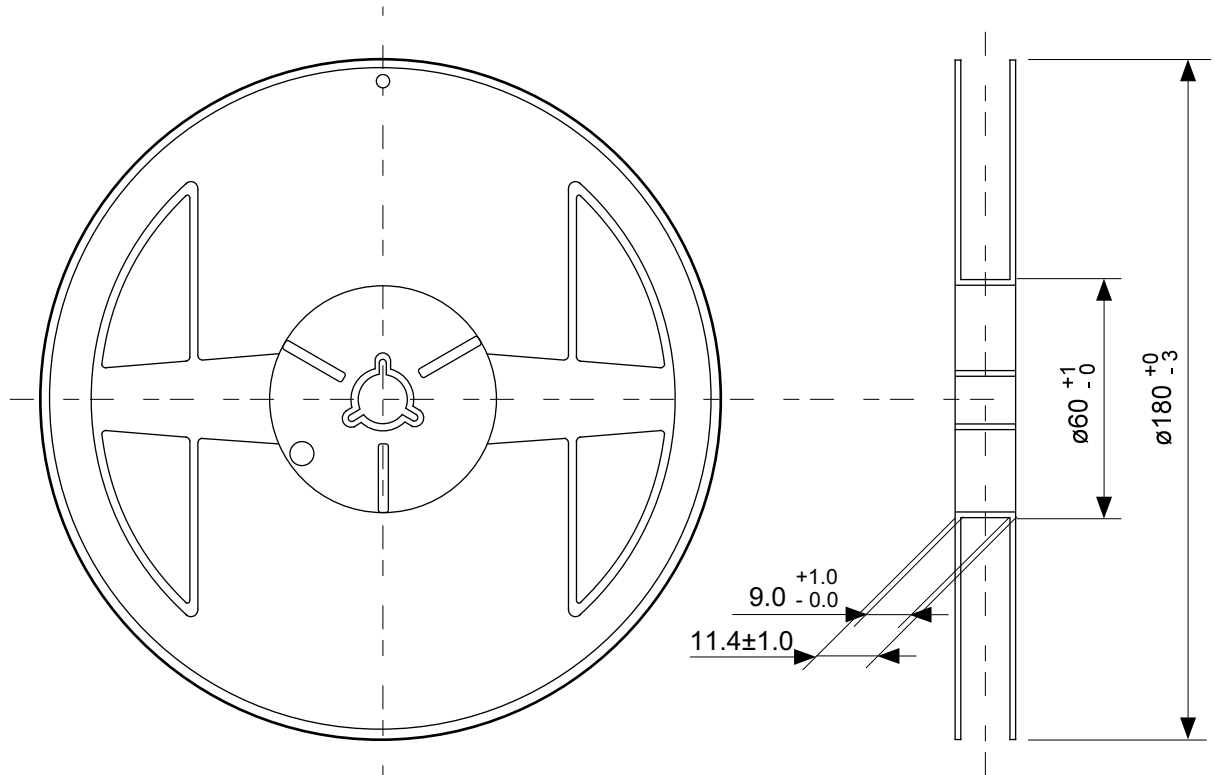
TITLE	HSNT-8-B-PKG Dimensions
No.	PY008-A-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



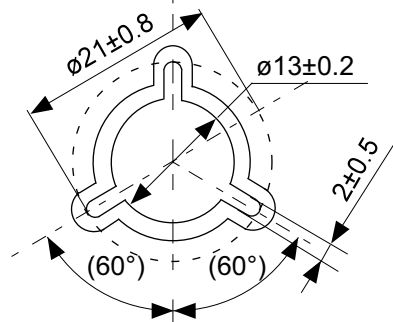
Feed direction

No. PY008-A-C-SD-1.0

TITLE	HSNT-8-B-Carrier Tape
No.	PY008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



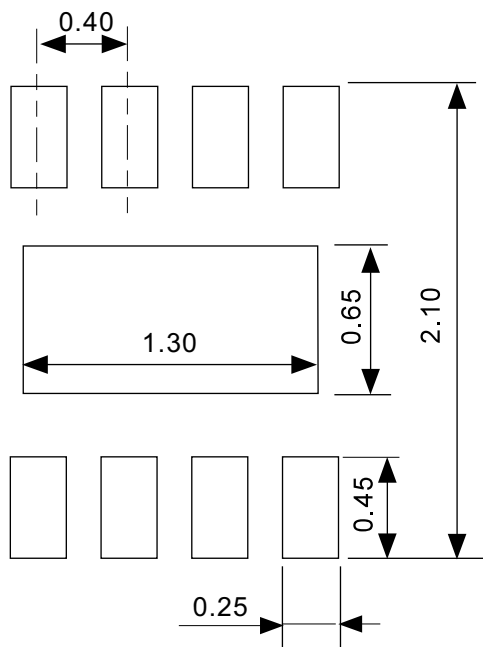
Enlarged drawing in the central part



No. PY008-A-R-SD-1.0

TITLE	HSNT-8-B-Reel		
No.	PY008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

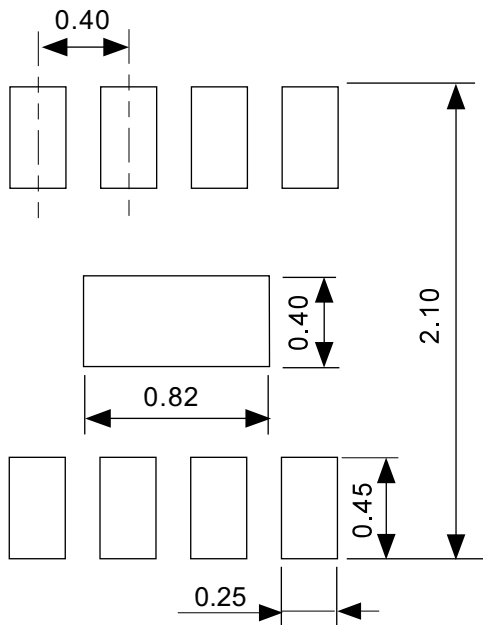
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板(ヒートシンク)を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.  
② Mask aperture ratio of the heat sink mounting part is 40%.  
③ Mask thickness: t0.12 mm

注意 ①リード実装部のマスク開口率は100%です。  
②放熱板実装のマスク開口率は40%です。  
③マスク厚み：t0.12 mm

No. PY008-A-L-SD-1.0

TITLE	HSNT-8-B -Land Recommendation
No.	PY008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ABLIC:](#)

[S-82D1AAA-A8T2U7](#) [S-82D1AAB-A8T2U7](#) [S-82D1AAD-A8T2U7](#) [S-82D1AAE-A8T2U7](#) [S-82D1AAP-A8T2U7](#) [S-](#)  
[82D1AAL-A8T2U7](#) [S-82D1AAK-A8T2U7](#) [S-82D1AAO-A8T2U7](#) [S-82D1AAN-A8T2U7](#) [S-82D1AAQ-A8T2U7](#) [S-](#)  
[82D1AAJ-A8T2U7](#) [S-82D1AAM-A8T2U7](#) [S-82D1AAI-A8T2U7](#)