www.ablic.com

OCTAL ±100V 1.6A 5-LEVEL ULTRASOUND PULSER

Rev.2.2_00

The ABLIC Inc. HDL6M05585 is an octal, 5-level RTZ, high-voltage, high-speed ultrasound pulser.
The HDL6M05585 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

Functions

- Octal 5-level pulser with active T/R switch with 2-input per channel

Features

- 0 to ±100V output voltage
- ±1.6A source and sink peak current for the 1st and 2nd high-voltage pulses ($V_{PP}1/V_{NN}1$,$V_{PP}2/V_{NN}2$)
- TXSEL to select either $V_{PP}1/V_{NN}1$ or $V_{PP}2/V_{NN}2$ drive commonly for all channels
- ±1.6A source and sink peak current for active ground clamp
- 250Ω (±0.1A) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock (transparent mode available)
- 12Ω active T/R switch
- 20MHz output frequency @±60V output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 2-mode output current control for the 2nd high-voltage rail
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 68-lead 10x10mm QFN package (RoHS compliant)

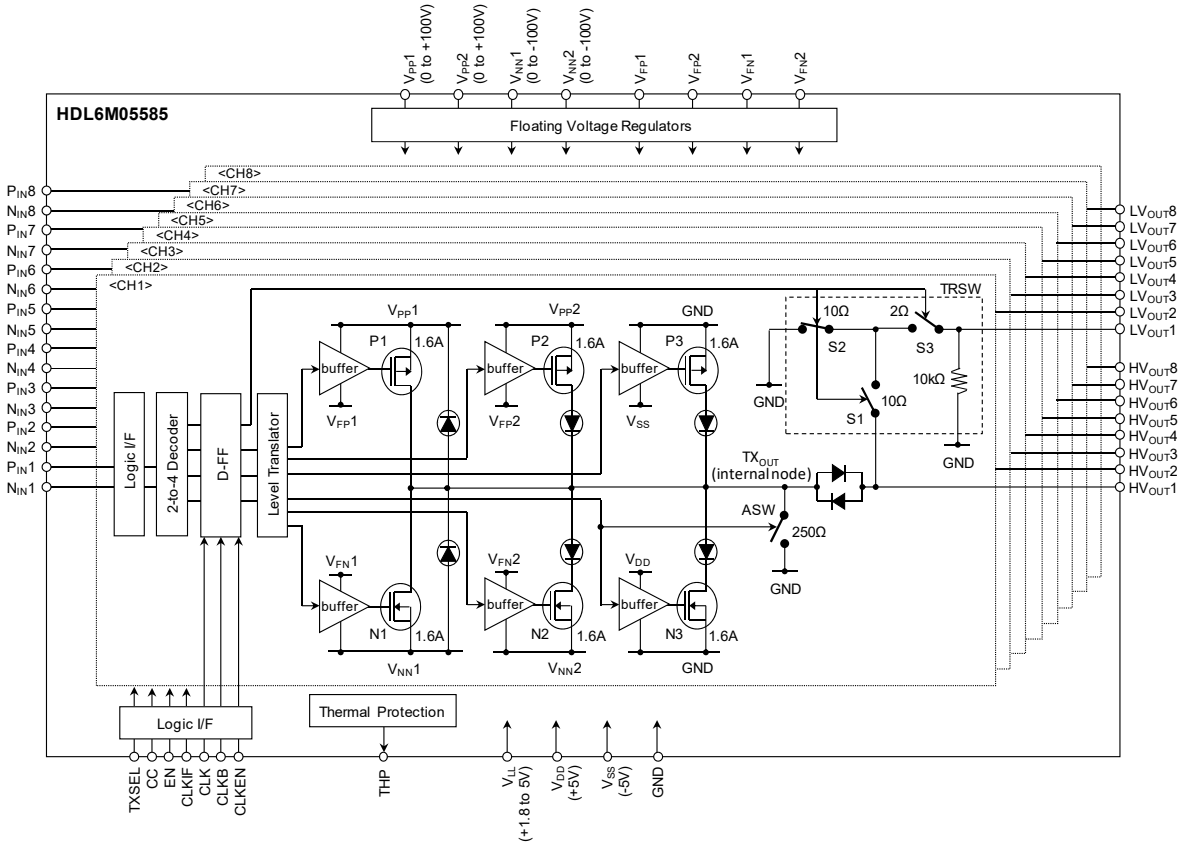


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Negative supply voltage	V_{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	$V_{PP}1$, $V_{PP}2$	-0.5 to +105	V	
5	Negative high-voltage supplies	$V_{NN}1$, $V_{NN}2$	-105 to +0.5	V	
6	Positive high-voltage difference	($V_{PP}1$-$V_{PP}2$)	-0.5 to +105	V	$P_{IN}x$=1, $N_{IN}x$=0, TXSEL=1
			-105 to +105	V	Other than above
7	Negative high-voltage difference	($V_{NN}1$-$V_{NN}2$)	-105 to +0.5	V	$P_{IN}x$=0, $N_{IN}x$=1, TXSEL=1
			-105 to +105	V	Other than above
8	High-voltage outputs (x=1~8)	$HV_{OUT}x$	-105 to +105	V	
9	Low-voltage outputs (x=1~8)	$LV_{OUT}x$	-1 to +1	V	
10	THP (Thermal Protection) output	THP	-0.4 to +7	V	
11	All Logic input voltages (x=1~8)	$P_{IN}x$, $N_{IN}x$, EN, CLKEN, CLK, CLKB, CLKIF, CC, TXSEL	-0.4 to +7	V	
12	Operating junction temperature	T_{Jop}	-20 to +150	°C	
13	Storage temperature	T_{STG}	-55 to +150	°C	
14	Maximum power dissipation	P_{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V_{DD}	V	Transparent mode
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	$V_{PP}1$, $V_{PP}2$	0	-	100	V	
5	Negative high-voltage supplies	$V_{NN}1$, $V_{NN}2$	-100	-	0	V	
6	Positive high-voltage difference	($V_{PP}1$-$V_{PP}2$)	0	-	100	V	
7	Negative high-voltage difference	($V_{NN}1$-$V_{NN}2$)	-100	-	0	V	
8	IC substrate voltage *	V_{SUB}	-	0	-	V	
9	$V_{PP}x$, $V_{NN}x$ slew rate (x=1,2)	SR_{MAX}	-	-	25	V/ms	
10	Operating free-air Temperature	T_A	0		75	°C	

NOTE: * The package exposed pad internally connected to the chip substrate must be soldered to the ground.

2.2 Logic Inputs

2.2.1 Synchronizing Data Inputs

Clock (CLK) mode synchronizes data inputs $P_{IN}x$, $N_{IN}x$ (x=1~8) and TXSEL with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. $P_{IN}x$, $N_{IN}x$, and TXSEL are decoded, clocked, level-translated, then sent to high-voltage output stage.

Differential clock input has two modes as shown below.

- LVDS CLK mode: Set CLKIF=0. Connect external 100Ω between CLK and CLKB. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: Set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. $P_{IN}x$, $N_{IN}x$ and TXSEL are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

2.2.2 Selecting Output Drivers

TXSEL selects either P1/N1 or P2/N2 high-voltage output stage commonly for all channels.

- P1/N1-driver selection for all channels: Set TXSEL=0.
- P2/N2-driver selection for all channels: Set TXSEL=1.

See Table 3 for the timing. See also Table 13 for the truth table.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	-	V_{LL}	V	
2	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LL}$	V	
3	Logic input capacitance	C_{IN}	-	3	-	pF	
4	Logic input high current	I_{IH}	-10	-	10	μA	
5	Logic input low current *1	I_{IL}	-10	-	10	μA	
6	Input rise/fall time	t_r, t_f	-	-	800	ps	CLK≥100MHz, CMOS CLK mode 10~90% CLK, CLKB, $P_{IN}x$, $N_{IN}x$, TXSEL
			-	-	2.0	ns	CLK<100MHz
7	Input clock frequency	f_{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB, $f_{CLK}=1/T$, $D_{CLK}=\tau/T$, See Fig.3
8	Clock duty cycle	D_{CLK}	40	50	60	%	
9	Data setup time	t_{SU_D}	1.4	-	-	ns	CLK mode, $P_{IN}x$,$N_{IN}x$ to CLK/CLKB See Fig.3
10	Data hold time	t_{HLD_D}	1.4	-	-	ns	
11	TXSEL setup time	t_{SU_S}	1.4	-	-	ns	CLK mode, TXSEL to CLK/CLKB See Fig.3
			1.4	-	-	ns	TP mode, TXSEL to $P_{IN}x$,$N_{IN}x$ See Fig.3
12	TXSEL hold time	t_{HLD_S}	1.4	-	-	ns	CLK mode, TXSEL to CLK/CLKB See Fig.3
			1.4	-	-	ns	TP mode, TXSEL to $P_{IN}x$,$N_{IN}x$ See Fig.3

NOTE:

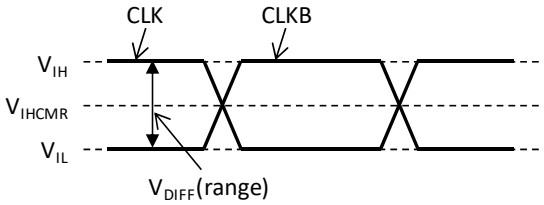
*1) EN, CC, CLKEN, and CLKIF have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V_{IH}	1.265	-	-	V	V_{IHCMR}(Typ)+V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	-	-	1.135	V	V_{IHCMR}(Typ)-V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	|CLK-CLKB| differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R_{IN}	85	100	115	Ω	External 100Ω
7	High-level input current	I_{IH}	-	-	5.8	mA	
8	Low-level input current	I_{IL}	-	-	5.8	mA	
9	Input rise/fall time	t_r, t_f	-	-	600	ps	20% to 80% of V_{DIFF}
10	Input clock frequency	f_{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.3
11	Clock duty cycle	D_{CLK}	40	50	60	%	

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range (V_{DIFF}(range))



Differential input voltage peak to peak swing (V_{DIFF}(p-p))

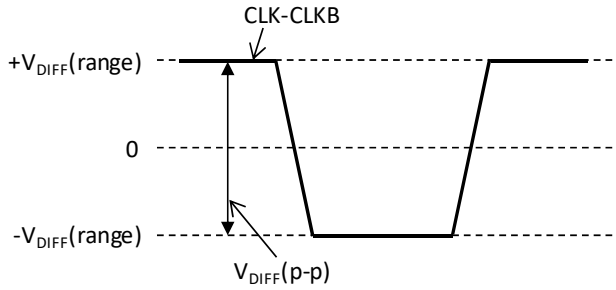
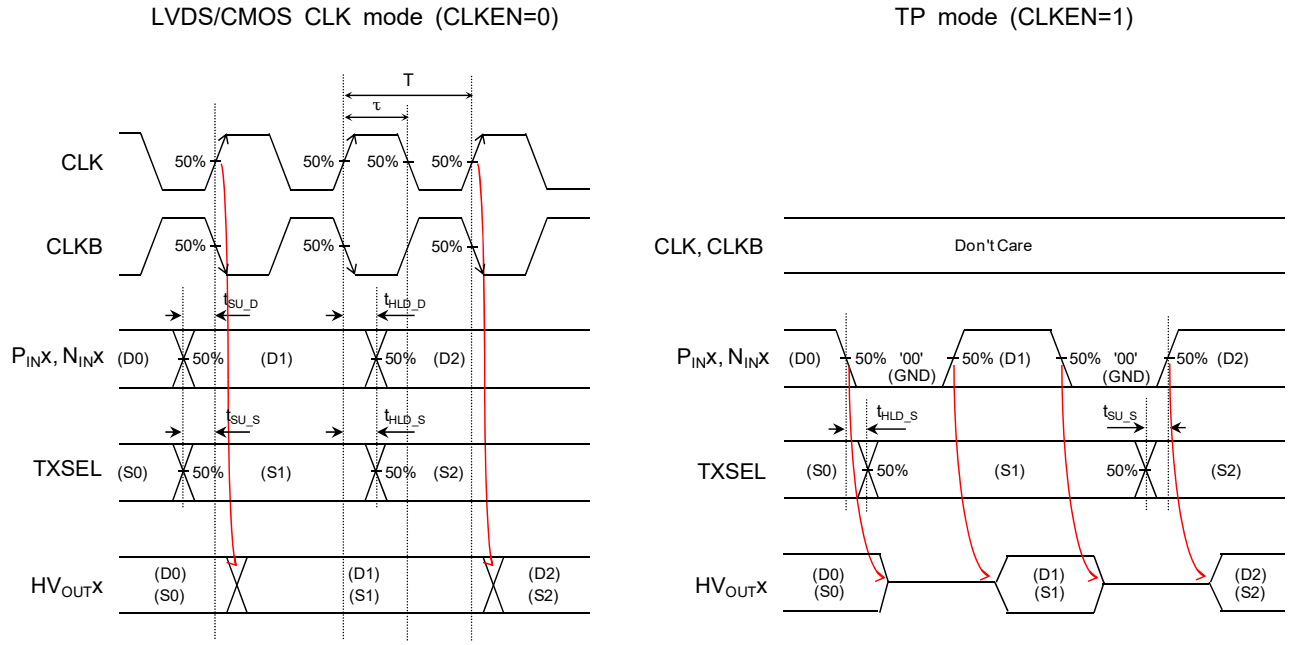


Fig.2 LVDS clock inputs



NOTE: (Sx, x=0,1,2,⋯) represents the selected drive. Either P1/N1 or P2/N2 drive is commonly selected for all channels.

Fig.3 Setup/Hold Time

2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outpus will be enabled.

3. Typical Application Circuit

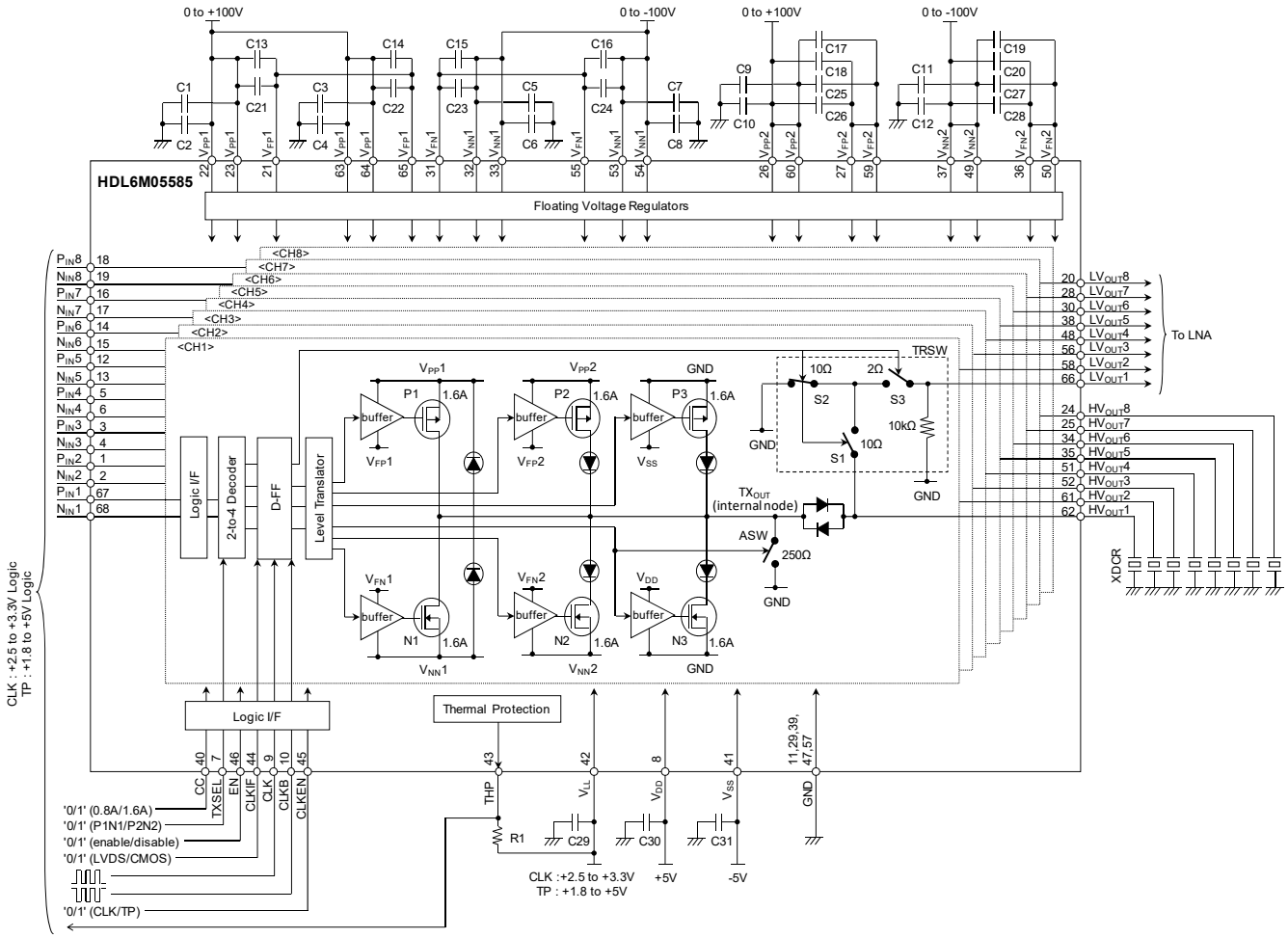


Fig.4 Typical Application Circuit

Note:

1. High-voltage power supply pins, $V_{PP}x/V_{NN}x$ (x=1,2), can draw fast transient currents up to ±1.6A. Therefore, ceramic capacitors of ≥200V 0.1μF to 1μF (C1~12) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 10μF (C13~20), ≥16V 100nF (C21~28), and ≥16V 0.1μF to 1μF (C29~31) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V_{FP}/V_{FN}, and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. External 100Ω should be connected between CLK and CLKB in LVDS CLK mode.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25ºC, CLK=CLKB=100MHz/0(CLKEN=0/1),
HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	V_{LL} current	TP	I_{LLQD}	-	0.03	-	mA	Quiescent current-1 EN=1(Disable) $P_{IN}x$=$N_{IN}x$=0 Current mode 1 (CC=1) $V_{PP}1$/$V_{NN}1$=+/-100V $V_{PP}2$/$V_{NN}2$=+/-100V
		LVDS CLK		-	0.13	-	mA	
		CMOS CLK		-	0.08	-	mA	
2	V_{DD} current	TP	I_{DDQD}	-	3.3	-	mA	
		LVDS CLK		-	3.3	-	mA	
		CMOS CLK		-	3.3	-	mA	
3	V_{SS} current		I_{SSQD}	-	1.0	-	mA	
4	$V_{PP}1$ current		I_{PP1QD}	-	0.03	-	mA	
5	$V_{NN}1$ current		I_{NN1QD}	-	0.03	-	mA	
6	$V_{PP}2$ current		I_{PP2QD}	-	0.05	-	mA	
7	$V_{NN}2$ current		I_{NN2QD}	-	0.05	-	mA	
8	V_{LL} current	TP	I_{LLQE}	-	0.08	-	mA	Quiescent current-2 EN=0(Enable) $P_{IN}x$=$N_{IN}x$=0 Current mode 1 (CC=1) $V_{PP}1$/$V_{NN}1$=+/-100V $V_{PP}2$/$V_{NN}2$=+/-100V
		LVDS CLK		-	0.18	-	mA	
		CMOS CLK		-	0.13	-	mA	
9	V_{DD} current	TP	I_{DDQE}	-	11	-	mA	
		LVDS CLK		-	33	-	mA	
		CMOS CLK		-	30	-	mA	
10	V_{SS} current		I_{SSQE}	-	10	-	mA	
11	$V_{PP}1$ current		I_{PP1QE}	-	0.15	-	mA	
12	$V_{NN}1$ current		I_{NN1QE}	-	0.15	-	mA	
13	$V_{PP}2$ current		I_{PP2QE}	-	0.17	-	mA	
14	$V_{NN}2$ current		I_{NN2QE}	-	0.17	-	mA	
15	V_{LL} current	TP	I_{LLPW}	-	0.18	-	mA	PW operating current EN=0 Current mode 1 (CC=1) 8-channel active Bipolar 3-level 2-cycle P1/N1-drive f=5MHz, PRT=200µs $V_{PP}1$/$V_{NN}1$=+/-60V $V_{PP}2$/$V_{NN}2$=+/-60V
		LVDS CLK		-	0.18	-	mA	
		CMOS CLK		-	0.13	-	mA	
16	V_{DD} current	TP	I_{DDPW}	-	11	-	mA	
		LVDS CLK		-	37	-	mA	
		CMOS CLK		-	35	-	mA	
17	V_{SS} current		I_{SSPW}	-	10	-	mA	
18	$V_{PP}1$ current		I_{PP1PW}	-	4.0	-	mA	
19	$V_{NN}1$ current		I_{NN1PW}	-	4.6	-	mA	
20	$V_{PP}2$ current		I_{PP2PW}	-	0.17	-	mA	
21	$V_{NN}2$ current		I_{NN2PW}	-	0.17	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
22	V_{LL} current	TP	I_{LLCW3}	-	0.43	-	mA	CW operating current-1 EN=0 Current mode 1 (CC=1) 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V
		LVDS CLK		-	0.53	-	mA	
		CMOS CLK		-	0.48	-	mA	
23	V_{DD} current	TP	I_{DDCW3}	-	39	-	mA	
		LVDS CLK		-	60	-	mA	
		CMOS CLK		-	58	-	mA	
24	V_{SS} current		I_{SSCW3}	-	26	-	mA	
25	$V_{PP}1$ current		I_{PP1CW3}	-	0.15	-	mA	
26	$V_{NN}1$ current		I_{NN1CW3}	-	0.15	-	mA	
27	$V_{PP}2$ current		I_{PP2CW3}	-	171	-	mA	
28	$V_{NN}2$ current		I_{NN2CW3}	-	173	-	mA	
29	V_{LL} current	TP	I_{LLCW1}	-	0.48	-	mA	CW operating current-2 EN=0 Current mode 0 (CC=0) 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
30	V_{DD} current	TP	I_{DDCW1}	-	31	-	mA	
		LVDS CLK		-	53	-	mA	
		CMOS CLK		-	51	-	mA	
31	V_{SS} current		I_{SSCW1}	-	19	-	mA	
32	$V_{PP}1$ current		I_{PP1CW1}	-	0.15	-	mA	
33	$V_{NN}1$ current		I_{NN1CW1}	-	0.15	-	mA	
34	$V_{PP}2$ current		I_{PP2CW1}	-	153	-	mA	
35	$V_{NN}2$ current		I_{NN2CW1}	-	155	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	$HV_{OUT}x$ output voltage range	$HV_{OUT}x$	-100	-	+100	V	
2	$HV_{OUT}x$ high-side peak current	I_{OH}	-	1.6	-	A	P1 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
			-	1.6	-	A	P2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 1 (CC=1)
			-	0.8	-	A	P2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 0 (CC=0)
3	$HV_{OUT}x$ high-side GND clamp peak current	I_{OHCL}	-	1.6	-	A	N3 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
4	$HV_{OUT}x$ low-side peak current	I_{OL}	-	1.6	-	A	N1 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
			-	1.6	-	A	N2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 1 (CC=1)
			-	0.8	-	A	N2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 0 (CC=0)
5	$HV_{OUT}x$ low-side GND clamp peak current	I_{OLCL}	-	1.6	-	A	P3 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
6	$HV_{OUT}x$ high-side on-resistance	R_{ONH}	-	15	-	Ω	P1 active, I_{OH}=100mA
			-	15	-	Ω	P2 active, I_{OH}=100mA Current mode 1 (CC=1)
			-	23	-	Ω	P2 active, I_{OH}=100mA Current mode 0 (CC=0)
7	$HV_{OUT}x$ high-side GND clamp on-resistance	R_{ONHCL}	-	15	-	Ω	N3 active, I_{OHCL}=100mA
8	$HV_{OUT}x$ low-side on-resistance	R_{ONL}	-	15	-	Ω	N1 active, I_{OL}=100mA
			-	15	-	Ω	N2 active, I_{OL}=100mA Current mode 1 (CC=1)
			-	23	-	Ω	N2 active, I_{OL}=100mA Current mode 0 (CC=0)
9	$HV_{OUT}x$ low-side GND clamp on-resistance	R_{ONLCL}	-	15	-	Ω	P3 active, I_{OLCL}=100mA
10	$HV_{OUT}x$ off-capacitance	C_{HVOFF}	-	34	-	pF	$TX_{OUT}x$=GND, TRSW=off

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V, T_A=25ºC, CC=1,
CLK=CLKB=100MHz/0(CLKEN=0/1), HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions	
				Min	Typ	Max			
1	Output frequency		f_{OUT}	-	20	-	MHz		
2	Output rise propagation delay	TP mode	t_{dr}	-	28	-	ns	See Fig.5	
		CLK mode		-	36	-	ns		
3	Output fall propagation delay	TP mode	t_{df}	-	28	-	ns		
		CLK mode		-	36	-	ns		
4	Output rise propagation delay clamp	TP mode	t_{drCL}	-	28	-	ns		
		CLK mode		-	36	-	ns		
5	Output fall propagation delay clamp	TP mode	t_{dfCL}	-	28	-	ns		
		CLK mode		-	36	-	ns		
6	Propagation delay matching		Δt_d	-	±1	±3	ns		
7	Output rise time		t_r	-	19	-	ns	P1 active	See Fig.5
				-	19	-	ns	P2 active, CC=1	
				-	36	-	ns	P2 active, CC=0	
			t_{rCL}	-	10	-	ns	P3 active	
8	Output fall time		t_f	-	19	-	ns	N1 active	
				-	19	-	ns	N2 active, CC=1	
				-	36	-	ns	N2 active, CC=0	
			t_{fCL}	-	10	-	ns	N3 active	
9	2nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f_{OUT}=5MHz See Fig.6	
10	Pulse cancellation		HDPC	-	-40	-	dBc		
			HDPC2	-	-40	-	dBc		
11	RMS output jitter		t_J	-	10	-	ps	Bipolar CW, f_{OUT}=5MHz $V_{PP}1/V_{NN}1= V_{PP}2/V_{NN}2$=+/-5V	
12	Crosstalk between channels		X_{TLK}	-	-70	-	dB	f_{OUT}=5MHz, $10V_{p-p}$, HV_{OUT} load=50Ω	
13	Output enable time	TP	t_{EN}	-	28	-	ns	See Fig.7	
		LVDS CLK		-	115	-	ns		
		CMOS CLK		-	140	-	ns		
14	Output disable time		t_{DS}	-	36	-	ns		
15	Clock mode enable time		t_{CLKEN}	-	36	-	ns		
16	Clock mode disable time		t_{CLKDS}	-	36	-	ns		

4.4 Integrated Peripheral Circuits Characteristics

T/R Switch

Table 8 T/R Switch Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	$LV_{OUT}x$ output voltage range	$LV_{OUT}x$	-0.85	-	0.85	V	
2	TRSW on-resistance	R_{ONTR}	-	12	-	Ω	$HV_{OUT}x$=100mV, $LV_{OUT}x$=0V
3	TRSW on-capacitance	C_{ONTR}	-	13	-	pF	$LV_{OUT}x$=0V
4	TRSW off-resistance on HVOUTx	$R_{OFFTRHV}$	1	-	-	MΩ	
5	TRSW off-resistance on LVOUTx	$R_{OFFTRLV}$	8	10	12	kΩ	
6	Spike voltage on $HV_{OUT}x$ and $LV_{OUT}x$	V_{TRN}	-	-	50	mV_{PP}	50pF//200Ω load on $HV_{OUT}x$ 20pF//200Ω load on $LV_{OUT}x$
7	TRSW turn-on time	t_{dTRON}	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.8
8	TRSW turn-off time	t_{dTROFF}	-	50	100	ns	See Fig.8
9	Tx setup time	t_{TXSU}	100	-	-	ns	$P_{IN}x=N_{IN}x$=0 (GND) for at least 100ns before Tx burst. See Fig.8

Analog Switch

Table 9 Analog Switch Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R_{ONASW}	-	250	-	Ω	

HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FHVD}	-	1.0	-	V	I_F=100mA
			-	1.2	-	V	I_F=200mA
2	Reverse voltage	V_{RHVD}	200	-	-	V	I_R=1μA

LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FLVD}	-	1.1	-	V	I_F=100mA
			-	1.25	-	V	I_F=200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=2.5V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

5. Switching Time Diagram

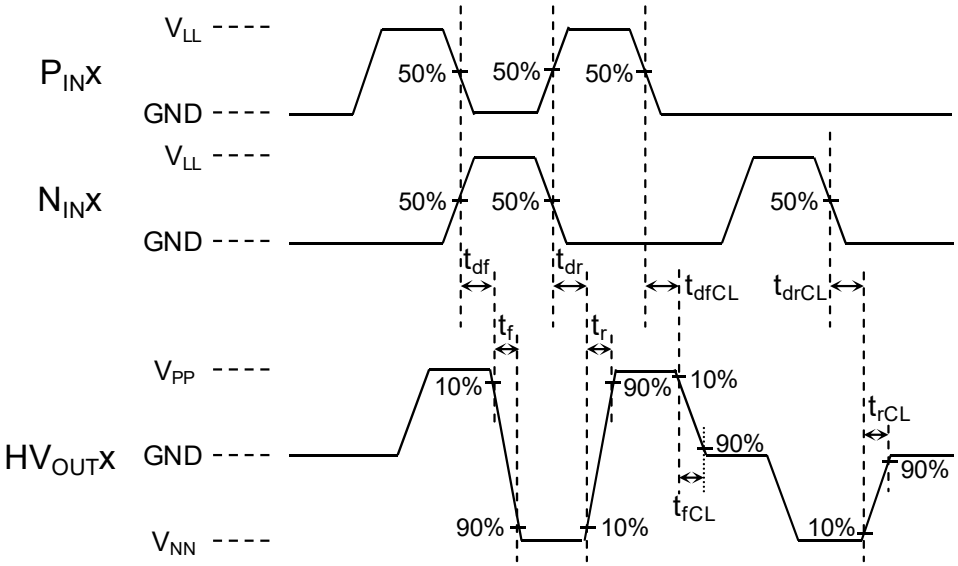
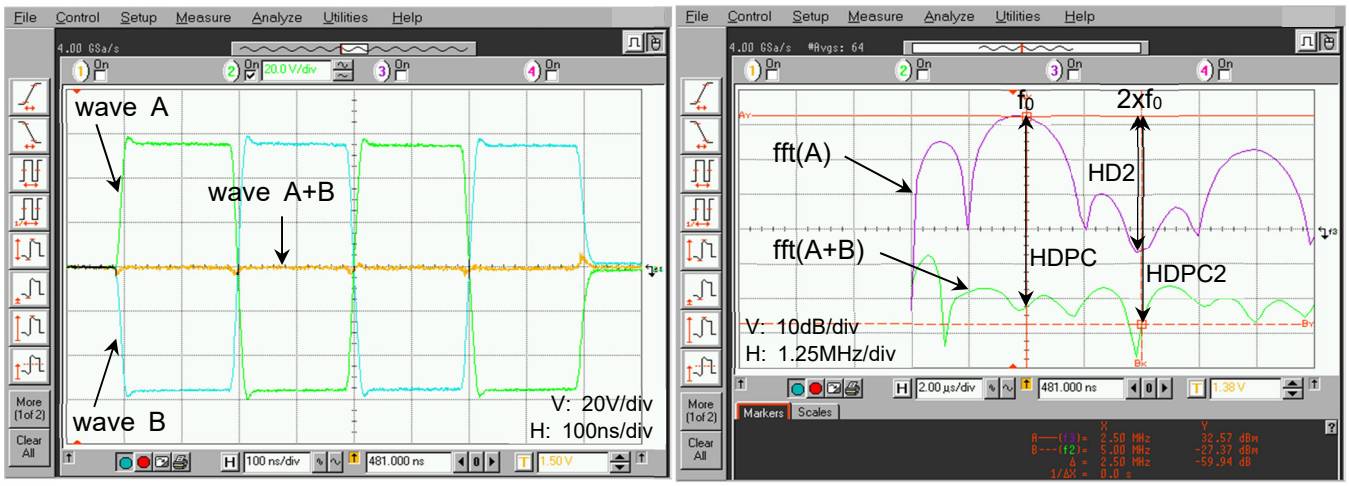


Fig.5 Propagation delay and Output rise/fall time



Example waveforms: VPP/VNN=+/-60V, f_0=2.5MHz, 2-cycle, HV_{OUT} load=220pF//200Ω

Fig.6 2nd harmonic distortion and Pulse cancellation

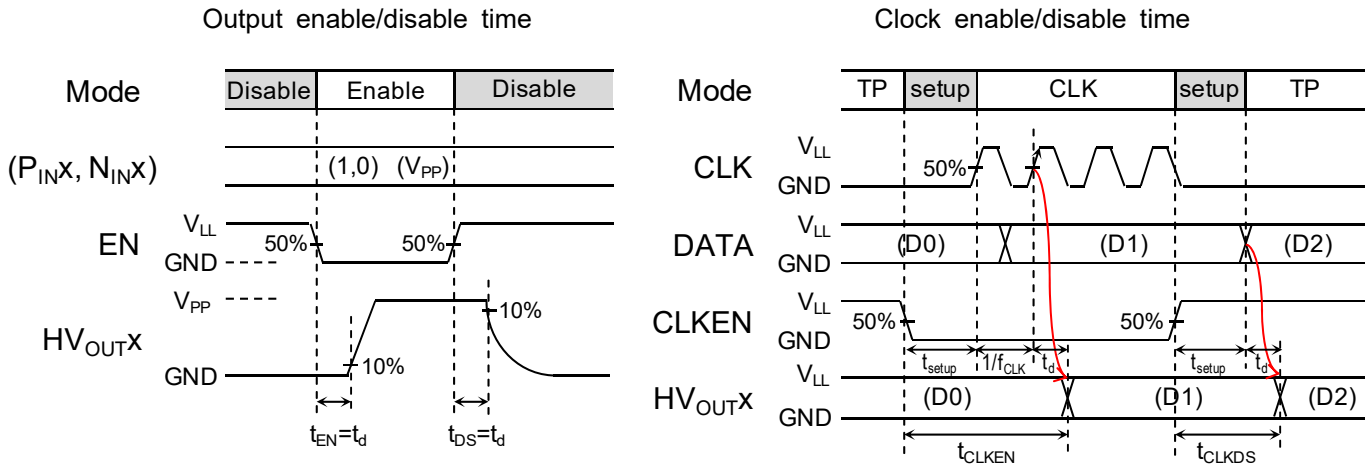


Fig.7 Output enable/disable and Clock enable/disable time

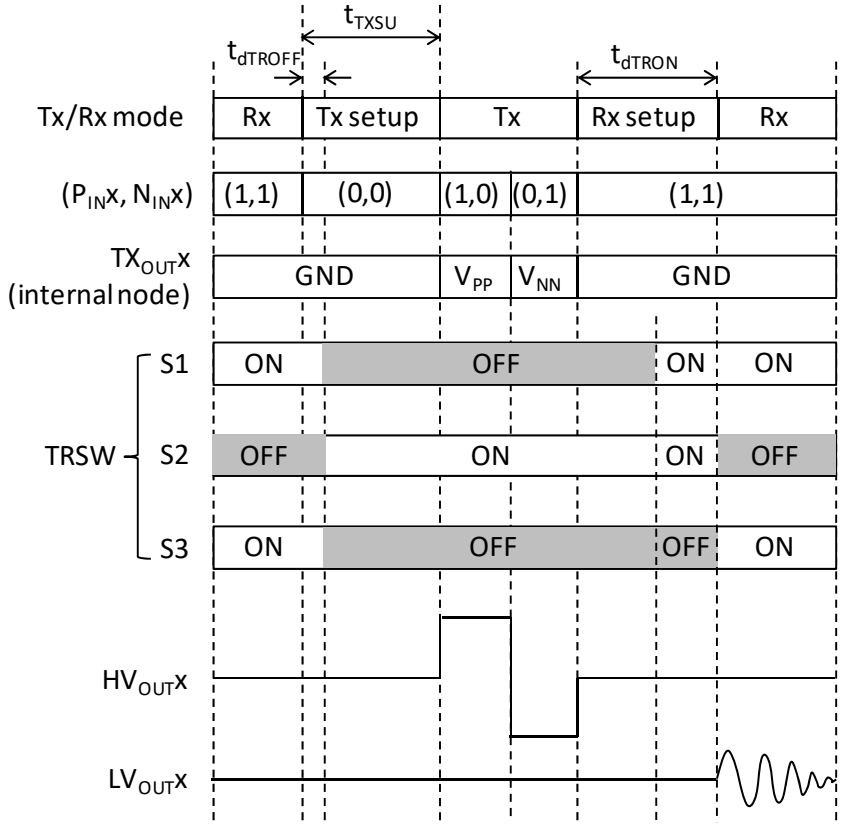


Fig.8 T/R Switch turn-on/off time

6. Truth Table and Mode Control table

Table 13 Truth table

Logic Inputs				Internal MOSFET state										Output state	
EN	**TXSEL**	**$P_{IN}x$**	**$N_{IN}x$**	**P1**	**N1**	**P2**	**N2**	**P3**	**N3**	**ASW**	**TRSW**			**$TX_{OUT}x$**	**$LV_{OUT}x$**
				+HV1	-HV1	+HV2	-HV2	GND	GND	GND	S1	S2	S3	(internal node)	
0	0	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	OFF	**ON**	OFF	GND	10kΩ
0	0	0	1	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	-HV1	10kΩ
0	0	1	0	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	+HV1	10kΩ
0	0	1	1	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**	GND	$HV_{OUT}x$
0	1	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	OFF	**ON**	OFF	GND	10kΩ
0	1	0	1	OFF	OFF	OFF	**ON**	OFF	OFF	OFF	OFF	**ON**	OFF	-HV2	10kΩ
0	1	1	0	OFF	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	+HV2	10kΩ
0	1	1	1	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**	GND	$HV_{OUT}x$
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	HiZ	10kΩ

Note: $V_{PP}1$/ $V_{NN}1$=+/-HV1, $V_{PP}2$/ $V_{NN}2$=+/-HV2, x=1~8

Table 14 P2/N2 drive current mode

		Iout [A]	
Current Mode	CC	P2	N2
0	0	0.8	0.8
1	1	1.6	1.6

Note:
Recommended mode is as follows:

- Current mode 1 for high-amplitude short cycle pulse waveforms, or for driving a heavy load
- Current mode 0 for low-amplitude long pulse train waveforms (e.g. CW), or for driving a light load

7. Pin Configuration

Table 15 Pin Configuration

Pin#	Pin Name	I/O	Function
1	$P_{IN}2$	I	Logic input of channel 2
2	$N_{IN}2$	I	Logic input of channel 2
3	$P_{IN}3$	I	Logic input of channel 3
4	$N_{IN}3$	I	Logic input of channel 3
5	$P_{IN}4$	I	Logic input of channel 4
6	$N_{IN}4$	I	Logic input of channel 4
7	TXSEL	I	Control of output drive selection, Hi=P2/N2, Low=P1/N1
8	V_{DD}	-	Positive low voltage power supply (+5V)
9	CLK	I	Positive clock input (up to 200MHz)
10	CLKB	I	Negative clock Input (up to 200MHz)
11	GND	-	Drive power ground (0V)
12	$P_{IN}5$	I	Logic input of channel 5
13	$N_{IN}5$	I	Logic input of channel 5
14	$P_{IN}6$	I	Logic input of channel 6
15	$N_{IN}6$	I	Logic input of channel 6
16	$P_{IN}7$	I	Logic input of channel 7
17	$N_{IN}7$	I	Logic input of channel 7
18	$P_{IN}8$	I	Logic input of channel 8
19	$N_{IN}8$	I	Logic input of channel 8
20	$LV_{OUT}8$	O	Low voltage output of channel 8
21	$V_{FP}1$	-	Built-in power supply for P-MOS (P1) gate drive
22	$V_{PP}1$	-	Positive high voltage power supply 1 (0 to +100V)
23	$V_{PP}1$	-	Positive high voltage power supply 1 (0 to +100V)
24	$HV_{OUT}8$	O	High voltage output of channel 8
25	$HV_{OUT}7$	O	High voltage output of channel 7
26	$V_{PP}2$	-	Positive high voltage power supply 2 (0 to +100V)
27	$V_{FP}2$	-	Built-in power supply for P-MOS (P2) gate drive
28	$LV_{OUT}7$	O	Low voltage output of channel 7
29	GND	-	Drive power ground (0V)
30	$LV_{OUT}6$	O	Low voltage output of channel 6
31	$V_{FN}1$	-	Built-in power supply for N-MOS (N1) gate drive
32	$V_{NN}1$	-	Negative high voltage power supply 1 (0 to -100V)
33	$V_{NN}1$	-	Negative high voltage power supply 1 (0 to -100V)
34	$HV_{OUT}6$	O	High voltage output of channel 6

Table 15 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
35	$HV_{OUT}5$	O	High voltage output of channel 5
36	$V_{FN}2$	-	Built-in power supply for N-MOS (N2) gate drive
37	$V_{NN}2$	-	Negative high voltage power supply 2 (0 to -100V)
38	$LV_{OUT}5$	O	Low voltage output of channel 5
39	GND	-	Drive power ground (0V)
40	CC	I	Control of P2/N2 drive current, Hi=1.6A, Low=0.8A (50kΩ internal pull-up resistor)
41	V_{SS}	-	Negative low voltage power supply (-5V)
42	V_{LL}	-	Positive voltage supply of logic input interface (1.8 to 5V)
43	THP	O	Thermal protection output flag, open N-MOS drain
44	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50kΩ internal pull-up resistor)
45	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
46	EN	I	Control of drive output enable, Hi=disable, Low=enable (50kΩ internal pull-up resistor)
47	GND	-	Drive power ground (0V)
48	$LV_{OUT}4$	O	Low voltage output of channel 4
49	$V_{NN}2$	-	Negative high voltage power supply 2 (0 to -100V)
50	$V_{FN}2$	-	Built-in power supply for N-MOS (N2) gate drive
51	$HV_{OUT}4$	O	High voltage output of channel 4
52	$HV_{OUT}3$	O	High voltage output of channel 3
53	$V_{NN}1$	-	Negative high voltage power supply 1 (0 to -100V)
54	$V_{NN}1$	-	Negative high voltage power supply 1 (0 to -100V)
55	$V_{FN}1$	-	Built-in power supply for N-MOS (N1) gate drive
56	$LV_{OUT}3$	O	Low voltage output of channel 3
57	GND	-	Drive power ground (0V)
58	$LV_{OUT}2$	O	Low voltage output of channel 2
59	$V_{FP}2$	-	Built-in power supply for P-MOS (P2) gate drive
60	$V_{PP}2$	-	Positive high voltage power supply 2 (0 to +100V)
61	$HV_{OUT}2$	O	High voltage output of channel 2
62	$HV_{OUT}1$	O	High voltage output of channel 1
63	$V_{PP}1$	-	Positive high voltage power supply 1 (0 to +100V)
64	$V_{PP}1$	-	Positive high voltage power supply 1 (0 to +100V)
65	$V_{FP}1$	-	Built-in power supply for P-MOS (P1) gate drive
66	$LV_{OUT}1$	O	Low voltage output of channel 1
67	$P_{IN}1$	I	Logic input of channel 1
68	$N_{IN}1$	I	Logic input of channel 1

■ Package

Table 16 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-68(1010)B	QN068-B-P-SD	QFN10x10-T-SD	QN068-B-M-S2	QN068-B-L-SD	QN068-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Fig. 9 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

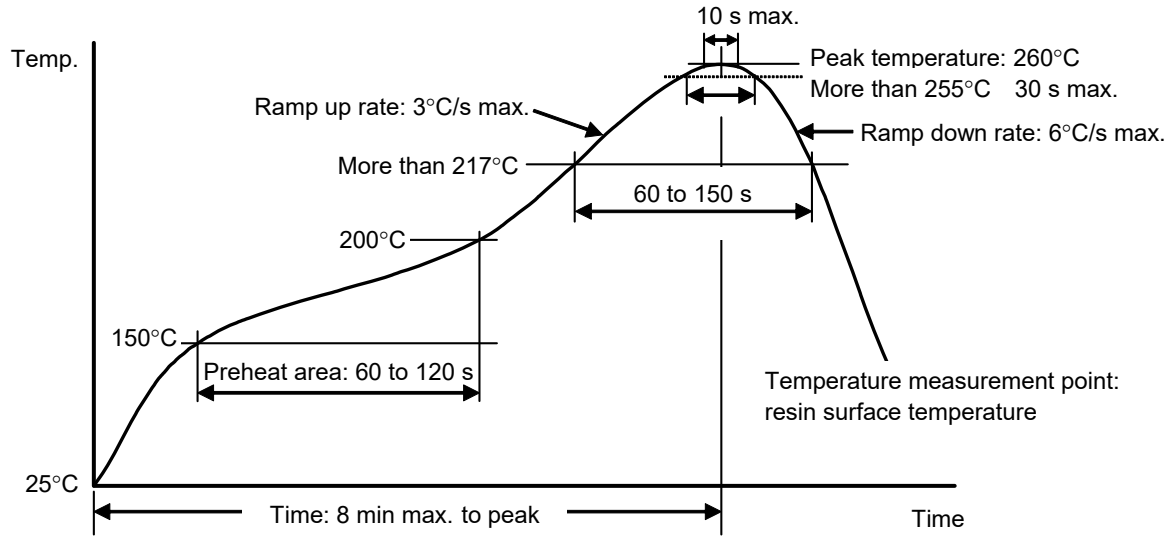


Fig. 9 Resistance to Soldering Heat Condition for Package (Reflow Method)

■ Important Notice

1. ABLIC Inc. warrants performance of its hardware products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent ABLIC Inc. needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before such claim shall not be counted for such response.

3. ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

4. ABLIC Inc. reserves the right to make changes to the Product Specification at any time and to discontinue mass production of the relevant products without notice. Customers are advised before placing orders to confirm that the Product Specification of inquiry is the latest version and that the relevant product is currently on mass production status.

5. In no event shall ABLIC Inc. be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to the Product Specification. ABLIC Inc. assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in the Product Specification.

6. No license is granted by the Product Specification under any patents or other rights of any third party or ABLIC Inc.

7. The Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of ABLIC Inc.

8. Resale of ABLIC Inc. products with statements different from or beyond the parameters described in the Product Specification voids all express and any implied warranties for the products, and is an unfair and deceptive business practice. ABLIC Inc. is not responsible or liable for any such statements.

9. Products (technologies) described in the Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting those products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

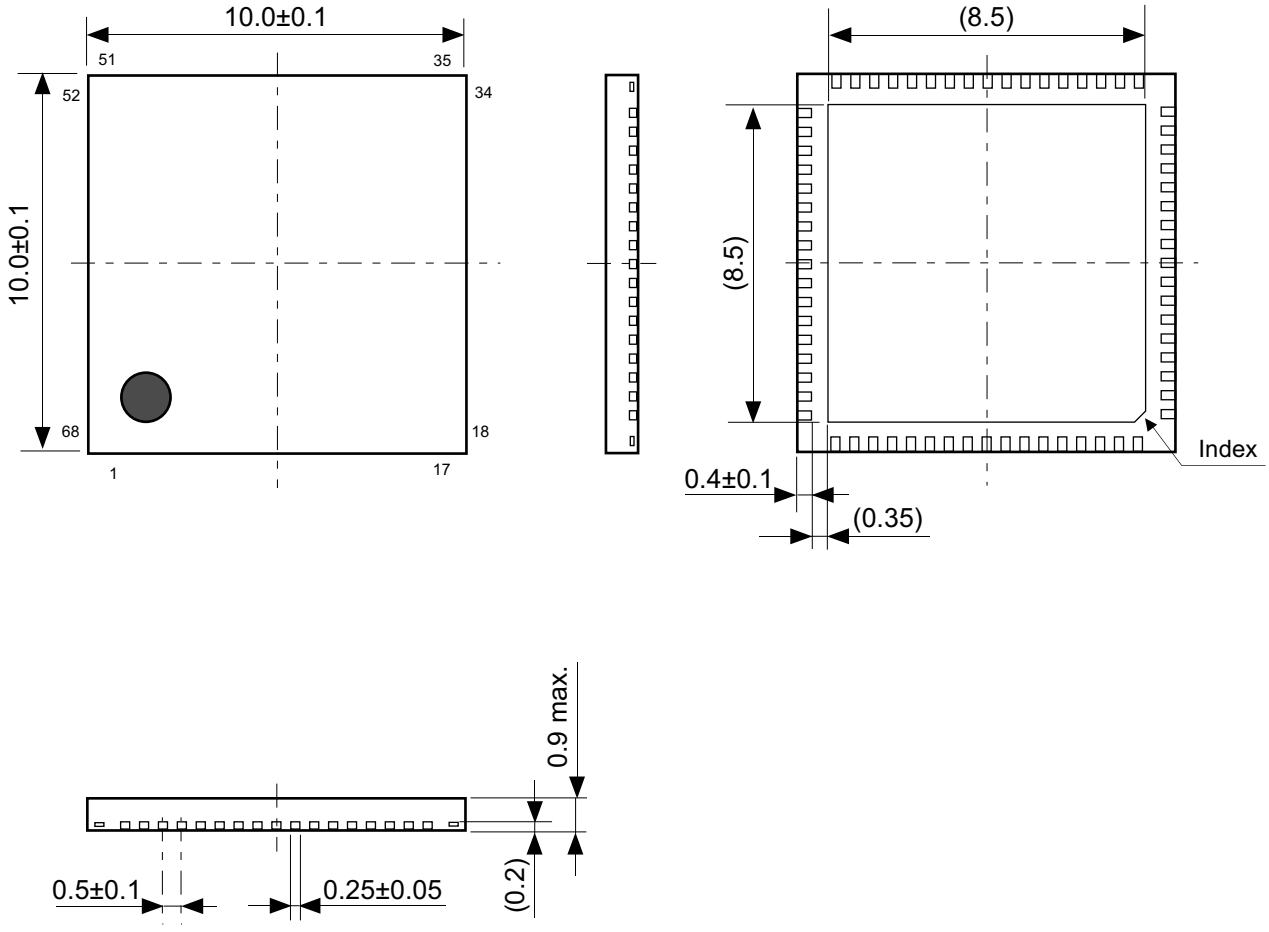
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

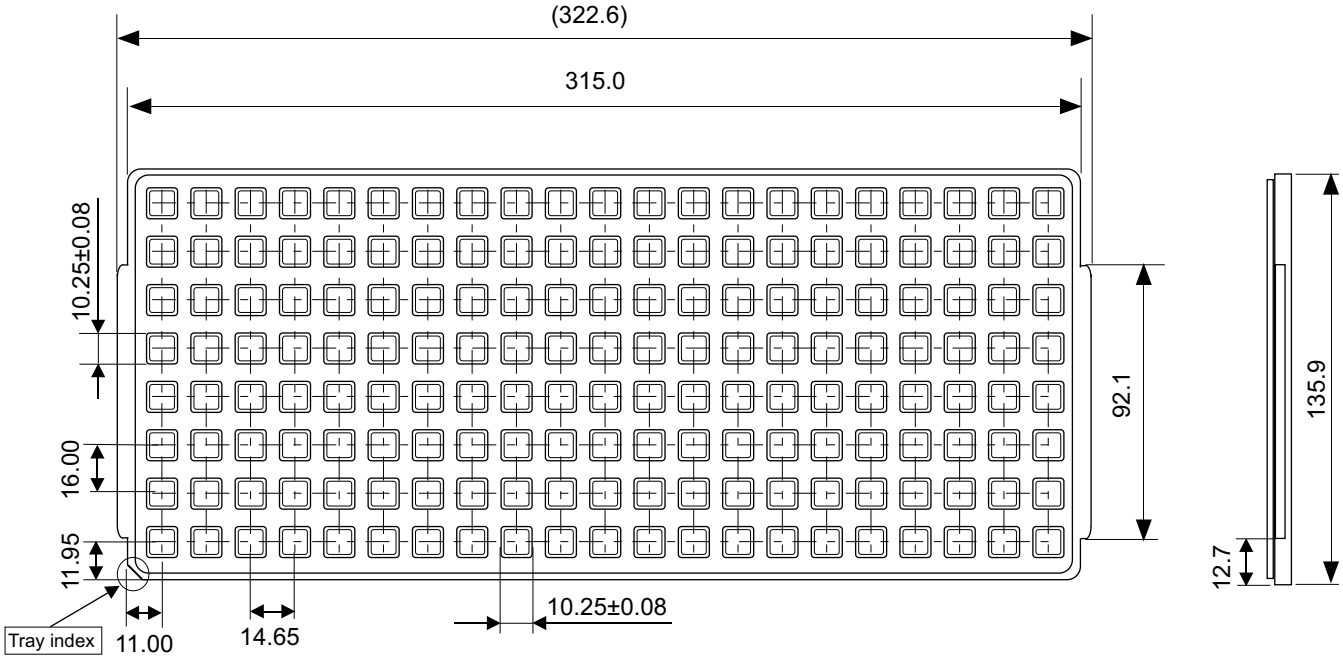
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

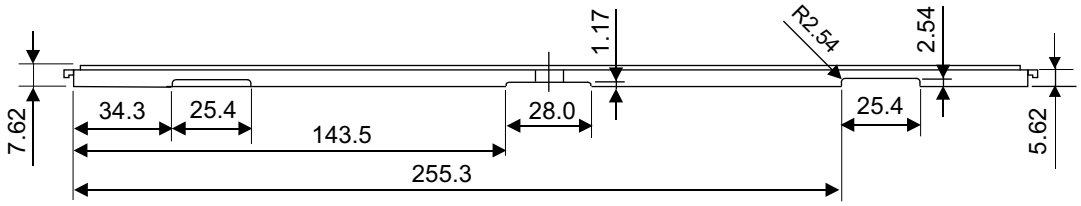
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.



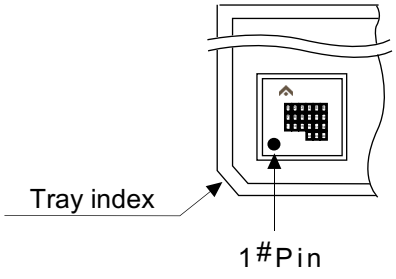
No. QN068-B-P-SD-2.0

TITLE	QFN68-B-PKG Dimensions
No.	QN068-B-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	





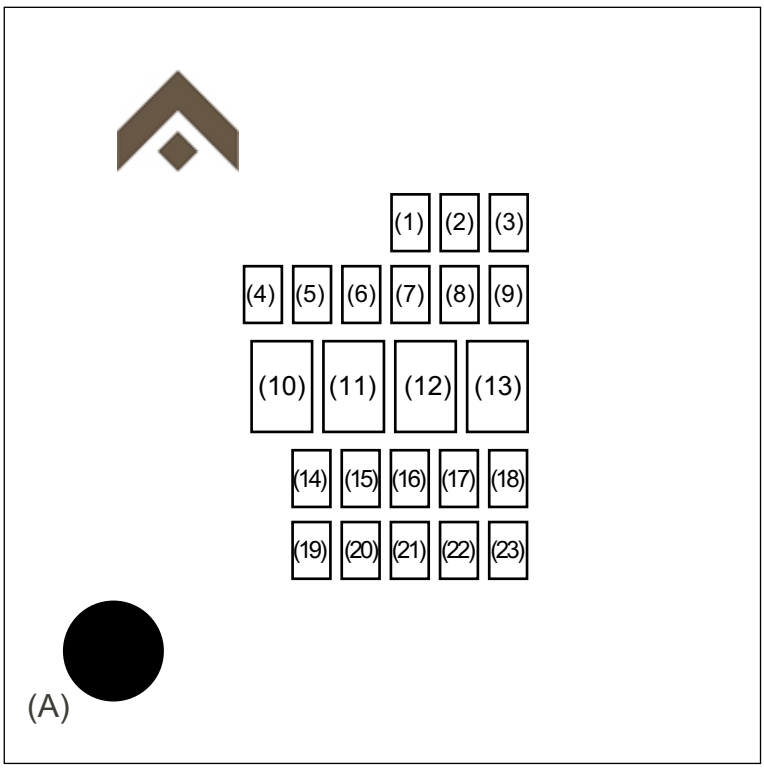
(Direction of IC in tray)



No. QFN10x10-T-SD-1.0

TITLE	QFN10x10-B-Tray		
No.	QFN10x10-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		

ABLIC Inc.



(1) : Year of assembly

(2) : Month of assembly

(3) : Week of assembly

(4) to (13) : Product code

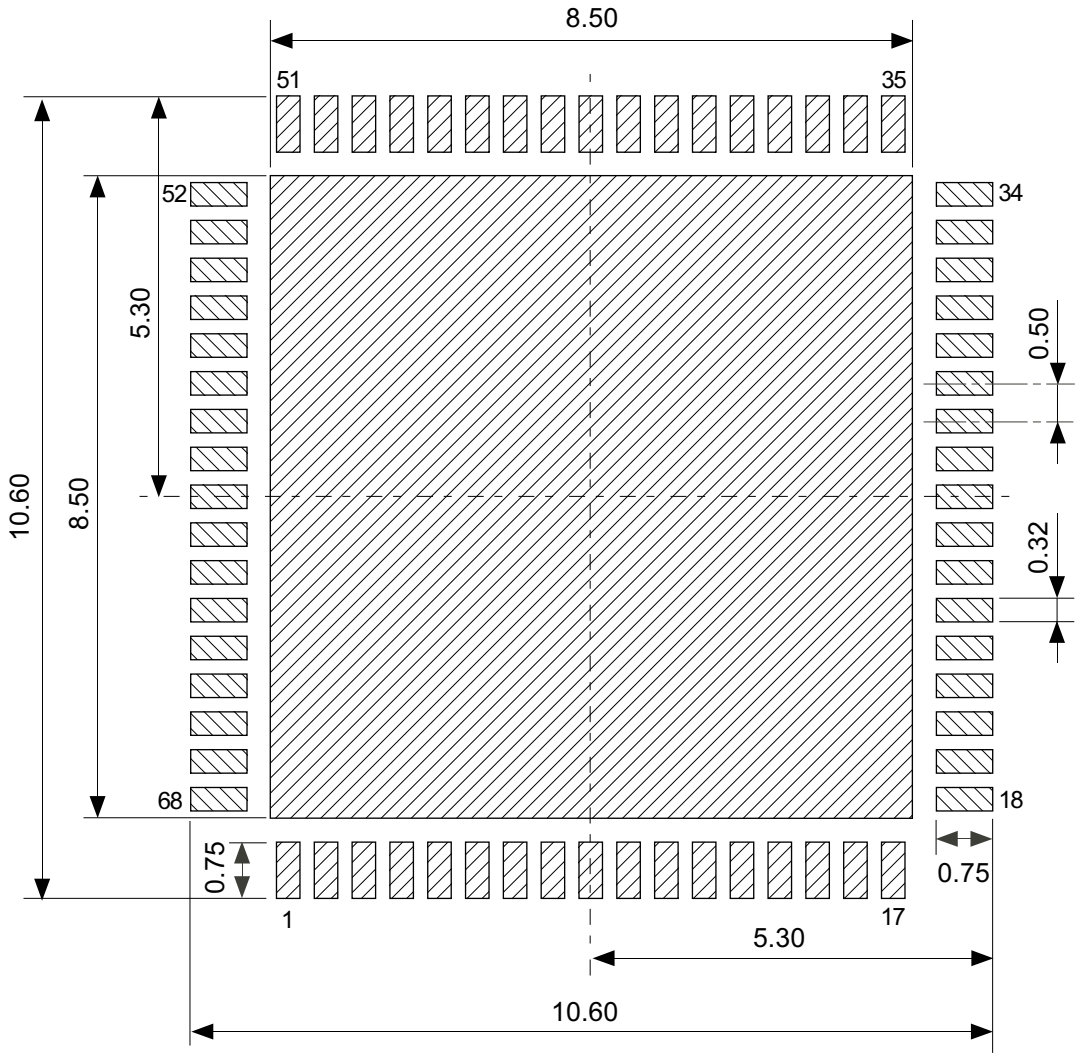
(14) to (23) : Quality control code

(A) : 1-pin mark

No. QN068-B-M-S2-1.0

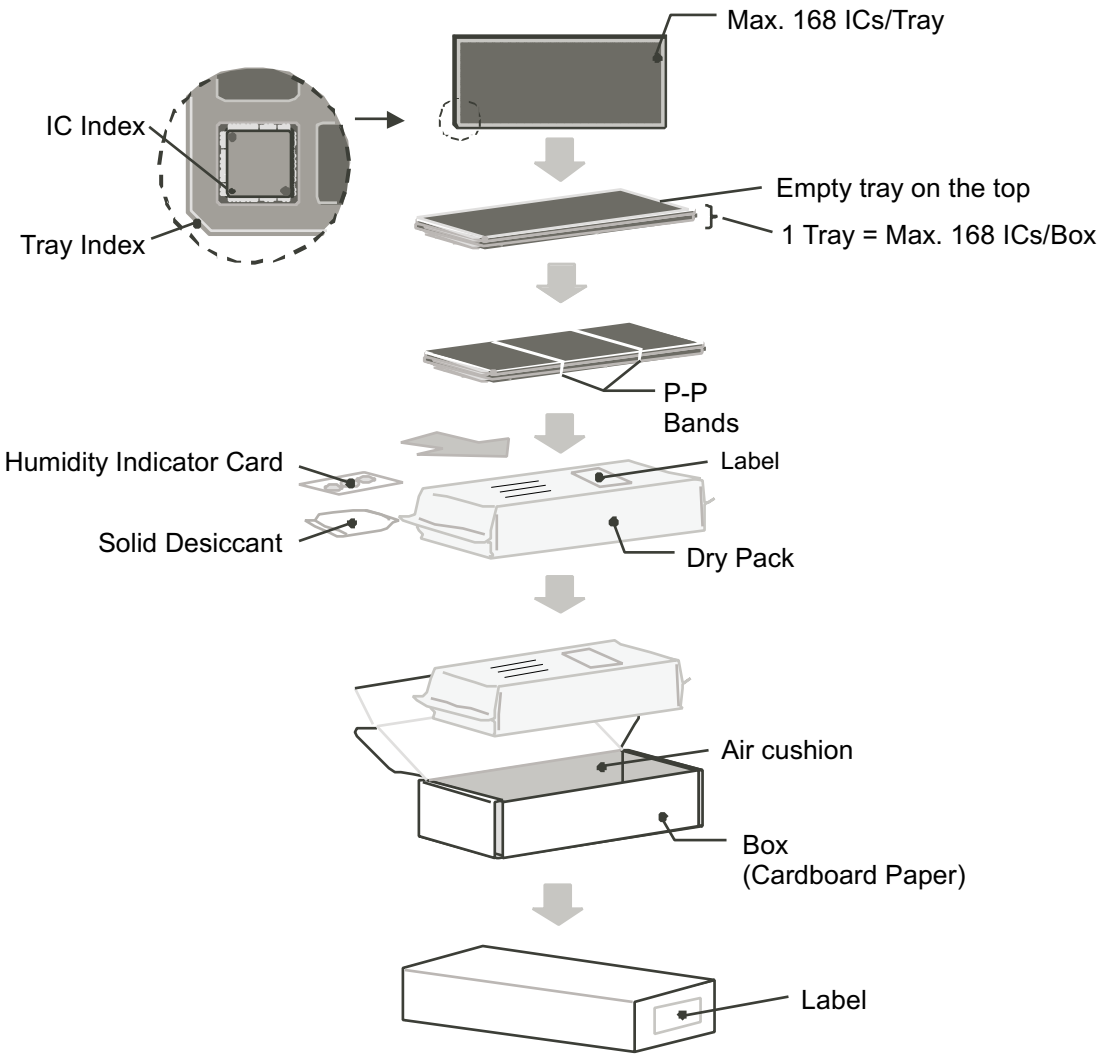
TITLE	QFN68-B-Markings (S-UM5585)		
No.	QN068-B-M-S2-1.0		
ANGLE			
UNIT		TYPE	LASER

ABLIC Inc.



No. QN068-B-L-SD-2.0

TITLE	QFN68-B -Land Recommendation
No.	QN068-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN068-B-K-SD-1.0

TITLE	QFN68-B -Packing Procedure
No.	QN068-B-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ABLIC:

HDL6M05585