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FAN7318 — LCD Backlight Inverter Drive

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The FAN7318 is a LCD backlight inverter drive IC that controls P-N half-bridge topology.

Description

The FAN7318 provides a low-cost solution and reduces external components by integrating proprietary wave rectifiers for open-lamp protection and regulation. The operating voltage range of the FAN7318 is wide, so an external regulator isn't necessary to supply the voltage to the IC.

The FAN7318 provides various protections, such as open-lamp regulation, open-lamp protection, short-Lamp protection, CMP-high protection, and FB-high protection, to increase the system reliability. The FAN7318 provides burst dimming and analog dimming.

The FAN7318 is available in a 20-SOIC package.

Part Number	Operating Temperature	Package	Packing Method
FAN7318M	N7318M	20 Load Small Outling Integrated Circuit (SOIC)	Rail
FAN7318MX -25 to +85 °C			Tape & Reel

LCD Backlight Inverter Drive IC

Features

- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 6V to 30V
- Backlight Lamp Ballast and Soft Dimming
- Minimal External Components Required
- Precision Voltage Reference Trimmed to 2%
- -Half-Bridge Topology
- Soft-Start
- PWM Control at Fixed Frequency
- Analog Dimming Function
- -**Burst Dimming Function**
- -Programmable Striking Frequency
- **Open-Lamp Protection**
- **Open-Lamp Regulation**
- -Short-Lamp Protection
- **CMP-High Protection**
- **FB-High Protection**
- Thermal Shutdown
- 20-Pin SOIC

Applications

- LCD TV
- LCD Monitor

Ordering Information



FAIRCHILD SEMICONDUCTOR

FAN7318





Pin Definitions

Pin #	Name	Description		
1	TIMER	This pin is for protection delay time setting.		
2	CMP	Error amplifier output. Typically, a compensation capacitor is connected to this pin from the ground.		
3	ADIM	This pin is the input for negative analog dimming.		
4	СТ	This pin is for programming the switching frequency. Typically, a capacitor is connected to this pin from ground and a resistor is connected to this pin from the REF pin.		
5	REF	This pin is 5V reference output. Typically, resistors are connected to this pin from the CT pin and the BCT pin.		
6	ВСТ	This pin is for programming the frequency of the burst dimming. Typically, a capacitor is connected to this pin from ground and a resistor is connected to this pin from the REF pin.		
7	BDIM	This pin is the input for negative burst dimming. The voltage range of 0.5 to 2V at this pin controls burst mode duty cycle from 0% to 100%.		
8	ENA	This pin is for turning on/off the IC.		
9	GND	This pin is the ground.		
10	OUTB	This pin is NMOS gate-drive output.		
11	OUTA	This pin is PMOS gate-drive output.		
12	VIN	This pin is the supply voltage of the IC.		
13	OLR4	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.		
14	OLP4	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.		
15	OLR3	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.		
16	OLP3	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.		
17	OLR2	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.		
18	OLP2	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.		
19	OLR1	This pin is for open-lamp regulation and short-lamp protection. It has the same functions as other OLR pins and is connected to the full-wave rectifier internally. When the maximum of rectified OLR inputs is between 1.34V and 2V, the error amplifier output current is limited to 3.2µA; and when the maximum of rectified OLR inputs reaches 2V, the error amplifier output current is 0.4 and its output voltage maintains constant. The maximum of rectified OLR inputs is inputted to the negative of another error amplifier for feedback control of lamp voltage. When the maximum of rectified OLR inputs is more than 2.2V, another error amplifier for OLR is operating and lamp voltage is regulated. In normal mode, if the maximum of rectified OLR inputs is higher than 1.35V or if the minimum of rectified OLR inputs is lower than 0.3V for a predetermined time by the TIMER pin capacitor and a internal current source 50µA, the IC shuts down to protect the system in over-voltage condition, short-lamp condition, respectively.		
20	OLP1	This pin is for open-lamp protection and feedback control of lamp currents. It has the same functions as other OLP pins and is connected to the half-wave rectifier and the full-wave rectifier internally. In striking mode, if the minimum of rectified OLP inputs is less than 0.7V for a predetermined time by the TIMER pin capacitor and an internal current source or, in normal mode, if the minimum of rectified OLP inputs is less than 0.5V for another predetermined time by the TIMER pin capacitor and another internal current source; the IC shuts down to protect the system in open-lamp condition. The maximum of rectified OLP inputs is inputted to the negative of the error amplifier for feedback control of lamp current.		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	IC Supply Voltage	6	30	V
T _A	Operating Temperature Range	-25	+85	°C
TJ	Operating Junction Temperature		+150	°C
T _{STG}	Storage Temperature Range	-65	+150	°C
θ _{JA}	Thermal Resistance Junction-Air ^(1,2)		90	°C/W
PD	Power Dissipation		1.4	W

Notes:

1. Thermal resistance test board; size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.

2. Assume no ambient airflow.

Pin Breakdown Voltage

Pin #	Name	Value	Unit
1	TIMER	7	
2	CMP	7	
3	ADIM	7	
4	СТ	7	
5	REF	7	
6	BCT	7	
7	BDIM	7	
8	ENA	7	
9	GND		
10	OUTB	10	V
11	OUTA	30	v
12	VIN	30	
13	OLR4	±7	
14	OLP4	±7	
15	OLR3	±7	
16	OLP3	±7	
17	OLR2	±7	
18	OLP2	±7	
19	OLR1	±7	
20	OLP1	±7	

Electrical Characteristics

For typical values, T_A =25°C, V_{IN} =15V, and -25°C $\leq T_A \leq$ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Under-Volta	ige Lockout Section (UVLO)			1		
V_{th}	Start Threshold Voltage	Increase V _{IN}	4.9	5.2	5.5	V
V_{thhys}	Start Threshold Voltage Hysteresis	Decrease V _{IN}	0.20	0.45	0.60	V
I _{st}	Startup Current	V _{IN} =4.5V	10	70	100	μA
l _{op}	Operating Supply Current	V _{IN} =15V, Not Switching	0.5	2.0	3.5	mA
ON/OFF Sec	ction					
Von	On-State Input Voltage		1.4		5.0	V
V _{off}	Off-State Input Voltage				0.7	V
I _{sb}	Standby Current	ENA=0V	50	120	190	μA
Rena	Pull-Down Resistor	ENA=2V	120	200	280	kΩ
Reference S	Section (Recommend 1µF X7R Capacit	or)		•		
V_5	5V Regulation Voltage		4.9	5.0	5.1	V
V _{5line}	5V Line Regulation	$6 \le V_{IN} \le 30 V$		4	50	mV
V _{5load}	5V Load Regulation	$10\mu A \le I_5 \le 3mA$		4	50	mV
Oscillator S	ection (Main)		1		1	
fosc	Oscillation Frequency	T _A =25°C, CT=220pF, RT=100kΩ	101.3	105.0	108.3	kHz
000		CT=220pF, RT=100kΩ	101	105	109	
f _{str}	Oscillator Frequency in Striking Mode	$T_A=25^{\circ}C, CT=220pF, RT=100k\Omega$	127.5	132.0	136.5	kHz
		CT=20pF, RT=100kΩ	127	132	137	
Ictdcs		Striking	1.03	1.18	1.33	mA
I _{ctdc}		Normal	770	870	970	μA
Ictcs	CT Charge Current	Striking	-15	-12	-9	μA
V _{cth}	CT High Voltage			2		V
V _{ctl}	CT Low Voltage			0.45		V
Oscillator S	ection (Burst)					
fosch	Burst Oscillation Frequency	T_A =25°C, BCT=4.7nF, BRT=1.4M Ω	324	333	345	Hz
-0300		BCT=4.7nF, BRT=1.4MΩ	320	333	346	
Ibctdc	BCT Discharge current		20	26	32	μA
V _{bcth}	BCT High Voltage			2		V
V _{bctl}	BCT Low Voltage			0.5		V

Electrical Characteristics (Continued)

For typical values, T_A =25°C, V_{IN} =15V, and -25°C $\leq T_A \leq$ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Analog Dim	ming Section					
		ADIM=0V, T _A =25°C	1.225	1.310	1.402	
A) (ADIM=0V	1.212	1.310	1.408	
AV _{rexx}	Reference Voltage	ADIM=0.5V		1.16		V
		ADIM=1.0V		0.99		
Error Ampli	fier Section		•			
I _{sin}	Output Sink Current	OLP=2.5V, ADIM=2.5V	63	76	94	μA
I _{sur1}	Output Source Current 1	OLP=0V, ADIM=0V	-65	-50	-35	μA
I _{sur2}	Output Source Current 2	CMP=3V	-1.7	-1.3	-0.9	μA
I _{bsin}	Burst CMP Sink Current	BDIM=5V, BCT=0V	41	52	63	μA
l _{olpi}	OLP Input Current	OLP=2V		0		μA
I _{olpo}	OLP Output Current	OLP=-2V	-30	-20	-10	μA
	Rectifiers Output of OLP	OLP=0.3V		0.31		V
V _{lpfx}		OLP=1.5V		1.5		V
V _{olpr}	OLP Input Voltage Range ⁽³⁾		-4		4	V
Open-Lamp	Regulation Section					
I _{olr1}	Error Amplifier Source Current for	Striking, OLR=1.6V	-4.0	-3.4	-2.9	μA
I _{olr2}	Open-Lamp Regulation	OLR Sweep		0		μA
V _{olr1}	Open-Lamp Regulation Voltage 1	OLR Sweep	1.24	1.34	1.44	V
V _{olr2}	Open-Lamp Regulation Voltage 2	Striking, OLR Sweep	1.88	1.98	2.08	V
V _{olr3}	Open-Lamp Regulation Voltage 3		2.1	2.2	2.3	V
G _{mOLR}	OLR Error Amplifier Trans-conductance		180	310	440	µmho
l _{ors}	OLR Error Amplifier Sink Current	Normal, OLR=2.5V	50	70	90	μA
I _{olri}	OLR Input Current	OLR=2.5V		0		μA
l _{olro}	OLR Output Current	OLR=-2.5V	-35	-25	-15	μA
Volrr	OLR Input Voltage Range ⁽³⁾		-4		4	V

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (Continued)

For typical values, T_A =25°C, V_{IN} =15V, and -25°C $\leq T_A \leq$ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Protection S	Section					
V _{olp0}	Open-Lamp Protection Voltage 0 ⁽⁴⁾	Striking	0.65	0.70	0.75	V
V _{olp1}	Open-Lamp Protection Voltage 1	Sweep OLP	0.42	0.49	0.56	V
V _{cmpr}	CMP-High Protection Voltage	Sweep CMP	3.4	3.5	3.6	V
V_{hfbp}	High-FB Protection Voltage ⁽⁴⁾		3.4	3.5	3.6	V
V_{slp}	Short-Lamp Protection Voltage	Sweep TIMER	0.22	0.30	0.38	V
V _{tmr1}	Timer Threshold Voltage 1	Striking, Sweep TIMER	2.87	3.02	3.17	V
V _{tmr2}	Timer Threshold Voltage 2	Sweep TIMER	1.0	1.1	1.2	V
I _{tmr1}	Timer Current 1	OLP=0V	1.7	2.1	2.5	μA
I _{tmr2}	Timer Current 2	OLR=1.8V	40	50	60	μA
TSD	Thermal Shutdown ⁽⁴⁾			150		°C
V _{ovp}	Over-Voltage Protection Voltage	Sweep OLR	1.24	1.34	1.44	V
dcr	ENA2.3V OLP Disable/Enable Change Voltage		2.1	2.3	2.5	V
Output Sect	tion					
V_{pdhv}	PMOS Gate High Voltage ⁽⁴⁾	V _{IN} =15V		V _{IN}		V
V _{phlv}	PMOS Gate Low Voltage	V _{IN} =15V	V _{IN} -9.5	V _{IN} -8.5	V _{IN} -7.0	V
V_{ndhv}	NMOS Gate High Voltage	V _{IN} =15V	8.0	9.0	10.5	V
V _{ndlv}	NMOS Gate Low Voltage ⁽⁴⁾	V _{IN} =15V		0		V
V _{puv}	PMOS Gate Voltage with UVLO Activated	V _{IN} =4.5V	V _{IN} -0.3			V
V _{nuv}	NMOS Gate Voltage with UVLO Activated	V _{IN} =4.5V			0.3	V
I _{pdsur}	PMOS Gate Drive Source Current ⁽⁴⁾	V _{IN} =15V		-300		mA
I _{pdsin}	PMOS Gate Drive Sink Current ⁽⁴⁾	V _{IN} =15V		400		mA
I _{ndsur}	NMOS Gate Drive Source Current ⁽⁴⁾	V _{IN} =15V		300		mA
I _{ndsin}	NMOS Gate Drive Sink Current ⁽⁴⁾	V _{IN} =15V		-400		mA
Maximum /	Minimum Duty Cycle					
DC _{MIN}	Minimum Duty Cycle ⁽⁴⁾	f _{osc} =100kHz		0		%
DC _{MAX}	Maximum Duty Cycle ⁽⁴⁾	f _{osc} =100kHz	45		49	%

Note:

4. These Parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics







Figure 5. Startup Current vs. Temperature





Figure 4. Start Threshold Voltage Hysteresis vs. Temperature



Figure 6. Operating Current vs. Temperature















Functional Description

UVLO: The under-voltage lockout (UVLO) circuit guarantees the stable operation of the IC's control circuit by stopping and starting it as a function of the V_{IN} value. The UVLO circuit turns on the control circuit when V_{IN} exceeds 5.2V. When V_{IN} is lower than 4.75V, the IC startup current is less than 100 μ A.

ENA: Applying voltage higher than 1.3V to the ENA pin enables the IC. Applying voltage lower than 0.7V to the ENA pin disables the IC. In terms of the protections, applying voltage higher than 2.5V to the ENA pin disables OLP and SLP. Applying voltage lower than 2.1V to the ENA pin enables the OLP and the SLP.

Main Oscillator: In normal mode, the external timing capacitor (CT) is charged by the current flowing from the reference voltage source, which is formed by the timing resistor (RT) and the timing capacitor (CT). The sawtooth waveform charges up to 2V. Once CT voltage reaches 2V, the CT begins discharging down to 0.45V. Next, the CT starts charging again and a new switching cycle begins, as shown in Figure 36. The main frequency is programmed by adjusting the RT and CT value. The main frequency is calculated as:



Figure 36. Main Oscillator Circuit

In striking mode, the external timing capacitor (CT) is charged by the current flowing from the reference voltage source and 12μ A current source, which increases the frequency. If the product of RT and CT value is constant, the striking frequency is depending on CT and is calculated as:

$$f_{str} = \frac{1}{RT \cdot CT \cdot ln \begin{pmatrix} 13.65 + (3l_1 - 4.55l_2)RT \\ -l_1 \cdot l_2 \cdot RT^2 \\ 13.65 + (4.55l_1 - 3l_2)RT \\ -l_1 \cdot l_2 \cdot RT^2 \end{pmatrix}} \begin{bmatrix} Hz \end{bmatrix}$$
(2)

Burst Dimming Oscillator: The burst dimming timing capacitor (BCT) is charged by the current flowing from the reference voltage source, which is formed by the burst dimming timing resistor (BRT) and the burst dimming timing capacitor (BCT). The sawtooth waveform charges up to 2V. Once the BCT voltage reaches 2V, the capacitor begins discharging down to 0.5V. Next, the BCT starts charging again and a new burst dimming cycle begins, as shown in Figure 37. The burst dimming frequency is programmed by adjusting the BCT and BRT values. The burst dimming frequency is calculated as:

$$f_{OSCB} = \frac{1}{BRT \cdot BCT \cdot In \left(\frac{0.039 \cdot BRT - 4500}{0.026 \cdot BRT - 4500}\right)} [Hz] (3)$$

To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.



Figure 37. Burst Dimming Oscillator Circuit

Analog Dimming: For analog dimming, the lamp intensity is controlled with the external dimming signal (V_{ADIM}) and resistors. Figure 38 shows how to implement an analog dimming circuit.



Figure 38. Analog Implementation Circuit

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In full brightness, the maximum rms value of the lamp current is calculated as:

$$i_{ms}^{\max} = V_{ref_max} \frac{\pi}{2\sqrt{2}R_{s1}} [A]$$
(4)

The lamp intensity is inversely proportional to V_{ADIM} . As V_{ADIM} increases, the lamp intensity decreases and the rms value of the lamp current is calculated as:

$$i_{ms}^{\max} = V_{ref} \frac{\pi}{2\sqrt{2}R_s} [A]$$

$$V_{ref} = V_{ref_max} - 0.30V_{ADIM} [A]$$
(5)

Figure 39 shows the lamp current waveform vs. V_{ADIM} in an analog dimming mode.



Figure 39. Analog Dimming Waveforms

Burst Dimming: Lamp intensity is controlled with the BDIM signal over a wide range. When BDIM voltage is lower than BCT voltage, the lamp current is turned on; 0V on BDIM commands full brightness. The duty cycle of the PWM pulse determines the lamp brightness. The lamp intensity is inversely proportional to BDIM voltage. As BDIM voltage increases, the lamp intensity decreases. Figure 40 shows the lamp current waveform vs. DIM in negative burst dimming mode.



Figure 40. Burst Dimming Waveforms

Burst dimming can be implemented, not only DC voltage, but also using PWM pulse as the BDIM signal. Figure 41 shows how to implement burst dimming using PWM pulse as BDIM signal.



Figure 41. Burst Dimming Implementation Circuit Using an External Pulse

Figure 42 shows the lamp current waveform vs. an external pulse in negative burst dimming mode.



Figure 42. Burst Dimming Waveform Using an External Pulse

During striking mode, burst dimming operation is disabled to guarantee continuous striking time. Figure 43 shows burst dimming disabled during striking mode.



Figure 43. Burst Dimming During Striking Mode

Soft-Start: A soft-start circuit ensures a gradual increase in the input and output power. FAN7318 has no soft-start pin, but provides soft-start function using the second BCT waveform. The second BCT waveform limits CMP voltage at initial operation, so lamp current increases gradually.



Figure 44. Soft-Start in Normal Mode



Output Drives: FAN7318 is designed to drive P-N halfbridge MOSFETs with symmetric duty cycle. FAN7318 can drive P-MOSFET directly without a level-shift capacitor and a Zener diode. A fixed dead time of 500ns is introduced between two outputs at maximum duty cycle, as shown in Figure 46.



Lamp Current Feedback Circuit: FAN7318 has four OLP pins for lamp current feedback and protections. The inputs of four OLP pins are connected to the internal half-wave and full-wave rectifier circuits. The half-wave rectified signals of four OLP inputs are connected the maximum detector circuit. The full-wave rectified signals of four OLP inputs are connected to the minimum detector circuit.

The two inputs among the inputs of four OLP pins should be inverse phase with the other two inputs. If not, FB-High protection may be triggered.

Lamp Voltage Feedback Circuit: FAN7318 has four OLR pins for lamp voltage feedback and protections. The inputs of four OLR pins are connected to the internal full-wave rectifier circuit. The full-wave rectified signals of four OLR inputs are connected to the maximum detector circuit for lamp voltage feedback and protections. Furthermore, they are connected to the minimum detector circuit for protections.

Protections: The FAN7318 provides the following latchmode protections: Open-Lamp Regulation (OLR), Open-Lamp Protection (OLP), Short-Lamp Protection (SLP), CMP-High Protection, FB-High Protection, and Thermal Shutdown (TSD). The latch is reset when V_{IN} falls to the UVLO voltage or ENA is pulled down to GND.

The protection delay time can be adjusted by a capacitor between the TIMER pin and GND.



Figure 47. Protection Timing Delay

Assume that the TIMER pin capacitor is 1µF.

The striking time is calculated as:

$$t_{strike} = \frac{C \Delta V_{str}}{I_{sur1}} = \frac{1\mu F \bullet 3V}{2\mu A} = 1.5s$$
(6)

The OVP and SLP delay time are calculated as:

$$t_{OVP_SLP} = \frac{C\Delta V_{nor}}{I_{sur2}} = \frac{1\mu F \bullet 1V}{50\mu A} = 20ms$$
(7)

The CMP high protection and OLP delay time are calculated as:

$$t_{OLP_CMPH} = \frac{C\Delta V_{nor}}{I_{sur1}} = \frac{1\mu F \bullet 1V}{2\mu A} = 500ms \tag{8}$$

Open-Lamp Regulation: When the maximum of the rectified OLR input voltages (V_{OLR}^{max}) is more than 2V, the IC enters regulation mode and controls CMP voltage. The IC limits the lamp voltage by decreasing CMP source current. If V_{OLR}^{max} is between 1.34V and 2V, CMP source current decreases to 3.2µA. Then, if V_{OLR}^{max} reaches 2V, CMP source current decreases to 0µA, so the CMP voltage remains constant and the lamp voltage also remains constant, as shown in Figure 48.



Figure 48. Open-Lamp Regulation in Striking Mode

Finally, if V_{OLR}^{max} is more than 2.2V, the error amplifier for OLR is operating and CMP sink current increases, so CMP voltage decreases and the lamp voltage maintains the determined value, as shown in Figure 49.



Figure 49. 2.2V Open-Lamp Regulation

Over-Voltage Protection: In normal mode, while V_{OLR}^{max} is higher than 1.34V, the TIMER pin capacitor is charged by an internal current source of 50µA. Once the TIMER reaches 1V, the IC enters shutdown, as shown in Figure 50. This protection is disabled in striking mode to ignite lamps reliably.



Figure 50. Over-Voltage Protection in Normal Mode

In burst dimming mode, while V_{OLR}^{max} is higher than 1.34V, burst dimming is disabled, so that the TIMER pin capacitor is charged continuously by an internal current source of 50µA. Once the TIMER reaches 1V, the IC enters shutdown, as shown in Figure 51.



Figure 51. Over-Voltage Protection in Burst Dimming Mode

Open-Lamp Protection: If the minimum of the rectified OLP voltages ($V_{\text{OLP}}^{\text{min}}$) is less than 0.7V during initial operation, the IC operates in striking mode for a time predetermined by the TIMER pin capacitor and an internal current source, 2µA, as shown in Figure 52.



Figure 52. Open-Lamp Protection in Striking Mode

The IC starts operating in striking mode and remains in striking mode until four pulses of V_{OLP}^{min} higher than 0.7V occur. If more than four pulses, the IC changes from striking mode into normal mode, as shown in Figure 53.



Figure 53. Mode Change from Striking to Normal

After ignition, if V_{OLP}^{min} is less than 0.5V for a time predetermined by the TIMER pin capacitor and an internal current source, $2\mu A$ in normal mode, the IC is shut down, as shown in Figure 54.



Figure 54. Open-Lamp Protection in Normal Mode

In burst dimming mode, if V_{OLP}^{min} is less than 0.5V for another time predetermined by the TIMER pin capacitor and an internal current source, 2µA, the IC is shut down, as shown in Figure 55. The open-lamp protection delay in burst dimming mode is shorter than in full-brightness because short-lamp condition is detected at rising interval of lamp voltage in burst dimming, then another internal current source is turned on during the interval.



Figure 55. Open-Lamp Protection in Burst Dimming Mode

Applying voltage lower than 2.1V to the ENA pin enables OLP. Applying voltage higher than 2.5V to the ENA pin disables OLP and is called as DCR mode. Regardless of DCR mode, OLP is enabled in striking mode.



Figure 56. Open-Lamp Protection Disable in DCR Mode

Short-Lamp Protection: If the minimum of the rectified OLR voltages (V_{OLR}^{min}) is less than 0.3V for a time predetermined by the TIMER pin capacitor and a internal current source of 50µA in normal mode, the IC is shut down, as shown in Figure 57. This protection is disabled in striking mode to ignite lamps reliably.



Figure 57. Short-Lamp Protection in Normal Mode

In burst dimming mode, if V_{OLR}^{min} is less than 0.3V for a time predetermined by the TIMER pin capacitor and a internal current source of 50µA turned on only burst dimming on time, the IC is shut down, as shown in Figure 58. SLP protection delay changes, depending on burst dimming on duty ratio.



Figure 58. Short-Lamp Protection in Burst Dimming Mode

Applying voltage higher than 2.5V to the ENA pin disables SLP. Applying voltage lower than 2.1V to the ENA pin enables SLP.



CMP-High Protection: If CMP is more than 3.5V for a time predetermined by the TIMER pin capacitor and a internal current source of 50μ A in normal mode, the IC is shut down, as shown in Figure 60.



Figure 60. CMP-High Protection

This protection is disabled by a pull-down resistor (a few M Ω) between CMP and GND. If CMP voltage reaches 2.5V, CMP source current decreases to 2 μ A. Determine a pull down resistor value such that the whole of this current can flow through the resistor. If so, CMP-High protection can be disabled, as shown Figure 61. This protection is disabled in striking mode to ignite the lamps reliably.



Figure 61. CMP-High Protection Disable by a Pull-Down Resistor

High-FB Protection: If the minimum of the rectified OLP voltages(V_{OLP}^{max}) is more than 3.5V, the counter starts counting eight rectified OLP pulses in normal mode, then the IC enters shutdown, as shown in Figure 62. This counter is reset by detecting the positive edge of BCT. This protection is disabled in striking mode to ignite the lamps reliably.



Figure 62. FB-High Protection

Thermal Shutdown: The IC provides the function to detect the abnormal over-temperature. If the IC temperature exceeds approximately 150°C, the thermal shutdown triggers.

Typical Application Circuit (LCD Backlight Inverter)

Application	Device	Input Voltage Range	Number of Lamps	
22-Inch LCD Monitor	FAN7318	15V±10%	4	

1. Features

- High-Efficiency Single-Stage Power Conversion
- P-N Half-Bridge Topology
- Reduces Required External Components
- Enhanced System Reliability through Protection Functions







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Definition of Terms					
Datasheet Identification	Product Status	Definition			
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.			
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