CD4538BC
Dual Precision Monostable

General Description
The CD4538BC is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active LOW and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_x and C_x. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility:
  Fan out of 2 driving 74L or 1 driving 74LS
- New formula:
  \[ PW_{OUT} = RC \] (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range: 1 \( \mu \)s to \( \infty \)
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current: 5 nA (typ.) @ 5 V_{CC}
- Pin compatible to CD4528BC

Ordering Code:

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Number</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4538BCM</td>
<td>M16A</td>
<td>16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150&quot; Narrow</td>
</tr>
<tr>
<td>CD4538BCWM</td>
<td>M16B</td>
<td>16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300&quot; Wide</td>
</tr>
<tr>
<td>CD4538BCN</td>
<td>N16E</td>
<td>16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300&quot; Wide</td>
</tr>
</tbody>
</table>

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram

Truth Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear</td>
<td>A</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
</tr>
</tbody>
</table>

H = HIGH Level
L = LOW Level
↑ = Transition from LOW to HIGH
↓ = Transition from HIGH to LOW
\( \sim \) = One HIGH Level Pulse
\( \overline{\sim} \) = One LOW Level Pulse
X = Irrelevant
Block Diagram

\[ R_X \text{ and } C_X \text{ are External Components} \]

\[ V_{DD} = \text{Pin 16} \]

\[ V_{SS} = \text{Pin 8} \]

Logic Diagram

FIGURE 1.
Theory of Operation

Trigger Operation
The block diagram of the CD4538BC is shown in Figure 1, with circuit operation following. As shown in Figure 1 and Figure 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor CX completely charged to VDD. When the trigger input A goes from VSS to VDD (while inputs B and CD are held to VDD) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1. At the same time the output latch is set. With transistor N1 on, the capacitor CX rapidly discharges toward VSS until VREF1 is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor CX begins to charge through the timing resistor, RX, toward VDD. When the voltage across CX equals VREF2, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from VDD to VSS (while input A is at VSS and input CD is at VDD). It should be noted that in the quiescent state CX is fully charged to VDD, causing the current through resistor RX to be zero. Both comparators are “off” with the total device current due only to reverse junction leakages. An added feature of the CD4538BC is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of CX, RX, or the duty cycle of the input waveform.

Retrigger Operation
The CD4538BC is retriggered if a valid trigger occurs followed by another valid trigger before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from VREF1, but has not yet reached VREF2, will cause an increase in output pulse width T. When a valid retrigger is initiated, the voltage at T2 will again drop to VREF1 before progressing along the RC charging curve toward VDD. The Q output will remain high until time T, after the last valid retrigger.

Reset Operation
The CD4538BC may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on CD sets the reset latch and causes the capacitor to be fast charged to VDD by turning on transistor Q1. When the voltage on the capacitor reaches VREF2, the reset latch will clear and then be ready to accept another pulse. If the CD input is held low, any trigger inputs that occur will be inhibited and the Q and Q outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the CD input, the output pulse T can be made significantly shorter than the minimum pulse width specification.
FIGURE 3. Retriggerable Monostables Circuitry

FIGURE 4. Non-Retriggerable Monostables Circuitry

FIGURE 5. Connection of Unused Sections
### Absolute Maximum Ratings (Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>DC Supply Voltage (V_{DD})</th>
<th>-0.5 to +18 V_{DC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (V_{IN})</td>
<td>0 to V_{DD}</td>
<td>0 to V_{DD}</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Storage Temperature Range (T_{S})</th>
<th>-65°C to +150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation (P_{D})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual-In-Line</td>
<td>700 mW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Small Outline</td>
<td>500 mW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (T_{L})</td>
<td></td>
<td></td>
<td>260°C</td>
</tr>
<tr>
<td>(Soldering, 10 seconds)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Note 1): Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

### Recommended Operating Conditions (Note 2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>DC Supply Voltage (V_{DD})</th>
<th>3 to 15 V_{DC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (V_{IN})</td>
<td>0 to V_{DD}</td>
<td>0 to V_{DD}</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Operating Temperature Range (T_{A})</th>
<th>-55°C to +125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{SS}</td>
<td>0V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Note 2): V_{SS} = 0V unless otherwise specified.

### DC Electrical Characteristics (Note 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>-55°C</th>
<th>-25°C</th>
<th>-125°C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{DD}</td>
<td>Quiescent</td>
<td>V_{DD} = 5V, V_{IN} = V_{DD}</td>
<td>0.005</td>
<td>5</td>
<td>150</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Device Current</td>
<td>V_{DD} = 10V, V_{IN} = V_{SS}</td>
<td>0.101</td>
<td>10</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 15V, All Outputs Open</td>
<td>0.15</td>
<td>20</td>
<td>600</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>LOW Level</td>
<td>I_{OL} = 1 µA</td>
<td>0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Voltage</td>
<td>V_{DD} = 10V, V_{IN} = V_{DD}, V_{IN} = V_{SS}</td>
<td>0.05</td>
<td>0</td>
<td>0.05</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 15V</td>
<td>0.05</td>
<td>0</td>
<td>0.05</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>HIGH Level</td>
<td>I_{OH} = 1 µA</td>
<td>4.95</td>
<td>4.95</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Voltage</td>
<td>V_{DD} = 10V, V_{IN} = V_{DD}, V_{IN} = V_{SS}</td>
<td>9.95</td>
<td>9.95</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 15V</td>
<td>14.95</td>
<td>14.95</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>LOW Level</td>
<td>I_{IL} = 1 µA</td>
<td>1.5</td>
<td>2.25</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Input Voltage</td>
<td>V_{DD} = 5V, V_{IN} = 0.5V or 4.5V</td>
<td>3.0</td>
<td>4.50</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 10V, V_{IN} = 1.0V or 9.0V</td>
<td>4.0</td>
<td>6.75</td>
<td>4.0</td>
<td></td>
</tr>
<tr>
<td>V_{IH}</td>
<td>HIGH Level</td>
<td>I_{IH} = 1 µA</td>
<td>3.5</td>
<td>3.5</td>
<td>2.75</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Input Voltage</td>
<td>V_{DD} = 5V, V_{IN} = 0.5V or 4.5V</td>
<td>7.0</td>
<td>7.0</td>
<td>5.50</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 10V, V_{IN} = 1.0V or 9.0V</td>
<td>11.0</td>
<td>11.0</td>
<td>8.25</td>
<td></td>
</tr>
<tr>
<td>I_{OL}</td>
<td>LOW Level</td>
<td>I_{OL} = 1 µA</td>
<td>0.51</td>
<td>0.88</td>
<td>0.36</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Output Current</td>
<td>V_{DD} = 10V, V_{IN} = 0.5V, V_{IN} = V_{DD}</td>
<td>1.3</td>
<td>2.25</td>
<td>0.9</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 15V, V_{IN} = 1.5V</td>
<td>3.4</td>
<td>8.8</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td>I_{OH}</td>
<td>HIGH Level</td>
<td>I_{OH} = 1 µA</td>
<td>-0.51</td>
<td>-0.88</td>
<td>-0.36</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Output Current</td>
<td>V_{DD} = 5V, V_{IN} = 4.8V</td>
<td>-1.3</td>
<td>-2.25</td>
<td>-0.9</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DD} = 10V, V_{IN} = 9.5V, V_{IN} = V_{DD}</td>
<td>-3.4</td>
<td>-8.8</td>
<td>-2.4</td>
<td></td>
</tr>
<tr>
<td>I_{IN}</td>
<td>Input Current, Pin 2 or 14</td>
<td>V_{DD} = 15V, V_{IN} = 0V or 15V</td>
<td>-0.02</td>
<td>-10^{-3}</td>
<td>-0.05</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Other Inputs</td>
<td>V_{DD} = 15V, V_{IN} = 0V or 15V</td>
<td>-0.1</td>
<td>-10^{-3}</td>
<td>-0.1</td>
<td>µA</td>
</tr>
</tbody>
</table>

**Note 3:** I_{OH} and I_{OL} are tested one output at a time.
### AC Electrical Characteristics (Note 4)

**Conditions:**
- $T_A = 25^\circ C$, $C_L = 50 \, \mu F$, and $t_r = t_f = 20 \, ns$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{THL}$</td>
<td>Output Transition Time</td>
<td>$V_{DD} = 5V$</td>
<td>100</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 10V$</td>
<td>50</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>40</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Propagation Delay Time</td>
<td>Trigger Operation — A or B to Q or $\overline{Q}$</td>
<td>300</td>
<td>600</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5V$</td>
<td>150</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>100</td>
<td>220</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Reset Operation — $C_D$ to Q or $\overline{Q}$</td>
<td>$V_{DD} = 5V$</td>
<td>250</td>
<td>500</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 10V$</td>
<td>125</td>
<td>250</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>95</td>
<td>190</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WL}$</td>
<td>Minimum Input Pulse Width</td>
<td>A, B, or $C_D$</td>
<td>35</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5V$</td>
<td>30</td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>25</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RR}$</td>
<td>Minimum Retrigger Time</td>
<td>$V_{DD} = 5V$</td>
<td>0</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 10V$</td>
<td>0</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>0</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>Pin 2 or 14</td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other Inputs</td>
<td>5</td>
<td>7.5</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**PW_OUT**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Output Pulse Width (Q or $\overline{Q}$)</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Note: For Typical Distribution, see Figure 6)</td>
<td>$R_X = 100 , k\Omega$, $V_{DD} = 5V$</td>
<td>208</td>
<td>226</td>
<td>244</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 10V$</td>
<td>211</td>
<td>230</td>
<td>248</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>216</td>
<td>235</td>
<td>254</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_X = 0.002 , \mu F$</td>
<td>8.83</td>
<td>9.60</td>
<td>10.37</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 10V$</td>
<td>9.02</td>
<td>9.80</td>
<td>10.59</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>9.20</td>
<td>10.00</td>
<td>10.80</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_X = 100 , k\Omega$, $C_X = 0.1 , \mu F$, $V_{DD} = 10V$</td>
<td>0.87</td>
<td>0.95</td>
<td>1.03</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>0.89</td>
<td>0.97</td>
<td>1.05</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_X = 10.0 , \mu F$, $V_{DD} = 10V$</td>
<td>0.91</td>
<td>0.99</td>
<td>1.07</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 15V$</td>
<td>±1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

**Pulse Width Match between Circuits in the Same Package**

<table>
<thead>
<tr>
<th>$R_X$</th>
<th>$C_X$</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$100 , k\Omega$</td>
<td>$0.1 , \mu F$, $R_X = 100 , k\Omega$</td>
<td>$V_{DD} = 5V$</td>
<td>±1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$100 , k\Omega$</td>
<td>$0.1 , \mu F$, $V_{DD} = 10V$</td>
<td>±1</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$100 , k\Omega$</td>
<td>$0.1 , \mu F$, $V_{DD} = 15V$</td>
<td>±1</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

**Operating Conditions**

<table>
<thead>
<tr>
<th>$R_X$</th>
<th>External Timing Resistance</th>
<th>5.0</th>
<th>(Note 5)</th>
<th>kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_X$</td>
<td>External Timing Capacitance</td>
<td>0</td>
<td>No Limit</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Note 4:** AC parameters are guaranteed by DC correlated testing.

**Note 5:** The maximum usable resistance $R_X$ is a function of the leakage of the Capacitor $C_X$, leakage of the CD4538BC, and leakage due to board layout, surface resistance, etc.
Typical Applications

FIGURE 6. Typical Normalized Distribution of Units for Output Pulse Width

FIGURE 7. Typical Pulse Width Variation as a Function of Supply Voltage $V_{DD}$

FIGURE 8. Typical Total Supply Current Versus Output Duty Cycle, $R_x = 100\, k\Omega$, $C_L = 50\, pF$, $C_X = 100\, pF$, One Monostable Switching Only

FIGURE 9. Typical Pulse Width Error Versus Temperature

FIGURE 10. Typical Pulse Width Error Versus Temperature

FIGURE 11. Typical Pulse Width Versus Timing RC Product
Test Circuits and Waveforms

FIGURE 12. Switching Test Waveforms

*C_L = 50 pF

Input Connections

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>CD</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH, tPHL, tTLH, tTHL</td>
<td>V_DD</td>
<td>PG1</td>
<td>V_DD</td>
</tr>
<tr>
<td>PWOUT, tWL</td>
<td>V_DD</td>
<td>V_SS</td>
<td>PG2</td>
</tr>
<tr>
<td>tPLH(R), tPHL(R), tWH, tWL</td>
<td>PG3</td>
<td>PG1</td>
<td>PG2</td>
</tr>
</tbody>
</table>

*Includes capacitance of probes, wiring, and fixture parasitic

Note: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 12.

FIGURE 13. Switching Test Circuit
Test Circuits and Waveforms (Continued)

$R_X = R_X' = 100 \text{k}\Omega$

$C_X = C_X' = 100 \text{pF}$

$C_1 = C_2 = 0.1 \mu\text{F}$

Duty Cycle = 50%

FIGURE 14. Power Dissipation Test
Circuit and Waveforms
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

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