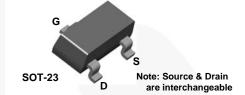


February 2015

# MMBF4117 / MMBF4118 / MMBF4119 N-Channel Switch

## **Description**

This device is designed for low current DC and audio applications. These devices provide excellent performance as input stages for sub-picoamp instrumentation or any high impedance signal sources. Sourced from process 53.



## **Ordering Information**

Part Number	Top Mark	Package	Packing Method
MMBF4117	61A	SOT-23 3L	Tape and Reel
MMBF4118	61C	SOT-23 3L	Tape and Reel
MMBF4119	61E	SOT-23 3L	Tape and Reel

## **Absolute Maximum Ratings**(1), (2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^{\circ}\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
V <sub>DG</sub>	Drain-Gate Voltage	40	V
$V_{GS}$	Gate-Source Voltage	-40	V
I <sub>GF</sub>	Forward Gate Current	50	mA
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Notes:

- 1. These ratings are based on a maximum junction temperature of 150°C.
- 2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

## Thermal Characteristics(3)

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Max.	Unit
P <sub>D</sub>	Total Device Dissipation	225	mW
	Derate Above 25°C	1.8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	556	°C/W

## Note:

3. Device mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.

### **Electrical Characteristics**

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	3	Min.	Max.	Unit
Off Chara	cteristics					•
V <sub>(BR)GSS</sub>	Gate-Source Breakdown Voltage	$I_G = -1.0 \mu\text{A},  V_{DS} = 0$		-40		V
I <sub>GSS</sub>	Gate Reverse Current	$V_{GS} = -20 \text{ V}, V_{DS} = 0$			-10	pA
		$V_{GS} = -20 \text{ V}, V_{DS} = 0, T_A$	= 150°C		-25	nA
V <sub>GS(off)</sub>	Gate-Source Cut-Off Voltage	V <sub>DS</sub> = -10 V, I <sub>D</sub> = 1.0 nA	MMBF4117	-0.6	-1.8	V
			MMBF4118	-1.0	-3.0	
			MMBF4119	-2.0	-6.0	
On Chara	cteristics					
	Zero-Gate Voltage Drain Current <sup>(4)</sup>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0	MMBF4117	30	90	μΑ
			MMBF4118	80	240	
			MMBF4119	200	600	
Small Sig	nal Characteristics					
	Common-Source Forward Transconductance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1.0 kHz	MMBF4117	70	210	μmhos
Or.			MMBF4118	80	250	
			MMBF4119	100	330	
(1	Common-Source Output Conductance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1.0 kHz	MMBF4117	/	3.0	μmhos
			MMBF4118		5.0	
			MMBF4119		10.0	
Ruch	Common-Source Forward Transconductance	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ f = 30 MHz MMBF4118 MMBF4119	MMBF4117	60		μmhos
			MMBF4118	70		
			MMBF4119	90		
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}$			3.0	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f =$	1.0 MHz		1.5	pF

#### Note:

4. Pulse test: pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  1.0%

## **Typical Performance Characteristics**

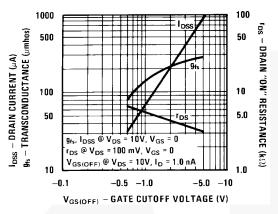


Figure 1. Parameter Interactions

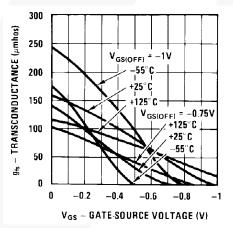


Figure 3. Transfer Characteristics

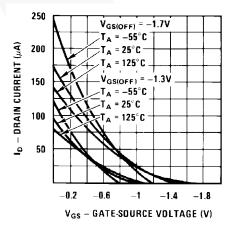


Figure 5. Transfer Characteristics

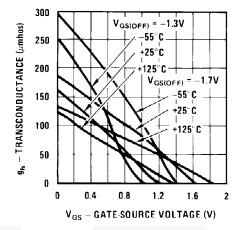


Figure 2. Transfer Characteristics

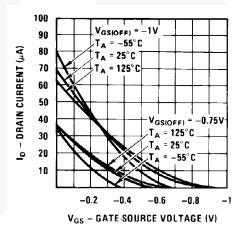


Figure 4. Transfer Characteristics

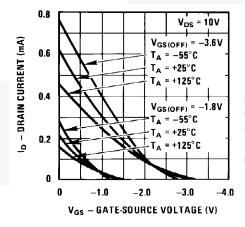


Figure 6. Transfer Characteristics

## **Typical Performance Characteristics** (Continued)

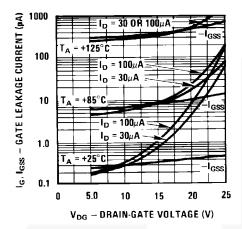


Figure 7. Leakage Current vs. Voltage

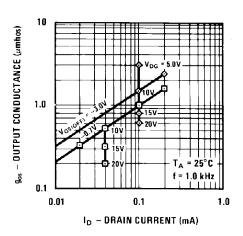


Figure 9. Output Conductance vs. Drain Current

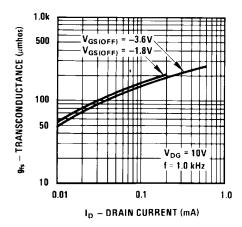


Figure 11. Transconductance vs. Drain Current

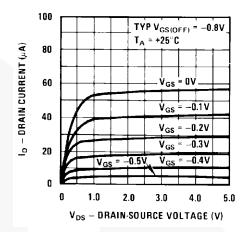


Figure 8. Common Drain-Source

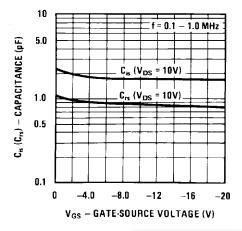


Figure 10. Conductance vs. Voltage

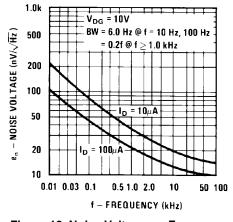


Figure 12. Noise Voltage vs. Frequency

## **Physical Dimensions** 0.95 2.92±0.20 3 1.40 1.30+0.20 2.20 2 0.60 0.37 (0.29) -0.95 ⊕ 0.20M A B 1.00 1.90 1.90 LAND PATTERN RECOMMENDATION SEE DETAIL A -1.20 MAX 0.10 (0.93) ○ 0.10 M C С 2.40±0.30 NOTES: UNLESS OTHERWISE SPECIFIED **GAGE PLANE**

A) REFERENCE JEDEC REGISTRATION
TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER
ASME Y14.5M - 1994.
E) DRAWING FILE NAME: MA03DREV10
PLANE

DETAIL A
SCALE: 2X

Figure 13. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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