

XP4NA1R4CMT-A

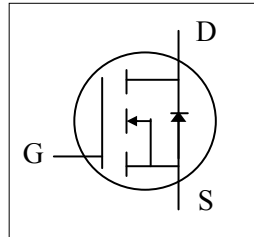
Halogen-Free Product



N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

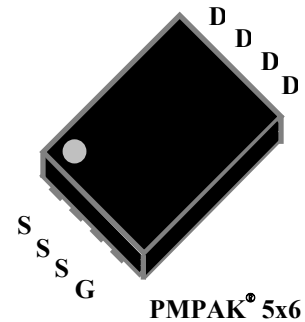


BV_{DSS}	45V
$R_{DS(ON)}$	1.4m Ω

Description

XP4NA1R4C series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings@ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	45	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}\text{C}$	Drain Current, V_{GS} @ $10V^4$ (Silicon Limited)	223	A
$I_D@T_C=25^{\circ}\text{C}$	Drain Current, V_{GS} @ $10V^4$	100	A
$I_D@T_A=25^{\circ}\text{C}$	Drain Current, V_{GS} @ $10V^3$	49	A
$I_D@T_A=70^{\circ}\text{C}$	Drain Current, V_{GS} @ $10V^3$	39	A
I_{DM}	Pulsed Drain Current ¹	400	A
$P_D@T_C=25^{\circ}\text{C}$	Total Power Dissipation	104	W
$P_D@T_A=25^{\circ}\text{C}$	Total Power Dissipation ³	5	W
E_{AS}	Single Pulse Avalanche Energy ⁵	125	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-c}	Maximum Thermal Resistance, Junction-case	1.2	$^{\circ}\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics@T_J=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	45	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	-	-	1.4	mΩ
		V _{GS} =4.5V, I _D =20A	-	-	2.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =20A	-	110	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =36V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =20V, V _{DS} =0V	-	-	100	nA
Q _g	Total Gate Charge	I _D =20A	-	47	75.2	nC
Q _{gs}	Gate-Source Charge	V _{DS} =20V	-	12	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	23	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =20V	-	14	-	ns
t _r	Rise Time	I _D =20A	-	42	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =1Ω	-	42	-	ns
t _f	Fall Time	V _{GS} =10V	-	11	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	4500	7200	pF
C _{oss}	Output Capacitance	V _{DS} =20V	-	1800	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	150	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =20A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _S =20A, V _{GS} =0V,	-	48	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	45	-	nC

Notes:

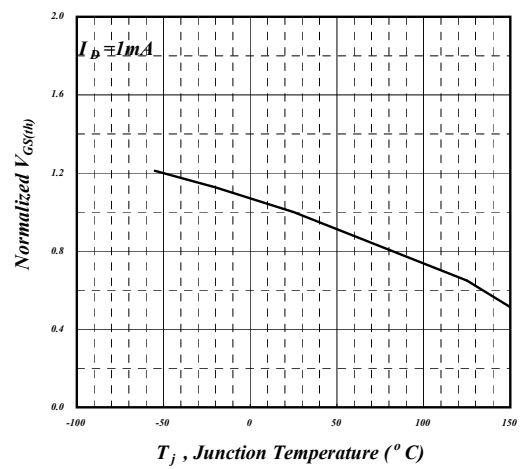
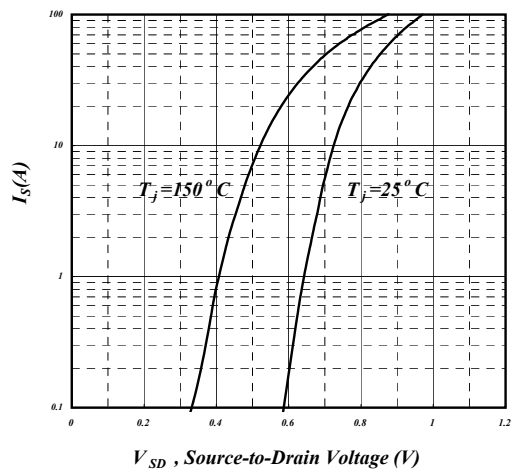
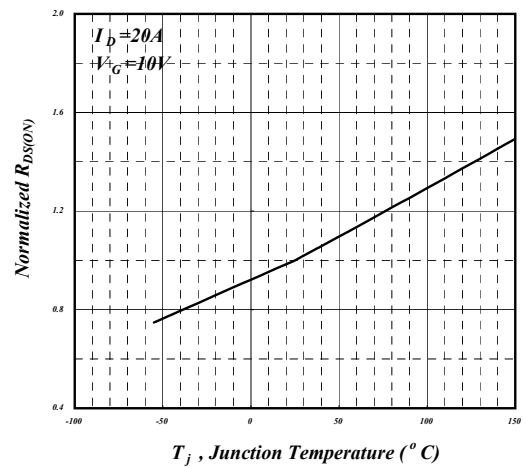
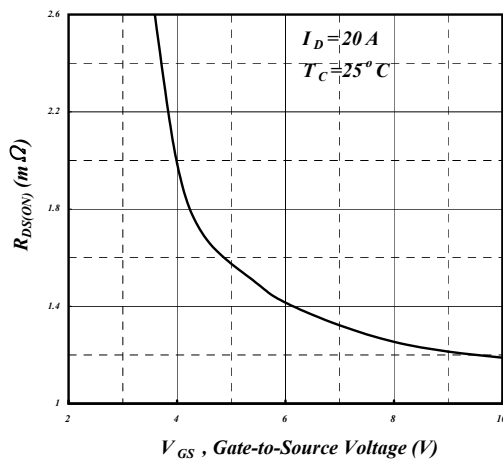
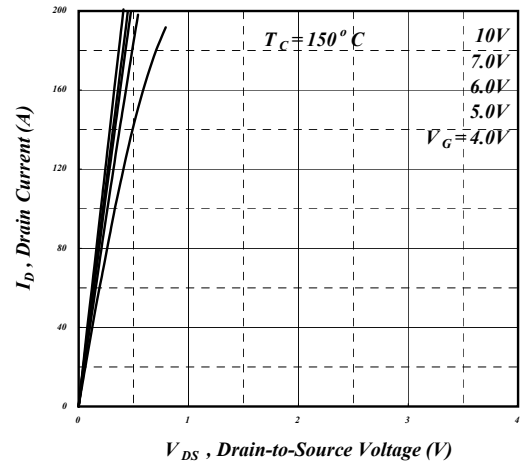
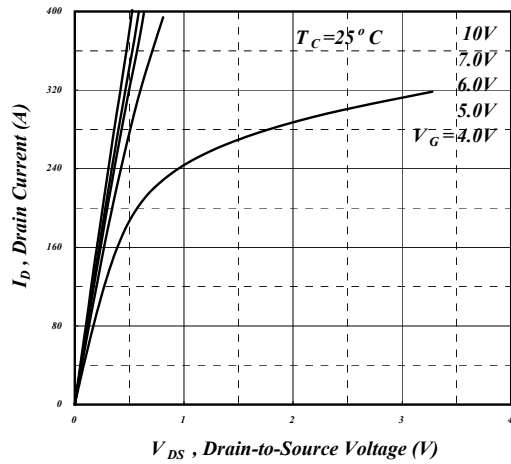
- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec ; 60°C/W at steady state.
- 4.Package limitation current is 100A .
- 5.Starting T_J=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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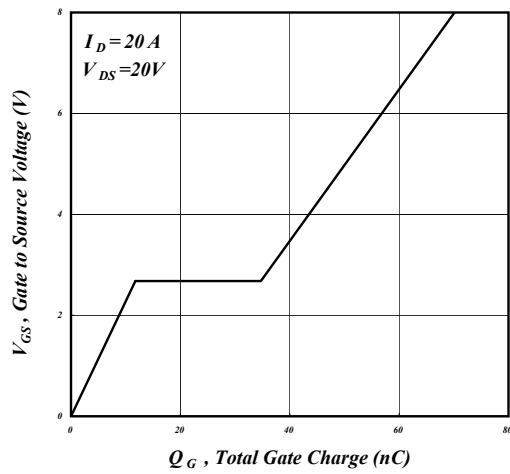


Fig 7. Gate Charge Characteristics

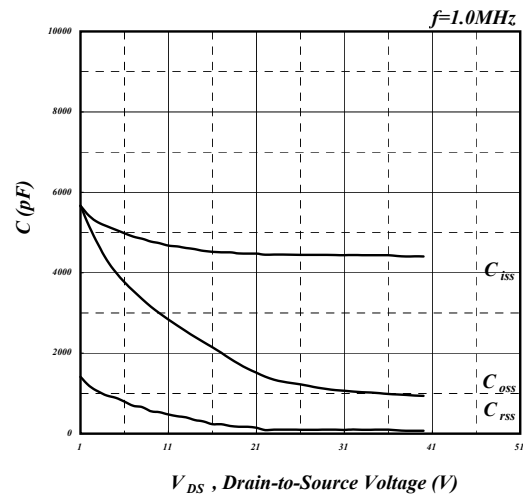


Fig 8. Typical Capacitance Characteristics

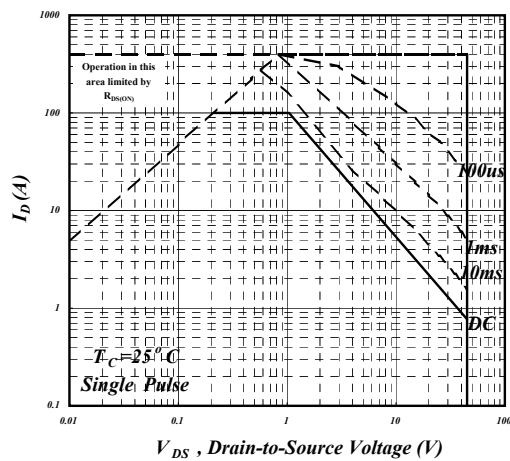


Fig 9. Maximum Safe Operating Area

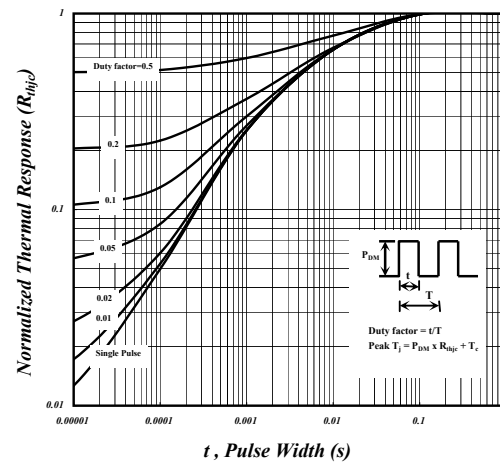


Fig 10. Effective Transient Thermal Impedance

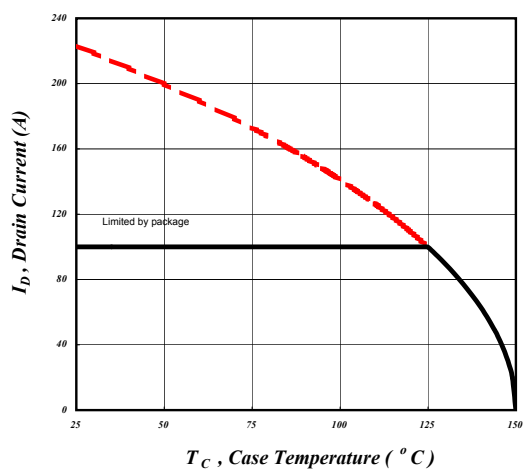


Fig 11. Drain Current v.s. Case Temperature

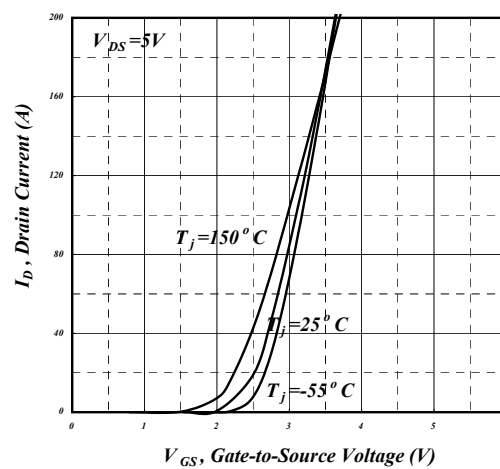


Fig 12. Transfer Characteristics

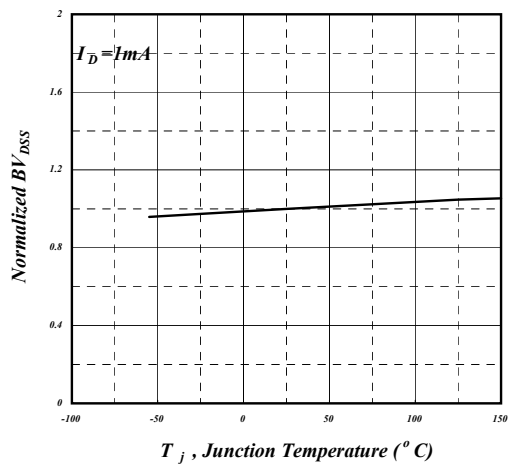


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

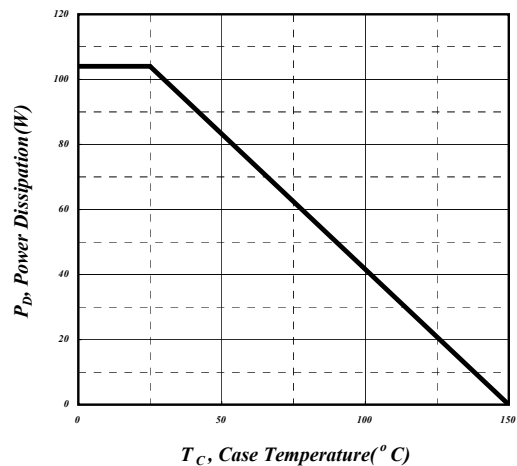


Fig 14. Total Power Dissipation

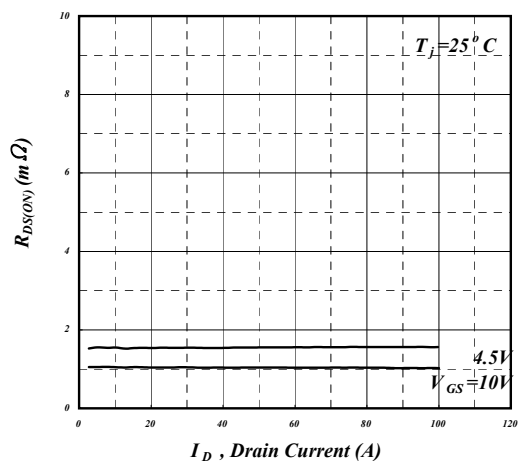
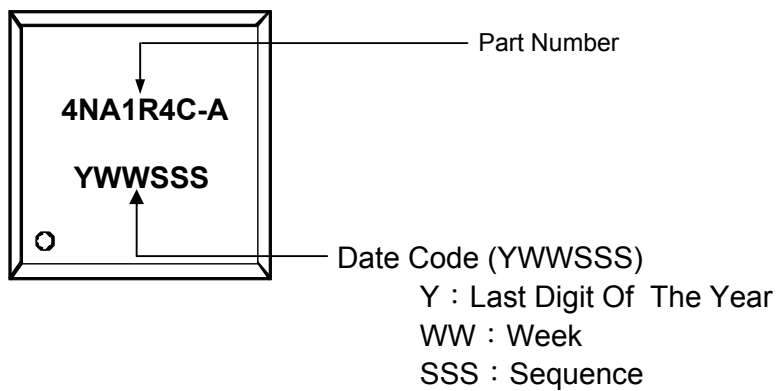


Fig 15. Typ. Drain-Source on State Resistance

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