XR77103-MoCA

Triple-Output PMIC for MaxLinear MoCA Solutions

Data Sheet

July 5, 2021

Description

The XR77103-MoCA PMIC is designed to power MaxLinear's G.hn chipsets, the MoCA 2.0 MxL370x and MoCA 2.5 MxL371x along with a single port ethernet phy such as the GPY241. It features 3 high-efficiency synchronous buck regulators with integrated power switches and sequencing engine to provide the 0.9V, 1.8V, and 3.3V rails of the MoCA SoC. The 0.9V core rail is capable of supplying the 3A peaks demanded by the SoC[1] and is compatible with the SoC DVS control.

The XR77103-MoCA can operate from 5V, 9V, and 12V powered systems with minimal required external components, and packaged in a 4x4mm QGN that provides the smallest size solution possible. With a nominal switching frequency of 560kHz, the regulators can also be synchronized to an external clock in applications where EMI control is critical. An internal supervisor circuit monitors each converter output and asserts PGOOD once sequencing is done, outputs are reported in regulation, and the reset timer expires. The polarity of the signal is active high.

1. Worst case supply condition at 0.9V power rails around 1ms.

FEATURES

- 4.5V to 14V wide input supply voltage range
- Built-in MOSFET and synchronous rectifier
- High accuracy 0.9V reference (1%)
- Current-mode control with simple compensation circuit
- External synchronization
- Power good
- Protection
  - Thermal shutdown
  - Overvoltage transient protection
  - Overcurrent protection
- 32-pin 4mm x 4mm TQFN package

APPLICATIONS

- MaxLinear MoCA 2.0 MxL370x power
- MaxLinear MoCA 2.5 MxL371x power

Ordering Information - back page

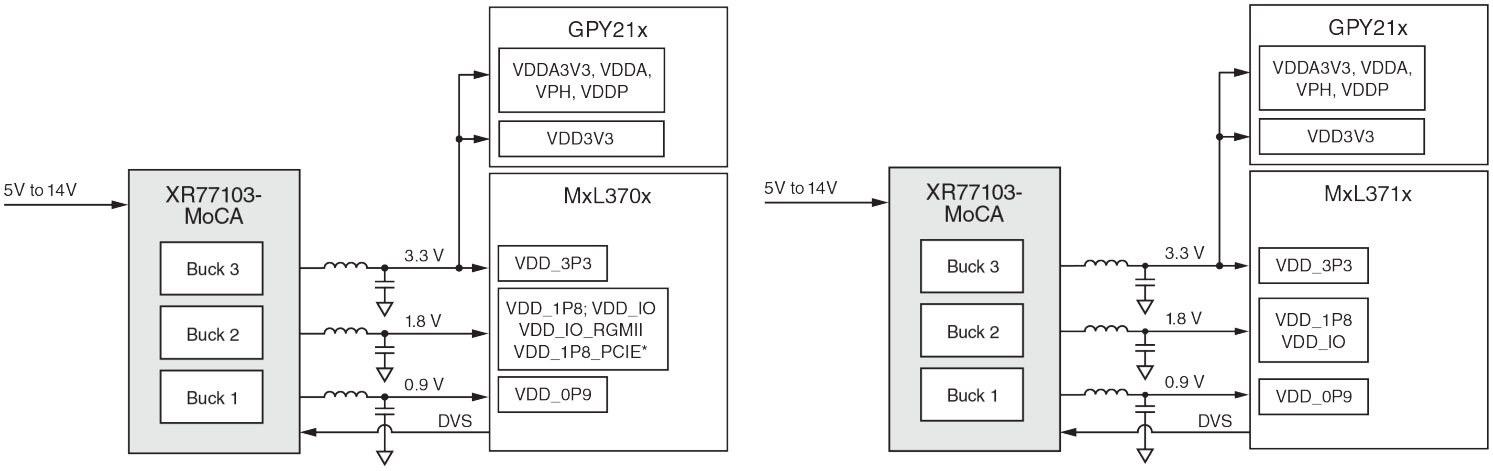


Figure 1. Power Solution for MoCA Coaxial Networking IC

Typical Application

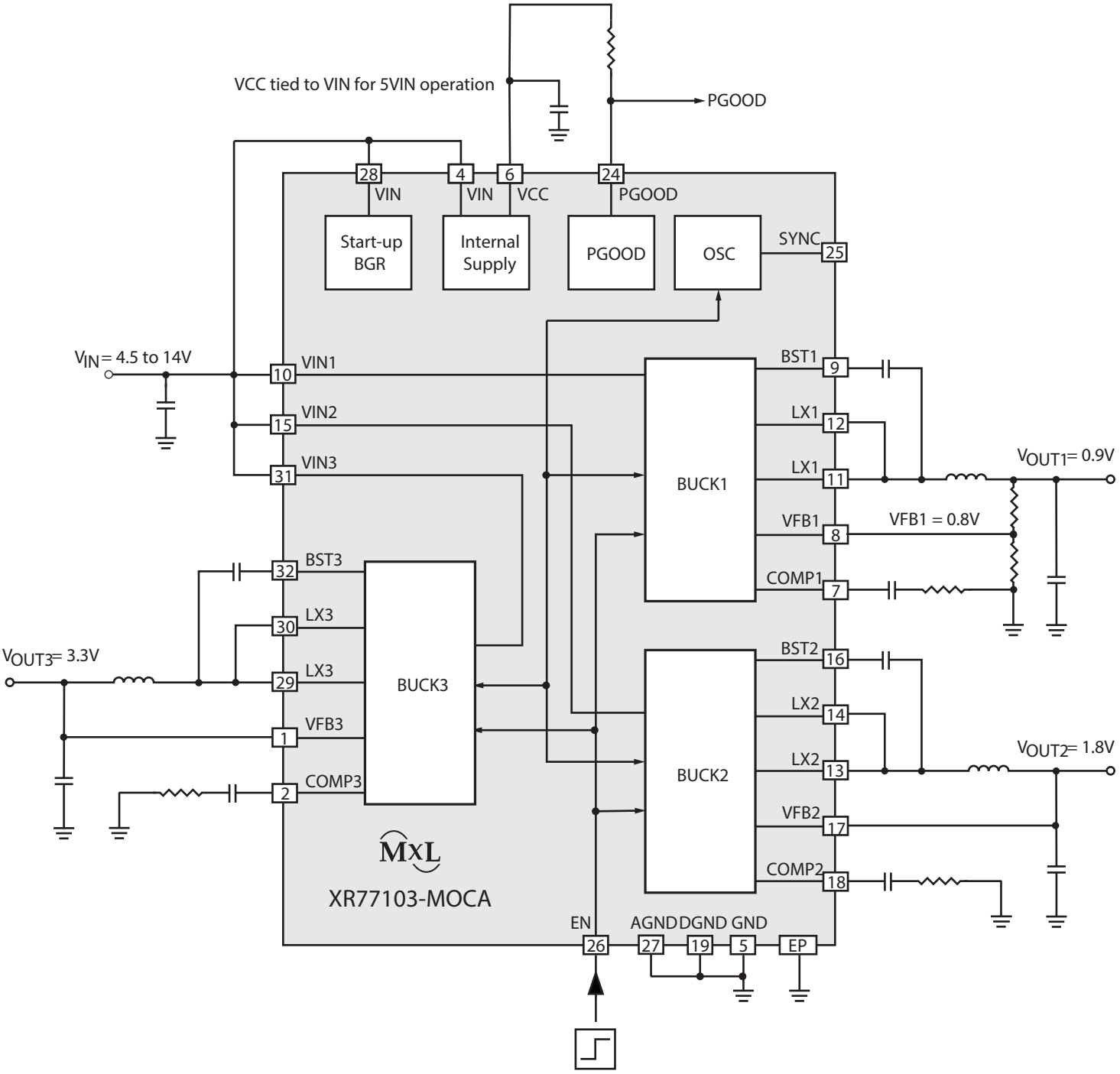


Figure 2. Typical Application

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

V_{IN1}, V_{IN2}, V_{IN3}, LX1, LX2, LX3 ..... -0.3V to 18V

EN, V_{CC} ..... -0.3V to 7V

PGOOD, SYNC ..... -0.3V to 7V

BST# to LX# ..... -0.3V to 7V

AGND, DGND to GND ..... -0.3V to 0.3V

Storage temperature ..... -65°C to 150°C

Junction temperature ..... 150°C

Power dissipation ..... Internally Limited

Lead temperature (soldering, 10 seconds) ..... 260°C

ESD ratin (CDM – charged device model) 700V

ESD rating (HBM – human body model) 2kV

Operating Conditions

V_{IN} ..... 4.5V to 14V

V_{CC} ..... 4.5V to 5.5V

LX# ..... -0.3V to 14V(1)

Junction temperature range (T_J) ..... -40°C to 125°C

XR77103 package power dissipation max at 25°C 3.4W

XR77103 thermal resistance θ_{JA} ..... 30°C/W

NOTE:

1. LX# pins' DC range is from -0.3V, transient -1V for less than 10ns.

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 560kHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range		•	5.5		14	V
V_{IN}	Input voltage range	V_{CC} tied to V_{IN}	•	4.5		5.5	V
V_{UVLO}	UVLO threshold	V_{IN} rising/falling			4.22/4.1		V
$UVLO_{DEGLITCH}$	UVLO deglitch	Rising/falling			110		µs
I_{VIN}	V_{IN} supply current	EN = GND			250		µA
I_{VINQ}		EN = high, no load			2.6		mA
Internal Supply Voltage							
V_{CC}	Internal biasing supply	I_{LOAD} = 0mA	•	4.9	5	5.1	V
I_{VCC}	Internal biasing supply current	V_{IN} = 12V	•			10	mA
V_{UVLO}	UVLO threshold for V_{CC}	V_{CC} rising			3.8		V
		V_{CC} falling			3.6		V
$UVLO_{DEGLITCH}$	UVLO deglitch for V_{CC}	Falling edge			110		µs

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 560kHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Protections							
T_{SD}	Thermal shutdown temperature	Temperature rising, Non-latch off. T_{SD} release threshold, temperature = T_{SD} - HY_{TSD}			160		°C
HY_{TSD}	Thermal shutdown hysteresis				20		°C
$T_{SD\_DEGLITCH}$	Thermal shutdown deglitch				110		µs
V_{OVBUCK}	Threshold voltage for buck overvoltage	Output rising (HS FET will be forced off)			109		%
		Output falling (HS FET will be allowed to switch)			107		%
Buck Converter							
f_{SW}	Switching frequency				560		kHz
t_{SS}	Soft-start period				0.83		ms
I_{LIMx}	Peak inductor current limit accuracy	Peak inductor current limit set at 2.5A for V_{OUT1}, and 2A for V_{OUT2} and V_{OUT3}		–30		+30	%
R_{ON_HSx}	HS switch on-resistance	V_{IN} = 12V			200		mΩ
R_{ON_LS1}	LS switch on-resistance of Buck1	V_{IN} = 12V			60		mΩ
$R_{ON\_LS2/3}$	LS switch on-resistance of Buck2/3	V_{IN} = 12V			80		mΩ
I_{Ox}	Output current capability	Loading(1)			2	3.2(2)	A
D_{MAX}	Maximum duty cycle				95		%
$t_{ON\ MIN}$	Minimum on time				120		ns
	Line regulation ($\Delta V_{OX}/V_{OX})/\Delta V_{INX}$	V_{INX} = 5.5V to 14V, I_{OX} = 1A			0.5		%/V
		V_{INX} = 4.5V to 5.5V, I_{OX} = 1A			0.5		%/V
	Load regulation ($\Delta V_{OX}/V_{OX}$)	I_{OX} = 10% to 90% of $I_{O(MAX)}$			0.5		%
	Output voltage accuracy	V_{IN} = 12V		–1		1	%
		V_{IN} = 5V		–1		1	%
		5.5V ≤ V_{IN} ≤ 14V	•	–2		2	%
		4.5V ≤ V_{IN} ≤ 5.5V	•	–2		2	%
$SYNC_{FREQ}$	Synchronization frequency				560		kHz
$SYNC_{D\_MIN}$	Synchronization signal minimum duty cycle		•	40			%
$SYNC_{D\_MAX}$	Synchronization signal maximum duty cycle		•			60	%

NOTE:
1. Subject to thermal derating and current limit setting. Design must not exceed the package thermal rating.
2. Only CH1 with 0.9V can support 3.2A with maximum loading condition.

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 560kHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Good Reset Generator							
V_{UVBUCK}	Threshold voltage for buck under voltage	Output falling, (disabled after t_{ON_HICCUP})			85		%
		Output rising, (PG will be asserted)			90		
$t_{PG\_DEGLITCH}$	Deglitch time	Rising and falling			11		ms
t_{ON_HICCUP}	Hiccup mode on time	$V_{UVBUCKX}$ asserted			12		ms
t_{OFF_HICCUP}	Hiccup mode off time	Once t_{OFF_HICCUP} elapses, all converters will start up again			15		ms
t_{RP}	Minimum reset period				1		s
	PGOOD output low	I_{SINK} = 1mA	•			0.4	V
Input Threshold (SYNC, EN)							
V_{IH}	Input threshold high	V_{INPUT} rising	•	2.53			V
V_{IL}	Input threshold low	V_{INPUT} falling	•			1.36	V

Pin Configuration

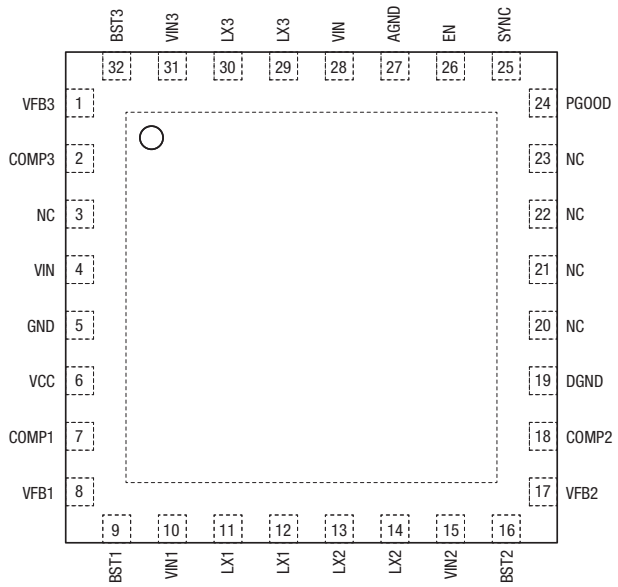


Figure 3. XR77103-MoCA Pinout

Pin Functions

Pin Number	Pin Name	Description
1	VFB3	Buck 3 feedback pin.
2	COMP3	Compensation pin for Buck 3. Connect a series RC circuit to this pin for compensation.
3	NC	No connect.
4	VIN	IC supply pin. Connect a capacitor as close as possible to this pin.
5	GND	Ground.
6	VCC	Internal supply. Connect a ceramic capacitor from this pin to ground.
7	COMP1	Compensation pin for Buck 1. Connect a series RC circuit to this pin for compensation.
8	VFB1	Buck 1 feedback pin.
9	BST1	Bootstrap capacitor for Buck 1. Connect a bootstrap capacitor from this pin to LX1.
10	VIN1	Input supply for Buck 1. Connect a capacitor as close as possible to this pin.
11	LX1	Switching node for Buck 1.
12	LX1	Switching node for Buck 1.
13	LX2	Switching node for Buck 2.
14	LX2	Switching node for Buck 2.
15	VIN2	Input supply for Buck 2. Connect a capacitor as close as possible to this pin.
16	BST2	Bootstrap capacitor for Buck 2. Connect a bootstrap capacitor from this pin to LX2.
17	VFB2	Buck 2 feedback pin.
18	COMP2	Compensation pin for Buck 2. Connect a series RC circuit to this pin for compensation.
19	DGND	Digital ground.

Pin Functions (Continued)

Pin Number	Pin Name	Description
20	NC	No connect.
21	NC	No connect.
22	NC	No connect.
23	NC	No connect.
24	PGOOD	Power good output. Open drain output asserted after all converters are sequenced and within regulation.
25	SYNC	External clock input pin. Connect to signal ground when unused.
26	EN	Enable control input. Set EN high to enable converters.
27	AGND	Analog ground.
28	VIN	IC supply pin. Connect a capacitor as close as possible to this pin.
29	LX3	Switching node for Buck 3.
30	LX3	Switching node for Buck 3.
31	VIN3	Input supply for Buck 3. Connect a capacitor as close as possible to this pin.
32	BST3	Bootstrap capacitor for Buck 3. Connect a bootstrap capacitor from this pin to LX3.
-	E-PAD	Connect to power ground.

Typical Performance Characteristics

All data taken at f_{SW} = 560kHz, T_A = 25°C, no airflow, unless otherwise specified.

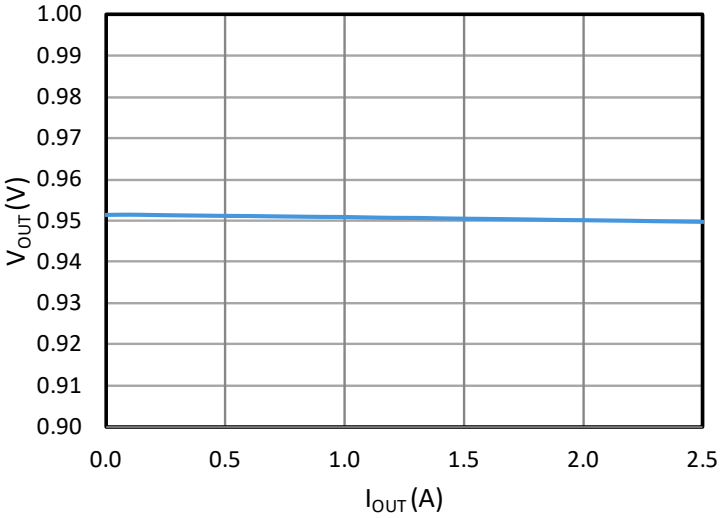


Figure 4. Load Regulation Channel 1, $12V_{IN}$, $0.9V_{OUT}$

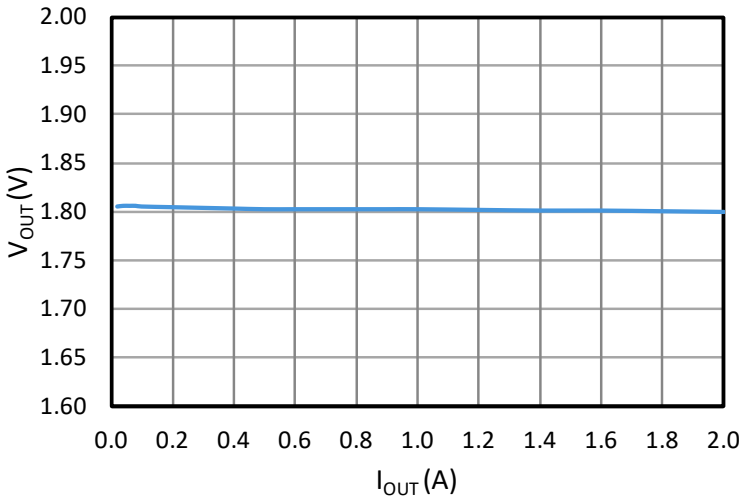


Figure 5. Load Regulation Channel 2, $12V_{IN}$, $1.8V_{OUT}$

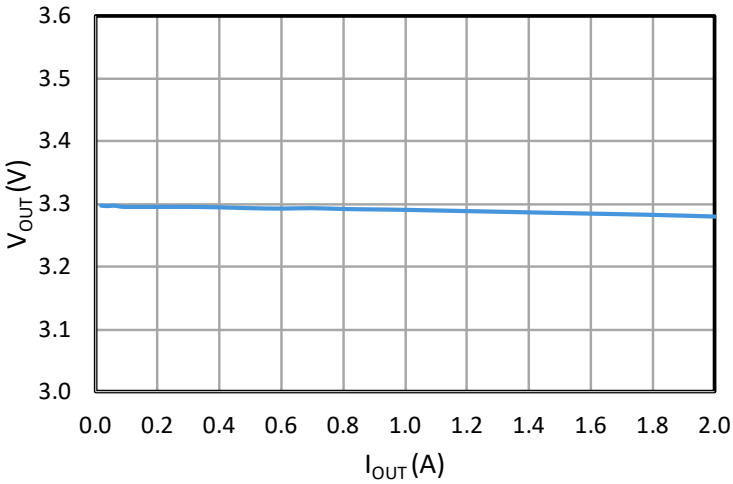


Figure 6. Load Regulation Channel 3, $12V_{IN}$, $3.3V_{OUT}$

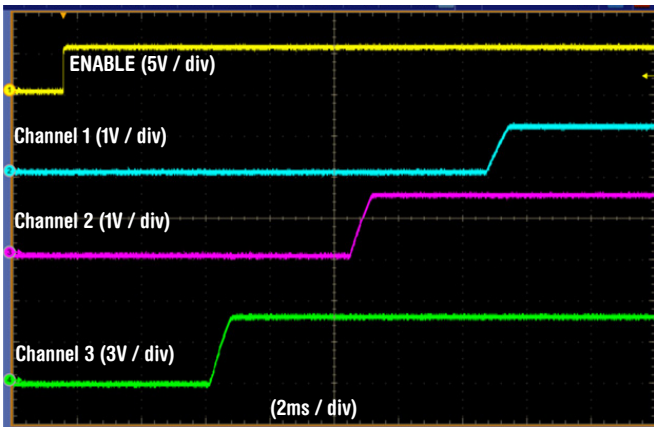


Figure 7. Power-up Sequence

Typical Performance Characteristics (Continued)

All data taken at f_{SW} = 560kHz, T_A = 25°C, no airflow, unless otherwise specified.

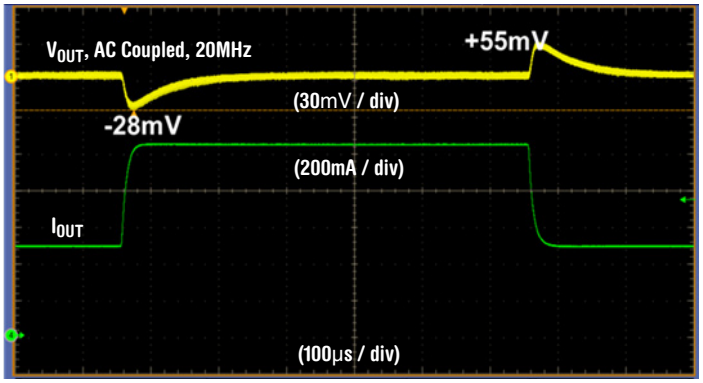


Figure 8. $12V_{IN}$, $0.9V_{OUT}$
Transient Response, 0.5A to 1.0A

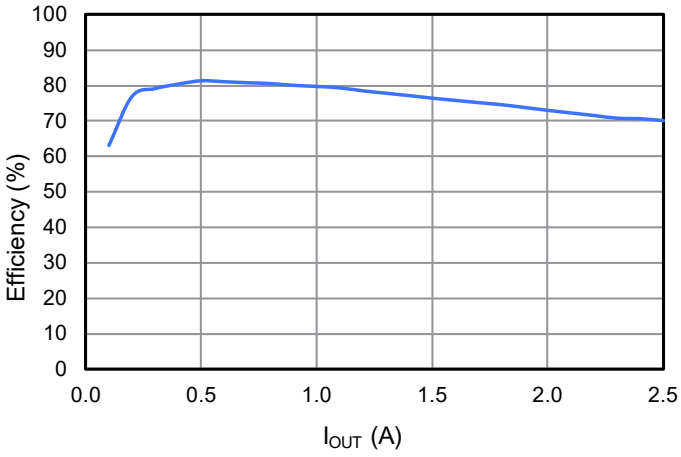


Figure 9. Efficiency Channel 1,
$12V_{IN}$ $0.9V_{OUT}$

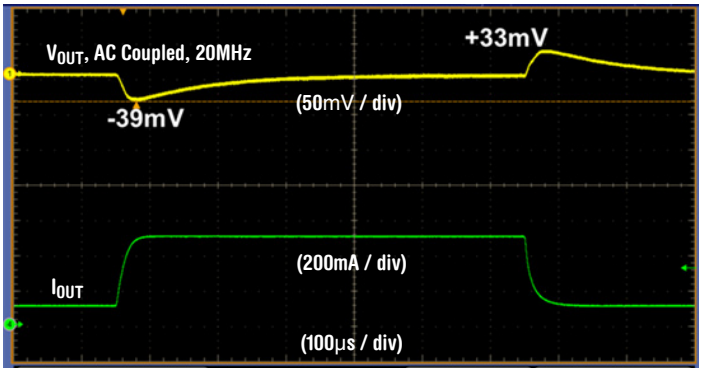


Figure 10. $12V_{IN}$, $1.8V_{OUT}$
Transient Response, 0.1A to 0.5A

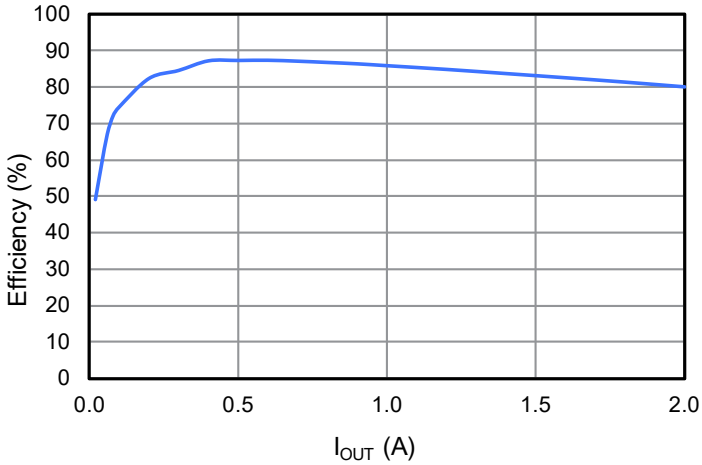


Figure 11. Efficiency Channel 2,
$12V_{IN}$ $1.8V_{OUT}$

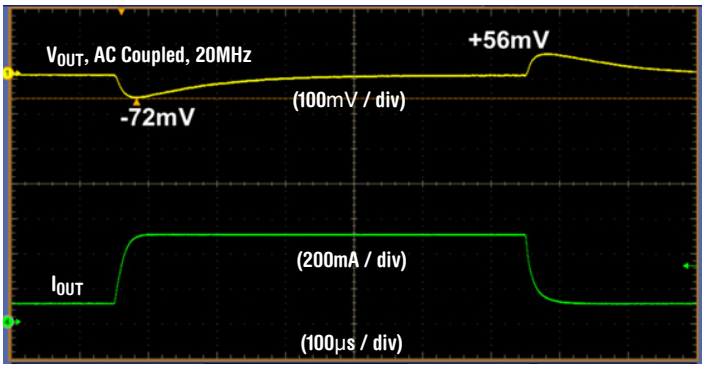


Figure 12. $12V_{IN}$, $3.3V_{OUT}$
Transient Response, 0.1A to 0.5A

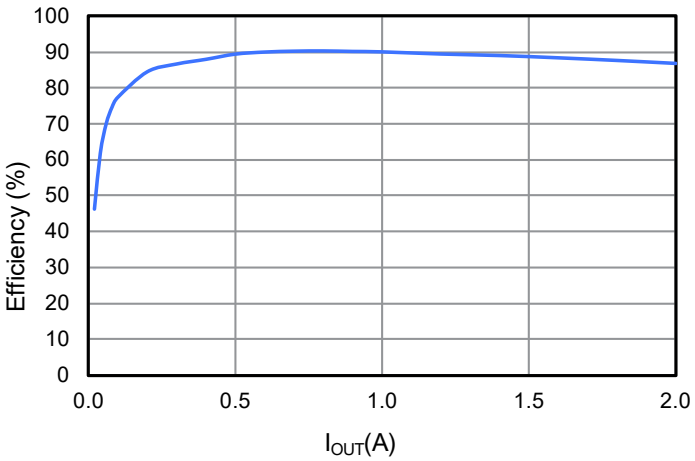


Figure 13. Efficiency Channel 3,
$12V_{IN}$ $3.3V_{OUT}$

Typical Performance Characteristics (Continued)

Thermal Characteristics

f_{SW} = 560kHz, T_A = 25°C, no airflow, only individual channel operating; inductor losses are included.

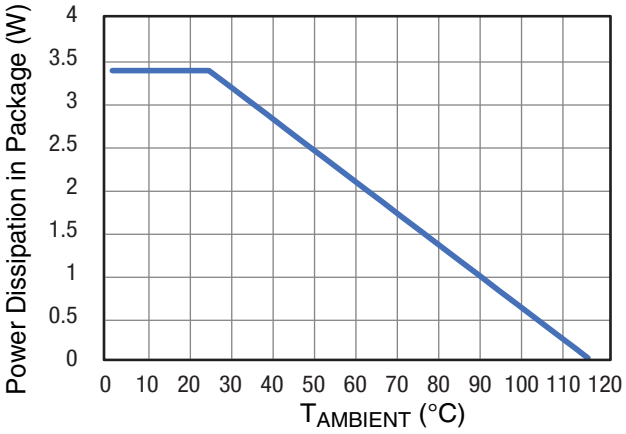


Figure 14. Package Thermal Derating

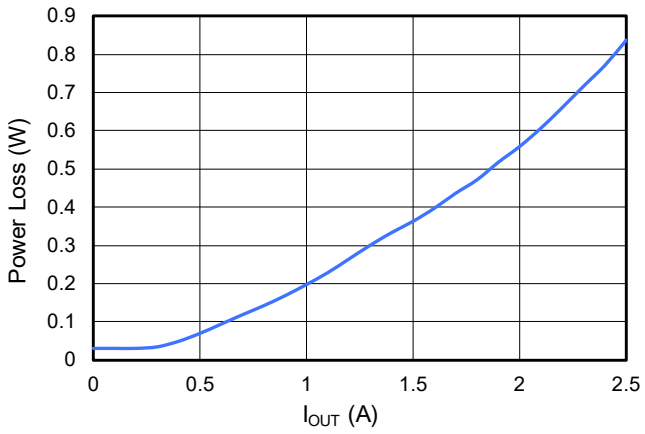


Figure 15. Channel 1 Power Loss at V_{IN} = 12V, 0.9V_{OUT}, No Airflow

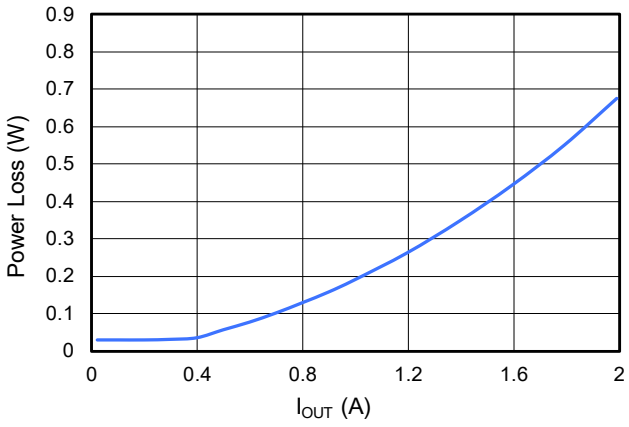


Figure 16. Channel 2 Power Loss at V_{IN} = 12V, 1.8V_{OUT}, No Airflow

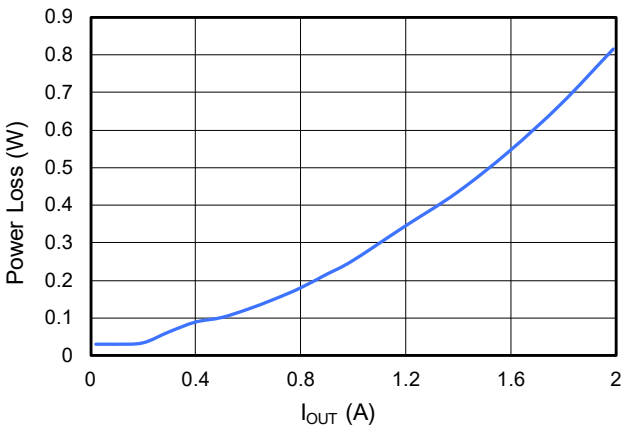


Figure 17. Channel 3 Power Loss at V_{IN} = 12V, 3.3V_{OUT}, No Airflow

Functional Block Diagram

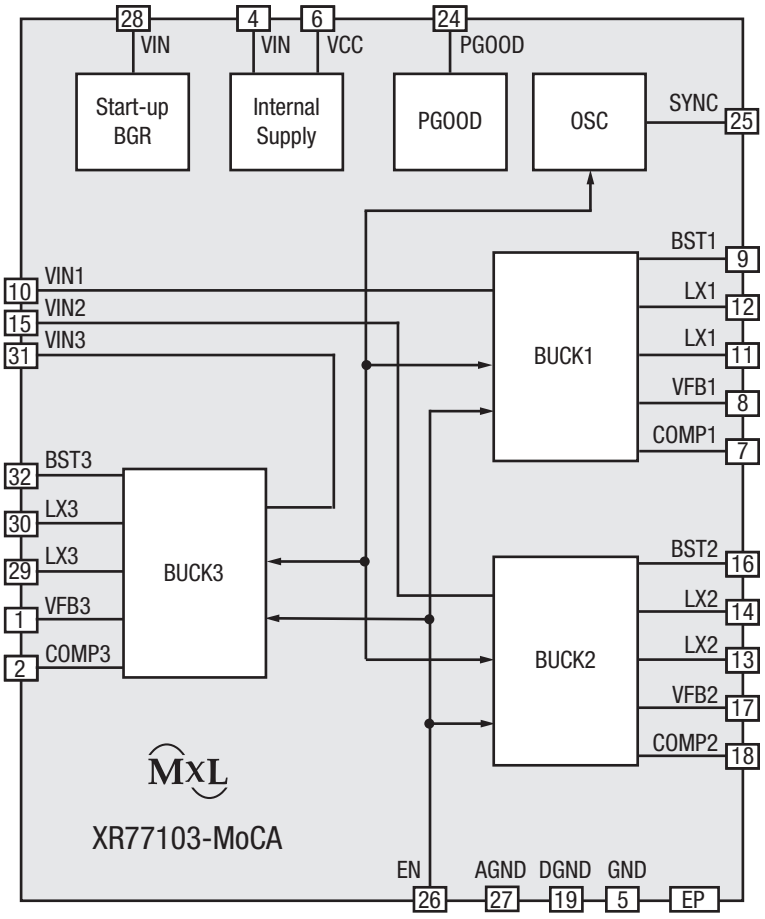


Figure 18. Functional Block Diagram

Applications Information

Operation

XR77103-MoCA is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. XR77103-MoCA can support a 4.5V to 14V input supply, high load current, and 560kHz clocking. The SYNC pin also provides a means to synchronize the power converter to an external signal. Input ripple is reduced by operation 180 degrees out-of-phase among converters. All three buck converters have peak current mode control which simplifies external frequency compensation. Buck converters 1, 2, and 3 have nominal peak inductor current limit of 4A, 2A, and 2A respectively. The device has a power good comparator monitoring the output voltage. Soft-start for each converter is 0.83ms. All outputs start up once the EN pin is set high.

Minimum On-Time $t_{ON\ (min)}$ Considerations

The XR77103 can regulate with pulse widths as low as 95ns. However, to ensure sufficent control range, the design must use 120ns as the minimum on-time as stated in the electrical table. Failure to meet this condition can result in overcharging of the output and V_{OUT} not meeting specification.

Output Voltage Setting

Output voltage is pre-programmed to V_{OUT1} = 0.9V, V_{OUT2} = 1.8V, and V_{OUT3} = 3.3V.

Frequency Compensation

In order to properly frequency compensate the device, the following component selection is recommended:

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (nF)
12/5.0	0.9	3.3	22 x 3	10	1
12/5.0	1.8	3.3	22 x 2	10	1
12/5.0	2.5	3.3	22 x 2	10	1
12/5.0	3.3	3.3	22 x 2	10	1

Synchronization

The status of the SYNC pin will be ignored during start-up and the XR77103-MoCA's control will only synchronize to an external signal after the PGOOD signal is asserted. When synchronization is applied, the sync pulse frequency must be higher than the PWM oscillator frequency (560kHz) to allow the external signal to trump the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to the signal ground.

Although the device can lock to an external clock running up to 2.31MHz, doing this will alter the timing characteristics and degrade thermal performance.

Out-of-Phase Operation

Channels 2 and 3 operate in phase while channel 1 operates 180 degrees out-of-phase with the other two converters (see Figure 19). This enables the system, having less input ripple, to lower component cost, save board space, and reduce EMI.

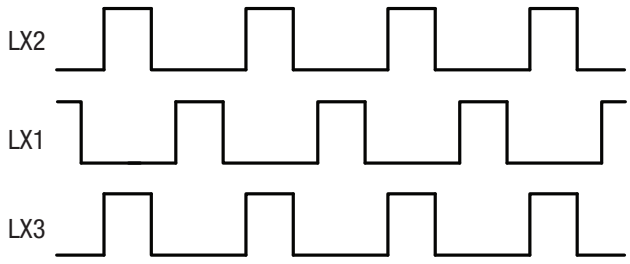


Figure 19. Out-of-Phase Operation

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all three buck converters' outputs are more than 90% of their nominal output voltage and the PGOOD reset timer expires. The polarity of the PGOOD is active high. The PGOOD reset time is 1s.

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR77103-MoCA (30°C/W) is specified in the Operating Conditions section of this datasheet. The θ_{JA} thermal resistance specification is based on the XR77103-MoCA evaluation board operating without forced airflow. Since the actual board design in the final application will be different, the thermal resistances in the final design may be different from those specified.

Applications Information (Continued)

Layout Guidelines

Proper PCB layout is crucial in order to obtain good thermal and electrical performance.

For thermal considerations, it is essential to use a number of thermal vias to connect the central thermal pad to the ground layer(s).

In order to achieve good electrical and noise performance , the following steps are recommended:

- Place the output inductor close to the LX pins and minimize the area of the connection. Doing this on the top layer is advisable.
- Connect the central thermal pad to the power ground connections to as many layers as possible.
- The output filtering capacitor and the input filtering capacitor shall share the same power ground connection. Connection to the signal ground plane shall be done with vias placed at the output filtering capacitors.
- Minimize AC current loops formed by input filtering capacitors, output filtering capacitors, output inductors, and the regulator pins.
- Connect the GND, AGND, DGND pins to the signal ground plane.
- Place compensation networks close to the pins and reference them to the signal ground.
- Place the V_{CC} bypass capacitor close to the pin.

Applications Information (Continued)

Typical Applications

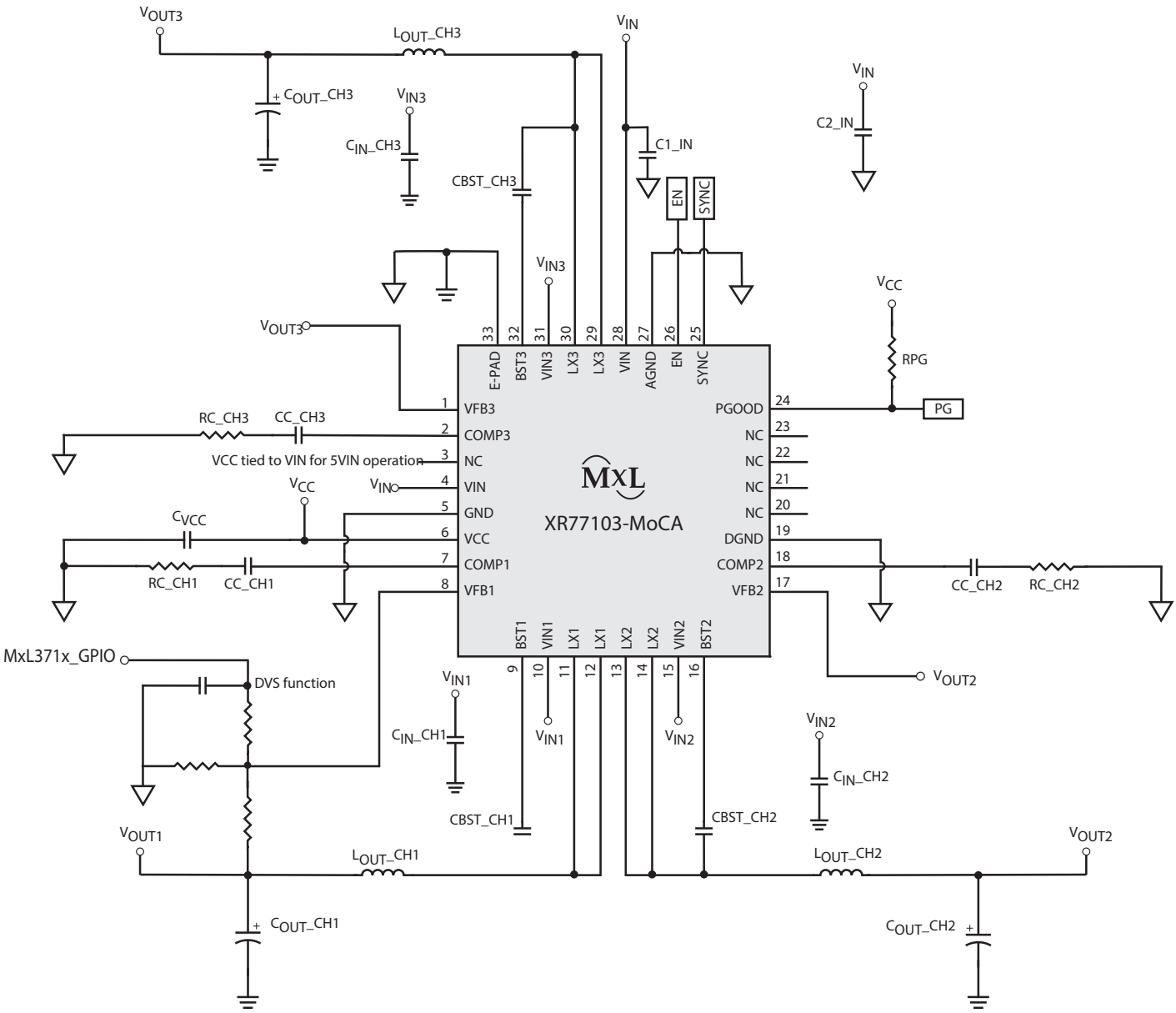
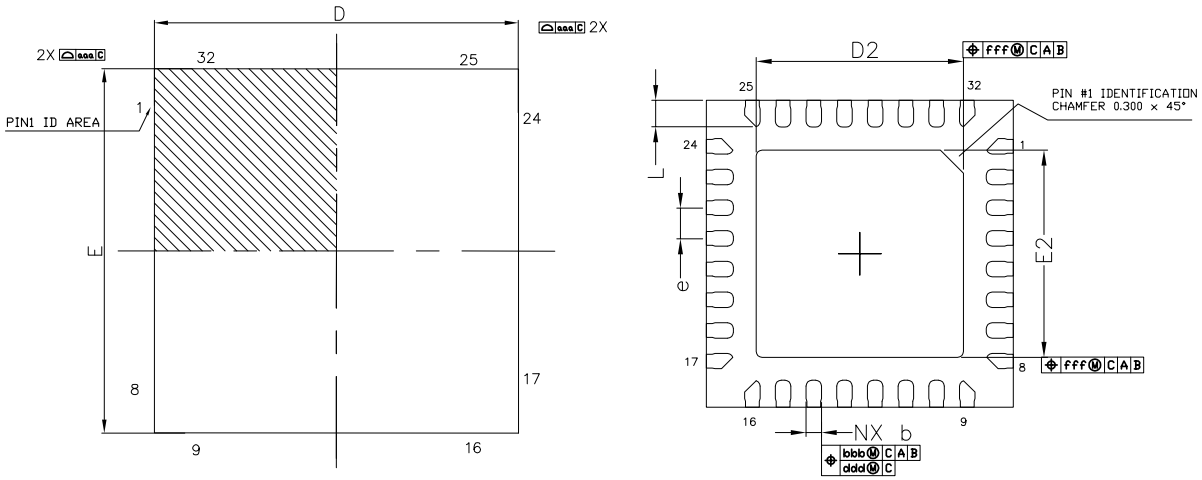


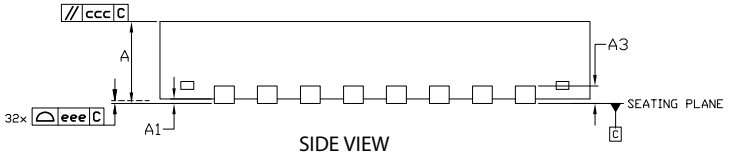
Figure 20. Typical Applications Schematic

Mechanical Dimensions



TOP VIEW

BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203Ref	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.30	0.35	0.40
K	0.20	–	–
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		32	

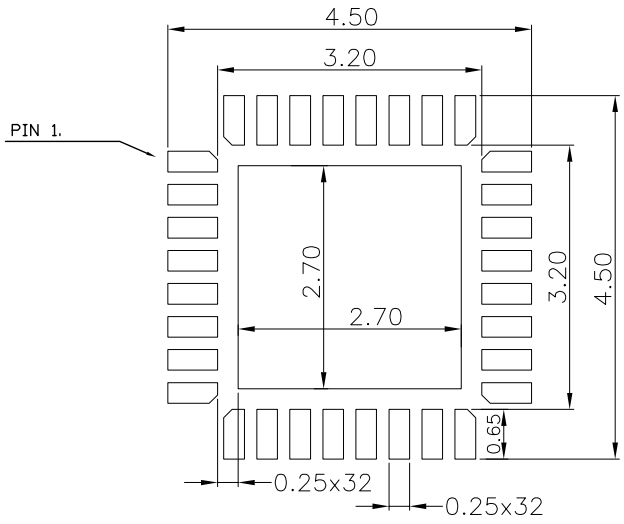
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

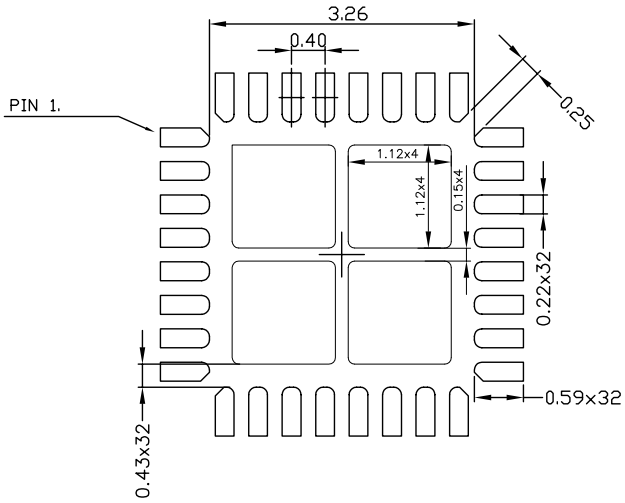
Drawing No.: POD-00000079

Revision: C

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000079

Revision: C

Order Information

Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free
XR77103ELBTR-MOCA	–40°C ≤ T_J ≤ 125°C	32-pin, 4mm x 4mm TQFN package	Tape and Reel	Yes
XR77103-MoCA-EVK-1	XR77103-MoCA evaluation board			

NOTE: for most up-to-date ordering information and additional information on environmental rating, go to to www.maxlinear.com/XR77103-MoCA.

Revision History

Revision	Date	Description
206DSR00	July 5, 2021	Initial Release

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XR77103ELBTR-MOCA XR77103-MOCA-EVK-1