XR46073

Two-Step LED Current Controller with Line Regulation Compensation

Description

The XR46073 is a two-step LED current controller with line regulation compensation for operating over a wide Alternative Current (AC) voltage source range. It can drive an external N-channel power MOSFET to regulate the current flowing through a High Voltage (HV) LED string.

The XR46073 works as a constant current sink with linear type Overvoltage Protection (OVP), linear type Over Temperature Protection (OTP) and line regulation compensation. It is suitable for applications with a rectified AC voltage source.

The PCB design can be very compact to meet various shape requirements. It is especially suitable for replacing incandescent light bulbs.

FEATURES

Device

- Two-current step control from a single device
- Excellent system power regulation over AC input range
- 6V to 76V chip supply voltage range
- Over temperature protection
- Overvoltage protection
- TDFN-6 2mm x 2mm package

System

- Single board LED lighting solution available
- No electrolytic capacitor or MOV required
- Scalable architecture allows optimization of performance vs. cost
- Driver-on-board and chip-on-board design solution available which minimize process flow and assembly cost
- High PF and Low THD performance
- Flexible PCB layout options
- TRIAC dimmable
- All solid state components

APPLICATIONS

- LED Lighting Applications
  - Downlight
  - High bay
  - Specialty
  - Architectural

Typical Application

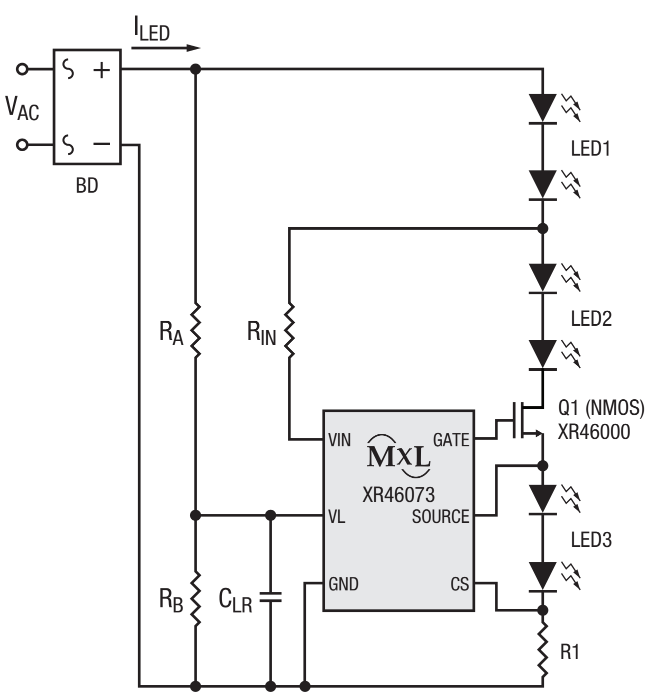


Figure 1. Typical Application

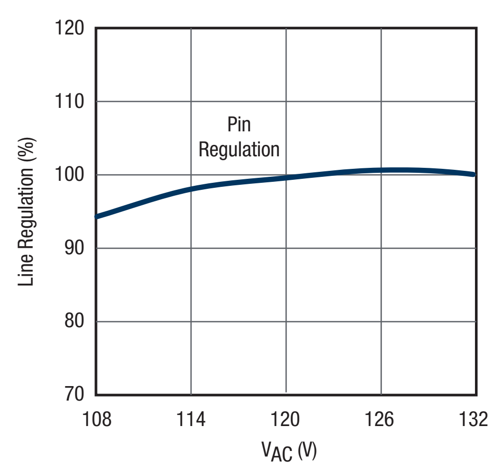


Figure 2. Two-Step 120V_{AC}

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_{IN}, GATE, SOURCE to GND .... -0.3V to 85V

SOURCE to CS .... -0.3V to 70V

GATE to SOURCE .... -0.3V to 7V

VL to GND .... -0.3V to 7V

CS to GND... -0.3V to 1V

V_{IN} input current 3mA

SOURCE to CS current.. 180mA

Maximum operating junction temperature, T_J........... 150°C

Operating temperature, T_{OPR} .... -40°C to 85°C

Storage temperature range .... -55°C to 150°C

Lead temperature (soldering, 10 seconds)................ 260°C

ESD Rating

HBM (Human Body Model) .... ±2kV

MM (Machine Model .... ±200V

Operating Conditions

V_{IN} ....6V to 76V

Peak level current... 20 to 180mA

NOTES:

1. All voltages are with respect to ground. Currents are positive into negative out of the specified terminal.
2. All parameters having min/max specifications are guaranteed. Typical values are for reference purpose only.
3. Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

Unless otherwise noted, typical values are at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN,MIN}$	Minimum V_{IN} supply voltage		6			V
I_{IN}	V_{IN} supply current	V_{IN} = 6V to 73V		0.3		mA
$V_{IN,CLAMP}$	V_{IN} overvoltage clamp	When V_{IN}>$V_{IN,\ CLAMP}$, I_{IN} will increase to >1mA to clamp V_{IN} at $V_{IN,\ CLAMP}$	74	76	80	V
V_{CS}	CS voltage	V_{IN} = 15V and 75V, V_{VL} = 1.75V	244	250	256	mV
ΔV_{LR1}	CS voltage line regulation vs. V_{VL} (1)	V_{VL} = 1.57V to 1.75V		-0.28		mV/mV
ΔV_{LR2}		V_{VL} = 1.75V to 2.10V		-0.24		
ΔV_{LR3}		V_{VL} = 2.10V to 2.28V		-0.3		
V_{REF1}/V_{REF0}	Reference voltge ratio		86	90	94	%
$V_{CS,CLAMP}$	Maximum $V_{CS,\ CLAMP}$	VL under voltage protection, V_{VL} < 1.45V	310	323	336	mV
V_{GATE}	Gate voltage	Gate to SOURCE		5.4		V
I_{SOURCE}	GATE source current(2)	V_{GATE} to V_{SOURCE} = 3V		30		µA
I_{SINK}	GATE sink current(2)	V_{GATE} to V_{SOURCE} = 3V		500		µA
T_{TP}	Thermal protection trip temperature(2)	When T_J is higher than T_{TP}, V_{CS} decreases linearly	135	145		°C
$\Delta V_{CS}/\Delta T_J$	Thermal protection mode V_{CS} decreasing slope(2)	$T_J > T_{TP}$		-1.1		%/°C

NOTES:

1. The CS voltage line regulation is defined as:

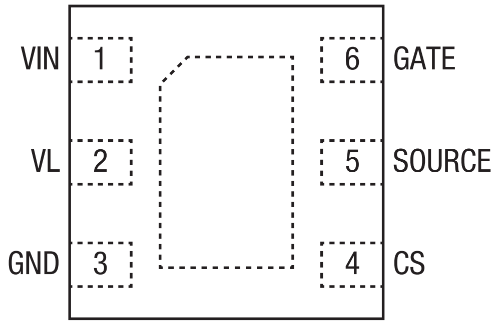
$$\Delta V_{LR1} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS(V_{VL} = 1.75V)} - V_{CS(V_{VL} = 1.57V)}}{1.75V - 1.57V}$$

$$\Delta V_{LR2} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS(V_{VL} = 2.10V)} - V_{CS(V_{VL} = 1.75V)}}{2.10V - 1.75V}$$

$$\Delta V_{LR3} = \frac{\Delta V_{CS}}{\Delta V_{VL}} = \frac{V_{CS(V_{VL} = 2.28V)} - V_{CS(V_{VL} = 2.10V)}}{2.28V - 1.10V}$$

2. Guaranteed by design, not by production test.

Pin Configuration



TDFN-6 2mm x 2mm

Pin Functions

Pin Number	Pin Name	Description
1	VIN	Power supply pin.
2	VL	Line regulation sense pin. The reference voltage is adjusted according to V_L to provide the line regulation compensation and to provide overvoltage protection.
3	GND	Ground pin.
4	CS	Current sense pin. Connect a sense resistor, R_{CS}, between this pin and the GND pin. The peak current is set by: $I_{OUT} = \frac{V_{CS}}{R_{CS}}$
5	SOURCE	External HV NMOS source pin. The VF of the LED segment connected between the SOURCE pin and the CS pin should not be higher than 70V.
6	GATE	External HV NMOS gate driving pin, limited to 5.5V maximum.
EP		Exposed thermal pad (EP) of the chip. Use this pad to enhance the power dissipation capability. The thermal conductivity will be improved if a copper foil on PCB is soldered with the thermal pad. It is recommended to connect the exposed thermal pad to the GND pin.

Typical Performance Characteristics

For a typical 2-step driving scheme using a single XR46073, the electrical performance is good enough to meet applications where the Power Factor (PF) is higher than 0.92 and the Total Harmonic Distortion (THD) is around 30%. If higher PF or lower THD is required, one more XR46083 or XR46084 can be added to the circuit to make a 3-step driving scheme, as shown below. The 3-step system can provide better electrical performance with PF greater than 0.96 and THD approximately 20%.

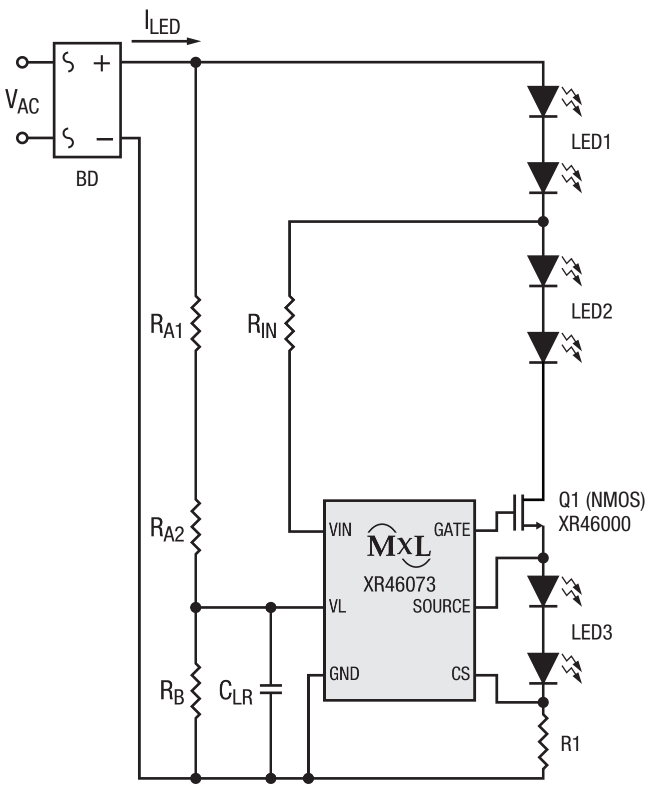


Figure 3. Two-Step (PF > 0.92 and THD = ~ 30%)

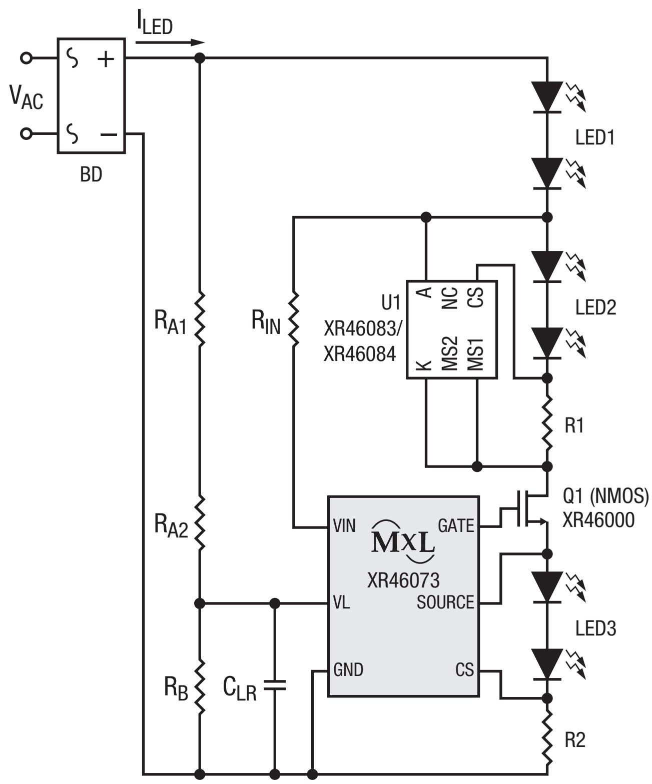


Figure 4. Three-Step (PF > 0.96 and THD = ~ 20%)

Functional Block Diagram

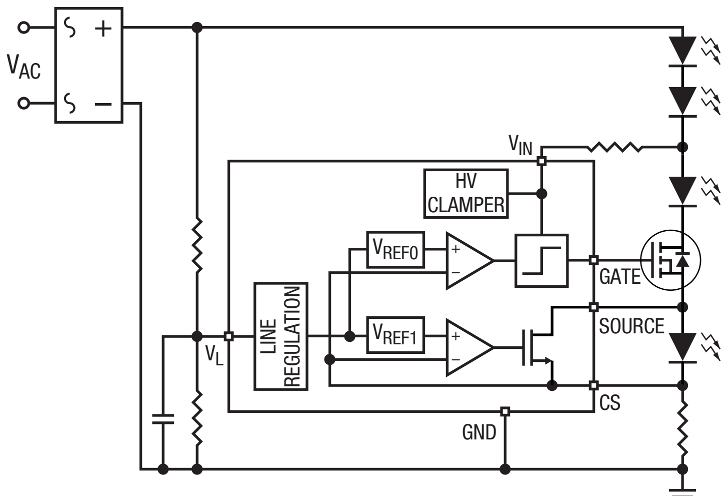


Figure 5. Functional Block Diagram

Applications Information

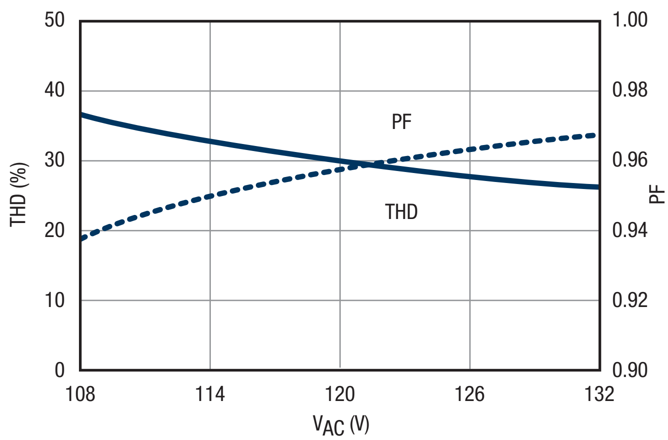


Figure 6. PF and THD, $120V_{AC}$

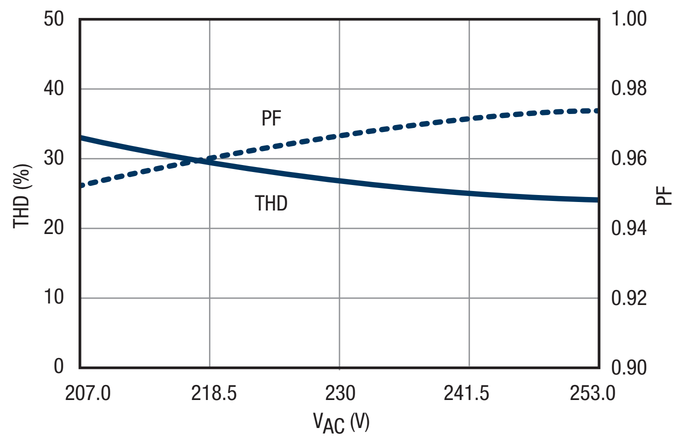


Figure 7. PF and THD, $230V_{AC}$

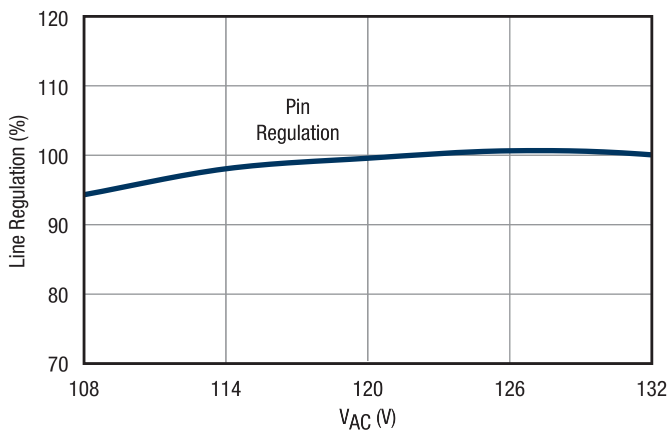


Figure 8. Line Regulation, $120V_{AC}$

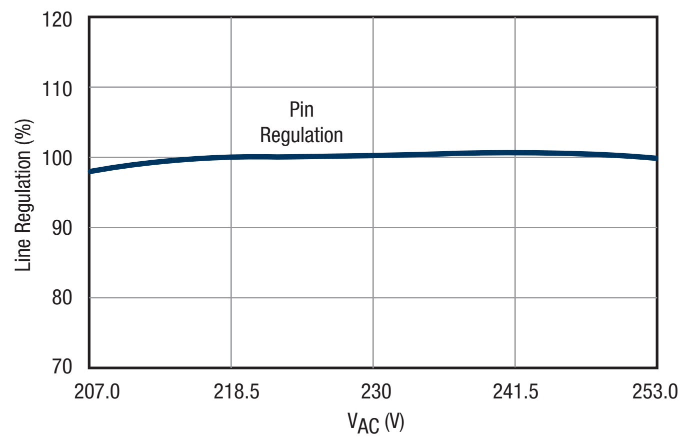


Figure 9. Line Regulation, $230V_{AC}$

Applications Information (Continued)

Linear Type Thermal Protection

When the junction temperature T_J rises to the Thermal Protection Trip Temperature T_{TP} (typically 145°C), the current sense voltage V_{CS} starts to decrease linearly at a slope of -1.1%/°C. The LED driving current decreases proportionally with the V_{CS} voltage. The system will function normally during the thermal protection mode with the lower driving current but the power dissipation of the XR46073 chip will decrease until thermal equilibrium is reached.

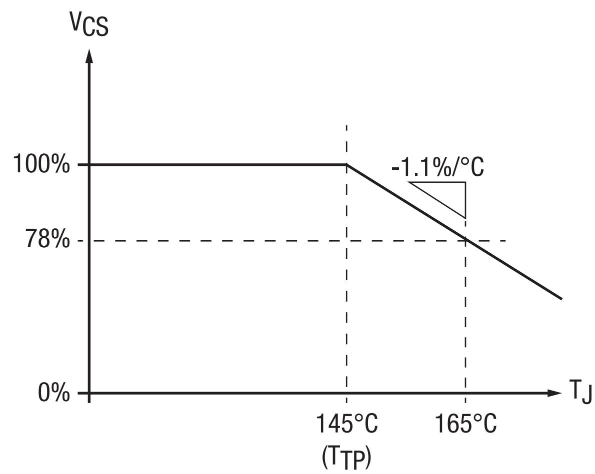


Figure 10. Linear Type Thermal Protection

Line Regulation Compensation

When there is variation in line voltage (V_{AC}), the power of the lamp will also change if the LED driving current is kept unchanged. In order to provide good line regulation when V_{AC} varies within a ±20% range, the average of the rectified V_{AC} is sensed by the VL pin to provide compensation in order to attempt to keep the power of lamp at the same level.

The LED driving current is adjusted as the voltage level V_{VL} at VL pin is changed. Based on the design, the LED driving current will be lower when V_{AC} is higher than the nominal value, and the LED driving current will be higher when V_{AC} is lower than the nominal value. The system power can then be maintained at approximately the same level. During power on, the driving current may be slightly higher for a few cycles until steady state is reached.

With the compensation function, the XR46073 provides excellent power line regulation over a ±20% V_{AC} variation range, as shown below.

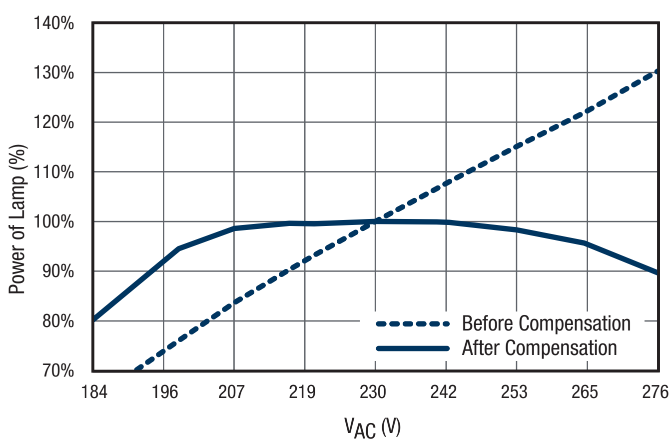


Figure 11. Power Line Regulation,
$230V_{AC}$ ±20%

Applications Information (Continued)

Layout Suggestion

The exposed thermal pad under the chip is used to enhance the power dissipation capability of the DFN package. The thermal conductivity will be improved if a copper foil on the PCB that is soldered to the thermal pad can be as large as possible. It is strongly recommended to connect the GND pin to the exposed thermal pad.

The external HV NMOS is also recommended to be placed close to the XR46073. The pull-high resistors for the VIN pin and the VL pin should be placed close to the chip. In addition, the current sense resistor connected between the CS pin and GND pin should be placed as close as possible to the CS pin and GND pin, as shown below.

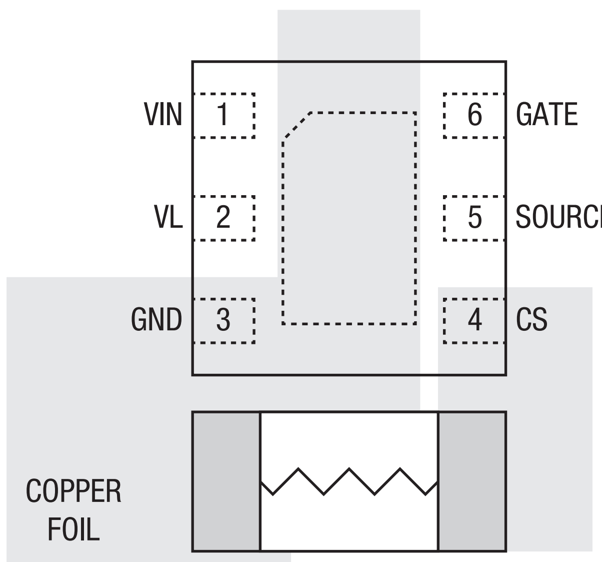
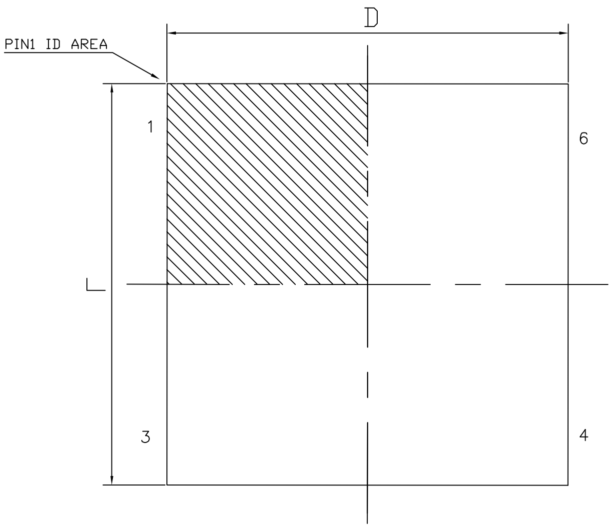
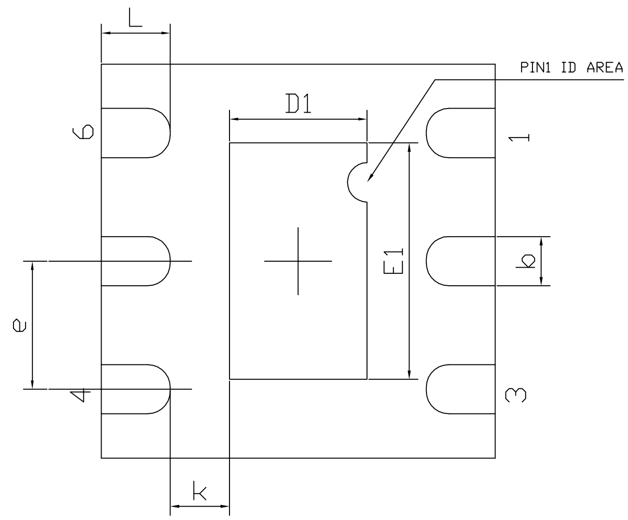


Figure 12. Positioning Illustration

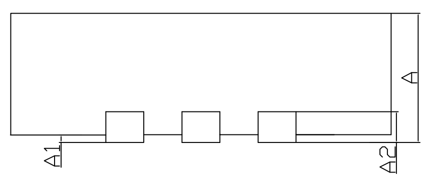
Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL \ DIM	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	–	0.050
A2	0.203Ref		
b	0.200	0.250	0.300
D	2.00 BSC		
E	2.00 BSC		
e	0.650 BSC		
D1	0.600	0.700	0.800
E1	1.100	1.200	1.300
L	0.274	0.350	0.426
K	0.200	–	–
N	6		

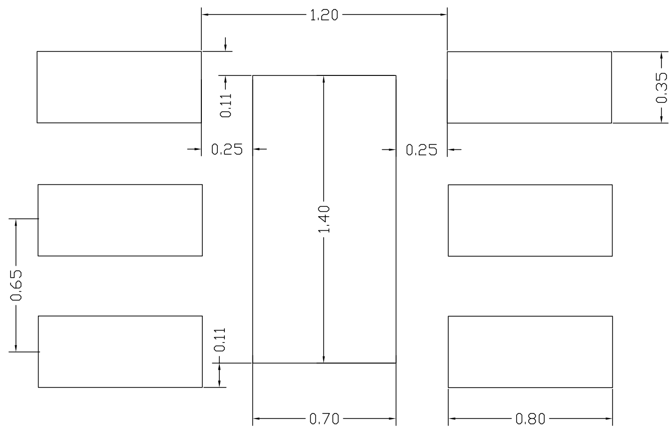
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-229.

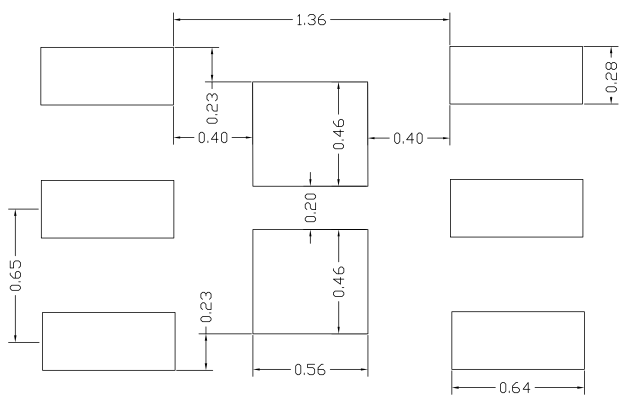
Drawing No.: POD-00000072

Revision: B

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000072

Revision: B

Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR46073IHBTR	-40°C to 85°C	Yes[2]	TDFN6 2x2	Tape and reel

NOTE:
1. Refer to www.exar.com/XR46073 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	June 2015	Initial release.
1B	Nov 2016	Update Package Description and Ordering Information table.
1C	Aug 2018	Update to MaxLinear logo. Update format.

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