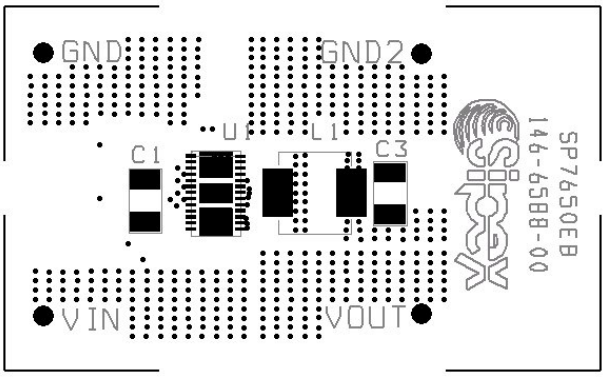
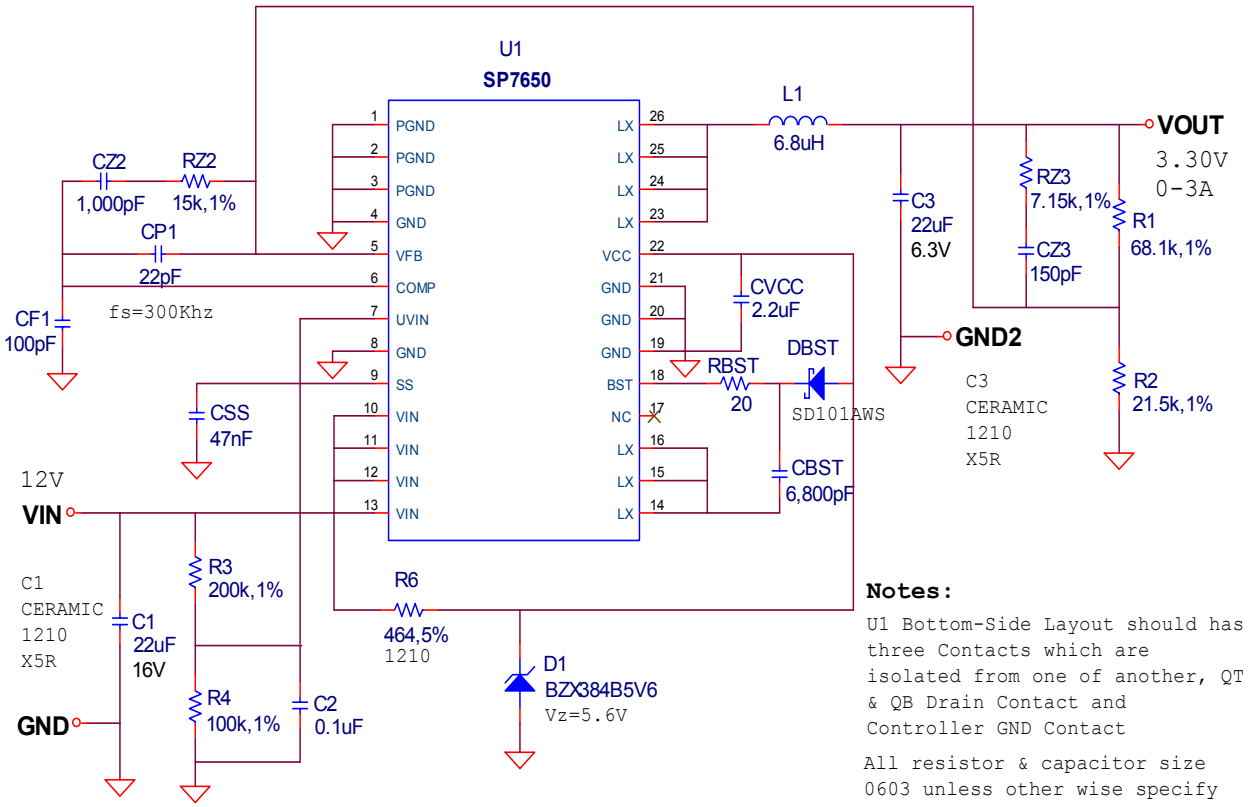
SP7650
Evaluation Board Manual

- Easy Evaluation for the SP7650ER 12V Input, 0 to 3A Output Synchronous Buck Converter
- Built in Low Rds(on) Power FETs
- UVLO Detects Both VCC and VIN
- High Integrated Design, Minimal Components
- High Efficiency: 90%
- Feature Rich: UVIN, Programmable Softstart, External VCC Supply and Output Dead Short Circuit Shutdown



SP7650EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP7650EB Circuit

Connect the SP7650 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

It’s best to GND reference scope and digital meters using the Star GND post in the center of the board. VOUT ripple can best be seen touching probe tip to the pad for C3 and scope GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7650 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7650 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$Vout = 0.80V \left(R1 / R2 + 1 \right) \Rightarrow R2 = R1 / \left[\left(Vout / 0.80V \right) - 1 \right]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP7650 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7650ER provides short circuit protection by sensing Vout at GND.

POWER SUPPLY DATA

The SP7650ER is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP7650 Evaluation Board Efficiency plot, with efficiencies to 90% and output currents to 3A. SP7650ER Load Regulation is shown in Figure 2 of only 0.1% change in output voltage from no load to 3A load. Figures 3 and 4 illustrate a 1.5A to 3A and 0A to 3A Load Step. Start-up Response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. In Figure 8 the SP7650ER is configured for hiccup mode in response to an output dead short circuit condition and will Softstart until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 40mV at no load to 3A load.

While data on individual power supply boards may vary, the capability of the SP7650ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

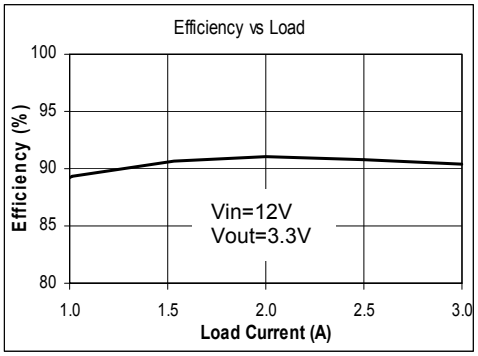


Figure 1. Efficiency vs Load

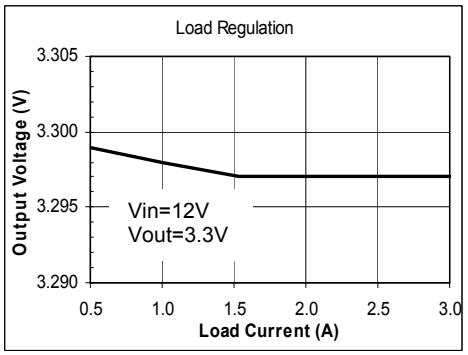


Figure 2. Load Regulation

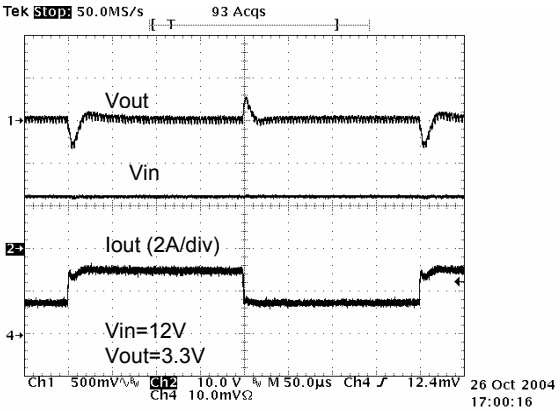


Figure 3. Load Step Response: 1.5->3A

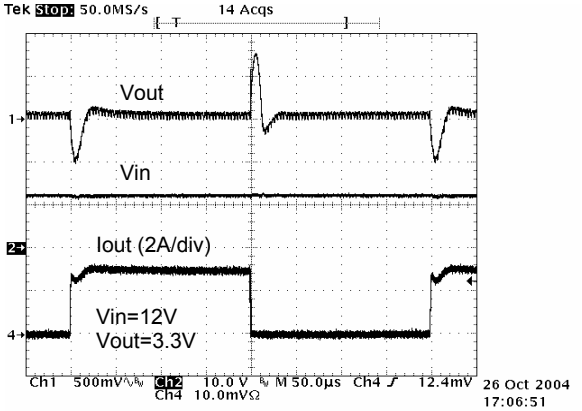


Figure 4. Load Step Response: 0->3A

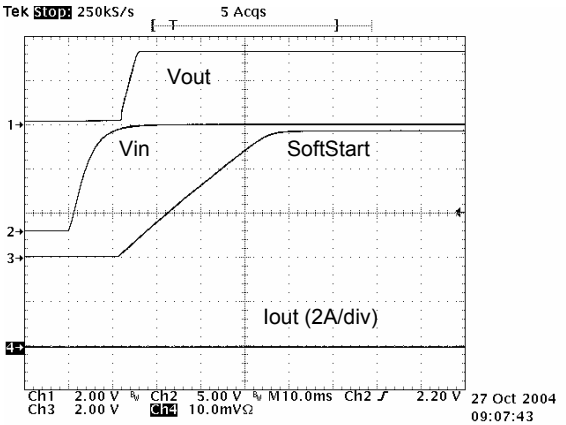


Figure 5. Start-Up Response: No Load

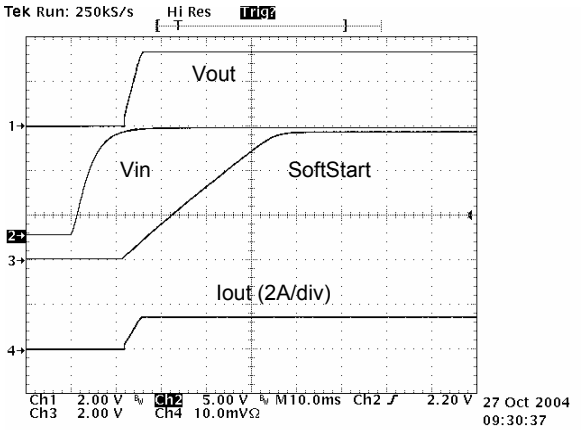


Figure 6. Start-Up Response: 1.5A Load

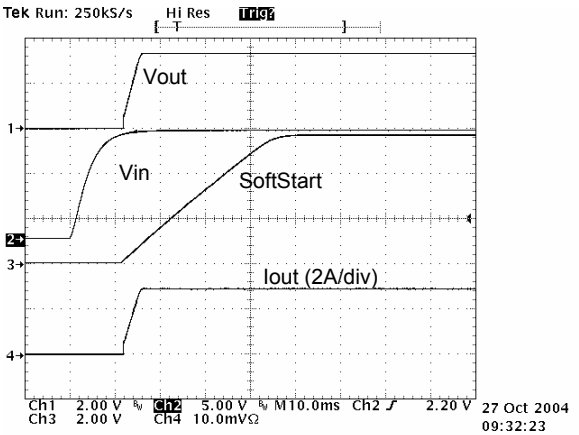


Figure 7. Start-Up Response: 3A Load

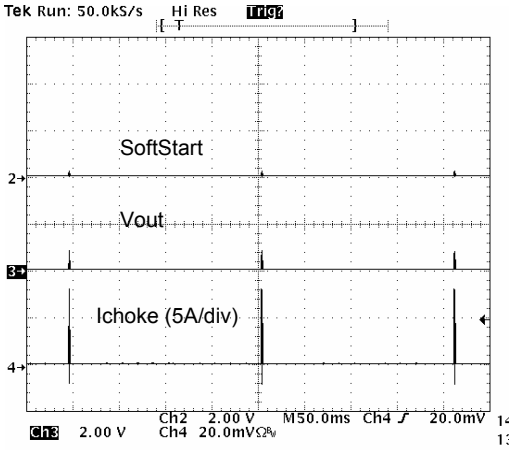
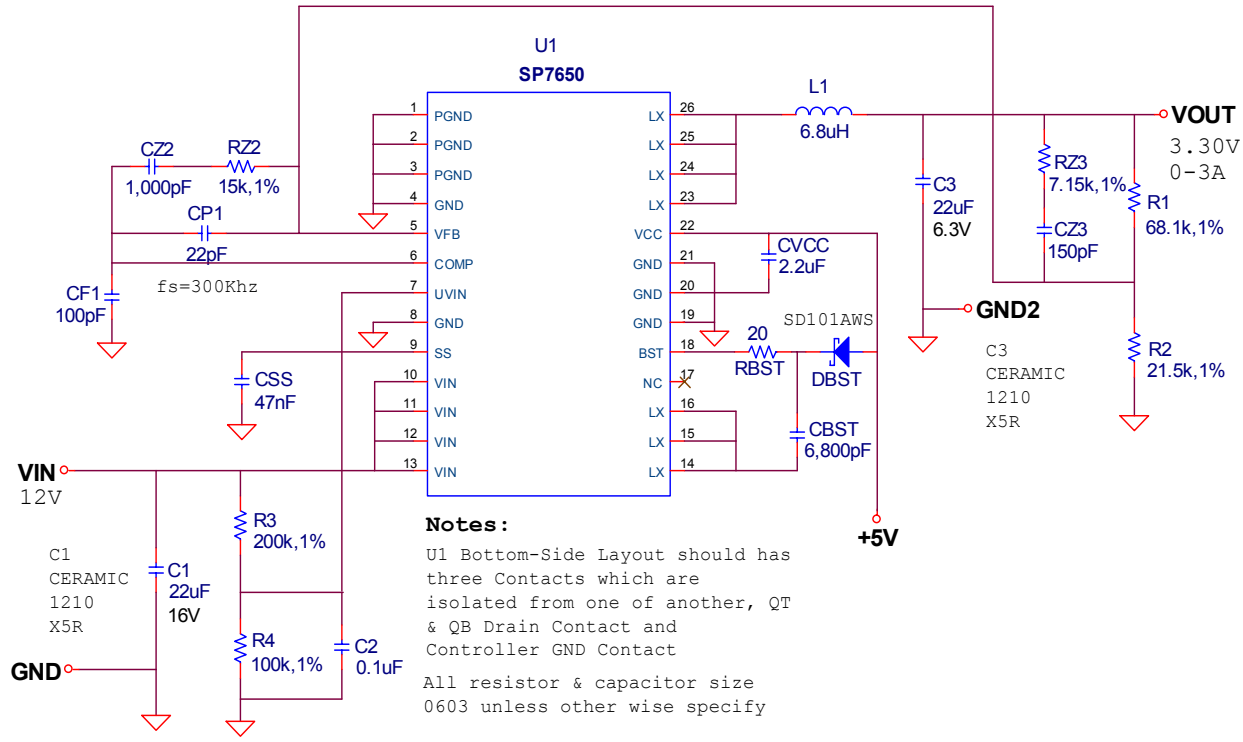


Figure 8. Output Load Short Circuit

+5V BIAS SUPPLY APPLICATION SCHEMATIC

In this application example, the SP7650ER is power by an external +5V bias supply which current consumption of 20mA Maximum. If this supply is not available than it is recommend Sipex SPX5205 Low-Noise LDO Voltage Regulator.



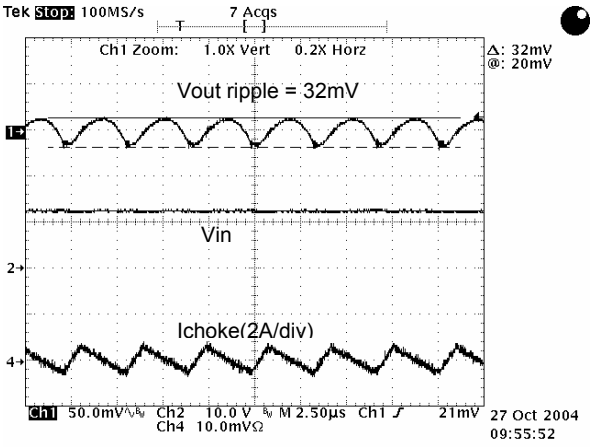


Figure 9. Output Ripple: No Load

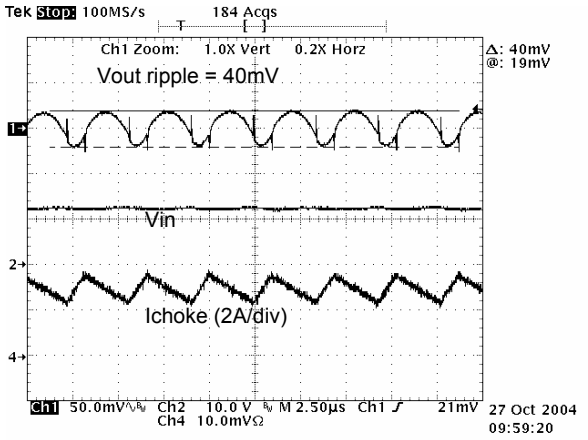


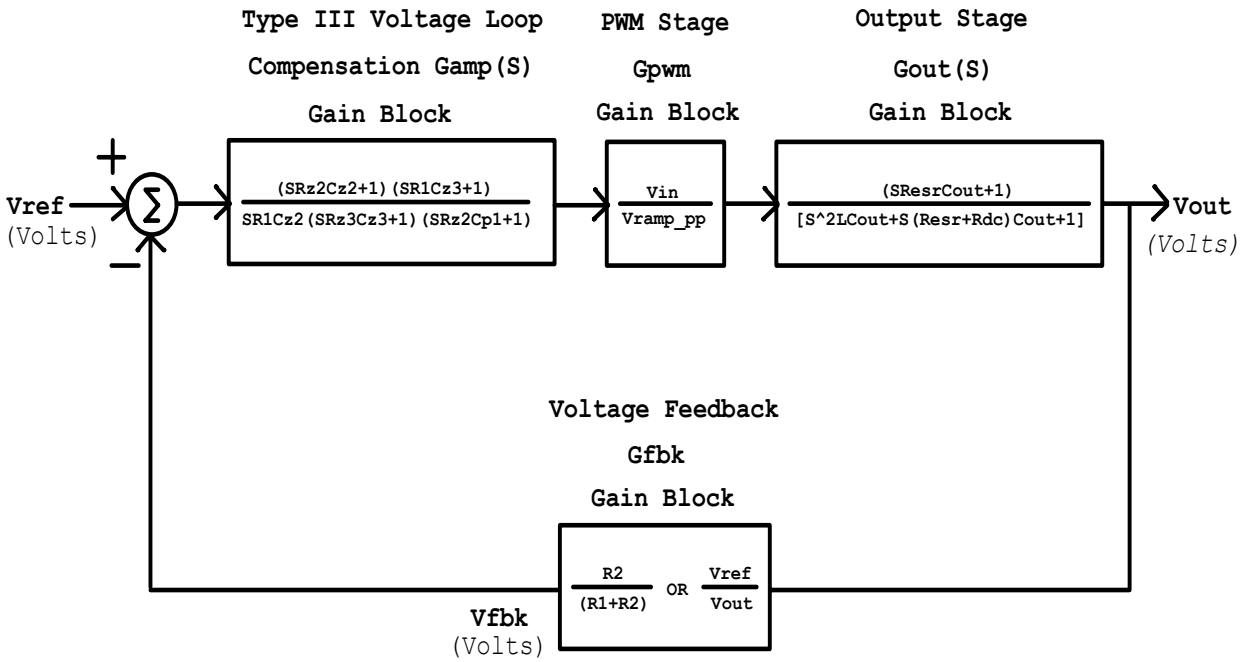
Figure 10. Output Ripple: 3A Load

Table 1: SP7650EB Suggested Components and Vendor Lists

INDUCTOR - SURFACE MOUNT							
Inductance (uH)	Manufacturer/Part No.	Inductor Specification				Inductor Type	Manufacturer Website
		Series R (mOhms)	Isat (A)	Size LxW(mm)	Ht.(mm)		
6.8	Vishay IHLP-2525CZ-01-6R8MTR	54	8	6.86x6.47	3.0	Shielded Ferrite Core	www.vishay.com
6.8	SD75-6R8M	46	3.06	7.0x7.8	5.0	Non-Shielded Ferrite Core	www.inter-technical.com
CAPACITOR-SURFACE-MOUNT							
Capacitance (uF)	Manufacturer/Part No.	Capacitor Specification				Capacitor Type	Manufacturer Website
		ESR (mOhms)	Ripple current (A) @ 45°C	Size / Voltage	(V)		
22	TDK C3225X5R1C226M	2	4	1210	16.0	X5R Ceramic	www.vishay.com
22	TDK C2012X5R0J226M	2	4	805	6.3	X5R Ceramic	www.inter-technical.com

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7650EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to crossover at the selecting frequency **fco**, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7650EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7650 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 11. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows:

a. Choose **fco** = fs / 10

b. Calculate **fp_LC**
fp_LC = 1 / 2π [(L) (C)] ^ 1/2

c. Calculate **fz_ESR**
fz_ESR = 1 / 2π (Resr) (Cout)

d. Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ

e. Calculate **R2** base on the desired Vout
R2 = R1 / [(Vout / 0.80V) – 1]

f. Select the ratio of **Rz2 / R1** gain for the desired gain bandwidth
Rz2 = R1 (Vramp_pp / Vin_max) (fco / fp_LC)

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
Cz2 = 1 / π (Rz2) (fp_LC)

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
Cp1 = 1 / 2π (Rz2) (fz_ESR)

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
Rz3 = 2 (R1) (fp_LC) / fs

j. Calculate **Cz3** from **Rz3** component value above
Cz3 = 1 / π (Rz3) (fs)

k. Choose 100pF ≤ **Cf1** ≤ 220pF to stabilize the SP7650ER internal Error Amplify

As a particular example, consider for the following SP7650EB with a **Type III** Voltage Loop Compensation component selections:

Vin = 5 to 15V
Vout = 3.30V @ 0 to 3A load
Select **L = 6.8uH** => yield ≈ 40% of maximum 3A output current ripple.
Select **Cout = 22uF Ceramic** capacitor (Resr ≈ **4mΩ**)
fs = 300khz SP7650 internal Oscillator Frequency
Vramp_pp = 1.0V SP7650 internal Ramp Peak to Peak Amplitude

<u>Step by step design procedures</u>:

a. **fco** = 300khz / 5 = 60khz

b. **fp_LC** = 1 / 2π [(6.8uH)(22uF)]^1/2 ≈ 15khz

c. **fz_ESR** = 1 / 2π (2mΩ)(22uF) ≈ 3.6Mhz

d. **R1** = 68.1kΩ, 1%

e. **R2** = 68.1kΩ / [(3.30V / 0.80V) – 1] ≅ 21.5kΩ, 1%

f. **Rz2** = 68.1kΩ (1.0V / 15V) (60khz / 15khz) ≈ 15kΩ, 1%

g. **Cz2** = 1 / π (18kΩ) (20khz) ≈ 1,000pF, X7R

h. **Cp1** = 1 / 2π (15kΩ) (3.6Mhz) ≈ 10pF => Select **Cp1** = 22pF for noise filtering

i. **Rz3** = 2 (68.1kΩ) (15khz) / 300khz ≈ 7.15kΩ, 1%

j. **Cz3** = 1 / π (7.15kΩ) (300khz) ≅ 100pF, COG

k. **Cf1** = 100pF to stabilize SP7650ER internal Error Amplify

+5V INPUT WITH A TYPE III COMPENSATION APPLICATION SCHEMATIC

Figure 12 shows another example of SP7650ER configures for +5V input by simply changing a few external resistors and capacitors components value for delivering a 0-3A output with excellent line and load regulation.

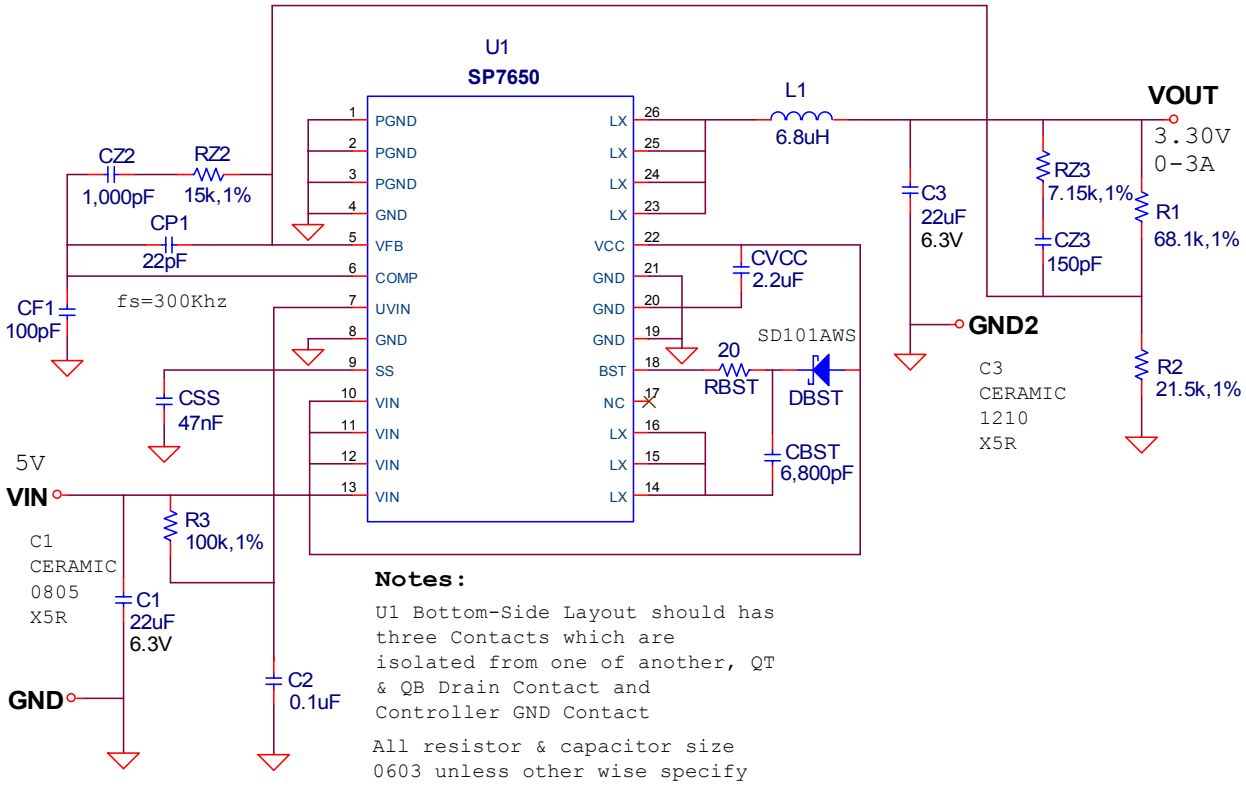


Figure 12. SP7650ER Configures for Vin = 5V, Vout = 3.3V at 0-3A Output Load Current

PC LAYOUT DRAWINGS

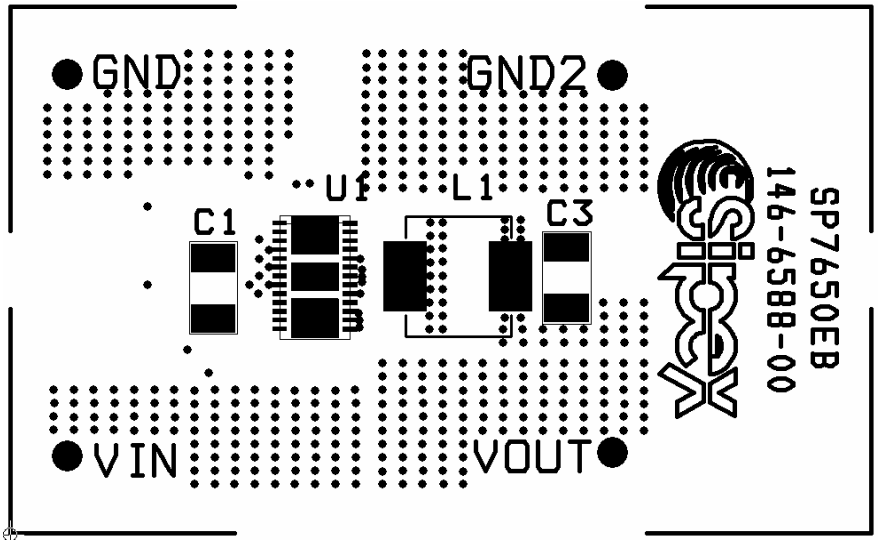


Figure 13. SP7650EB Component Placement

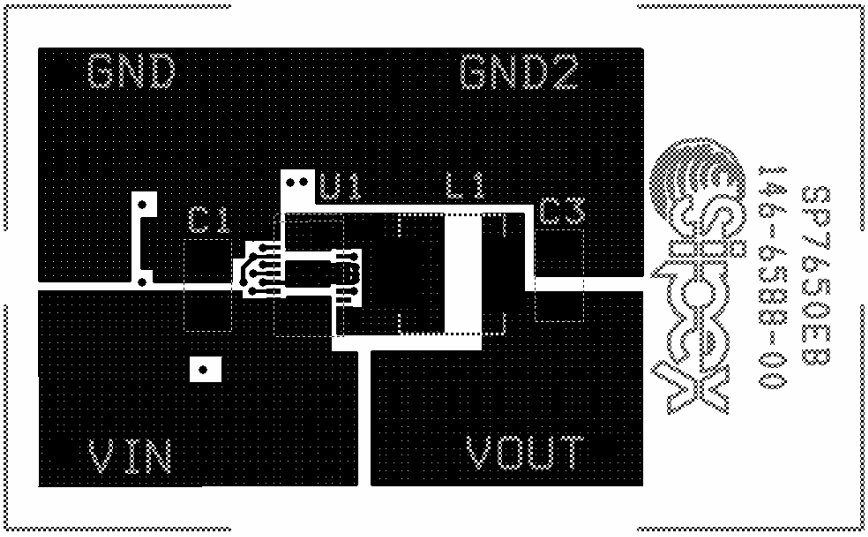


Figure 14. SP7650EB PC Layout Top Side

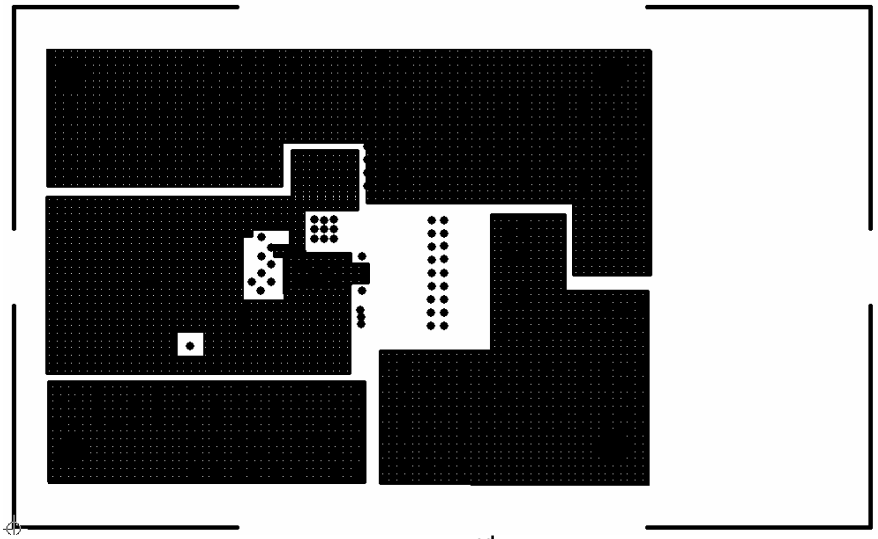


Figure 15. SP7650EB PC Layout 2nd Layer Side

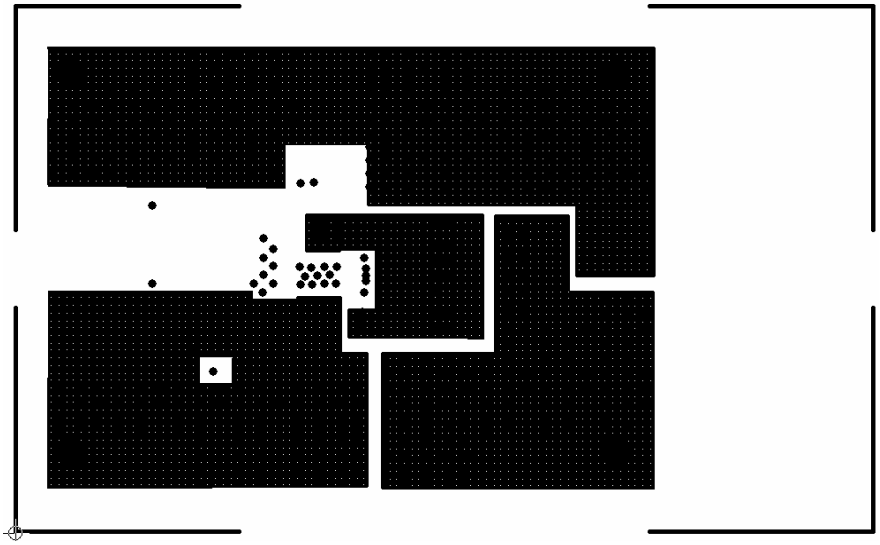


Figure 16. SP7650EB PC Layout 3rd Layer Side

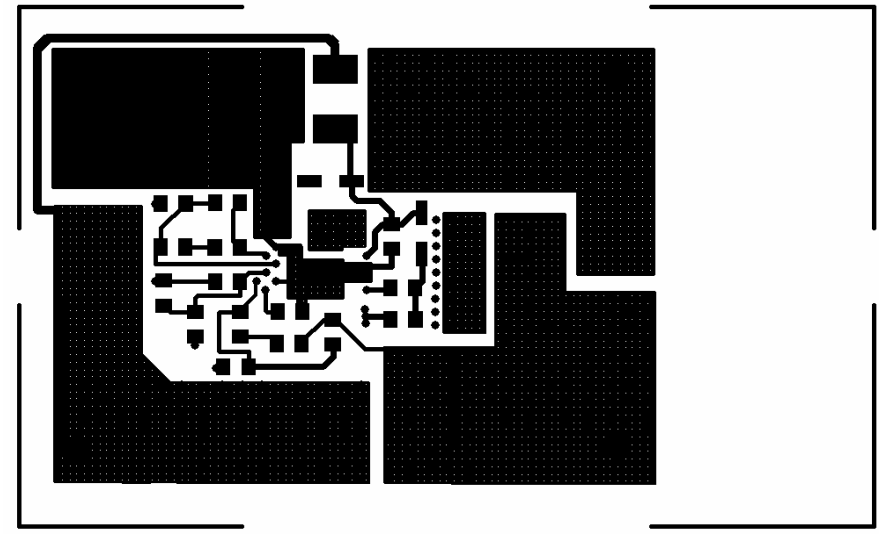


Figure 17. SP7650EB PC Layout Bottom Side

Table 2: SP7650EB List of Materials

			SP7650 Vin=12V Evaluation Board Rev. 00 List of Materials			10/2004
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
1	PCB	1	Sipex	146-6588-00	1.75"X2.75"	SP7650EB	978-667- 8700
2	U1	1	Sipex	SP7650ER	DFN-26	2-FETs Buck Ctrl	978-667- 8700
3	D1	1	Vishay Semi	BZX384B5V6S	SOD-323	5.6V, 200mW Zener	402-563-6866
4	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA Schottky Diode	402-563-6866
5	L1	1	VishayDale	IHLP-2525CZ-01-6R8MTR	6.86X6.47mm	6.8uH Coil 8A 54mohm	402-563-6866
		or	Inter-Technical	SD75-6R8M	7.0X7.8mm	6.8uH Coil 3.06A 46mohm	914-347-2474
6	C3	1	TDK	C3225X5R0J226M	1210	22uF Ceramic X5R 6.3V	978-779-3111
7	C1	1	TDK	C3225X5R1C226M	1210	22uF Ceramic X5R 16V	978-779-3111
8	CVCC	1	TDK	C1608X5R1A225K	0603	2.2uF Ceramic X5R 10V	978-779-3111
9	C2	1	TDK	C1608X7R1H104K	0603	0.1uF Ceramic X7R 50V	978-779-3111
10	CBST	1	AVX	06035C682KAT2A	0603	6,800pF Ceramic X7R 50V	843-448-9411
11	CSS	1	AVX	06035C473KAT2A	0603	47,000pF Ceramic X7R 50V	843-448-9411
12	CP1	1	AVX	06035A220JAT2A	0603	22pF Ceramic COG 50V	843-448-9411
13	CZ2	1	AVX	06035A102JAT2A	0603	1,000pF Ceramic COG 50V	843-448-9411
14	CZ3	1	AVX	06035A151JAT2A	0603	150pF Ceramic COG 50V	843-448-9411
15	CF1	1	AVX	06035A101JAT2A	0603	100pF Ceramic COG 50V	843-448-9411
16	RZ2	1	Dale	CRCW0603-1502FRT1	0603	15.0K Ohm Thick Film Res 1%	402-563-6866
17	R2	1	Dale	CRCW0603-2152FRT1	0603	21.5K Ohm Thick Film Res 1%	402-563-6866
18	RZ3	1	Dale	CRCW0603-7152FRT1	0603	7.15K Ohm Thick Film Res 1%	402-563-6866
19	R1	1	Dale	CRCW0603-6813FRT1	0603	68.1K Ohm Thick Film Res 1%	402-563-6866
20	R3	1	Dale	CRCW0603-2003FRT1	0603	200K Ohm Thick Film Res 1%	402-563-6866
21	R4	1	Dale	CRCW0603-1003FRT1	0603	100K Ohm Thick Film Res 1%	402-563-6866
22	RBST	1	Dale	CRCW0603-20RFT1	0603	20 Ohm Thick Film Res 1%	402-563-6866
23	R6	1	Dale	CRCW1210-464RFT1	0603	464 Ohm Thick Film Res 5%	402-563-6866
24	VIN, VOUT, GND, GND2	4	Vector Electronic	K24C/M	.042 Dia	Input/Output Terminal Posts	800-344-4539

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7650EB	-40°C to +85°C	SP7650 Evaluation Board
SP7650ER	-40°C to +85°C	26-pin DFN

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

MaxLinear:
SP7650EB