RICHTEK®

RT9426A

System-Side Single-Cell Fuel Gauge

1 General Description

The RT9426A Li-Ion/Li-Polymer battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell battery packs. The RT9426A resides within the battery pack or on the system's main board and manages a non-removable battery or removable battery pack.

The RT9426A uses the Voltaic Gauge with Current Sensing (VGCS) algorithm to report State of Charge (SOC), State of Health (SOH), Full Charge Capacity (FCC), Time to Empty (TTE), and Cycle Count. It calculates the increasing or decreasing state of charge based on the voltage difference between the battery voltage and Open Circuit Voltage (OCV), and employs current sensing compensation to report battery SOC.

The Voltaic Gauge with Current Sensing algorithm can support smooth SOC tracking and does not accumulate error over time and with current changes. That is an advantage compared to Coulomb counter which suffers from SOC drift caused by current sense errors and battery self-discharge.

The RT9426A provides a complete battery status monitor with an interrupt alarm function. It can actively alert the host processor when conditions of battery overvoltage, undervoltage, or over-temperature conditions during charging or discharging. This is especially useful for high C-rate battery charging applications, as it can measure battery voltage using a Kelvin sense connection to eliminate the IR drop effect for an optimal charging profile and safety. Additional useful alarm functions include under SOC alert, SOC change, and battery presence status change.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Features

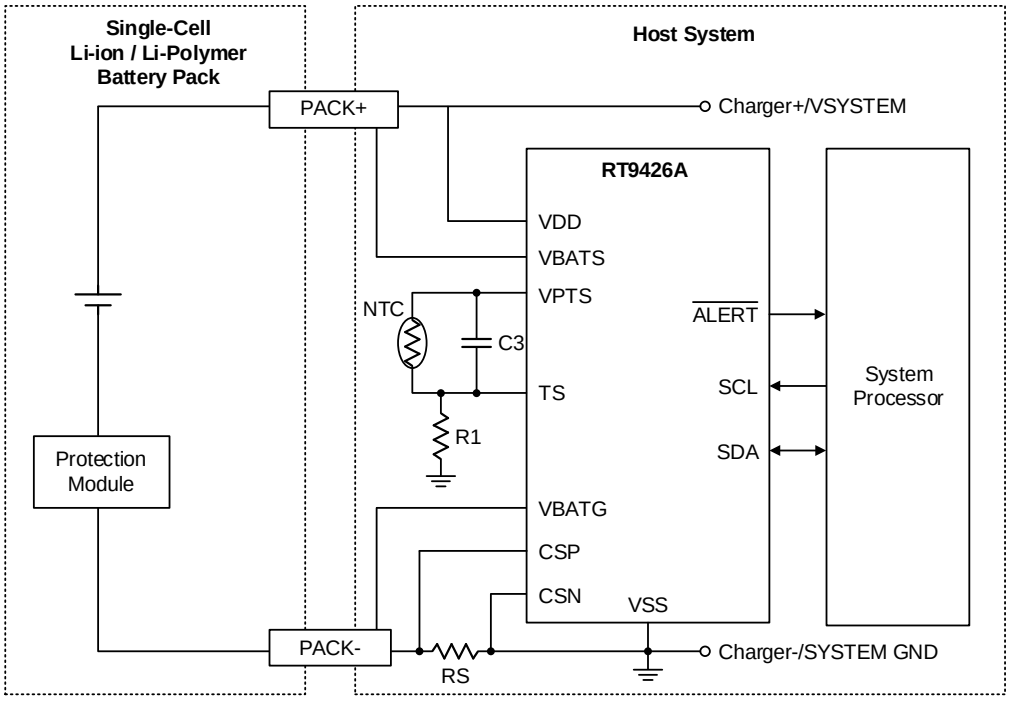
- **Support System-Side Fuel Gauging**
- **Battery Fuel Gauge for 1-Series (1sXp) Li-Ion/Li-Polymer Applications**
- **State of Charge Calculation Using VoltaicGauge™ with Current Sensing (VGCS)**
- **Accurate Capacity Calculation with No Accumulation Error**
- **Report Battery SOC, SOH, FCC, TTE, and Cycle Count**
- **Voltage Measurement: ±7.5mV**
- **Current Measurement: ±1%**
- **Battery Temperature Measurement: ±3°C**
- **Battery Monitoring with Alert Indicators for Voltage, Current, Temperature, SOC, and Presence**
- **High C-Rate Battery Charging Compliance**
- **Low Power Consumption**
- **Support Low-Value Sense Resistor (1mΩ to 40mΩ, Typical 10mΩ)**
- **12-Pin WDFN Package with 0.4mm Pitch**
- **9-Bump WL-CSP Package with 0.5mm Pitch**
- **I^2C Communication Interface**

3 Applications

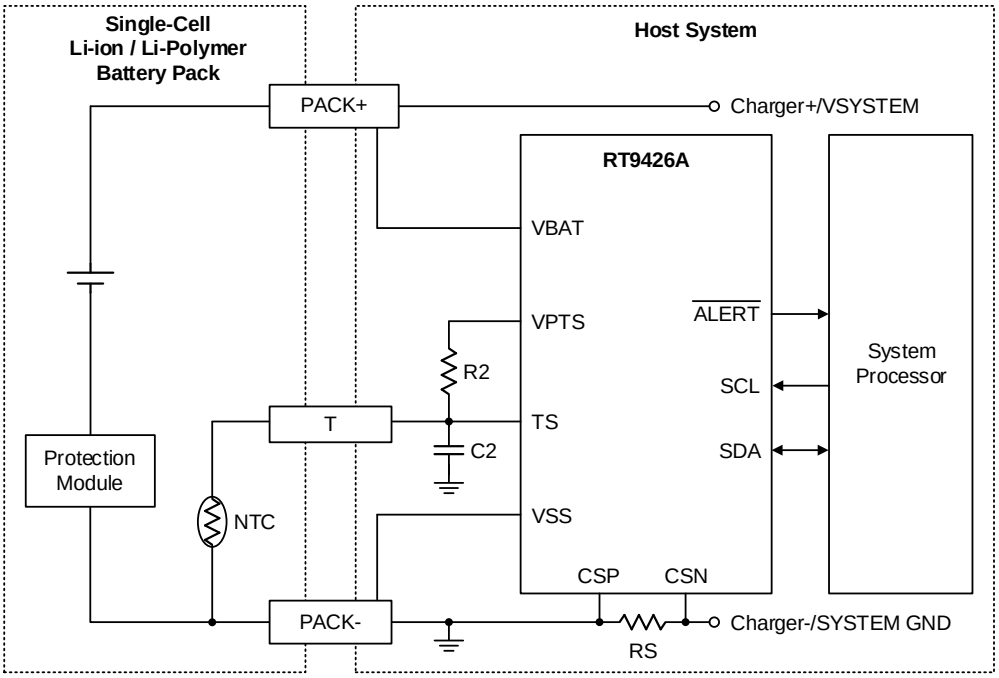
- Smartphones
- Tablet PCs
- Wearable Devices
- Digital Still Cameras
- Digital Video Cameras
- Handheld and Portable Applications

4 Simplified Application Circuit

4.1 WDFN-12L 2.5x4



4.2 WL-CSP-9B 2.29x1.74 (BSC)



5 Ordering Information

RT9426A □□

Package Type(1)
QW: WDFN-12L 2.5x4 (W-Type)
WSC: WL-CSP-9B 2.29x1.74 (BSC)

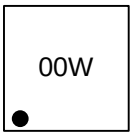
Lead Plating System
G: Richtek Green Policy Compliant(2)
(For WDFN-12L 2.5x4 Only)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

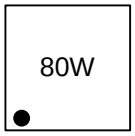
6 Marking Information

RT9426AGQW



00 : Product Code
W : Date Code

RT9426AWSC



80 : Product Code
W : Date Code

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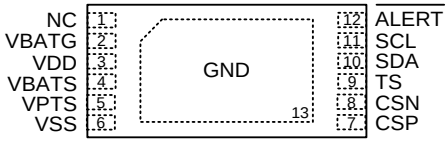
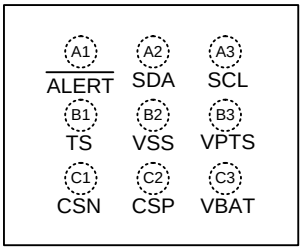
7 Pin Configuration

(TOP VIEW)



WDFN-12L 2.5x4

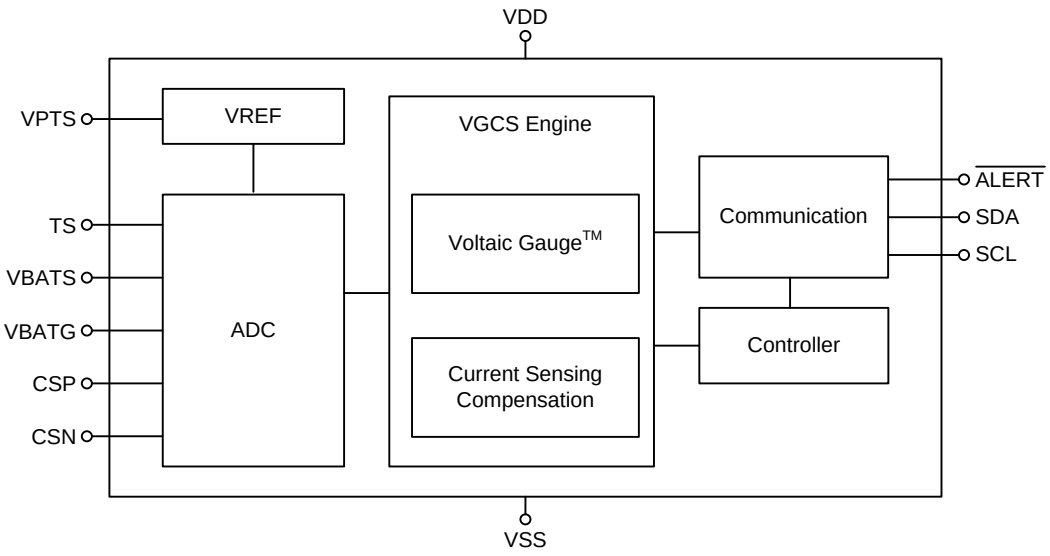


WL-CSP-9B 2.29x1.74 (BSC)

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-12L 2.5x4	WL-CSP-9B 2.29x1.74 (BSC)		
1	--	NC	No connection. Please keep it floating.
2	--	VBATG	Battery voltage sensing negative input. Connect to the battery connector with Kelvin Sense connections.
3	C3	VDD/VBAT	Power supply input and battery voltage sensing input for WL-CSP package.
4	--	VBATS	Battery voltage sensing positive input. Connect to the battery connector with Kelvin Sense connections.
5	B3	VPTS	Power reference output pin for temperature measurement.
6	B2	VSS	Device ground.
7	C2	CSP	Battery current sensing positive input. Connect a 10mΩ sense resistor with Kelvin Sense connections.
8	C1	CSN	Battery current sensing negative input. Connect a 10mΩ sense resistor with Kelvin Sense connections.
9	B1	TS	Temperature measurement input.
10	A2	SDA	Serial data input. Slave I^2C serial communications data line for communication with system. Open-drain I/O.
11	A3	SCL	Serial cock input. Slave I^2C serial communications clock line for communication with system. Open-drain I/O.
12	A1	$\overline{\text{ALERT}}$	Alert open-drain indicator output.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Voltage on CSN Pin to CSP ---------- –0.3V to 2V
- Voltage on VBATS, VBATG, VPTS, TS to VSS ---------- –0.3V to (V_{DD} + 0.3V)
- Voltage on VDD Pin Relative to VSS ---------- –0.3V to 6V
- Voltage on All Other Pins Relative to VSS ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-12L 2.5x4 ---------- 3.25W

  WL-CSP-9B 2.29x1.74 (BSC) ---------- 1.65W
- Package Thermal Resistance (Note 3)

  WDFN-12L 2.5x4, θ_{JA} ---------- 30.7°C/W

  WDFN-12L 2.5x4, θ_{JC} ---------- 4°C/W

  WL-CSP-9B 2.29x1.74 (BSC), θ_{JA} ---------- 60.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and the functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VDD ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(2.5V ≤ V_{DD} ≤ 5.5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage	V_{DD}	VDD – VSS	2.5	--	5.5	V
Active Current	I_{ACTIVE}	Active mode, VDD = 3.8V, BD_PRES_EN = 0 and not including external temperature measurement current.	--	14	20	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sleep Current	I_{SLP}	Sleep mode, VDD = 3.8V, BD_PRES_EN = 0 and not including external temperature measurement current.	--	5	7	μA
Shutdown Current	I_{SHDN}	VDD = 3.8V	--	0.5	1	μA
Voltage Measurement Range	V_{VOLT_RNG}		2.5	--	VDD	V
Voltage Measurement Error	V_{ERR}	VBATS = 4V, VBATG = 0V	–7.5	--	7.5	mV
Current Measurement Range	V_{CURR_RNG}	$V_{CSP} – V_{CSN}$	–125	--	125	mV
Current Measurement Gain Error	I_{GERR}	$\|V_{CSP} – V_{CSN}\|$ = 20mV	–1	--	1	%
Current Measurement Offset Error	I_{OERR}	$\|V_{CSP} – V_{CSN}\|$ = 0V (Note 6)	–10	±5	10	μV
Temperature Measurement Error	$ExtT_{GERR}$	T_A = 25°C (Note 7)	–3	--	3	°C
Internal Temperature Measurement Range	T_{INTT_RNG}	(Note 8)	–40	--	85	°C
Internal Temperature Measurement Error	$IntT_{GERR}$	T_A = 25°C	--	±3	--	°C
Input Impedance: VBATS, VBATG, TS	Z_{IN_VBATS} Z_{IN_VBATG} Z_{IN_TS}		15	--	--	MΩ
Input Impedance: CSN, CSP	Z_{IN_CSP} Z_{IN_CSN}		1	--	--	MΩ
Battery Presence Detect Threshold	V_{BD_TH}		0.91x VDD	0.94x VDD	0.97x VDD	V
Battery Presence Detect Pull-High Resistor	R_{BD_PH}		--	150	--	kΩ
Battery Insertion Detection Time	t_{BID}		--	--	25	ms
Battery Removal Detection Time	t_{BRD}		--	--	1.1	ms
VPTS Output Drive	V_{VPTS}	I_{OUT} = 0.5mA	1.146	1.2	1.254	V
Input Logic-High: SCL, SDA, $\overline{ALERT}$	V_{IH}	Reference to VSS	1.4	--	--	V
Input Logic-Low: SCL, SDA, $\overline{ALERT}$	V_{IL}	Reference to VSS	--	--	0.5	V
Output Logic-Low: SDA, $\overline{ALERT}$	V_{OL}	I_{OL} = 3mA (Reference to VSS)	--	--	0.4	V
Pull-Down Current: SCL, SDA, $\overline{ALERT}$	I_{PDN}	VDD = 4.5V, $V_{SCL, SDA, \overline{ALERT}}$ = 0.4V	0.05	0.2	0.4	μA

Note 6. The typical result is a long-term average.

Note 7. The thermistor utilizes a 10k NTC with a beta value of 3435k. The default model is SEMITEC 103KT1608T.

Note 8. Specifications are 100% tested at T_A = 25°C. Limits over the operating range are guaranteed by design and characterization.

13 Electrical Characteristics: I²C Interface

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Operating Frequency	f_{SCL}	(Note 9)	10	--	400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	µs
Hold Time After START Condition	$t_{HD:STA}$	(Note 9)	0.6	--	--	µs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	µs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD;DAT}$	(Note 10)	0	--	0.9	µs
Data Setup Time	$t_{SU;DAT}$	(Note 10)	100	--	--	ns
Clock Data Rise Time	t_R		20	--	300	ns
Clock Data Fall Time	t_F		20	--	300	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 11)	0	--	50	ns
Capacitive Load for Each Bus Line	C_B	(Note 12)	--	--	400	pF
SCL, SDA Input Capacitance	C_{BIN}		--	--	60	pF

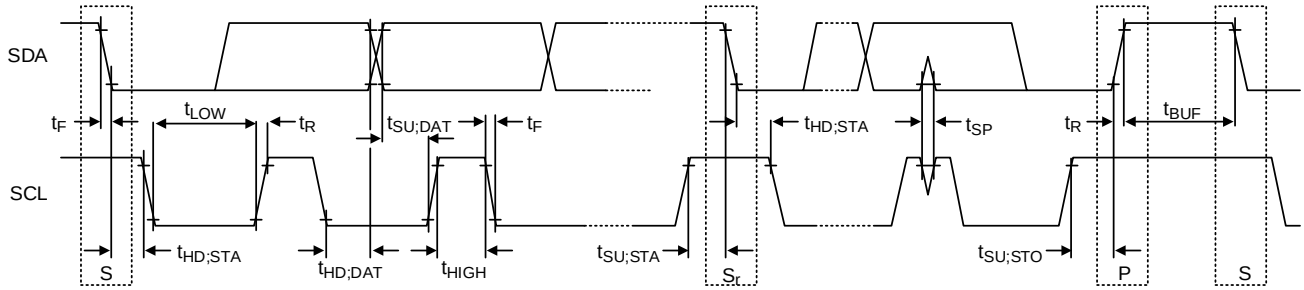
Note 9. f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 10. The maximum $t_{HD;DAT}$ must only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 11. Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 12. C_B represents the total capacitance of one bus line, measured in pF.

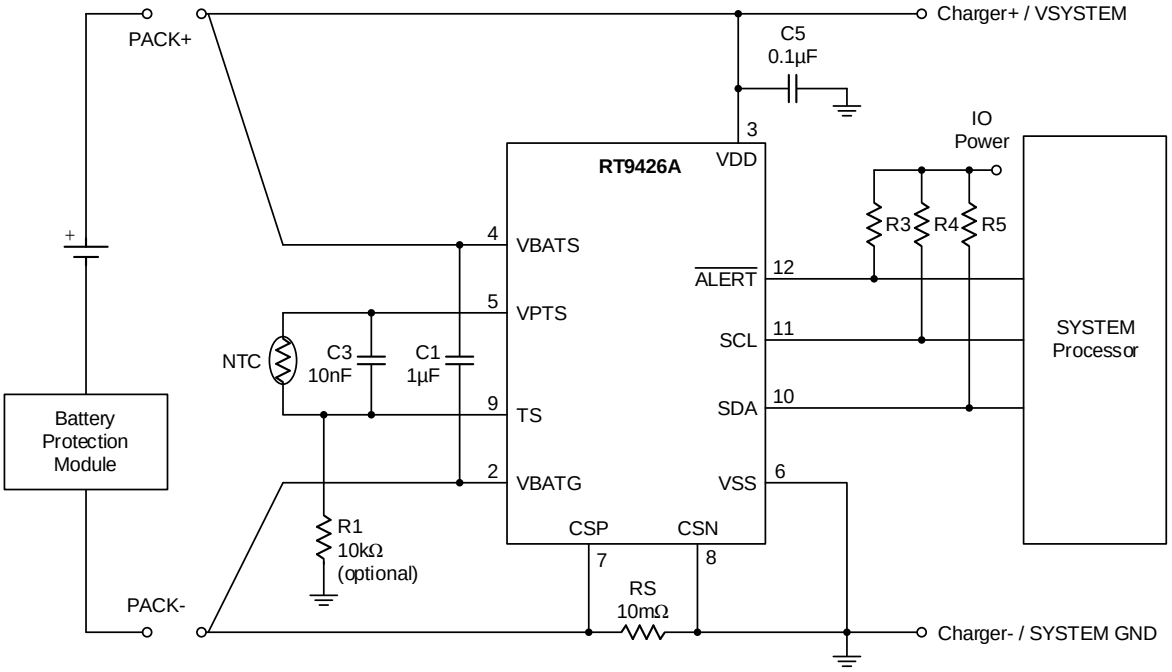
14 I²C Timing Diagram



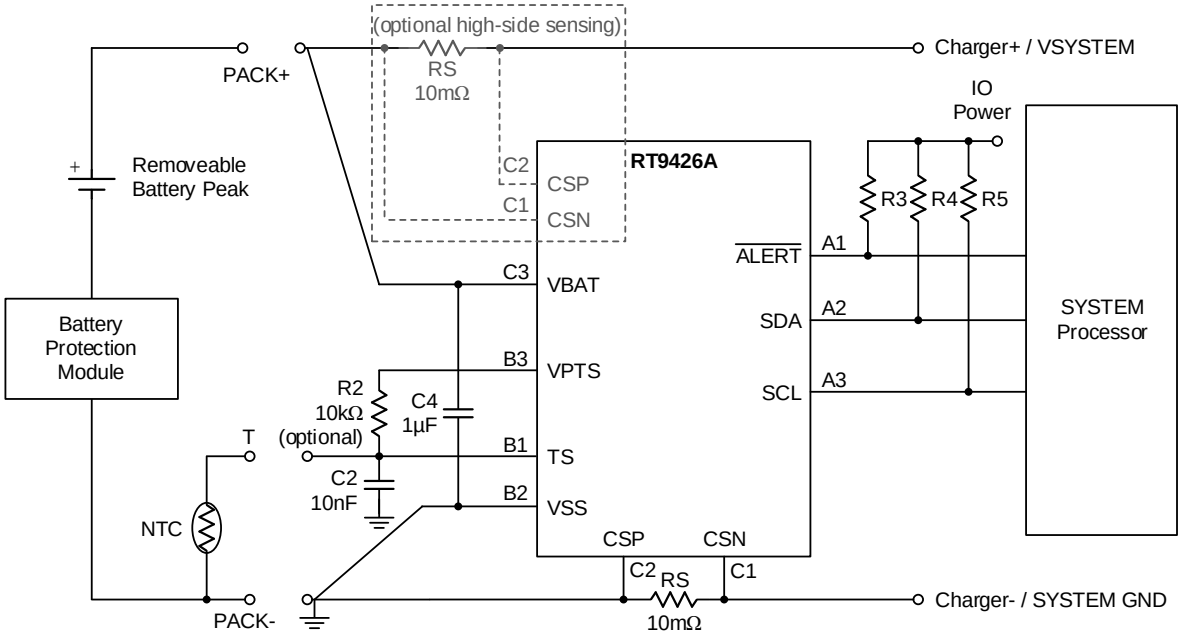
15 Typical Application Circuit

Both WL-CSP and WDFN options can have a high/low-side NTC.

15.1 WDFN-12L 2.5x4

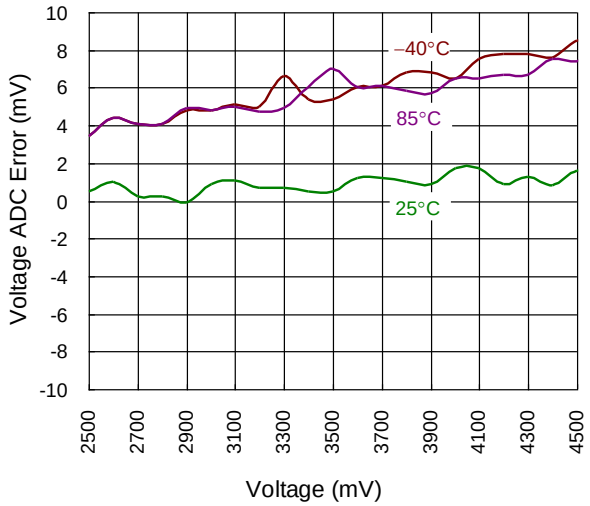


15.2 WL-CSP-9B 2.29x1.74 (BSC)

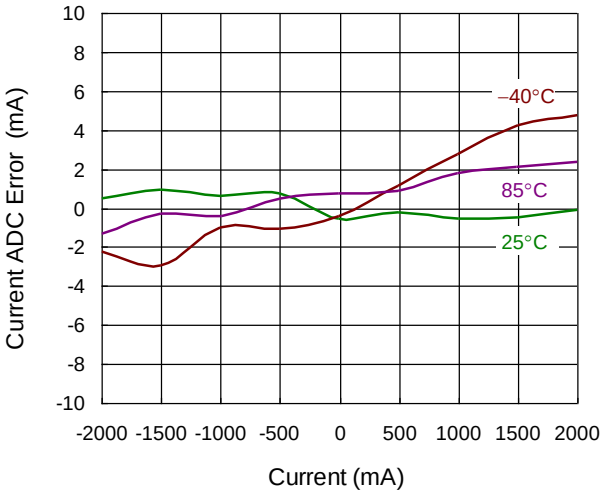


16 Typical Operating Characteristics

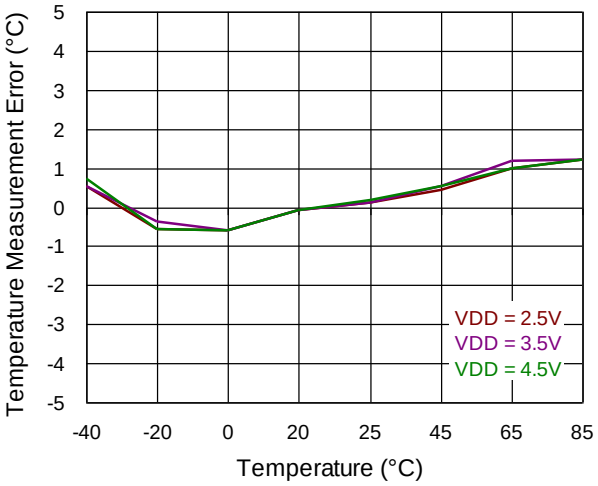
Voltage ADC Error vs. Temperature



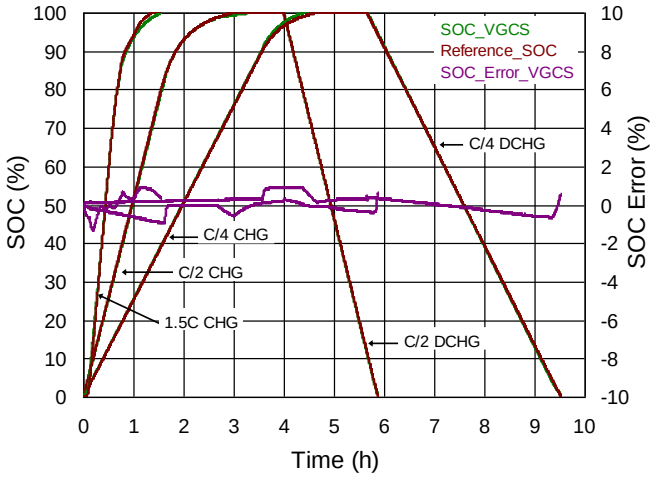
Current ADC Error vs. Temperature



Temperature Measurement Error vs. Temperature



SOC Accuracy*



*: SOC accuracy requires applying custom parameters into the IC.

17 Application Information

(Note 13)

17.1 ADC for Voltage, Current, and Temperature

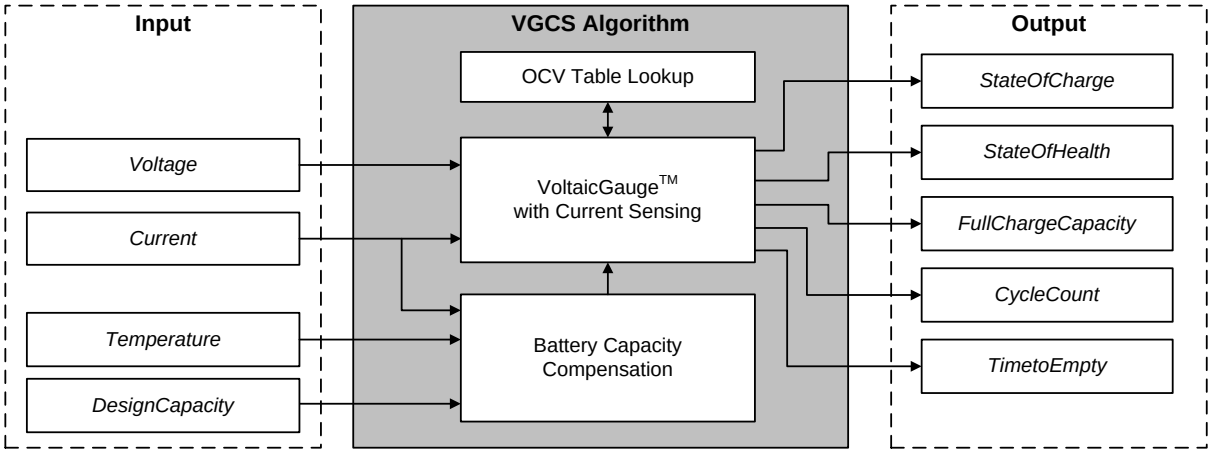
Battery voltage is measured at the VBATS pin input with respect to VBATG over a range of 2.5 to 5.5V with a resolution of 1mV. The ADC calculates the first cell voltage for a period of 250ms after the IC's Power-On Reset (POR) and then for a period of 1s for every subsequent cycle. The voltage register requires 1s to update after exiting sleep mode. The result is placed in the *Voltage* register at the end of each conversion period.

The RT9426A Fuel Gauge measures the battery current during charging and discharging and reports the values to the *Current* register. The measurement range is 10A (when RS = 10mΩ), and the resolution is 1mA.

The RT9426A reports the temperature to the *Temperature* register by measuring either the battery temperature or the chip temperature. When measuring the battery temperature, an external NTC resistor is used.

17.2 VoltaicGauge™ with Current Sensing (VGCS) Algorithm

The VGCS algorithm is based on the battery voltage and the dynamic difference between the battery voltage and battery current measurements. It iterates battery voltage information and compensates with current information to increase or decrease the delta State of Charge (SOC), which is then integrated into the SOC. The figure below illustrates the VGCS functional block.



The RT9426A obtains battery voltage information, and then uses an OCV table along with iterative calculations that include current correction to calculate the delta SOC. It references the design capacity and actual battery capacity as references to optimize the result and outputs the final SOC. Additionally, VGCS also supports high C-RATE charging technology.

Coulomb counter-based fuel gauges are subject to SOC drift, which can be attributed to errors in current sensing and the natural self-discharge of cells. Over time, even minimal errors in current sensing can result in significant drift due to cumulative error.

The VGCS system, however, employs a voltage-based iterative algorithm that ensures consistent SOC readings.

It incorporates current data primarily to enhance the accuracy of transient responses. As a result, VGCS avoids the issue of error accumulation and the resultant SOC drift commonly associated with traditional coulomb counters.

17.3 Design Capacity

The *DesignCapacity* register should be set to the correct value after the IC's Power-On Reset (POR). The Design Capacity represents the cell's expected capacity at the time of manufacture and should remain unchanged while the VGCS is active. It serves as a reference input for the VGCS algorithm. The resolution of the design capacity is 1mAh, with a default value of 0x07D0 (2000mAh), which corresponds to 2000mAh.

17.4 SOC Report

The *StateOfCharge* register is a read-only register that displays the cell's state of charge as calculated by the VGCS algorithm. The result is expressed as a percentage of the cell's full capacity. This register automatically adjusts to changes in battery size, as the fuel gauge naturally accounts for relative SOC. The SOC is measured in percent (%). The reported SOC also includes residual capacity, which may not be accessible to the actual application due to the requirements for early termination voltage. When the SOC reads 0%, it typically indicates that there is no remaining capacity for standard applications. The register is first updated 250ms after the IC's Power-On Reset (POR).

17.5 Power Mode

The RT9426A features three power modes, each tailored for various applications with differing power consumption requirements. These modes include active mode, sleep mode, and shutdown mode.

17.6 Active Mode

Active mode is recommended and is the default power mode after a Power-On Reset (POR). In active mode, the *Voltage*, *Current*, *Temperature*, *AverageVoltage*, *AverageCurrent,* and *AverageTemperature* registers are updated every second.

17.7 Sleep Mode

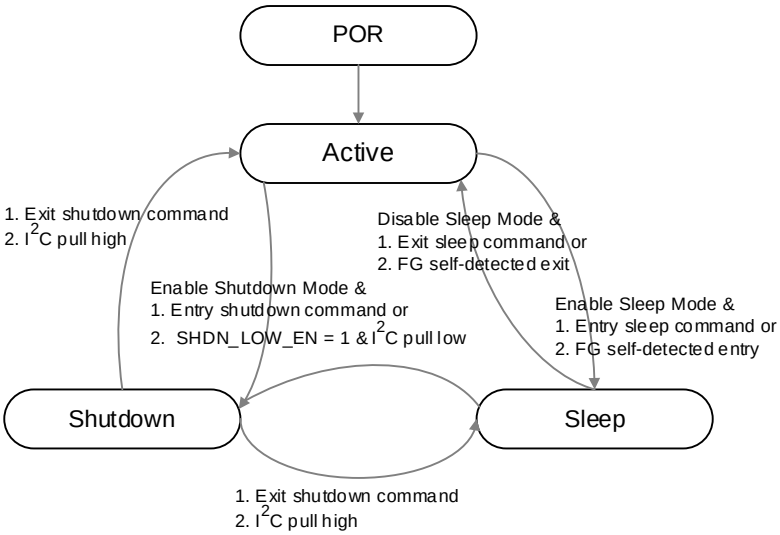
Sleep mode operates similarly to active mode but with a longer measurement period. The period is programmable in the sleep mode, with the minimum being twice that of active mode and the maximum being sixteen times longer. The default period is four times that of active mode. Sleep mode can be entered or exited by sending specific commands or through the fuel gauge's self-detection feature.

17.8 Shutdown Mode

In shutdown mode, the RT9426A stops all measurement activities and does not update registers, thereby maintaining minimum power consumption. To enter shutdown mode, the function must first be enabled. It can then be activated either by sending a command or by pulling the I^2C bus low.

To exit shutdown mode, an exit shutdown command must be received if the mode was entered via command. Alternatively, if shutdown mode was initiated by pulling the I^2C bus low, the I^2C bus must be pulled high to exit the mode.

17.9 Power Mode Switching



*: Exit shutdown or sleep mode method must be follow as entry method last time. For example: To enter sleep mode by command, it must also use command to exit sleep mode.

17.10 Controller

The controller manages the control flow of system routines, ADC measurement processes, algorithm calculations, and alert determinations.

17.11 Power-Up Sequence

When the RT9426A is powered on, the fuel gauge measures the battery voltage and estimates the initial state of charge (SOC) based on that voltage over a period of 250ms. The initial SOC estimation will be accurate if the battery has been at rest for more than 30 minutes. If not, there may be an initial SOC discrepancy. However, this discrepancy will diminish over time as the SOC adjusts gradually and eventually aligns with the open circuit voltage (OCV) when the battery is at rest.

17.12 Quick Sensing

A Quick Sensing operation enables the RT9426A to resume battery voltage sensing and state of charge calculation promptly. This operation is used to minimize the initial state of charge error that may result from an improper power-on sequence. A quick sensing operation can be initiated by sending the I^2C quick sensing command (0x4000) to the *Control* register.

17.13 Alert Function

The RT9426A supports various alerts to inform the system of abnormal conditions, such as over-temperature or undervoltage. These alerts include Over-Temperature in Charge (OTC), Over-Temperature in Discharge (OTD), Overvoltage (OV), Undervoltage (UV), Under-State of Charge (US), and State of Charge Change (SC), Overcurrent in Charge (OCC), Overcurrent in Discharge (ODC) and Temperature Change (TC) alerts.

The host can periodically poll the ALERT flag to monitor the system status or configure it to receive an interrupt notification from the RT9426A $\overline{\text{ALERT}}$ pin. The alert must be enabled to function properly. There are two methods to enable the alert: one involves enabling a specific bit operation, and the other requires setting an appropriate value for the detection threshold. For detailed information, please refer to the diagram and the descriptions below.

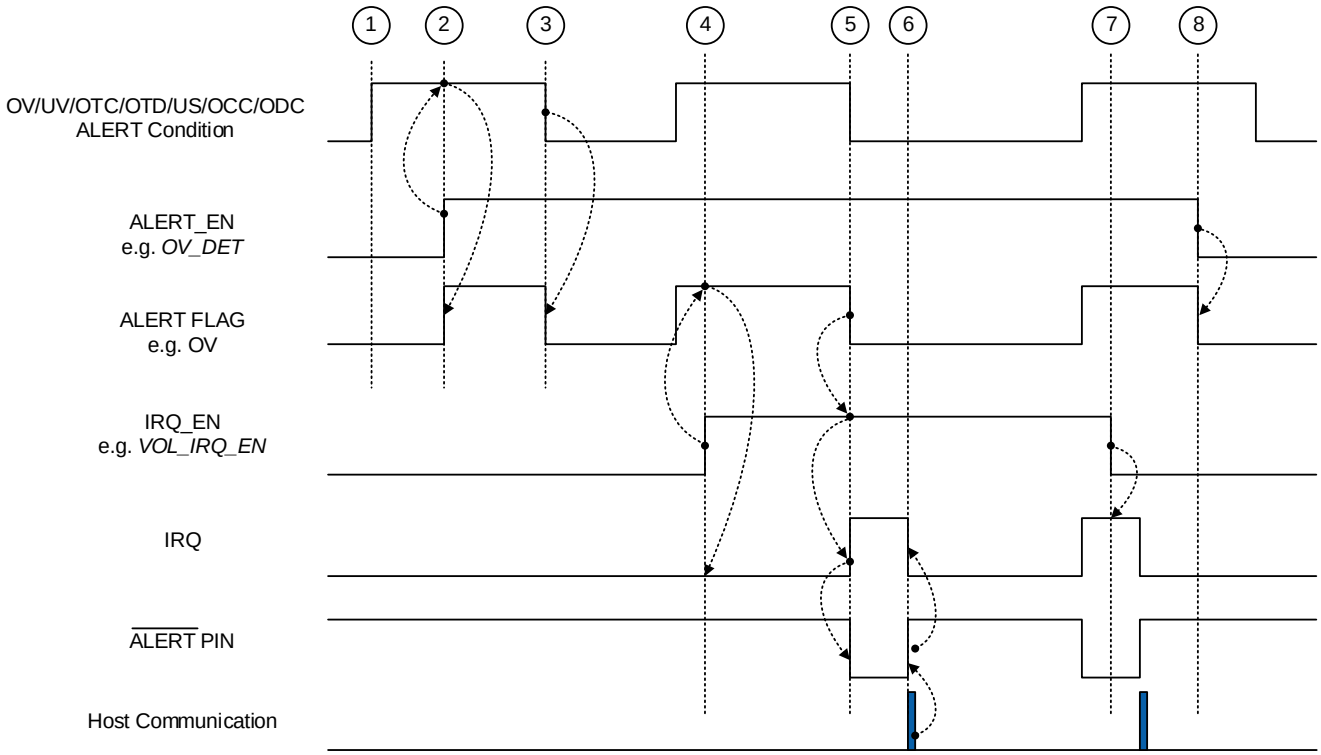


Figure 1. ALERT Function Timing Diagram

1. When an ALERT occurs but ALERT_EN is disabled, the ALERT FLAG will not generate a response.
2. When an ALERT_EN is enabled, the ALERT FLAG is set when an ALERT condition occurs.
3. The ALERT FLAG is cleared when the ALERT condition is recovered.
4. When the ALERT FLAG is already set and IRQ_EN is also set, the IRQ and $\overline{\text{ALERT}}$ PIN outputs will not generate a response.
5. The IRQ is set, and the $\overline{\text{ALERT}}$ PIN outputs low only when the IRQ_EN is set, and the ALERT FLAG state changes.
6. The IRQ and the $\overline{\text{ALERT}}$ PIN are read-only and will be cleared upon a read action by the driver.
7. Clearing the IRQ_EN has no effect on the the IRQ and the $\overline{\text{ALERT}}$ PIN outputs.
8. Disabling the ALERT_EN will also clear the ALERT FLAG.

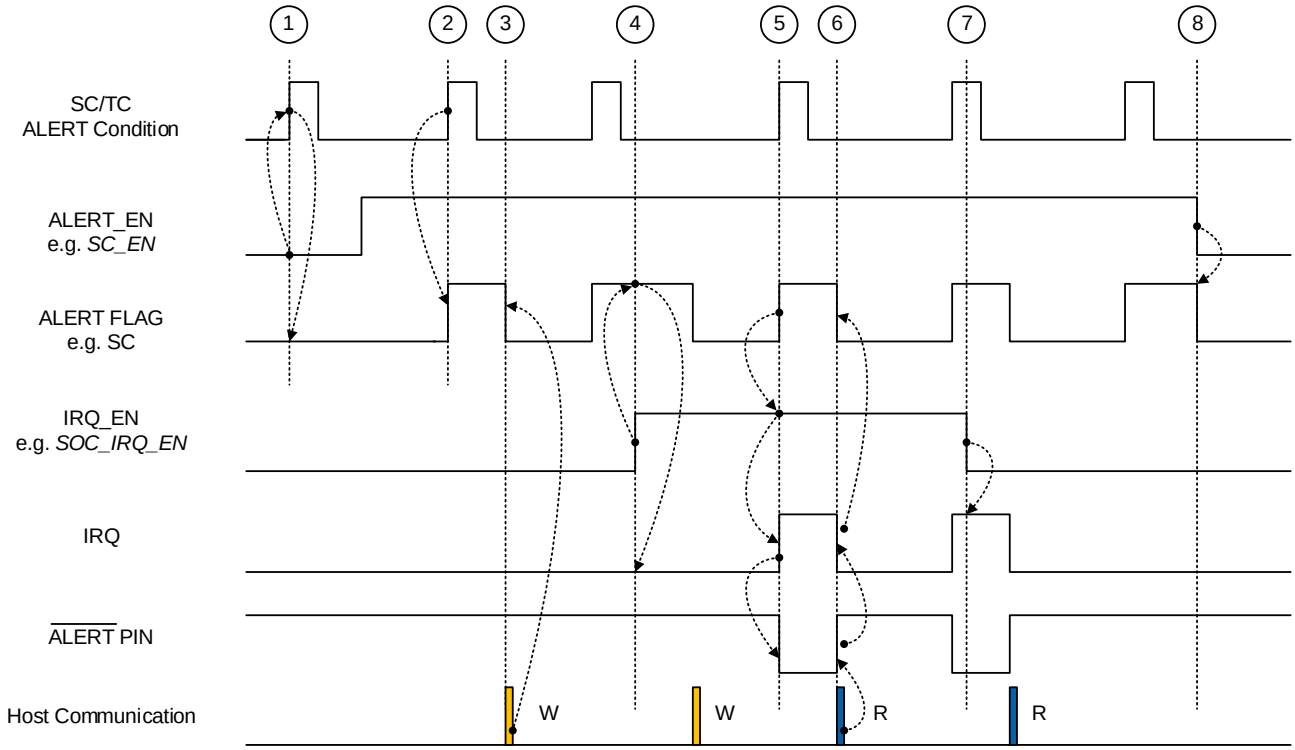
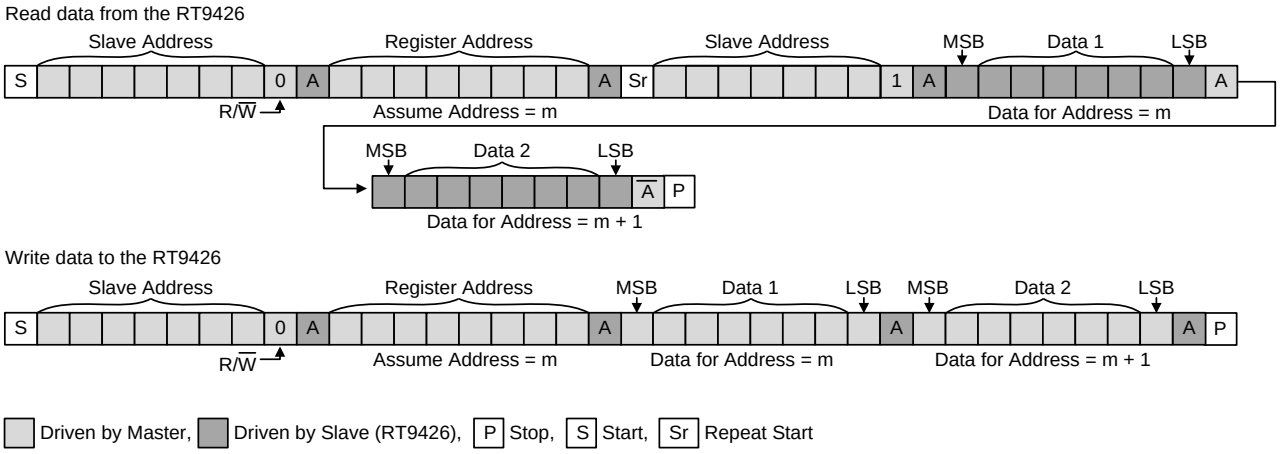


Figure 2. SC ALERT Function Timing Diagram

1. When an ALERT condition occurs but the ALERT_EN is disabled, the ALERT FLAG will not generate a response.
2. When the ALERT_EN is enabled, the ALERT FLAG is set when an ALERT condition occurs.
3. The ALERT FLAG is cleared when the driver writes ALERT_FLAG to 0.
4. When the ALERT_FLAG is already set and IRQ_EN is also set, the IRQ and the $\overline{\text{ALERT}}$ PIN outputs will not generate a response.
5. The IRQ is set and the $\overline{\text{ALERT}}$ PIN outputs low only when the IRQ_EN is set, and the ALERT FLAG state changes.
6. The IRQ and the $\overline{\text{ALERT}}$ PIN are read-only and will be cleared when the driver executes a read action.
7. Clearing the IRQ_EN has no effect on the IRQ and the $\overline{\text{ALERT}}$ PIN outputs.
8. Disabling the ALERT_EN will also clear the ALERT_FLAG.

17.14 I²C Interface

The RT9426A I²C slave address = 7'b1010101. The I²C interface supports fast mode with a bit rate of up to 400kb/s. The write or read bit stream is shown below:



17.15 Register Summary Table

Name	Symbol	Address	Unit	Mode	Reset
Control	CNTL	0x00 to 0x01	--	R/W	0x0000
Current	CURR	0x04 to 0x05	mA	R	0x0000
Temperature	TEMP	0x06 to 0x07	0.1°K	R/W	0x0BA6
Voltage	VBAT	0x08 to 0x09	mV	R	0x0ED8
Flag1	FLAG1	0x0A to 0x0B	--	R	0x0000
Flag2	FLAG2	0x0C to 0x0D	--	R	0x0000
DeviceID	DVCID	0x0E to 0x0F	--	R	0x426A
RemainingCapacity	RM	0x10 to 0x11	mAh	R	0x03CF
FullChargeCapacity	FCC	0x12 to 0x13	mash	R	0x07D0
AverageCurrent	AI	0x14 to 0x15	mA	R	0x0000
TimeToEmpty	TTE	0x16 to 0x17	minute	R	0xFFFF
Version	VER	0x20 to 0x21	--	R	0x0001
VGCOMP12	VGCOMP12	0x24 to 0x25	--	R/W	0x3232
VGCOMP34	VGCOMP34	0x26 to 0x27	--	R/W	0x3232
InternalTemperature	INTT	0x28 to 0x29	0.1°K	R	0x0BA6
CycleCount	CYC	0x2A to 0x2B	Counts	R/W	0x0000
StateOfCharge	SOC	0x2C to 0x2D	%	R	0x0032
StateOfHealth	SOH	0x2E to 0x2F	%	R	0x0064
Flag3	FLAG3	0x30 to 0x31	--	R	0x0000
IRQ	IRQ	0x36 to 0x37	--	R	0x0000
DesignCapacity	DC	0x3C to 0x3D	mAh	R	0x07D0
ExtendedControl	EXTDCNTL	0x3E to 0x3F	--	W	0x0000
ExtendReg0 to 15	EXTREG0 to 15	0x40 to 0x4F	--	R/W	0xFFFF
ExtPageChecksum	PAGE_CKS	0x50 to 0x51	--	R	0xFFFF

Name	Symbol	Address	Unit	Mode	Reset
AverageVoltage	AV	0x64 to 0x65	mV	R	0x0ED8
AverageTemperature	AT	0x66 to 0x67	0.1°K	R	0x0BA6
ExtTotalChecksum	TOTAL_CKS	0x68 to 0x69	--	R	0x0000

17.16 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-12L 2.5x4 package, the thermal resistance, θ_{JA}, is 30.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WL-CSP-9B 2.29x1.74 (BSC) package, the thermal resistance, θ_{JA}, is 30.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (30.7°C/W) = 3.25W for a WDFN-12L 2.5x4 package.

$P_{D(MAX)}$ = (125°C - 25°C) / (60.3°C/W) = 1.65W for a WL-CSP-9B 2.29x1.74 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

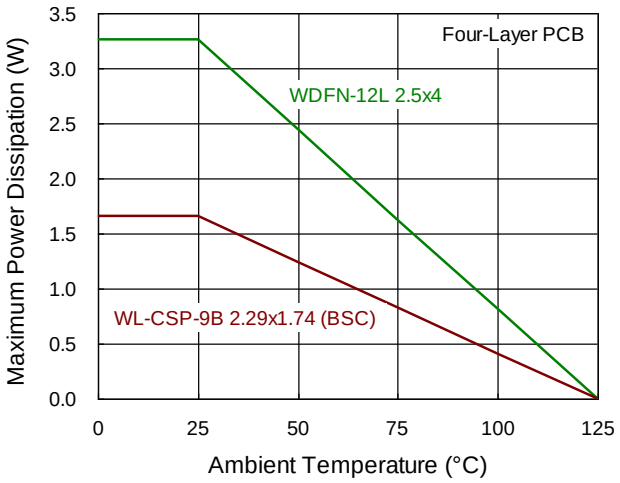


Figure 3. Derating Curves of Maximum Power Dissipation

17.17 Layout Considerations

To ensure the measurement accuracy of the RT9426A, the recommended layout guideline are as follows:

- The capacitors on the VBATS and the VDD pins must be placed as close as possible to each other to minimize noise interference.
- The VBATS and the VBATG paths must form Kelvin Sense connections with the P+ and the P- terminals to minimize the effect of IR drop on voltage measurement accuracy.
- The CSN and the CSP paths must form Kelvin Sense connections with the RS to minimize the impact of IR drop on current measurement accuracy.
- The NTC should be placed as close as possible to the battery and far away from the heat-generating area.
- There are no special layout requirements for the other pins.

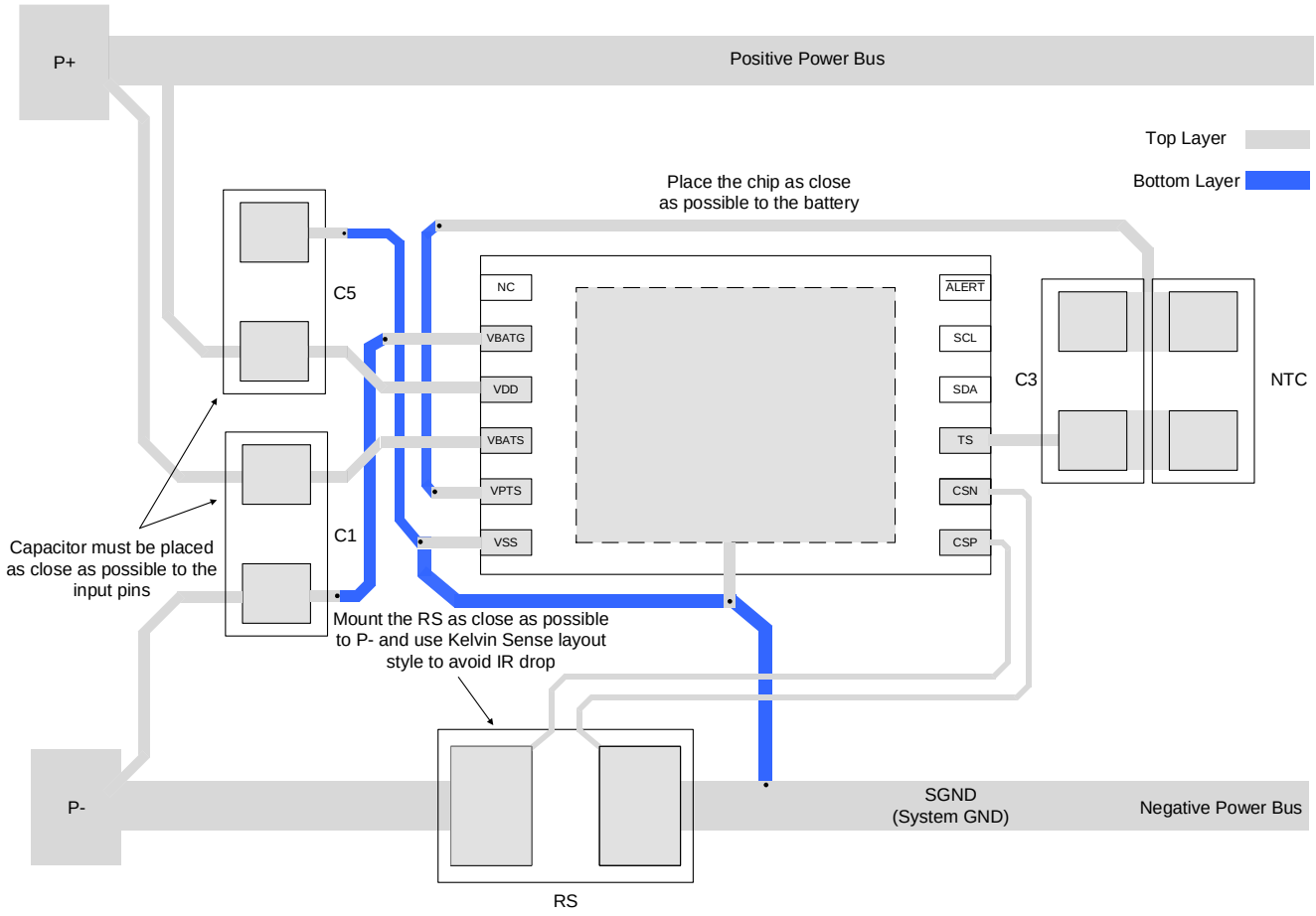


Figure 4. PCB Layout Guide for WDFN-12L 2.5x4 Package

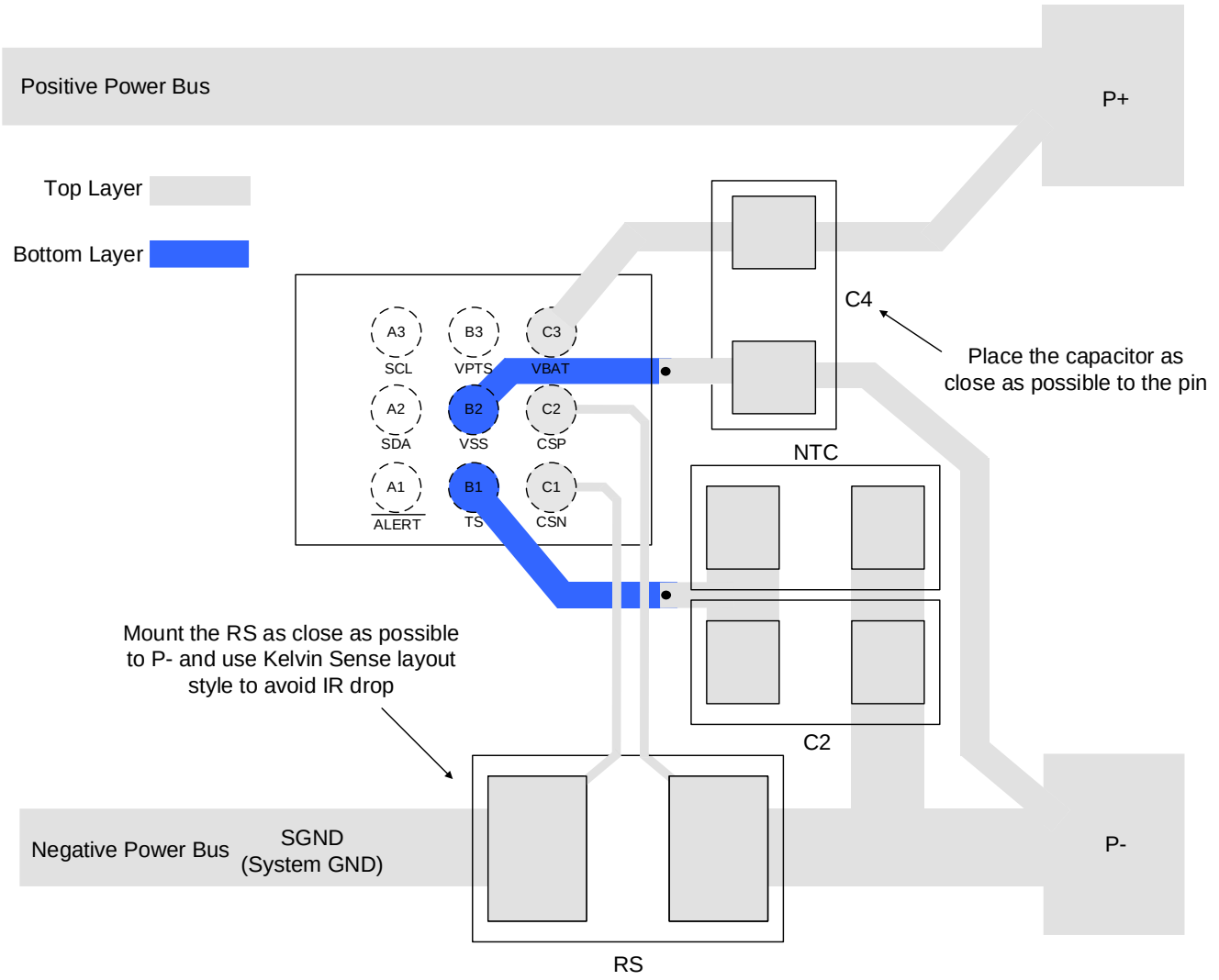


Figure 5. Low-Side Sensing PCB Layout Guide for WL-CSP-9B 2.29x1.74 (BSC) Package

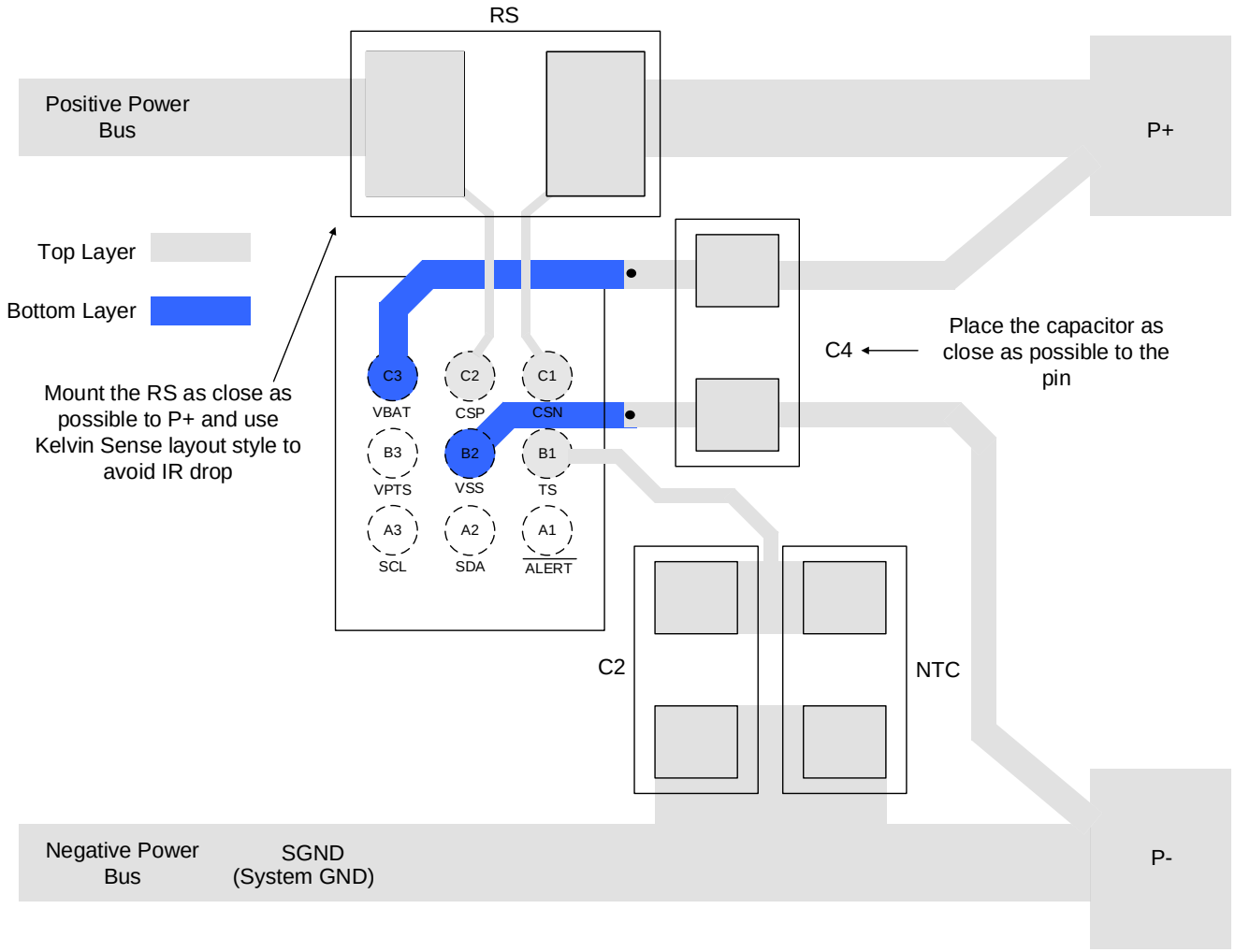
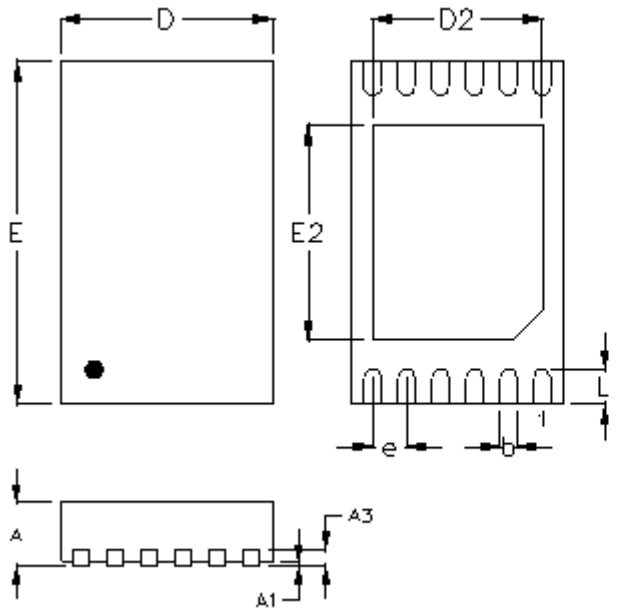


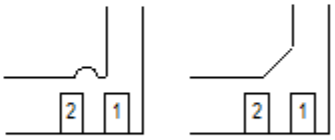
Figure 6. High-Side Sensing PCB Layout Guide for WL-CSP-9B 2.29x1.74 (BSC) Package

Note 13. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

18.1 WDFN-12L 2.5x4





DETAIL A

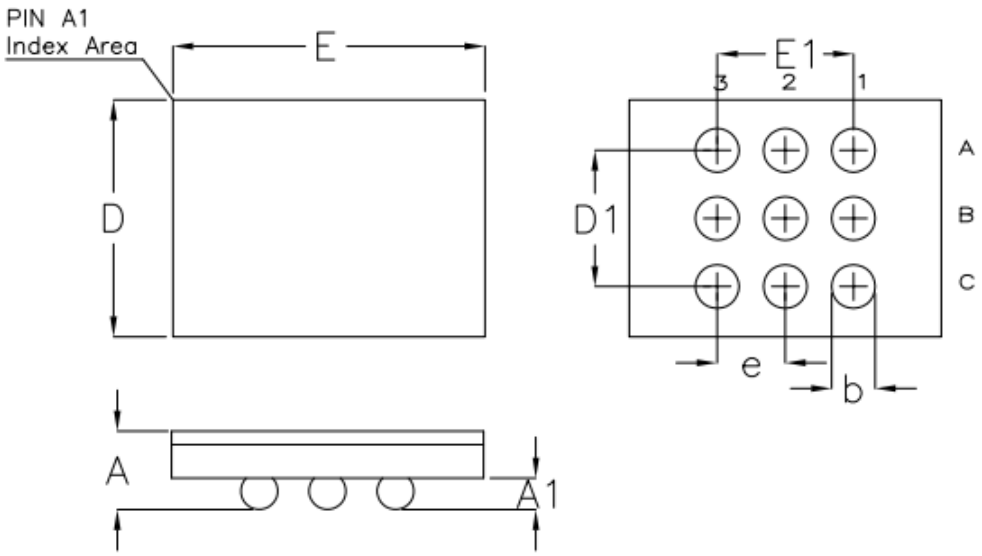
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.400	2.600	0.094	0.102
D2	1.950	2.050	0.077	0.081
E	3.900	4.100	0.154	0.161
E2	2.450	2.550	0.096	0.100
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 2.5x4 Package

18.2 WL-CSP-9B 2.29x1.74 (BSC)

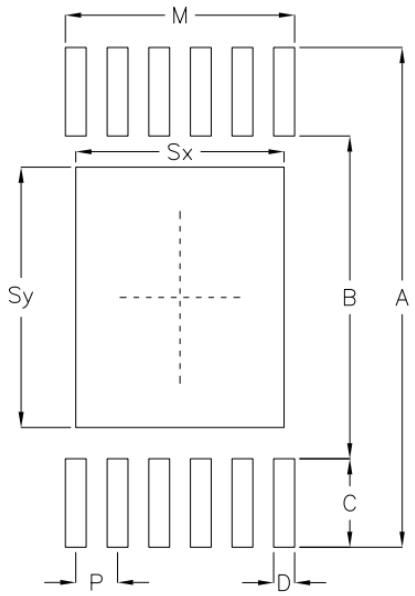


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.525	0.625	0.021	0.025
A1	0.200	0.260	0.008	0.010
b	0.290	0.350	0.011	0.014
D	1.700	1.780	0.067	0.070
D1	1.000		0.039	
E	2.250	2.330	0.089	0.092
E1	1.000		0.039	
e	0.500		0.020	

9B WL-CSP 2.29x1.74 Package (BSC)

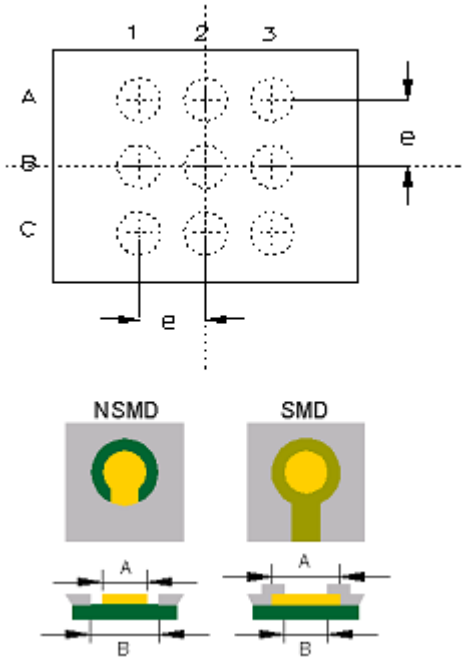
19 Footprint Information

19.1 WDFN-12L 2.5x4



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2.5x4-12	12	0.40	4.80	3.10	0.85	0.20	2.50	2.50	2.20	±0.05

19.2 WL-CSP-9B 2.29x1.74 (BSC)

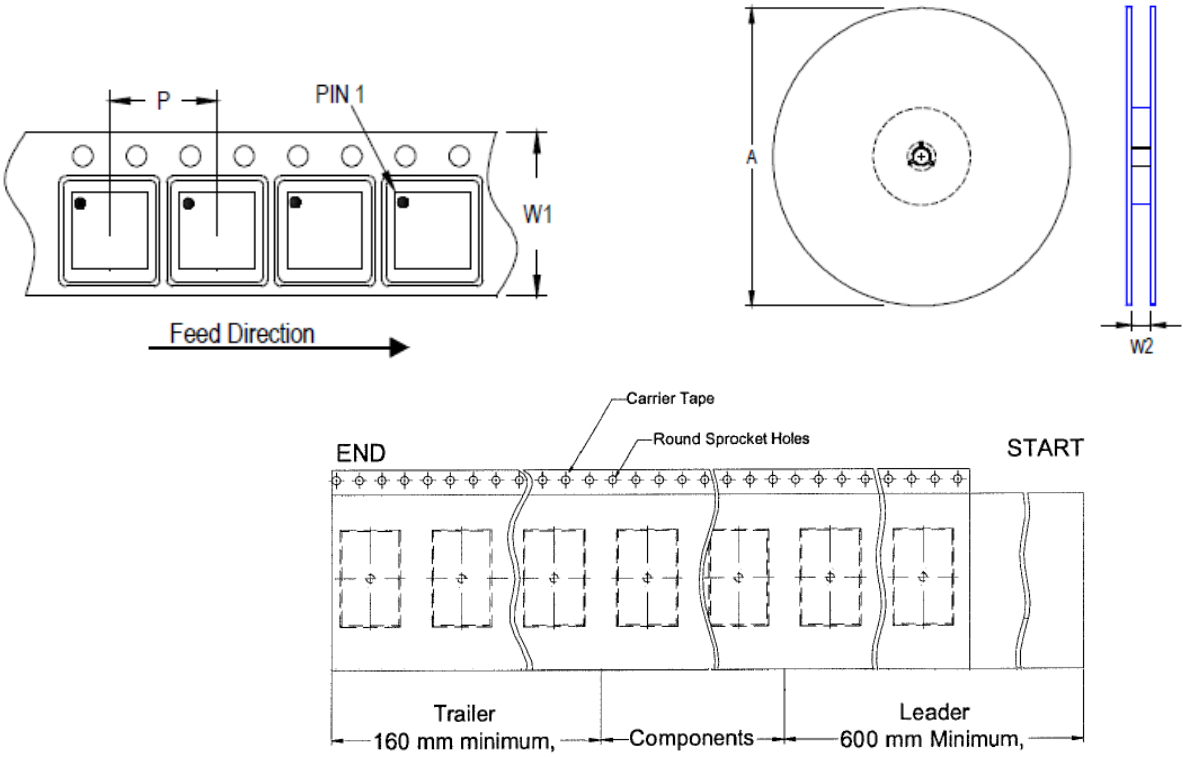


Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.29x1.74-9(BSC)	9	NSMD	0.500	0.275	0.375	±0.025
		SMD		0.375	0.275	

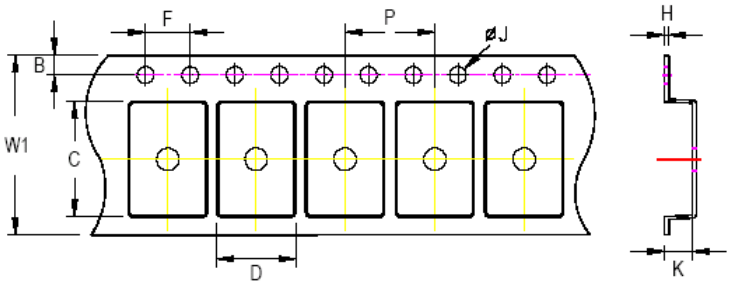
20 Packing Information

20.1 Tape and Reel Data

20.1.1 WDFN-12L 2.5x4



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2.5x4	12	8	180	7	1,500	160	600	12.4/14.4

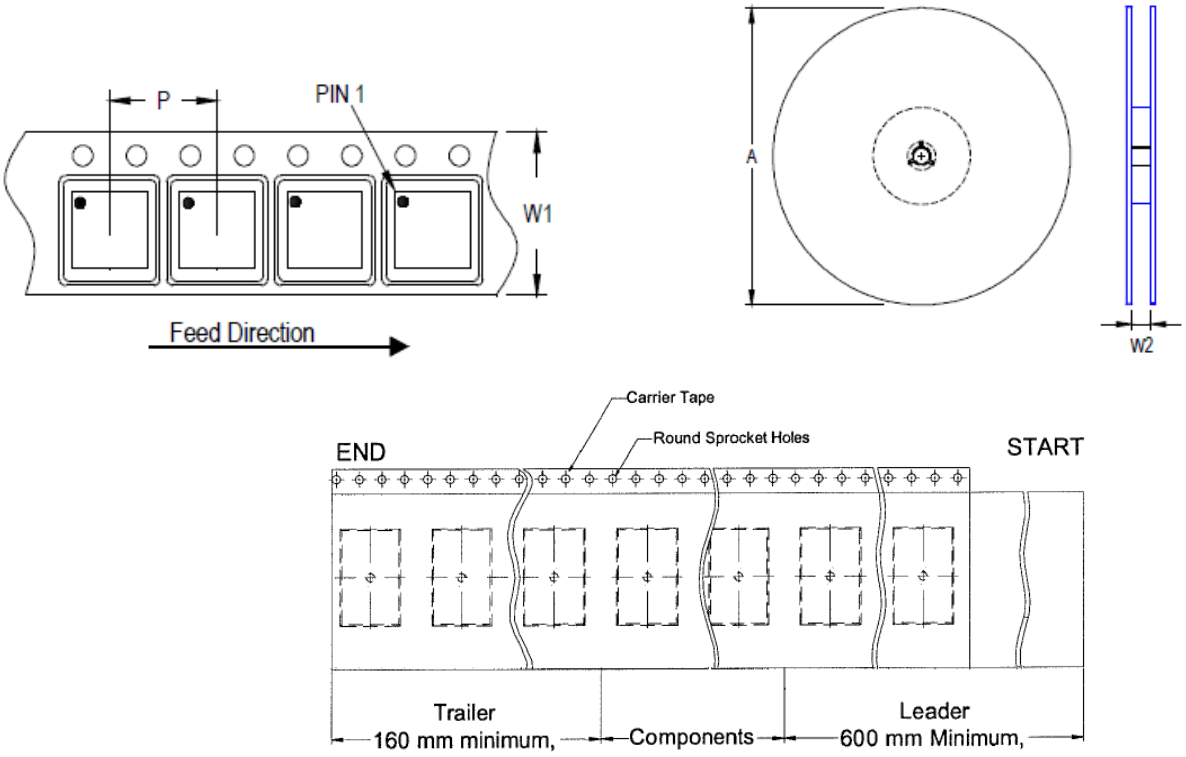


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

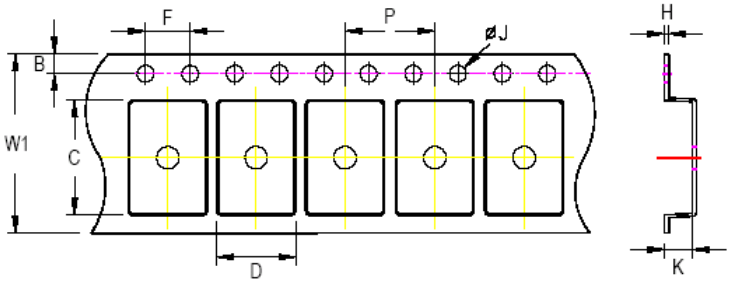
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.1.2 WL-CSP-9B 2.29x1.74 (BSC)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 2.29x1.74	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.8mm	0.6mm

20.2 Tape and Reel Packing

20.2.1 WDFN-12L 2.5x4

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 2.5x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.2.2 WL-CSP-9B 2.29x1.74 (BSC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.29x1.74	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
01	2024/12/6	Modify	*General Description on page 1* - Added temperature range *Ordering Information on page 3* - Added note *Electrical Characteristics on page 7, 8, 9* - Updated symbol - Added Note 6 *Typical Application Circuit on page 11* - Added description *Application Information on page 22* - Updated the declaration *Packing Information on page 27, 28, 29, 30, 31* - Updated packing information

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