PWM Controller for Programmable Power Converter (USBPD)

General Description

The RT7753GCV series is specifically designed to work with controllers, such as RT7202, to provide a total solution for the USB Power Delivery (USB PD) or a programmable power adapter. This RT7753GCV not only provides a control scheme of high power efficiency, but also gives a very low standby power control below 50mW when under the 5V standby condition.

The RT7753GCV is such a special design to achieve a wide-range of output voltage by utilizing several innovations, including (1) By using the DMAG pin, the RT7753GCV senses the output voltage to adjust the loop gain for system stability, to adjust the threshold voltage of the output over-voltage protection, to protect external devices, and to adjust the current limit to meet Limited Power Source (LPS) safety requirements; (2) The RT7753GCV is also equipped with comprehensive protection features, including Bulk-Capacitor brown-in /brown-out protection, VDD over-voltage protection (VDD OVP), output over-voltage/under-voltage protection (Output OVP/UVP), secondary rectifier short-circuit protection (SRSP), and external over-temperature protection (External OTP); (3) For constant output power regulation, a resistor connected to CS pin can be used to achieve an accurate line compensation across the universal input voltage range; and (4) The RT7753GCV also provides various features to protect against any failures occurring at the secondary-side component, such as the RT7202 or a shunt regulator.

In applications, the RT7753GCV is suggested to use with a secondary controller RT7202 to realize a robust and safe design so as to prevent all potential fault conditions due to misconnection of various devices, cables, plugs or receptacles.

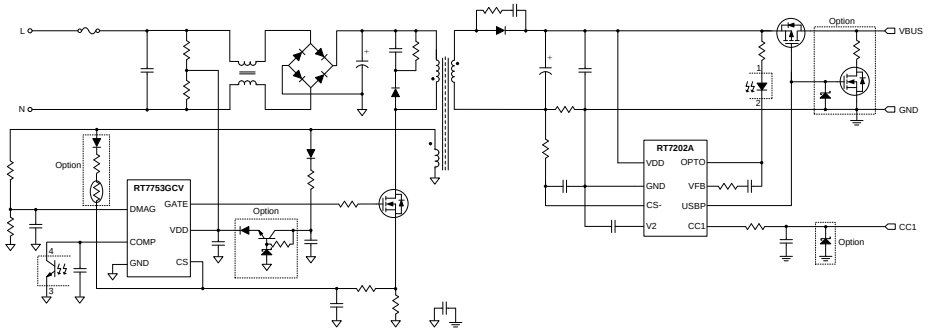
Features

- **Optimized for Adaptive Output Power**
  - **Wide VDD Range : 9V to 42V**
  - **Adaptive Output Over-Voltage Protection**
  - **Adaptive Over-Current Protection**
  - **Adaptive Loop Gain Control for Loop Stability**
- **High Efficiency**
  - **Green Mode Operation at Light Load and No Load**
- **Comprehensive Protection Features**
  - **Bulk-Capacitor Brown-In and Brown-Out Protection**
  - **VDD Over-Voltage Protection**
  - **Output Over-Voltage and Under-Voltage Protection**
  - **External Over-Temperature Protection**
  - **Secondary Rectifier Short-Circuit Protection**
  - **Programmable Line Compensation**
- **Others**
  - **< 50mW in 5V Standby Mode for Power Saving**
  - **Driver Capability : 300mA/–300mA**
  - **SmartJitter™ Technology**

Applications

- USB PD and Programmable Power Adapters

Simplified Application Circuit



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Ordering Information

RT7753GCV□□

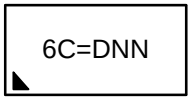
- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green
  (Halogen Free and Pb Free)
- V_{OUT} Application Version
  (Refer to Functional Table)
- Protection Mode Version
  (Refer to Functional Table)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

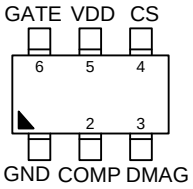
Marking Information



6C= : Product Code
DNN : Date Code

Pin Configuration

(TOP VIEW)



SOT-23-6

RT7753GCV Functional Table

Version	RT7753GCV
Operation Mode	CCM (I_{DMAG} < I_{DMAG_HVSW}) QR Mode (I_{DMAG} > I_{DMAG_HVSW})
Normal-Mode PWM Frequency	84kHz
Minimum Green-Mode Frequency	25kHz
Minimum QR Frequency	33.3kHz
Adaptive OVP	O
Start-Up OVP	O
VDD OVP	Auto-Recovery
Output OVP	Auto-Recovery
Output Voltage Threshold of OVP, V_{O_OVP}	14.4V
Output UVP	Auto-Recovery
Adaptive OCP	Auto-Recovery
Adaptive OCP Delay Time	49ms
SRSP	Auto-Recovery
External OTP	Auto-Recovery
Valley Switching Mode	O

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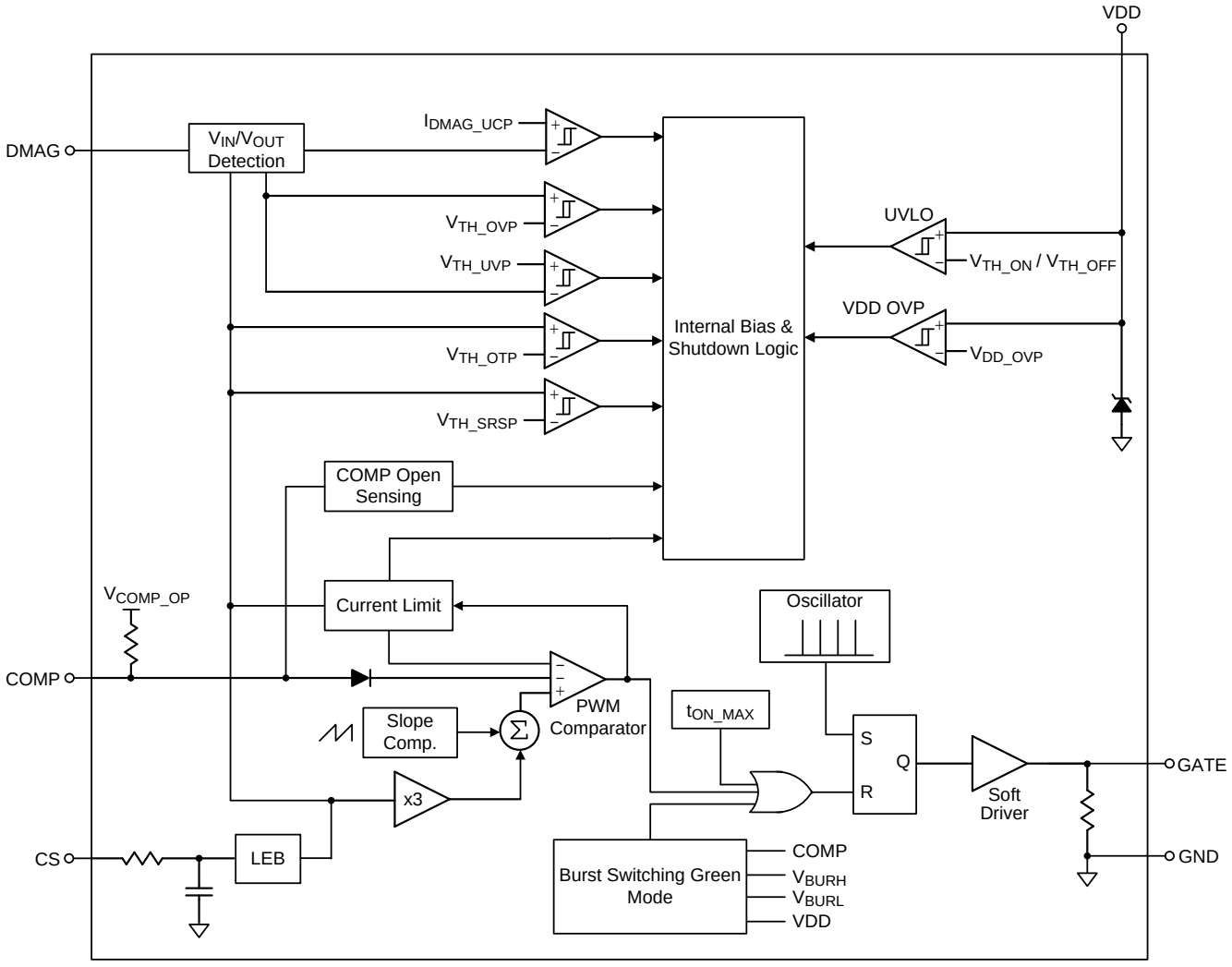
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground.
2	COMP	Feedback input. Connect an opto-coupler from the COMP pin to GND to close the control loop to achieve output voltage regulation.
3	DMAG	Demagnetization input. Input and output voltages are sensed from the auxiliary winding.
4	CS	Current sense input. The current sense resistor, connected from the CS pin to GND, is used to set current limit for the power system.
5	VDD	Supply input voltage. The controller is enabled when the VDD voltage exceeds V_{TH_ON}, and is disabled when the VDD voltage drops below V_{TH_OFF}.
6	GATE	Gate driver output.

Functional Block Diagram



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Operation

The RT7753GCV series is specifically designed to work with a USB PD controller or a programmable power adapter controller so as to provide a total solution. For applications with wide output voltage range, the RT7753GCV features many innovations, including the adaptive output over-voltage protection, the adaptive over-current protection and the adaptive loop stability control.

Multi-Mode PWM

The RT7753GCV is a PWM controller providing a multi-mode control to optimize performance under different load conditions. With an internal oscillator to generate a PWM frequency for the system to operate in a Continuous-Conduction Mode (CCM) or a Quasi-Resonant mode (QR mode), this controller will automatically enter into green mode when in light load or in no load condition.

Gate Driver

A totem-pole gate driver is designed to meet both the EMI limitation and the efficiency requirement in low-power applications. An internal pull-down circuit is built to prevent the external MOSFET from being falsely turned on when the VDD is too low and an under-voltage lockout (UVLO) event is triggered.

SmartJitter™ Technology

In general PWM controllers, the frequency jittering scheme is usually adopted to spread frequency spectrum in order to alleviate EMI problems. However, due to the inherent operating characteristics of a valley switching mode and a green mode, the frequency spectrum in high line conditions or in deeper extended valley switching conditions cannot be spread wide enough as expected, and thus the targeted frequency jittering range cannot be achieved, which therefore degrades suppression of the EMI emissions.

The RT7753GCV incorporates RICHTEK's proprietary SmartJitter™ technology to optimize the frequency jittering range. This innovative SmartJitter™ technology can effectively reduce EMI emissions of a switch-mode power supply as well as the output ripple as a consequence of frequency jittering in all operation conditions.

Adaptive Loop Stability Control

The RT7753GCV features the proprietary adaptive loop stability control to adjust the loop gain automatically, which can ensure the system stability for the operation across a wide range of output voltage.

Adaptive Output Over-Voltage Protection

For applications with a wide output voltage range, the RT7753GCV also provides the proprietary adaptive output over-voltage protection, of which the threshold value is automatically adjusted according to the output voltage when a fault occurs.

Adaptive Over-Current Protection

In general, a power system designed for 20V/3A may deliver a current of 12A when output is down to 5V, under a constant output power operation. This, however, may violate the Limited Power Source (LPS) safety requirements for the maximum output current, and may damage to its connected devices. To solve this, the RT7753GCV offers a cycle-by-cycle current limit protection, automatically decreasing the current limit and the maximum output current if the output voltage V_{OUT} is too low or the output current is too high. Afterward, the protection mode is activated if the fault condition sustains for an over-current protection delay time t_{D_OCP}.

Secondary Rectifier Short Protection (SRSP)

When a short-circuit occurred on the secondary rectifier or MOSFET during the primary MOSFET on-time, the main transformer becomes saturated and the rising rate of the primary-side current is then limited only by the leakage inductance of the transformer. In this case, the inductance is a few percentage of the primary magnetizing inductance, which produces a current with a very steep slope. In high line condition, the peak current through the primary MOSFET becomes extremely high after the over-current protection delay time elapses. Moreover, the controller is designed to shut down in a few cycles once a secondary rectifier short-circuit condition is detected.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 50V
- GATE to GND ---------- –0.3V to 16.5V
- DMAG, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
  SOT-23-6, θ_{JC} ---------- 135°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 9V to 42V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Over-Voltage Protection Threshold Voltage	V_{DD_OVP}		43	46	49	V
Turn-On Threshold Voltage	V_{TH_ON}		12.5	14.5	16.5	V
Turn-Off Threshold Voltage	V_{TH_OFF}		6	7	8	V
VDD Holdup Mode Entry Point	V_{DD_ET}	V_{COMP} < V_{ZD_ET}, Max. operating 512 cycles.	7.35	7.9	8.45	V
VDD Holdup Mode Ending Point	V_{DD_ED}	V_{COMP} < V_{ZD_ET}	V_{DD_ET} + 0.2	V_{DD_ET} + 0.6	V_{DD_ET} + 0.9	V
VDD Holdup Mode Delay Time	t_{D_VDDHD}	f_{OSC} = 25kHz (Note 5)	16.4	20.5	24.6	ms
Latched-Off Clamp Voltage	V_{DD_LH}		3.8	5	6.2	V
Latched-Off Release Threshold Voltage	V_{LH_RST}		3.3	4.5	5.7	V
Start-Up Current	I_{DD_ST}	V_{DD} < V_{TH_ON} – 0.1V	--	1.5	4	μA
Operating Supply Current	I_{DD_OP}	V_{DD} = 15V, V_{COMP} = 0V	--	300	500	μA
I_{DD} Sinking Current for Auto-Recovery Mode	I_{DD_ARP}	During entering auto-recovery mode	350	575	800	μA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay Time for Exit Auto-Recovery Protection	t_{D_AUTO}		678	964	1250	ms
Oscillator Section						
Normal-Mode PWM Frequency	f_{NOR}	$V_{COMP} > V_{GM\_ET}$	79	84	89	kHz
Minimum QR Mode Frequency	f_{MIN_QR}		26.6	33.3	40	kHz
Minimum Green Mode Frequency	f_{MIN_GM}	$V_{COMP} < V_{GM\_EX}$	20	25	30	kHz
Maximum Duty for CCM	D_{MAX}	$I_{DMAG} < I_{DMAG\_HVSW}$	70	76	82	%
Duty of Maximum On Time for QR Mode	D_{MAX_ON}	$I_{DMAG} > I_{DMAG\_HVSW}$	54	67.5	81	%
PWM Frequency Jittering Range	Δf	$V_{COMP} > V_{GM\_ET}$	±3	±6	±9	%
PWM Frequency Jittering Period	t_{JIT}	f_{OSC} = 84kHz (Note 5)	9.7	12.2	14.7	ms
Frequency Variation Versus VDD Deviation	f_{DV}	V_{DD} = 9V to 40V (Note 5)	--	2	3	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A = –30°C to 105°C (Note 5)	--	5	6	%
COMP Input Section						
Open-Loop Voltage	V_{COMP_OP}	Comp pin open-circuited	3.2	3.4	3.6	V
COMP Short-Circuit Current	I_{ZERO}	V_{COMP} = 0V	120	150	180	μA
COMP Open-Loop Protection Delay Time	t_{COMP_OP}	f_{OSC} = 84kHz	39	48.8	58.6	ms
Green Mode Entry Voltage	V_{GM_ET}	$V_{DMAG} > 1.575V$, $I_{DMAG} > I_{DMAG\_HVSW}$	1.8	1.86	1.92	V
		$V_{DMAG} > 1.575V$, $I_{DMAG} < I_{DMAG\_HVSW}$	1.7	1.76	1.82	
Green Mode Exit Voltage	V_{GM_EX}	$V_{DMAG} > 1.575V$, $I_{DMAG} > I_{DMAG\_HVSW}$	1.6	1.66	1.72	V
		$V_{DMAG} > 1.575V$, $I_{DMAG} < I_{DMAG\_HVSW}$	1.5	1.56	1.62	
Zero Duty Entry Voltage	V_{ZD_ET}	$V_{DMAG} > V_{SW\_BSTEX}$	1.29	1.35	1.41	V
		$V_{DMAG} < V_{SW\_BSTET}$	1.04	1.1	1.16	
Zero Duty Exit Voltage	V_{ZD_EX}	$V_{DMAG} > V_{SW\_BSTEX}$	1.34	1.4	1.46	V
		$V_{DMAG} < V_{SW\_BSTET}$	1.09	1.15	1.21	
Current Sense Section						
Maximum Current Limitation	V_{CS_OCP}	V_{DMAG} = 1.8V	0.38	0.41	0.44	V
		V_{DMAG} = 0.45V	0.29	0.32	0.35	
Over-Current Protection Delay Time	t_{D_OCP}	f_{OSC} = 84kHz	39	48.8	58.6	ms

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Leading-Edge Blanking Time	t_{LEB}		340	475	610	ns
Secondary Rectifier Short-Circuited Protection Threshold Voltage	V_{TH_SRSP}	(Note 5)	1.1	1.2	1.3	V
External Over-Temperature Protection Threshold Voltage	V_{TH_OTP}	V_{DMAG} = 1.8V	0.75	0.80	0.85	V
External Over-Temperature Protection Delay Time	t_{D_OTP}	f_{OSC} = 84kHz	39	48.8	58.6	ms
GATE Section						
Rising Time	t_R	C_L = 1nF	150	280	410	ns
Falling Time	t_F	C_L = 1nF	10	45	80	ns
GATE Output Clamp Voltage	V_{CLAMP}	V_{DD} = 23V	10	12	14	V
DMAG Section						
Output Over-Voltage Protection Threshold Voltage During Start-Up	V_{DMAG_INOVP}	(Note 5)	0.9	1	1.1	V
Output Over-Voltage Protection Threshold Voltage	V_{DMAG_OVP}		2.04	2.15	2.26	V
Output Under-Voltage Protection Threshold Voltage	V_{DMAG_UVP}	Start detection after soft-start + 512 cycles. Trigger if V_{COMP} > 1.8V and V_{DMAG} < V_{DMAG_UVP}.	0.55	0.6	0.65	V
Output Under-Voltage Protection Exit Threshold Voltage	V_{DMAG_UVPEX}		0.6	0.65	0.7	V
Detected Time of DMAG Under-Voltage Protection	$t_{D\_DMAGUVP}$	f_{OSC} = 84kHz	1.37	1.52	1.67	ms
Blanking Time of DMAG Pin	t_{BLK}	V_{CS} = 0.4V	1.8	2.3	2.8	μs
Brown-In Protection Threshold Current	I_{DMAG_BNI}		145	160	175	μA
Brown-Out Protection Threshold Current	I_{DMAG_BNO}		130	145	160	μA
Brown-Out Protection Delay Time	t_{D_BNO}	f_{OSC} = 84kHz	39	48.8	58.6	ms
High/Low Line Switching Threshold Current	I_{DMAG_HVSW}		280	330	380	μA
High/Low Line Switching Hysteresis	I_{DMAG_HVHYS}	(Note 5)	0.1	7	14	μA
De-Bounce Time of High Line to Low Line	t_{D_HTOL}	f_{OSC} = 84kHz (Note 5)	156	195	234	ms
Entry Switching Threshold Voltage of Zero Duty Mode	V_{SW_BSTET}	(Note 5)	0.94	1.05	1.16	V
Exit Switching Threshold Voltage of Zero Duty Mode	V_{SW_BSTEX}	(Note 5)	1.04	1.15	1.26	V
Maximum DMAG Sourcing Current	I_{DMAG_MAX}	(Note 5)	1200	--	--	μA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DMAG Under-Current Protection Threshold Current	I_{DMAG_UCP}		10	22	34	μA

Note1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

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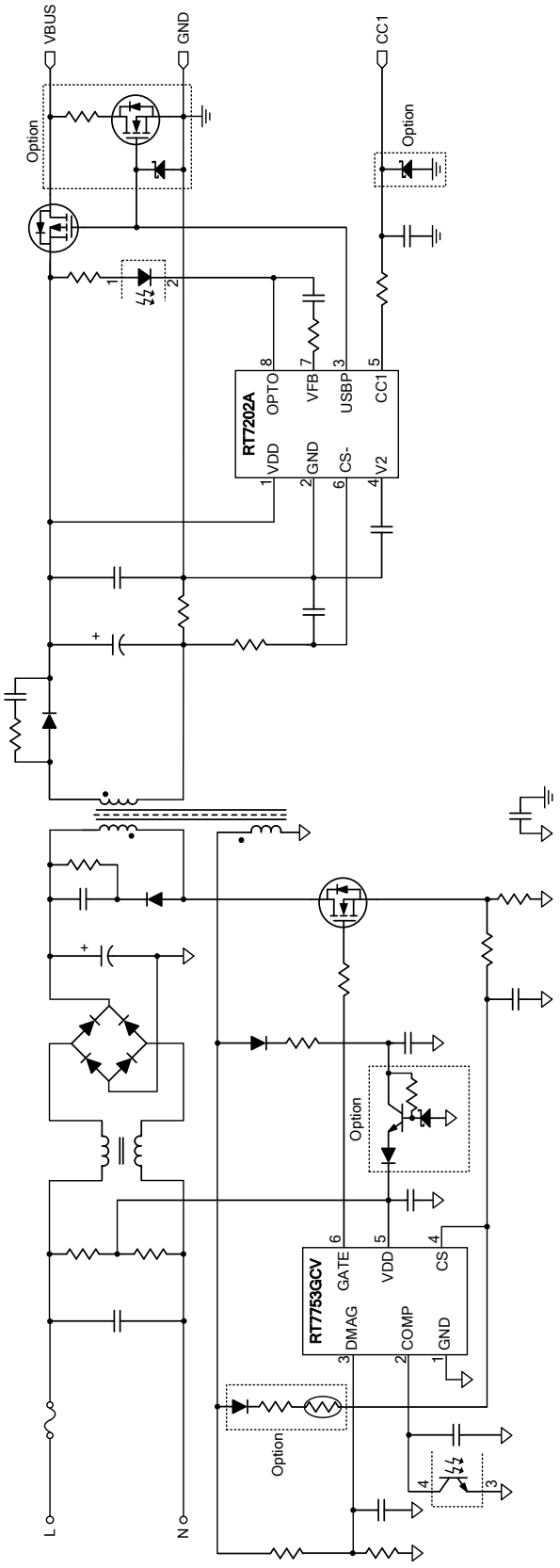
Typical Application Circuit



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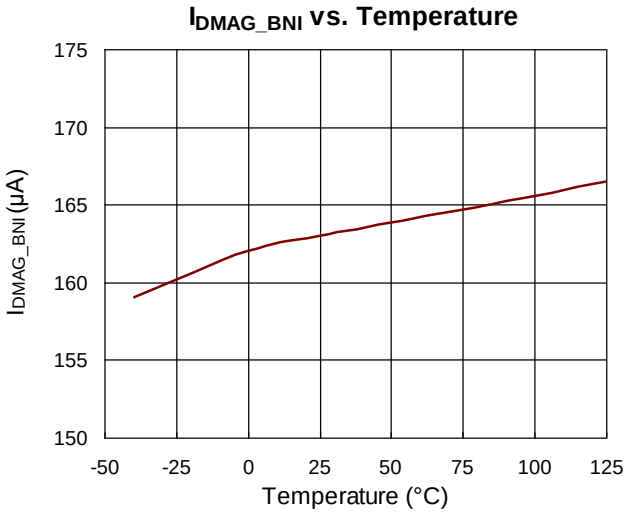
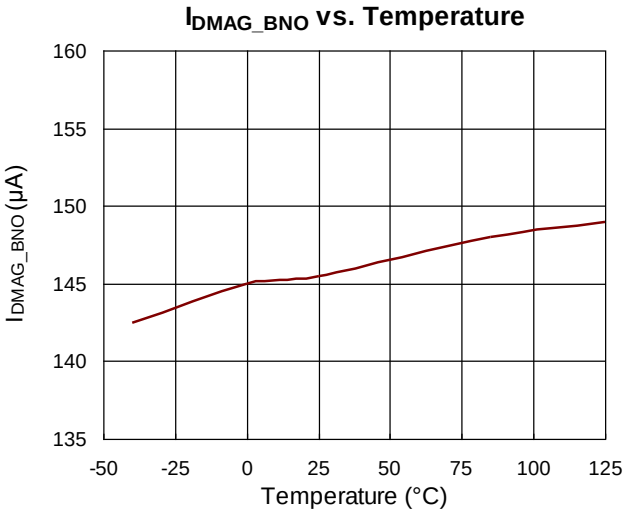
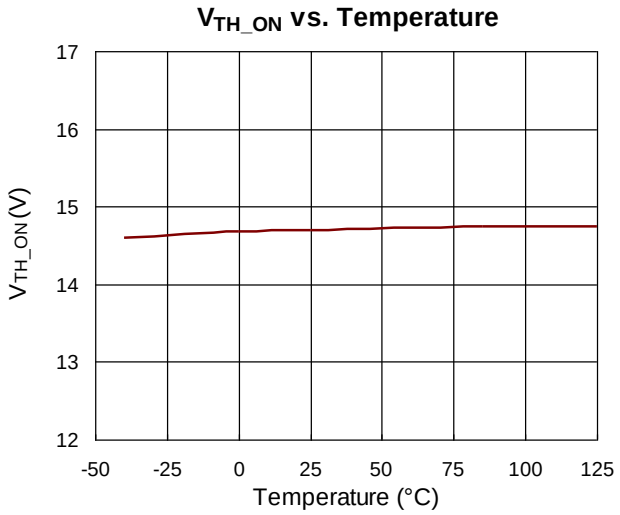
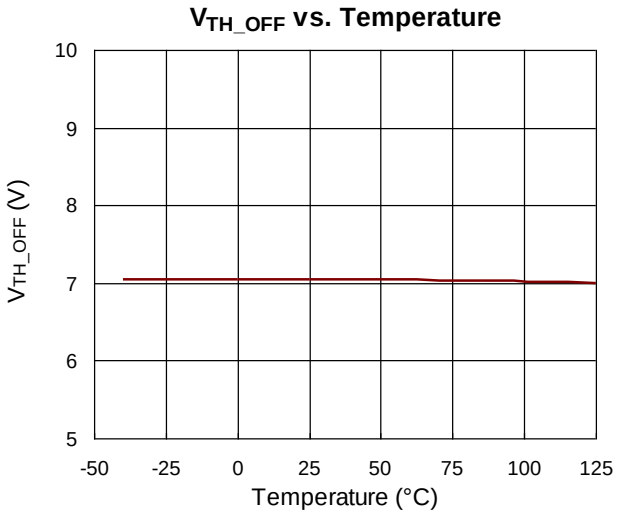
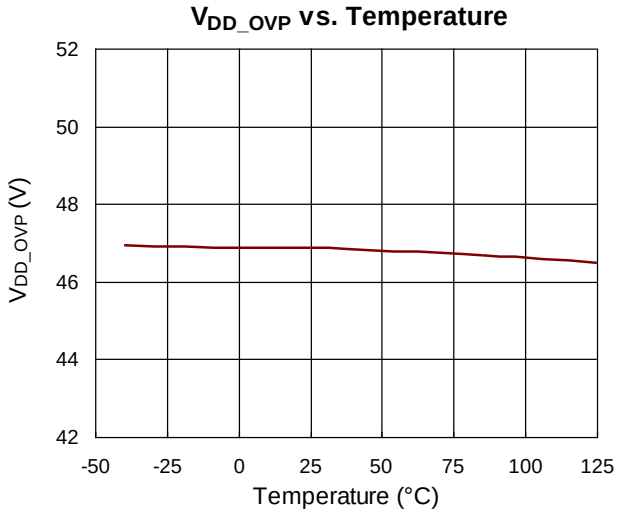
Typical Operating Characteristics

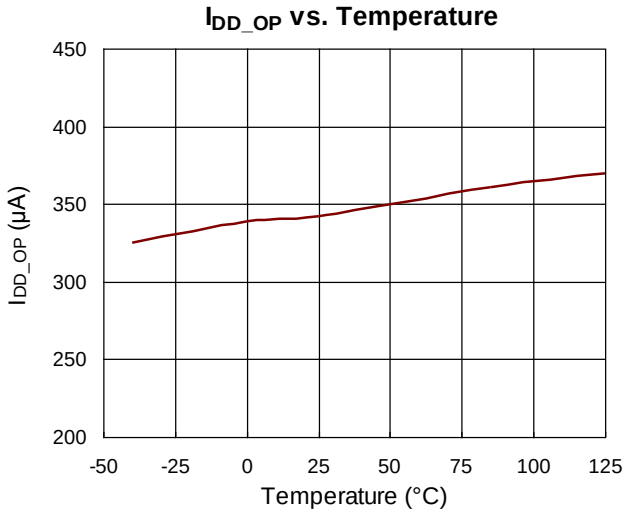












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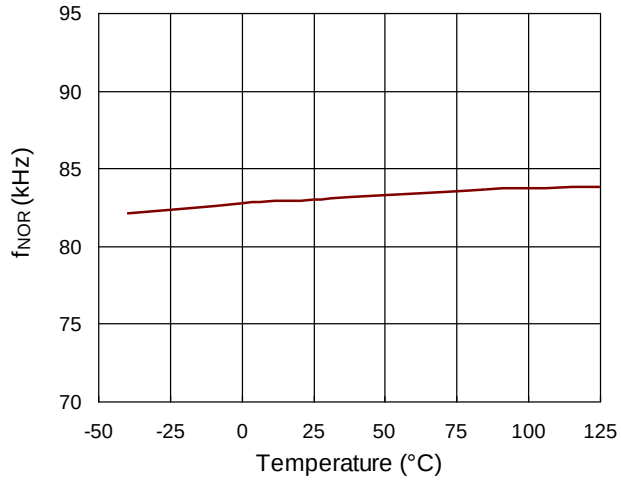
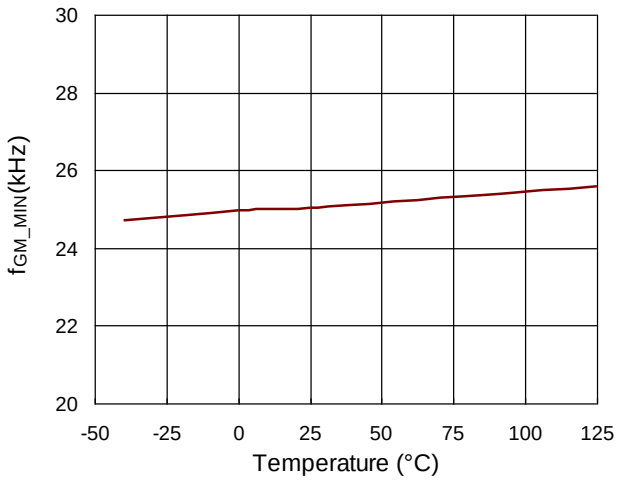
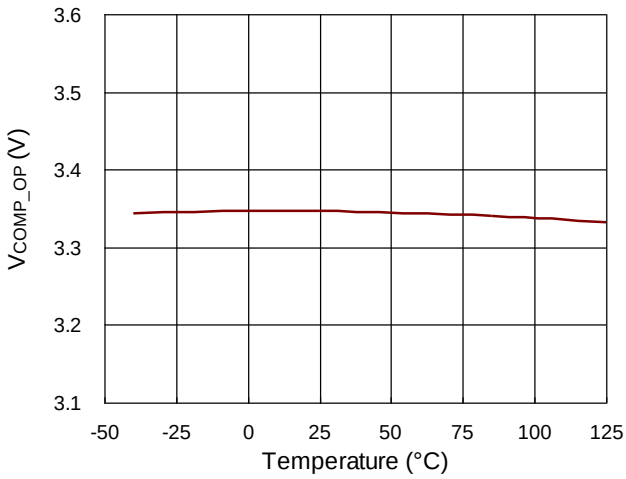
f_{NOR} vs. Temperature



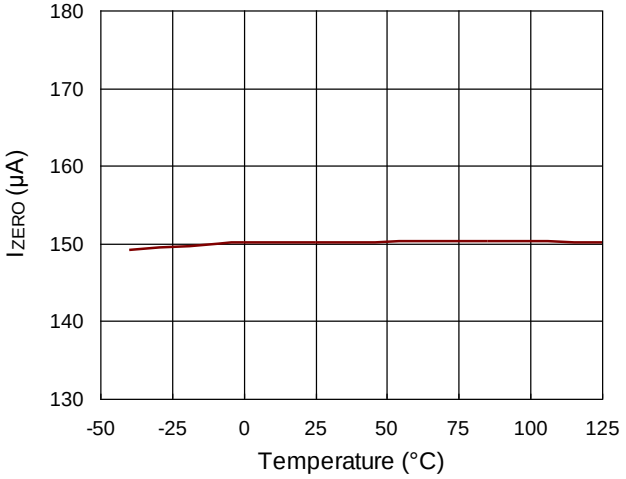
f_{GM_MIN} vs. Temperature



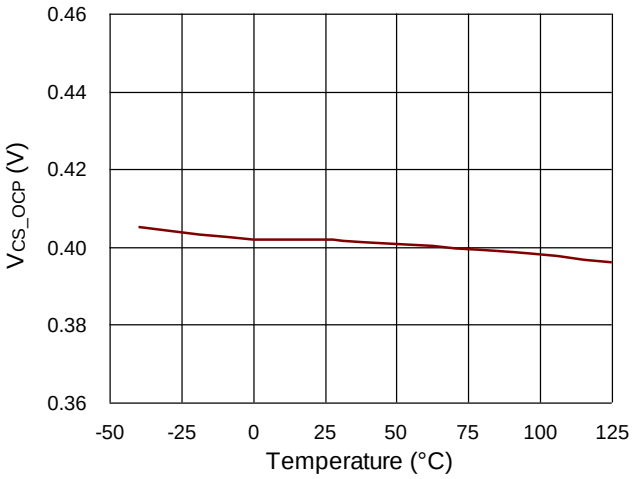
V_{COMP_OP} vs. Temperature



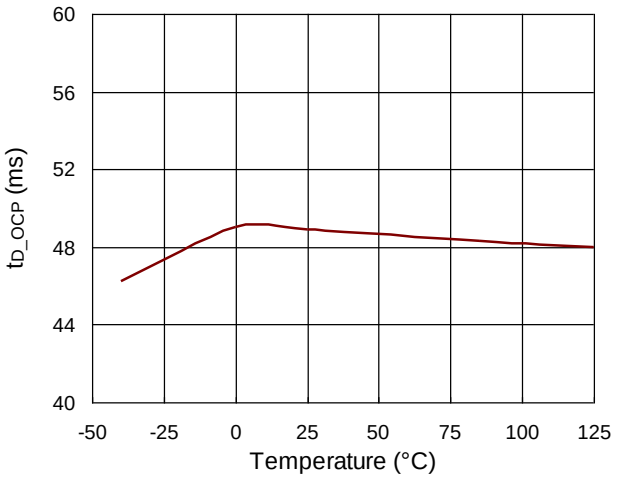
I_{ZERO} vs. Temperature



V_{CS_OCP} vs. Temperature



t_{D_OCP} vs. Temperature



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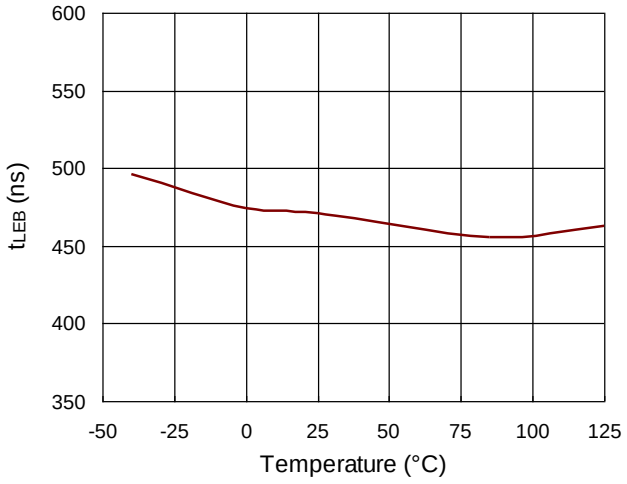
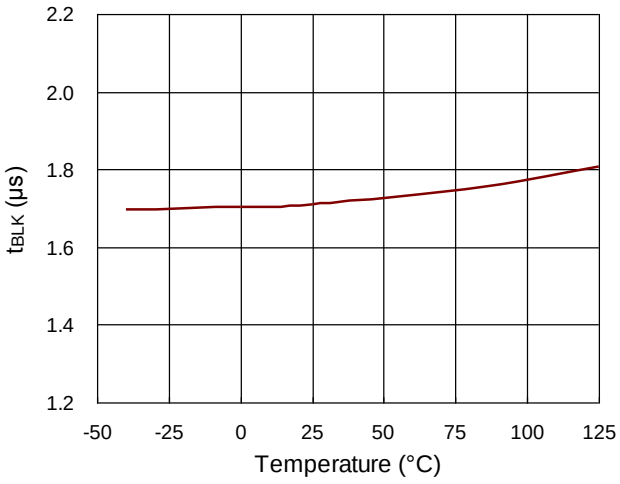
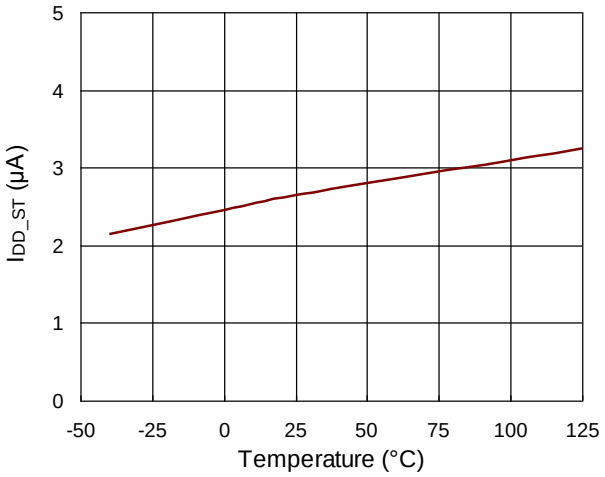
t_{LEB} vs. Temperature



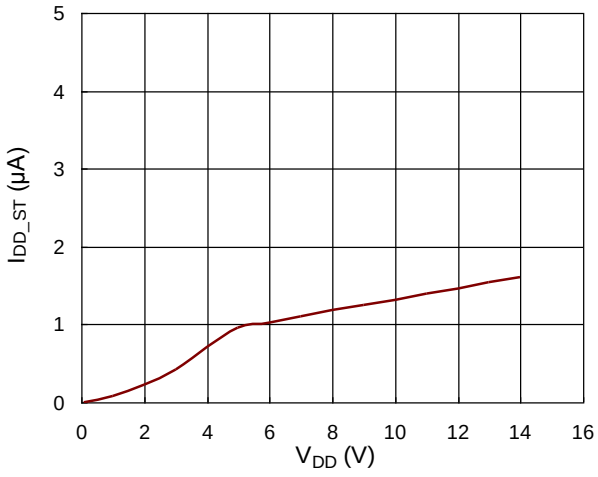
t_{BLK} vs. Temperature



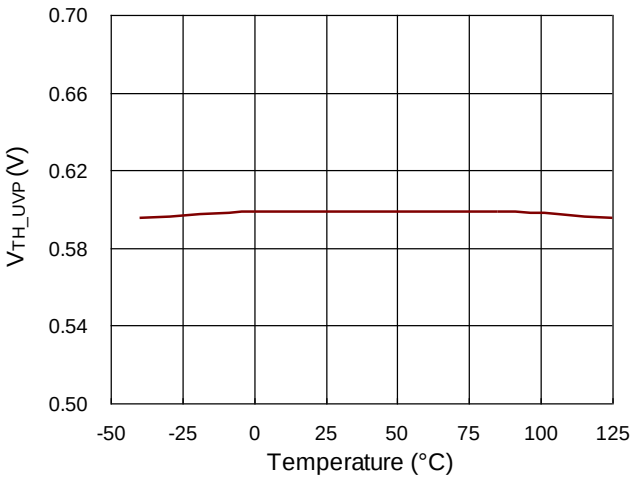
I_{DD_ST} vs. Temperature



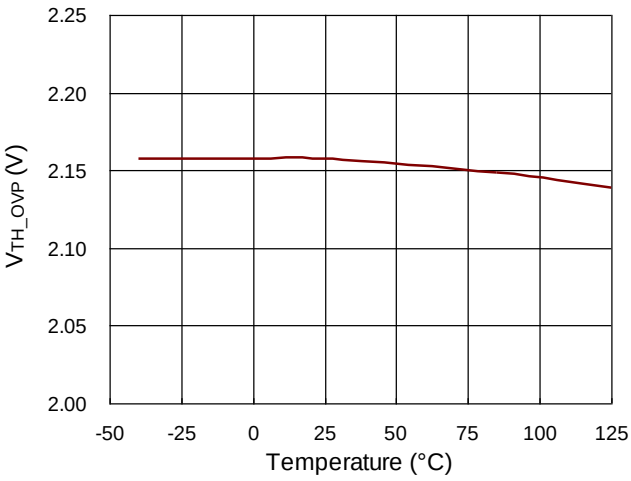
I_{DD_ST} vs. V_{DD}



V_{TH_UVP} vs. Temperature



V_{TH_OVP} vs. Temperature



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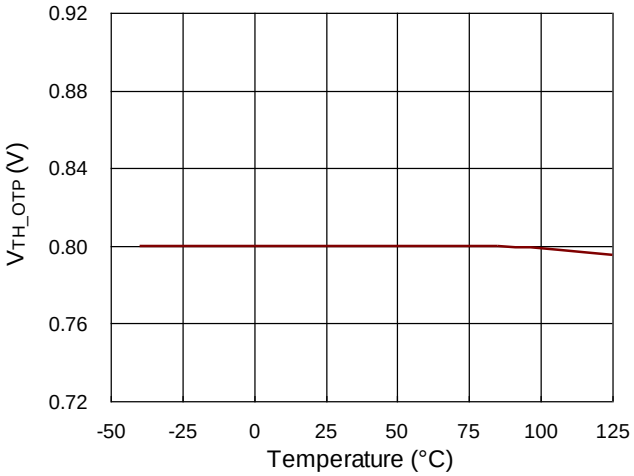
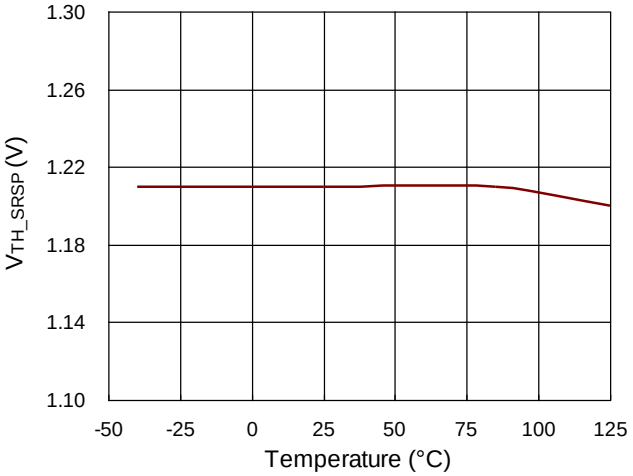
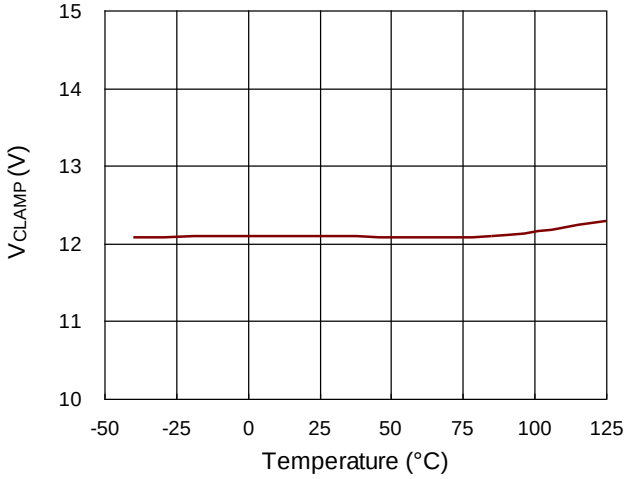
V_{TH_OTP} vs. Temperature



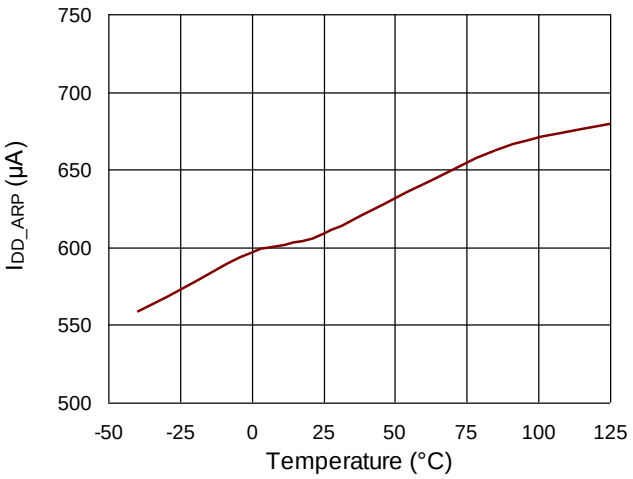
V_{TH_SRSP} vs. Temperature



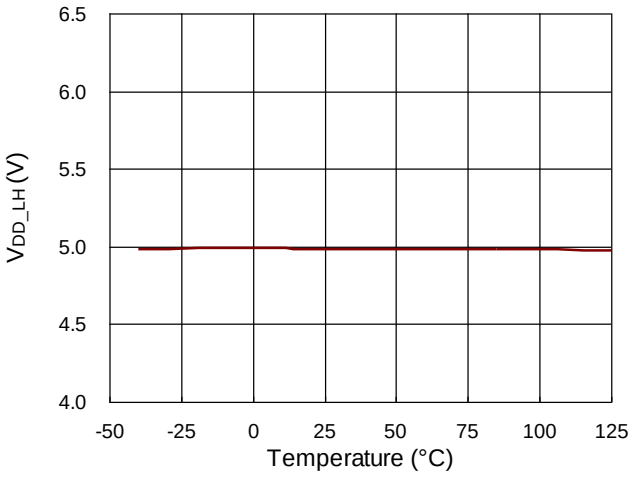
V_{CLAMP} vs. Temperature



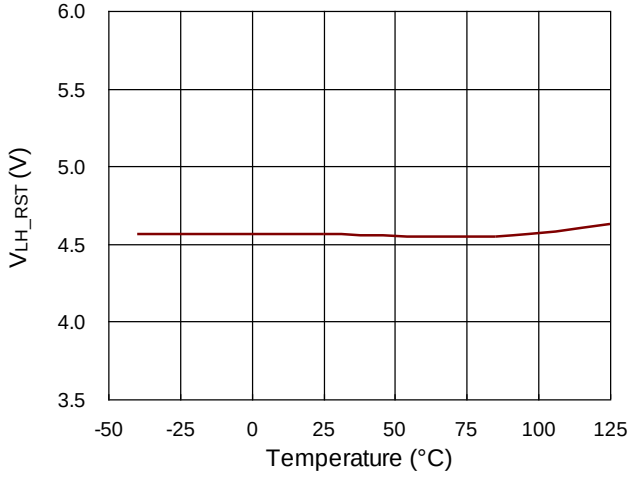
I_{DD_ARP} vs. Temperature



V_{DD_LH} vs. Temperature



V_{LH_RST} vs. Temperature



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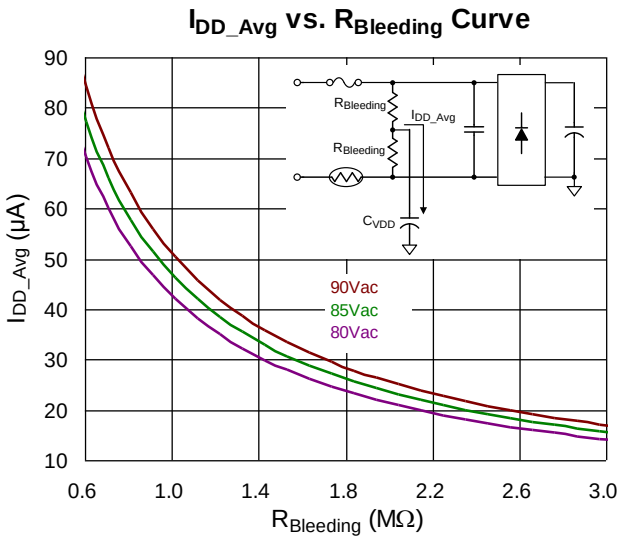
Application Information

The RT7753GCV is a multi-mode PWM flyback controller. As the load decreases, the controller may enter into different modes, such as the green mode or the burst mode. The RT7753GCV can automatically switch among several control modes to optimize the efficiency of a power system when operating under various load conditions.

Start-Up Circuit

To optimize the power efficiency, bleeder resistors can be added to the start-up circuit, which not only can reduce power loss but also helps to reset the latched-mode protections faster. Figure 1 shows the curve for IDD average current I_{DD_Avg} vs. bleeder resistance ($R_{Bleeder}$). The curve can be used to design the bleeder resistance values.

During hiccup mode, the off-time duration is extended to minimize power loss and heat dissipation. During auto-recovery protection mode, the controller sinks a very small sinking current, I_{DD_ARP}. The start-up current at the maximum AC line input voltage must be smaller than the I_{DD_ARP} (Min). Otherwise, when the controller enters an auto-recovery protection mode, the VDD capacitor cannot be discharged to V_{TH_OFF} by the sinking current I_{DD_ARP} to restart the controller. The controller will then behave as in a latched-protection mode, and even trigger the silicon controlled rectifier (SCR) of VDD.



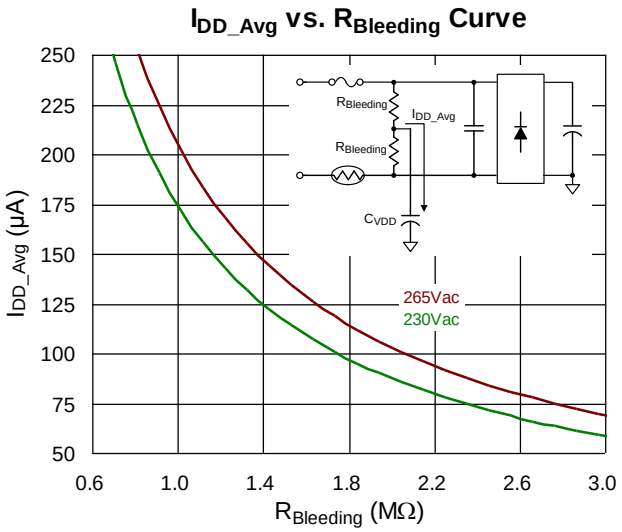


Figure 1. Start-Up Circuit

VDD Discharge Time in Auto-Recovery Mode

Figure 2 shows the V_{DD} and V_{GATE} waveforms during an auto recovery protection (e.g., OCP). In this mode, the start-up resistors, VDD sinking current and VDD decoupling capacitor will affect the restart time. The VDD voltage discharge time $t_{D\_Discharge}$ can be calculated by the following equation :

$$t_{D\_Discharge} = \frac{C_{VDD} \times \left(V_{DD\_DIS} - V_{DD\_LH}\right)}{I_{DD\_ARP} - I_{ST}}$$

Where C_{VDD} is the VDD decoupling capacitor; V_{DD_DIS} is the initial VDD voltage after entering the auto recovery mode; V_{DD_LH} (Typ.) is the latch-off voltage threshold of the controller; I_{DD_ARP} (Typ.) is the sinking current of the VDD pin in the auto recovery mode; and I_{ST} is the start-up current of the power system.

Please note that the start-up current at high input voltage must be smaller than the I_{DD_ARP}. Otherwise, the VDD voltage cannot reach the V_{TH_OFF} to activate the next start-up process after an auto-recovery protection. Therefore, the system behavior resembles the behavior of latch mode.

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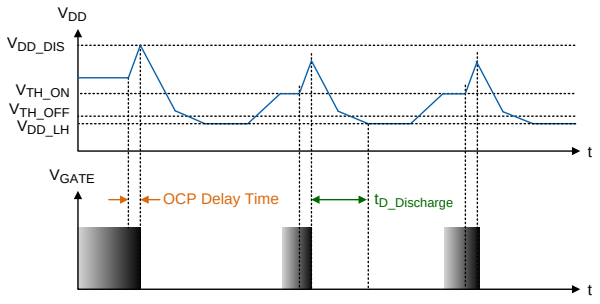

Figure 2. Auto-Recovery Mode (e.g., OCP)

VDD Holdup Mode

The VDD holdup mode is implemented to prevent VDD from dropping below the turn-off threshold voltage V_{TH_OFF} when the system operating under light load, no load, or fast load transient condition. However, compared to the zero-duty mode, the VDD holdup mode consumes more switching power loss. Hence, it is not recommended that the system is designed to operate in this mode under light load or no load condition. Furthermore the VDD holdup mode is designed and controlled by the clock counter. When the clock counter reaches 512 clock counts, the system will shut down if the system continually operates in this mode without leaving its zero-duty mode.

DMAG Pin

During the MOSFET on-time, the auxiliary winding voltage is negative, and the RT7753GCV outputs a clamp current, proportional to the input line voltage, to clamp the DMAG voltage at 0.1V. The RT7753GCV has built-in characteristics, a DMAG brown-in protection threshold current I_{DMAG_BNI} and a DMAG brown-out protection threshold current I_{DMAG_BNO}, for the DMAG pin. The bulk-capacitor brown-in and brown-out threshold voltages, V_{BULK_BNI} and V_{BULK_BNO}, can be programmed respectively by adjusting R_{DMAG1} and R_{DMAG2} at the DMAG pin, as shown in Figure 2.

Once either one of the brown-in and brown-out threshold voltages is set, the other one will be determined accordingly. The bulk-capacitor brown-out threshold voltage V_{BULK_BNO} can be obtained by the following equation :

$$V_{BULK\_BNO} = \frac{V_{BULK\_BNI} \times I_{DMAG\_BNO}}{I_{DMAG\_BNI}}$$

When the MOSFET turns off, the DMAG pin senses the output voltage of the power stage across the auxiliary winding, with a ratio equal to the turns ratio of the auxiliary and secondary windings, and then scaled with the resistive divider R_{DMAG2} / R_{DMAG1}, as shown in Figure 3. The voltage divider can be calculated by the following equations :

$$\begin{cases} \dfrac{V_{BULK\_BNI} \times \dfrac{N_A}{N_P} + 0.1}{R_{DMAG2}} + \dfrac{0.1}{R_{DMAG1}} = I_{DMAG\_BNI} \\ \dfrac{R_{DMAG2}}{\dfrac{(V_{O\_OVP} + V_F)}{V_{TH\_OVP}} \times \dfrac{N_A}{N_S} - 1} = R_{DMAG1} \end{cases}$$

where V_{O_OVP} is the output OVP threshold voltage.

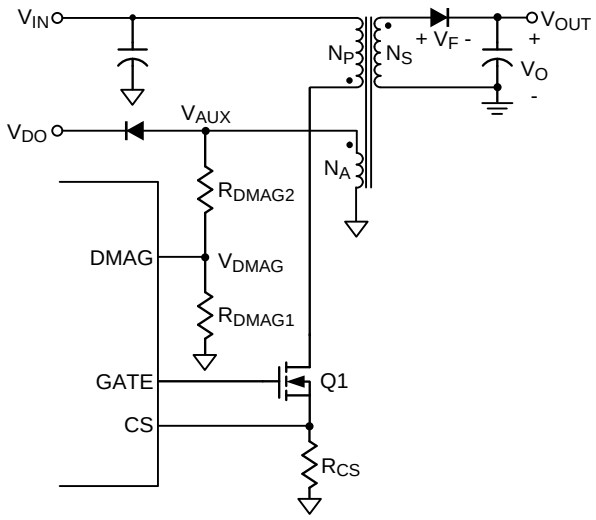

Figure 3. DMAG Pin Resistor

The DMAG UVP is implemented to detect the output UVP or a short protection. If the DMAG voltage is below the V_{DMAG_UVP}, the system starts to detect DMAG UVP and stop to detect if the DMAG voltage rises beyond the V_{DMAG_UVPEX} with a delay time $t_{D\_DMAGUVP}$. During the DMAG UVP detected range, the RT7753GCV will trigger the DMAG UVP if the COMP voltage is higher than 1.8V, as depicted in Figure 4.

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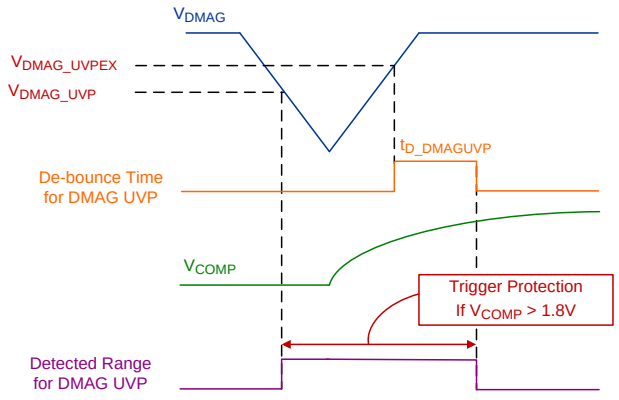

Figure 4. DMAG UVP

When the secondary-side current reduce to zero during the MOSFET turn-off period, the magnetic inductance (L_P) of the transformer and the equivalent parasitic capacitance (C_{DS}) of the MOSFET induces resonant oscillations on the DMAG pin, as shown in Figure 5.

The RT7753GCV with valley switching version provides valley switching function to save switching loss and improve power supply unit (PSU) efficiency. The valley switching function only works when the resonance period (t_{DCM}) is longer than 1.1μs and the DMAG voltage is higher than 0.3V. Otherwise DMAG pin can't detect valley signal, and the system will become hard-switching. During circuit design stage, tolerances of magnetic inductance (L_P) and the equivalent parasitic capacitance (C_{DS}) must be considered.

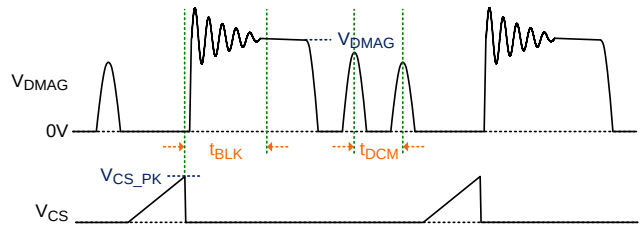

Figure 5. Resonant Oscillations on the DMAG Pin

Adaptive Blanking Time

When the MOSFET just turned off, the leakage inductance of the transformer and the parasitic capacitance (C_{OSS}) of the MOSFET induces resonant oscillations on the DMAG pin, as shown in Figure 5. These resonant oscillations may cause the controller to falsely trigger DMAG over-voltage protection ($V_{DMAG} > V_{TH\_OVP}$), which thus fails to reflect actual output over-voltage fault condition ($V_O > V_{O\_OVP}$) and causing controller's malfunction. In general as the load increases, the duration of the resonant oscillation may also increase. A small bypass capacitor, sized from 10pF to 22pF and placed as close to the DMAG pin as possible, is recommended to suppress such noises on the DMAG pin. A larger bypass capacitor may cause the DMAG voltage phase-shifted too much, and results in the MOSFET cannot be turned-on at exact valley points.

Correspondingly, the RT7753GCV provides adaptive blanking time to prevent DMAG over-voltage protection from being falsely triggered. The built-in blanking time for over-voltage protection (t_{BLK}) varies with the system peak current limit (as V_{CS_PK}), and can be calculated by the following equation :

$$t_{BLK} = 1.75\mu s + 1.375\ (\mu s/V) \times V_{CS\_PK}\ (Typ.)$$

External Over-Temperature Protection (Ext-OTP)

The RT7753GCV includes a programmable external over-temperature protection (Ext-OTP), implemented with a fast diode and a resistive voltage divider, which consists of an external NTC resistor (R_{NTC}) to sense the power system temperature, as shown in Figure 6. During the MOSFET off-time, the auxiliary winding voltage V_{AUX} is constant, and the CS voltage, sampled as a fraction of the clamped voltage V_{AUX_Clamp} and compared with the internal reference voltage to set the over-temperature protection threshold voltage. When the system temperature gets higher, the resistance of the NTC resistor becomes smaller. By adjusting the value of the setting resistor (R_{SET}), the threshold temperature for the over-temperature protection can be programmed. During the off-time, if the sampled CS voltage exceeds the external OTP threshold voltage V_{TH_OTP} and sustains for the external OTP delay time t_{D_OTP}, the controller will be shut down and the switching will be stopped. Once the OTP condition is removed, the controller with auto-recovery option will automatically resume the operation. The design equation for the external OTP threshold voltage is expressed as below :

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$$V_{TH\_OTP} = \left[\left(V_{O\_NOR\_MAX} + V_F \right) \times \frac{N_A}{N_S} - V_{F\_OTP} \right] \times \frac{R_{PDC} + R_{CS}}{R_{NTC\_OTP} + R_{SET} + R_{PDC} + R_{CS}}$$

where $V_{O\_NOR\_MAX}$ is the maximum normal output voltage, and R_{NTC_OTP} is the NTC resistance at the threshold temperature for the external OTP.

It is highly recommended to use a fast diode (CT ≤ 5pF and T_{rr} ≤ 50ns), ex. 1N4148 or BAV21 series for an external OTP application, so as to prevent the CS pin from the wrong regulation or being damaged by the negative voltage spikes.

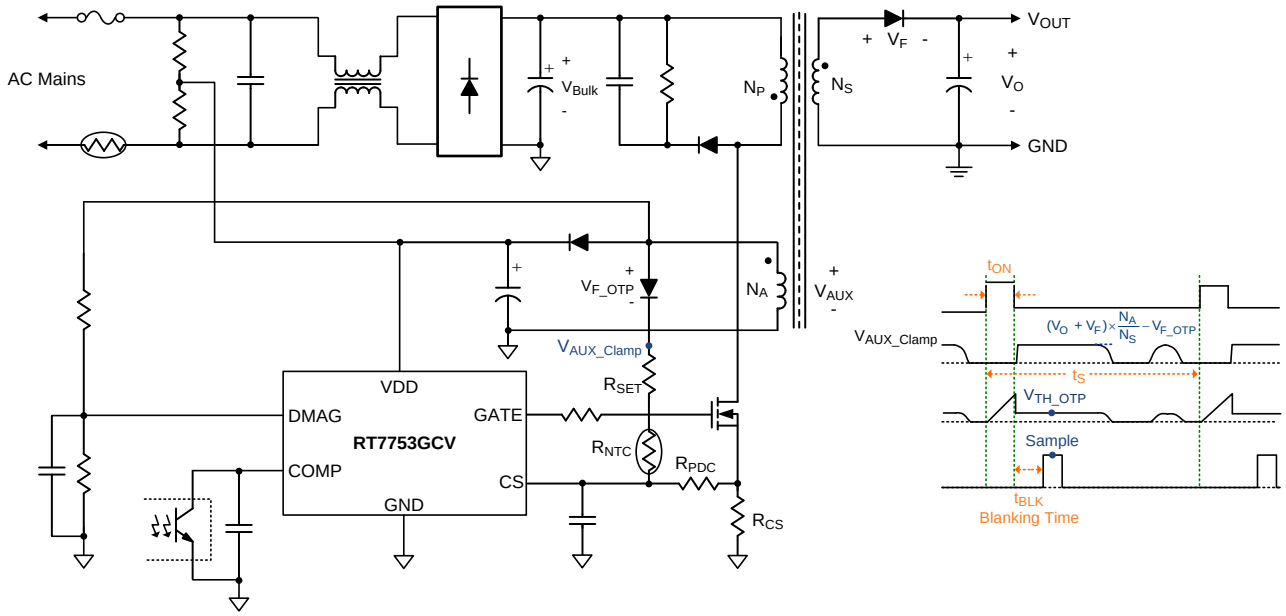

Figure 6. Application Circuit of External Over-Temperature Protection

Resistors at the GATE Pin

As the typical application circuit shown in Figure 7, a resistor R_G can be applied to mitigate ringing spikes induced by the gate drive loop. Therefore, the value of the resistor R_G should be chosen carefully to meet the requirements with considering the EMI as well as the efficiency issues.

The RT7753GCV has a built-in discharge resistor R_{ID}, internally connected from the GATE pin to GND, to prevent the MOSFET suffering from any uncertain condition. If the GATE pin is open-circuited, the MOSFET may be falsely triggered by the stored charge on the gate-to-drain parasitic capacitor C_{GD} of the MOSFET and then damaged. Therefore, it is recommended to add an external discharge resistor R_{ED} between the gate of MOSFET and GND so that the charge stored on the parasitic capacitor C_{GD} can be discharged by an external discharge resistor and the MOSFET can be protected from being falsely triggered even if the RT7753GCV is not in place or the GATE pin is open-circuited.

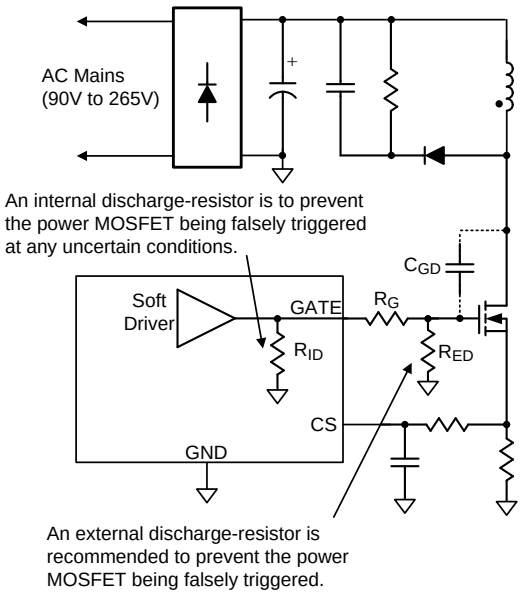

Figure 7. Resistors at the GATE Pin

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Feedback Resistor

To improve the efficiency at light load, the power loss caused by the feedback resistor, in parallel with the opto-coupler as shown in Figure 8, must be reduced. Since the current through the feedback resistor is very small, a shunt regulator (e.g. TL431), especially with its minimum regulated current, should be carefully chosen to ensure that the shunt regulator can still regulate the output voltage under such a small cathode current.

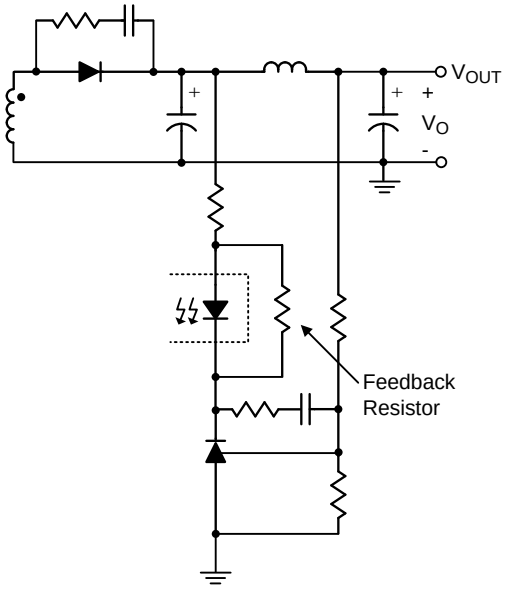

Figure 8. Feedback Resistor

Negative Voltage Spike on Each Pin

Any negative voltage which is less than −0.3V on each controller pin may cause a large injection current into the substrate to damage the controller or to falsely trigger the circuit. For example, the negative voltage spikes at the CS pin may result from a poor PCB layout or the inductance of the current sense resistor. Practically, an R-C filter, as shown in Figure 9, is suggested to prevent the CS pin from being damaged by the negative voltage spikes. During circuit design stage, a proper PCB layout and accurate component selection must be carefully devised and considered.

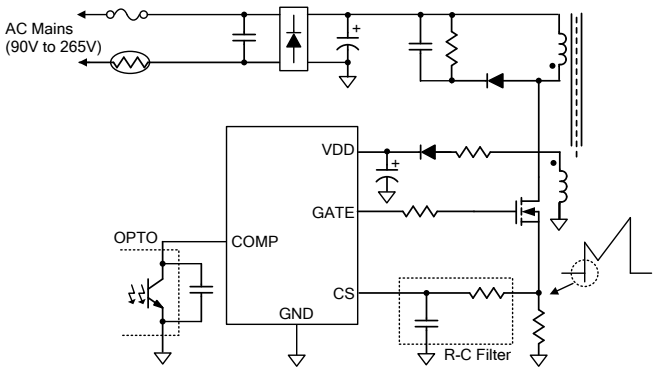

Figure 9. R-C Filter on the CS Pin

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For a continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-6 package, the thermal resistance, θ_{JA}, is 260.7°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated below :

$P_{D(MAX)}$ = (125°C - 25°C) / (260.7°C/W) = 0.38W for a SOT-23-6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

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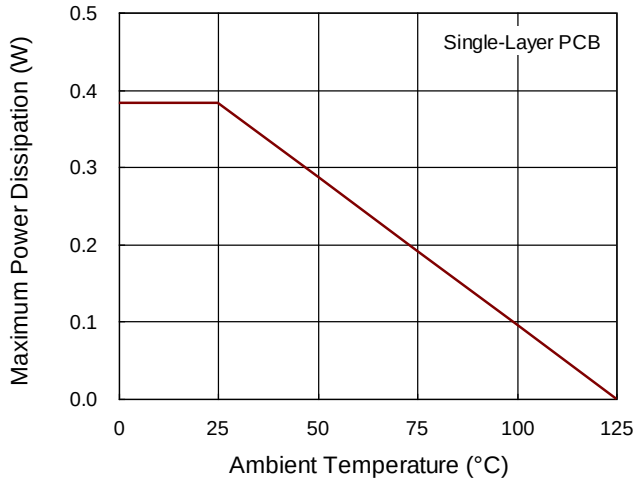

Figure 10. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can alleviate unknown noise interference and EMI emission in a switch-mode power supply (SMPS). It is recommended to follow the following PCB layout guidelines when designing a switch-mode power supply :

- The current path (1), starting from the bulk capacitor, through the transformer, the MOSFET, the resistor R_{CS} and back to the bulk capacitor, is a high-frequency and high-current loop. Another high-frequency and high current loop is the current path (2) which is from the GATE pin, through the MOSFET, the resistor R_{CS} and back to the IC ground. These two paths should be kept as small as possible to decrease noise coupling and kept away from other low-voltage traces, such as IC control circuit paths, especially.
- The path (3), starting from the auxiliary winding, through the resistor, the diode, and the VDD capacitor to the VDD pin, is also recommended to be as short as possible.

  Besides, the VDD capacitor should be placed as close to the VDD pin as possible.
- The path (4) from the RCD snubber circuit to the MOSFET should also be kept short as it is also a loop with high switching frequency.
- The ground traces of the bulk capacitor (a), the MOSFET (b), the VDD capacitor (c), the auxiliary winding (d) and the IC control circuit (e) should be separated to reduce noise, output ripple and EMI emission. The ground traces of the auxiliary winding (d) and the IC control circuit (e) are connected together at the VDD capacitor ground (c). Then the connected ground trace goes through the VDD capacitor ground (c), the MOSFET ground (b), and to the bulk capacitor ground (a) in turn. The area of the bulk capacitor ground trace should be large enough.
- The bypass capacitor should be placed as close to the controller as possible.
- In order to reduce the reflected trace inductance and EMI emission, the trace connecting the secondary winding, the output diode, and the output filter capacitor should be as short as possible. In addition, the copper areas at the anode and cathode of the diode must be large enough to ease sinking heat from the diode.

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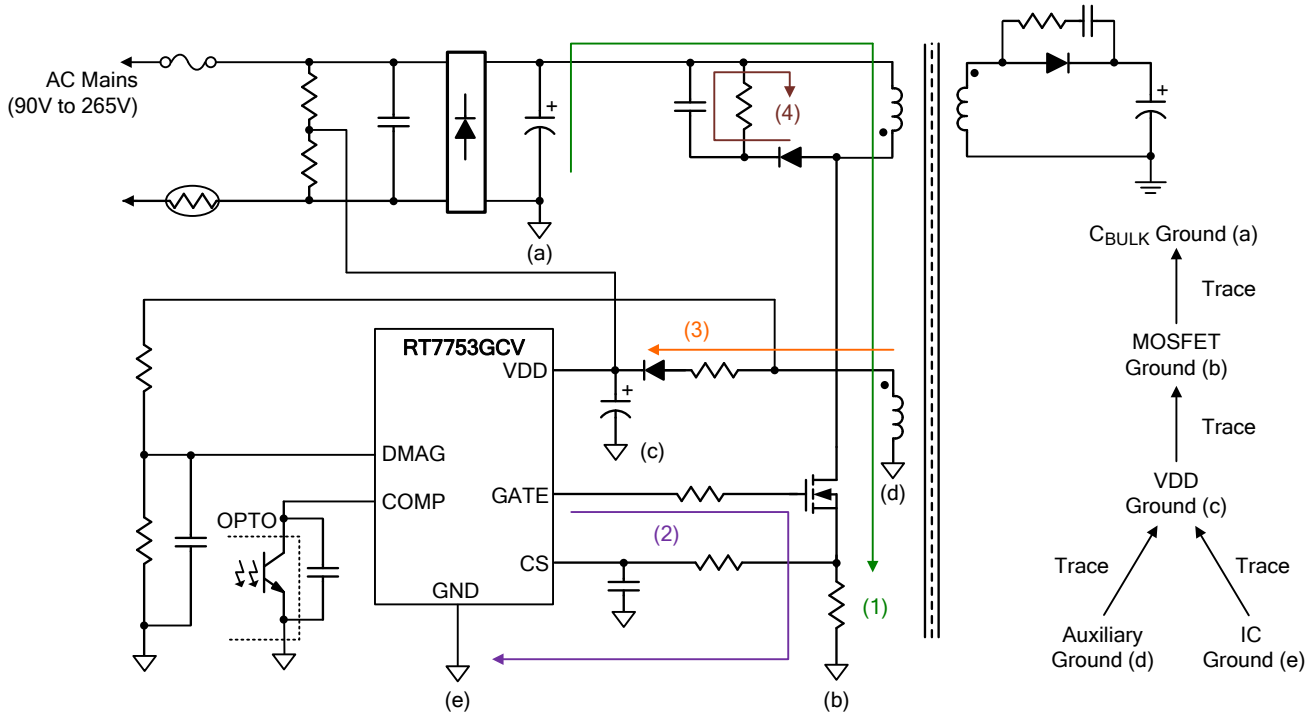

Figure 11. PCB Layout Guide

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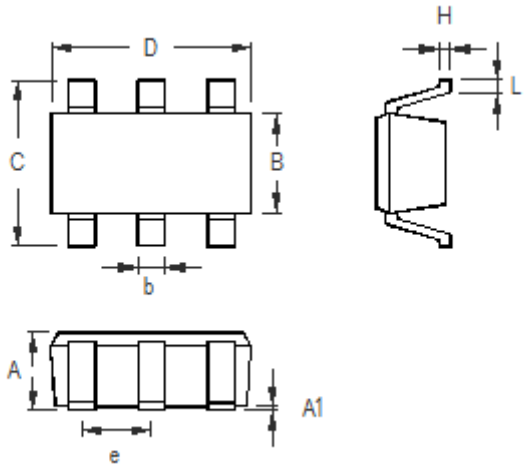
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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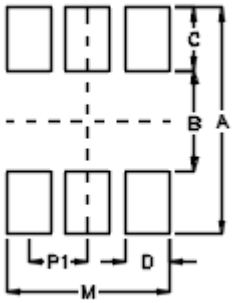
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

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