LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

SD-SST210/214

N-CHANNEL LATERAL DMOS SWITCH

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD210DE	30	1.5	45 @ V_{GS}=10V	0.5	2
SD214DE	20	1.5	45 @ V_{GS}=10V	0.5	2
SST210	30	1.5	50 @ V_{GS}=10V	0.5	2
SST214	20	1.5	50 @ V_{GS}=10V	0.5	2

PRODUCT SUMMARY

Features

- Ultra-High Speed Switching—t_{ON}: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

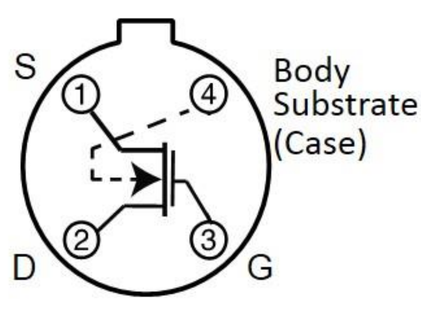
Description

The SD210DE/214 and SST210/214 are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD214DE and SST214 are normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not have a gate protection Zener diode which results in lower gate leakage and ± voltage capability from gate to substrate. A poly-silicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, Zener protected—SD211DE/SST211 Series.

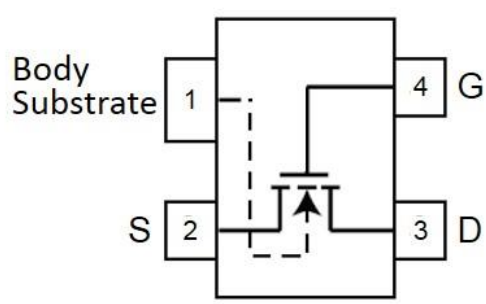
Top Views

SD210DE, SD214DE



TO-206AF
(TO-72)

SST210, SST214



TO-253
(SOT-143)

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Gate-Drain, Gate-Source Voltage		± 40V
Gate-Substrate Voltage		± 30V
Drain-Source Voltage	(SD210DE/SST210)	30V
	(SD214DE/SST214)	20V
Source-Drain Voltage	(SD210DE/SST210)	10V
	(SD214DE/SST214)	20V
Drain-Substrate Voltage	(SD210DESST210)	30V
	(SD214DE/SST214)	25V
Source-Substrate Voltage	(SD210DE/SST210)	15V
	(SD210DE/SST210)	25V
Drain Current		50mA
Lead Temperature (1/16" from ease for 10 seconds)		300°C
Storage Temperature		-65 to 150°C
Operating Junction Temperature		-55 to 125°C
Power Dissipation*		300mW

Note:
* Derate 3mW/°C above 25°C

Specifications[a]

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS 210 Series Min	210 Series Max	214 Series Min	214 Series Max	UNIT
Static									
Drain - Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0V$, $I_D = 10\ \mu A$		35	30				V
		$V_{GS} = V_{BS} = -5V$, $I_D = 10\ nA$		30	10		20		V
Source - Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5V$, $I_S = 10\ nA$		22	10		20		V
Drain - Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0V$, $I_D = 10\ nA$ Source Open		35	15		25		V
Source - Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0V$, $I_S = 10\ \mu A$ Drain Open		35	15		25		V
Drain – Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5V$	$V_{DS} = 10V$	0.4		10			nA
			$V_{DS} = 20V$	0.9				10	nA
Source - Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5V$	$V_{SD} = 10V$	0.5		10			nA
			$V_{SD} = 20V$					10	nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0V$, $V_{GB} = \pm 40V$		±0.001		±100		±100	pA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1\ \mu A$, $V_{SB} = 0V$		0.8	0.5	1.5	0.1	1.5	V
Drain – Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0V$ $I_D = 1mA$	$V_{GS} = 5V$ (SD Series)	58		70		70	Ω
			$V_{GS} = 5V$ (SST Series)	60		75		75	Ω
			$V_{GS} = 10V$ (SD Series)	38		45		45	Ω
			$V_{GS} = 10V$ (SST Series)	40		50		50	Ω
			$V_{GS} = 15V$	30					Ω
			$V_{GS} = 20V$	26					Ω
			$V_{GS} = 25V$	24					Ω

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[c]	LIMITS 210 Series Min	LIMITS 210 Series Max	LIMITS 214 Series Min	LIMITS 214 Series Max	UNIT
Dynamic									
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz	SD Series	11	10		10		mS
			SST Series	10.5	9		9		
	g_{os}		All	0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V	SD Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$		SD Series	1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$		SD Series	3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2					
			SD Series	0.2		0.5		0.5	
Switching									
Turn-On Time	$t_{D(on)}$	SD Series Only V_{SB} = 0V, V_{IN} 0 to 5V, R_G = 25Ω V_{DD} = 5V, R_L = 680Ω		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{D (off)}$			2					
	t_f			6					

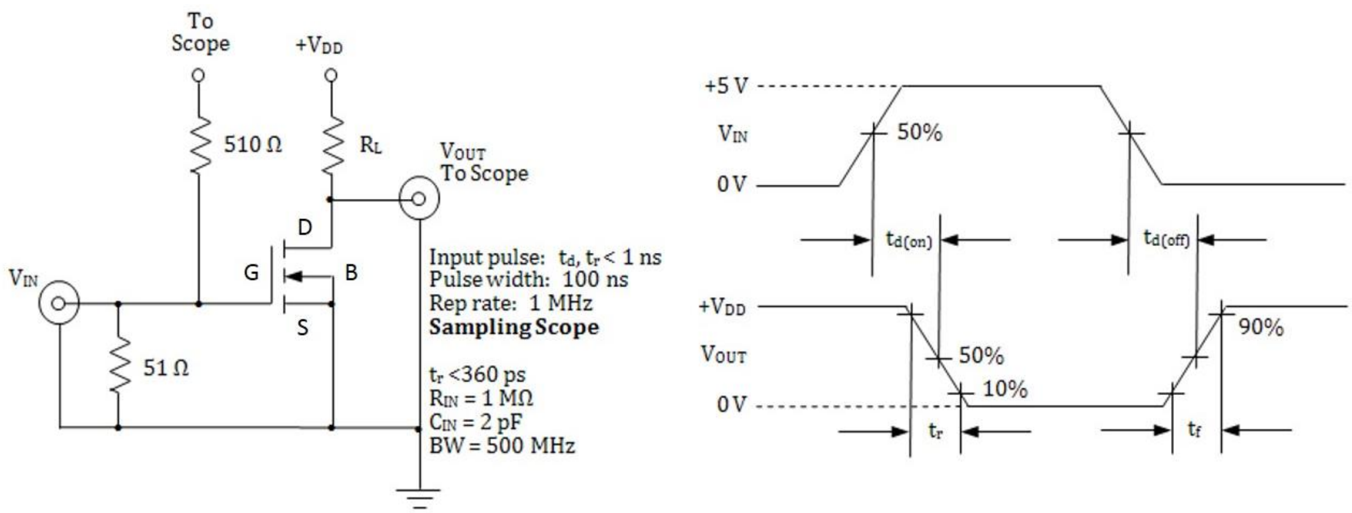
NOTES:

a. T_A = 25°C unless otherwise notes.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Switching Time Test Circuit



Linear Integrated Systems (LIS), established in 1987, is third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company Founder John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.